NASA-TM-112472

NDB R-0

PSB NASA
IN-33-TM

High-field fast-risetime pulse failures in 4H- and 6H-SiC *pn* junction diodes

Philip G. Neudeck[a)]
NASA Lewis Research Center, 21000 Brookpark Road, M.S. 77-1, Cleveland, Ohio 44135

Christian Fazi
U.S. Army Research Laboratory, 2800 Powder Mill Road, Adelphi, Maryland 20783

(Received 24 January 1996; accepted for publication 15 April 1996)

We report the observation of anomalous reverse breakdown behavior in moderately doped ($2-3\times10^{17}$ cm^{-3}) small-area micropipe-free 4H- and 6H-SiC *pn* junction diodes. When measured with a curve tracer, the diodes consistently exhibited very low reverse leakage currents and sharp repeatable breakdown knees in the range of 140–150 V. However, when subjected to single-shot reverse bias pulses (200 ns pulsewidth, 1 ns risetime), the diodes failed catastrophically at pulse voltages of less than 100 V. We propose a possible mechanism for this anomalous reduction in pulsed breakdown voltage relative to dc breakdown voltage. This instability must be removed so that SiC high-field devices can operate with the same high reliability as silicon power devices. [S0021-8979(96)06114-2]

I. INTRODUCTION

The inherent physical properties of silicon carbide (SiC) appear to be extremely well suited for power semiconductor electronic devices. Theoretical appraisals of the characteristics and applications of SiC power devices have suggested that once silicon carbide technology matures sufficiently to overcome some developmental obstacles, SiC may supplant silicon in many high-power electronic applications.[1,2] However, these analyses are primarily based on the numerical substitution of SiC physical properties into existing semiconductor device models. These models have limitations however, as they clearly do not take into account all behaviors of an actual physical SiC device. One behavior crucial to power device reliability that has necessarily been assumed to date is that the breakdown behavior of SiC *pn* junctions will (after technology improvements eliminate all crystalline defects such as micropipes) be similar to silicon-based *pn* junctions. Silicon *pn* junctions are highly reliable because they exhibit stabilizing properties such as positive temperature coefficient of breakdown voltage.[3–5] The experimental work presented in this article casts some doubt upon the presumption of siliconlike breakdown behavior for all SiC *pn* junctions. In particular, we will show that in at least some (but not necessarily all) cases, the breakdown behavior of 4H- and 6H-SiC *pn* junctions is strikingly and catastrophically different from the stable breakdown behavior taken for granted in silicon power devices.

II. EXPERIMENT

A. Device fabrication

The SiC homoepilayer structure shown in Fig. 1 was grown by NASA Lewis on substrates cut from commercially available[6] p^+ 4H and 6H silicon-face SiC substrates polished 3°–4° off the (0001) SiC basal plane. The atmospheric pressure chemical vapor deposition (CVD) system, gases, and general growth procedures used are described elsewhere.[7–9] Processing of the 4H and 6H samples was done in parallel, with pattern definitions, metallizations, etches, and oxidations being done simultaneously. To begin the postgrowth diode fabrication, a 2000 Å thick aluminum etch mask, which defined circular and square diode mesas ranging in area from 7×10^{-6} to 4×10^{-4} cm^2, was applied and patterned by metal liftoff. Diode mesas were defined by etching to a depth of ~1 μm using reactive ion etching (RIE) with 90% CHF_3—10% O_2 at 400 W rf with a chamber pressure of 150 mTorr. The etch mask was stripped, and the samples were sequentially cleaned with acetone, methanol, 3 NH_4OH : 3 H_2O_2 : 10 H_2O, HF, and 3 HCl : 3 H_2O_2 : 10 H_2O prior to undergoing wet thermal oxidation for 4 h at 1150 °C. After the wafers had been patterned for topside contacts, vias were etched in the oxide using 6:1 buffered HF solution. Gold contacts were then e-beam deposited and liftoff patterned for topside contacts and blanket evaporated for backside contact.

B. dc-measurements

Room temperature 1-MHz capacitance–voltage measurements on a few large-area diodes estimated the 0.6 μm thick n-layer doping at 2×10^{17} and 3×10^{17} cm^{-3} for the 4H and 6H devices, respectively. All current–voltage ($I-V$) measurements were carried out in the dark at room temperature on a probing station using either a Tektronix 576 curve tracer or a Keithley 237 source-measure unit. Over 50 devices were dc tested at room temperature, and typical linear scale and semilogarithmic scale $I-V$ characteristics are shown in Fig. 2.

Since crystal defect densities of SiC epilayers on commercial wafers are known to be on the order of 10^4 cm^{-2}, only devices with areas less than 5×10^{-5} cm^2 were selected for this work, so that around half should be free of micropipes and dislocations.[10] Furthermore, any diode showing dc characteristics that deviated in leakage current or sharpness of breakdown knee from the nominal $I-V$ characteristics of Fig. 2 was thrown out from the working data set presented in this article. Over half of the small-area devices

---

[a)] Electronic mail: neudeck@lerc.nasa.gov

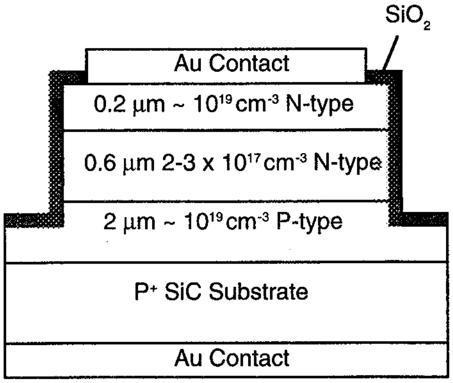
SiO$_2$
Au Contact
0.2 µm ~ 10^{19} cm^{-3} N-type
0.6 µm 2-3 x 10^{17} cm^{-3} N-type
2 µm ~ 10^{19} cm^{-3} P-type
P$^+$ SiC Substrate
Au Contact

FIG. 1. Cross-sectional structure of experimental 4H- and 6H-SiC diodes.

tested in this work, exhibited very well-behaved dc characteristics nearly identical to Fig. 2.

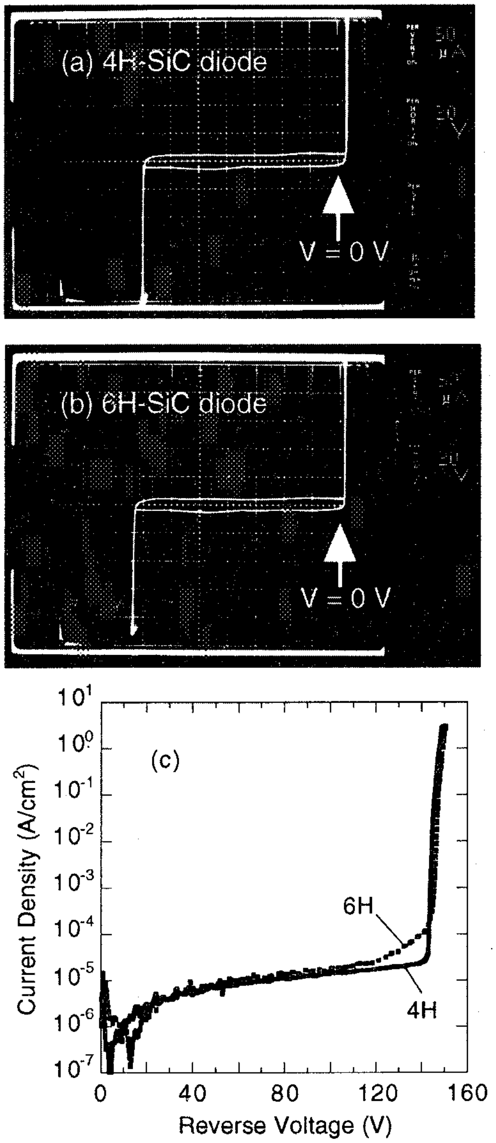

FIG. 2. Typical room-temperature $I-V$ characteristics of 1.96×10^{-5} cm^2 area SiC diodes. (a) Linear 4H-SiC characteristic and (b) linear 6H-SiC characteristic measured with curve tracer. (c) Semilogarithmic reverse characteristics measured with source-measure instrument.

For the well-behaved devices, the reverse breakdown knee voltage varied only slightly as a function of position on the wafer, 140–146 V for the 4H diodes, and 146–149 V for the 6H diodes. This small variation is consistent with doping and thickness nonuniformities that have been observed in similar samples produced by the growth system employed in this work. These dc-measured breakdown voltages are consistent with comparably doped SiC junction breakdowns reported in the literature.[11,12]

C. Pulse testing

1. Pulse testing procedure

Pulse bias testing was carried out using a conventional charge line circuit, depicted in Fig. 3. This circuit nominally stressed the device under test with rectangular-shaped pulses of 200 ns width (with ~1 ns risetime/falltime) on a manually triggered single-shot basis. The pulse voltage amplitude was controlled by adjusting the high-voltage supply, which charged a 1/2 in. 150 ft semirigid transmission line. The input voltage pulse to the device under test was formed by the discharge of the semirigid coax when the mercury vapor switch was momentarily triggered.

Device voltage and current waveforms were simultaneously recorded and stored for each applied pulse using a dual-channel digitizing oscilloscope. Great care was taken to ensure that the magnitude of the current and voltage data recorded on the oscilloscope were accurate to within 10%, and the circuit attenuator calibrations were verified through independent measurements periodically. Since the current probe employed in this work could not measure currents below 100 mA, it was not possible to record the time evolution of small reverse leakage currents under pulsed conditions.

The input voltage amplitude of the first pulse (or "shot") applied to a given diode was usually less than half of the dc-measured breakdown voltage. Following digital storage of the device voltage and current waveforms recorded with each shot, the dc $I-V$ characteristics of the diode were rechecked with the curve tracer. If the device characteristics remained unchanged, the supply voltage of the pulse circuit was increased, and an additional shot was taken at a higher voltage pulse amplitude. This procedure was repeated until diode damage was observed by a change in the dc $I-V$ characteristics.

2. SiC diode pulse results

A series of pulse-test data taken from a 4H-SiC diode is shown in Fig. 4. This data is representative of all pulse data collected on some 20 SiC diodes of both polytypes. As expected, displacement current spikes associated with the rising and falling edges of the voltage pulse are observed, as well as nonideal transmission-line reflection effects apparent in the 200–600 ns time range. The pulsed results in Figs. 4(a) and 4(b) are consistent with the measured dc $I-V$ data in that there is no detectable conduction current as the applied voltage pulse amplitude is increased from 72 V [Fig.

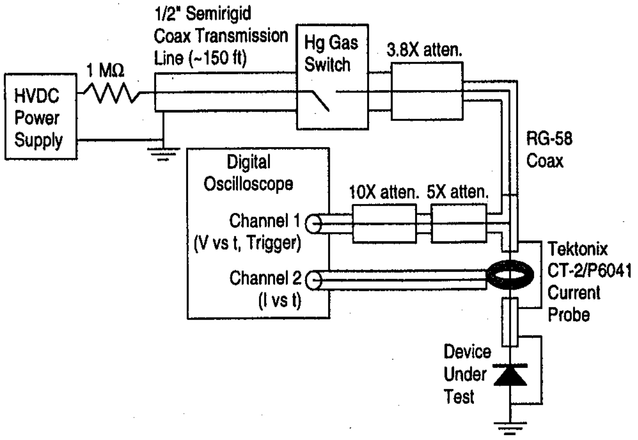

FIG. 3. Experimental apparatus employed to measure response of diodes to fast-risetime pulses.

4(a)] to 83 V [Fig. 4(b)]. Since no conduction current is drawn, the amplitude of the device voltage waveform matches the input voltage pulse amplitude. However, when the input pulse amplitude was increased for the third shot to 94 V [Fig. 4(c)], the measured voltage across the device collapsed, while the conduction current shot up.

The pulse-induced breakdown observed at less than 70% of the dc-measured breakdown voltage is anomalous, since the dc-measured current (Fig. 2) at 100 V was less than 1 μA. Curve tracer characterization immediately following this pulse revealed that the diode had catastrophically failed and became a resistor instead of remaining a rectifying junction. The Fig. 4(c) data indicates junction breakdown occurred in 20 ns or less.

The general results shown in Fig. 4 were found for all diodes tested in both 4H and 6H polytypes. All SiC devices failed catastrophically at pulse voltages that were only 60%–80% of the dc-measured breakdown voltage. Aside from displacement current observed at the rising and falling edges of the pulse, the conduction current flowing through these very small-area diodes before failure was too small to detect with the existing current probe. Microscopic examination of all failed devices revealed highly localized damage to the device mesa and contact, consistent with the two typical examples shown in Fig. 5. This strongly suggests that a current-filamentation type failure occurred in the bulk of the device.[13,14] When a filament occurs, the current density in a localized spot drastically increases, greatly stressing the junction material, often to the point of failure.

3. Silicon diode pulse results

We also conducted pulse measurements on well-characterized silicon diodes to confirm that our pulse-test apparatus could properly record the stable reverse avalanche breakdown behavior that is known to exist in silicon *pn* junctions.[3–5] Both packaged and unpackaged (probe-tested) silicon devices exhibited the general breakdown behavior displayed in Fig. 6. Figure 6 shows the series of device voltage and current traces recorded as a function of increasing input pulse amplitude from a packaged silicon *pn* junction diode whose curve-tracer dc-measured breakdown voltage was 150 V. No measurable current (neglecting displacement current at the pulse edges) was observed for any input pulse amplitudes below the dc-measured breakdown voltage of

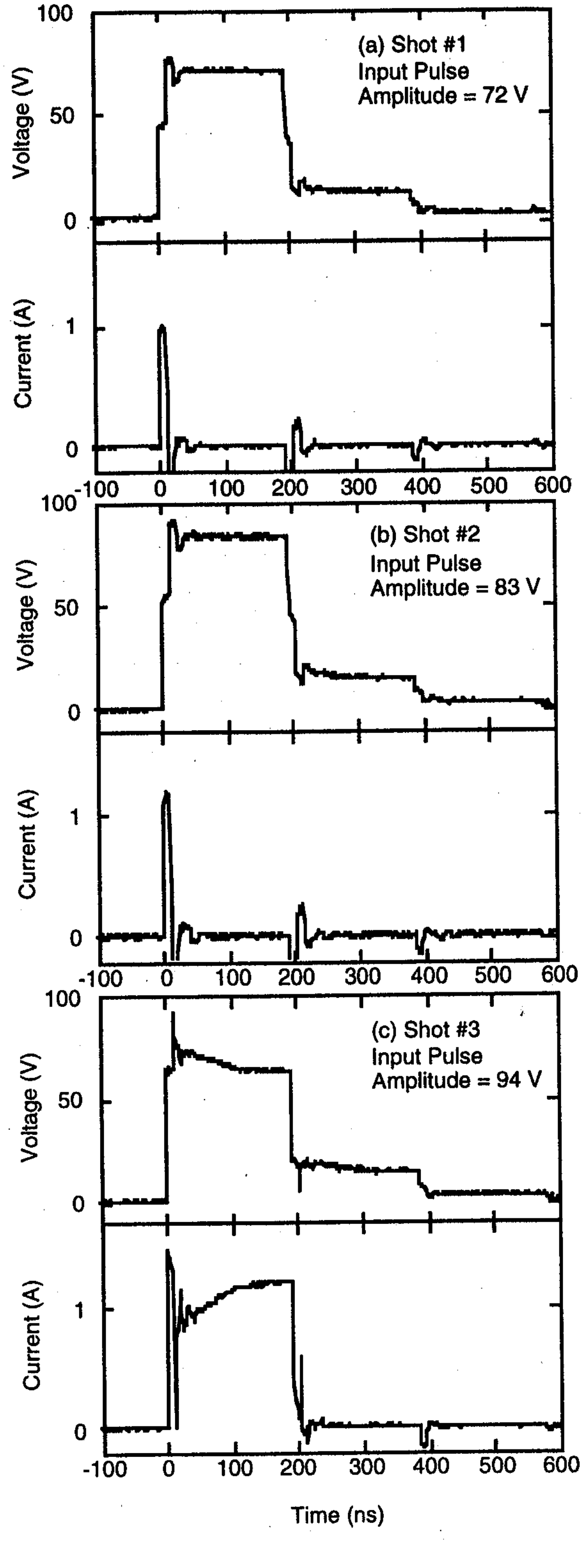

FIG. 4. Voltage and current transient response of 4H-SiC diode when subjected to 200 ns duration input pulse amplitudes of (a) 72 V, (b) 83 V, and (c) 94 V. The 94 V pulse failed the diode catastrophically, even though dc testing suggests the device should not fail until the pulse amplitude exceeds 140 V. Similar results were recorded for every 4H- and 6H-SiC diode pulse tested in this work.

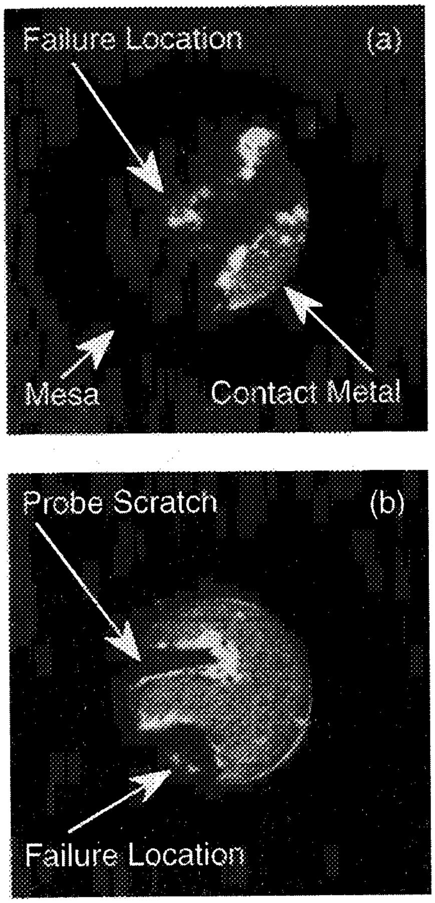

FIG. 5. Photomicrographs of 50 μm diam 4H-SiC diodes following pulse failure. The localized damage occurring in the bulk mesa regions strongly suggests a current-filamentation failure mechanism. The majority of the contact was destroyed in device (a), while the scratch mark left by the probe tip is evident in device (b).

150 V [Fig. 6(a)]. As the input voltage pulse amplitude increased sufficiently beyond 150 V, current flow consistent with the 150 V dc breakdown voltage knee is observed [Figs. 6(b) and 6(c)]. With significant currents flowing through the diode, the measured voltage waveform across the diode clamped in the neighborhood of 150 V, despite the fact that the input pulse amplitude (which can be measured "open circuit" when no device under test is present) had been increased to 225 V in Fig. 6(c). Prior to the 240 V input pulse that failed the diode [Fig. 6(d)], the dc-characteristics measured on the curve tracer between pulses remained unchanged from the initial $I-V$ characteristic. Diode failure occurs at $t=40$ ns in Fig. 6(d), as clearly evidenced by the voltage collapse and increase in current.

Figure 6(c) clearly shows the classic silicon behavior of positive temperature coefficient of breakdown voltage in that as the device heats up over the 200 ns pulse duration, the current flow through the device decreases while the voltage across the device increases. Because current flow decreases as junction temperature rises, the property of positive temperature coefficient of breakdown voltage in silicon junctions prevents the formation of damaging high-current filaments at junction hot spots. In other words, it forces breakdown current to flow relatively evenly distributed across the entire area of the silicon diode junction (bulk breakdown), as opposed to focusing current flow at a localized hot spot which would occur if negative temperature coefficient behavior were present. The excellent stability and durability of the Fig. 6 silicon *pn* junction enables it to reliably withstand input pulse amplitudes of nearly 150% of the dc-measured breakdown voltage.

III. DISCUSSION

A. Relevance of findings to SiC power device technology

The contrasting experimental pulse-testing results between 150 V rated silicon and SiC diodes help illustrate the great importance of stable breakdown behavior in semiconductor power devices. Silicon power devices exhibit stable reverse breakdown properties, such as positive temperature coefficient of breakdown voltage, that permit them to withstand overvoltages (i.e., glitches, transients, etc.) that commonly occur in power system circuits.[15] In other words, they can be rated for highly reliable operation at voltages near their avalanche breakdown voltage, because they can safely recover without damage from occasional brief bias excursions that take them into avalanche breakdown. The silicon diode of Fig. 6 clearly exhibits this behavior for both dc and fast-risetime pulse testing.

At first glance, the SiC diodes may appear to exhibit somewhat stable breakdown behavior, as the dc-measured $I-V$ characteristics of Fig. 2 misleadingly suggest, since they exhibit a sharp reverse knee that can be repeatedly traced. When subjected to fast-risetime pulses however, the SiC diodes tested in this work failed catastrophically from a single 200 ns input pulse with amplitude significantly less than the apparent dc breakdown voltage. Since the time leading to failure is extremely fast [<20 ns in Fig. 4(c)], the energy leading to failure is very small, indicative of unstable device behavior.

Clearly, the particular SiC devices tested above cannot be considered reliable if a single impulse glitch of modest (i.e., ~30% below dc breakdown) voltage can catastrophically fail every diode with very low energy. Since such impulse glitches occur in many kinds of power systems, it is unlikely that SiC power diodes exhibiting the unstable breakdown properties observed in this work could be operated reliably in a system at bias points anywhere near the dc breakdown voltage the way that silicon diodes are routinely operated. Furthermore, circuits would have to be carefully designed to insure that unstable SiC diodes would never see a single impulse glitch of sufficient amplitude to cause failure. Whether this involves the use of additional protection circuitry, or significant device voltage derating, or both, it is likely that there will be a significant performance, cost, and/or reliability penalty associated with compensating power circuits for unstable device breakdown behavior.

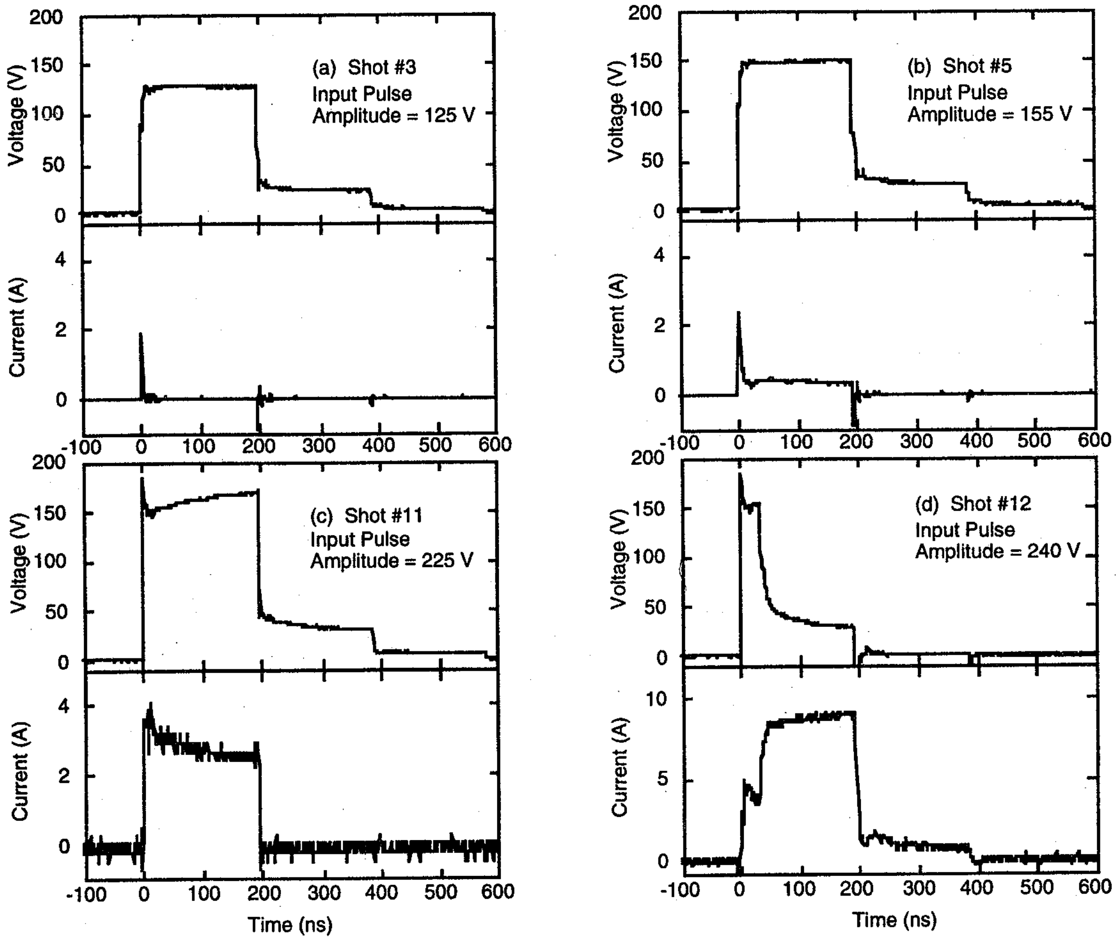

FIG. 6. Voltage and current transient response of a 150 V, 10 mA silicon diode when subjected to 200 ns duration input pulse amplitudes of (a) 125, (b) 155, (c) 225, and (d) 240 V. The positive temperature coefficient of breakdown voltage behavior is readily evident in part (c). The 240 V pulse failed the diode catastrophically at $t=40$ ns in part (d).

B. Proposed instability mechanism

The results above have only shown unstable behavior for two specific sets of SiC diodes. It is important to ascertain the cause of this behavior and whether it applies to all SiC diodes in general. Toward this end, we have initiated further experimental and theoretical investigations. Notwithstanding the future outcome of these further investigations, we have developed a preliminary working hypothesis as to the source of the SiC diode pulse-bias instabilities observed in the initial work reported in this article. While the theory is based upon fundamental differences between Si and SiC material properties, it suggests that SiC diodes with stable siliconlike breakdown properties may be realizable with proper device design and technology improvements.

There is extensive literature on the physics of breakdown in semiconductors, specifically including the breakdown behavior of silicon *pn* junctions.[3–5,14] A significant difference between Si and SiC is that in most silicon devices, it is taken for granted that all carriers are fully ionized over the normal operational temperature range including room temperature. In silicon carbide, the dopants are energetically deep enough that a nontrivial percentage are un-ionized at room temperature resulting in their exclusion from the transport process.[16] Also, SiC crystal growth technology is not yet mature, resulting in the presence of deep-level centers.[17–19] We believe that both deep-levels and incomplete ionization of dopants might contribute to the unstable SiC breakdown behavior observed in this work.

The band diagrams of Fig. 7 illustrate part of our working theory for the fast-risetime pulse instability observed in the SiC diodes of Sec. II C 2. For simplicity, only donorlike centers and electrons in a partially frozen-out n-type region of a junction will be considered in the following discussion. Nevertheless, the basic mechanism can also be applied to various permutations of centers (donorlike and acceptorlike) and carriers in any rectifying junction.

Before bias is applied to the SiC sample, there are a substantial number of carriers occupying un-ionized donors and deep-level defects in quasineutral regions near the depletion region edge [Fig. 7(a)]. When a fast-risetime bias pulse is applied, the emission of trapped carriers does not occur quickly enough to keep up with the expanding depletion region. A significant percentage (perhaps a majority) of carriers remain briefly trapped in the high-field depletion region

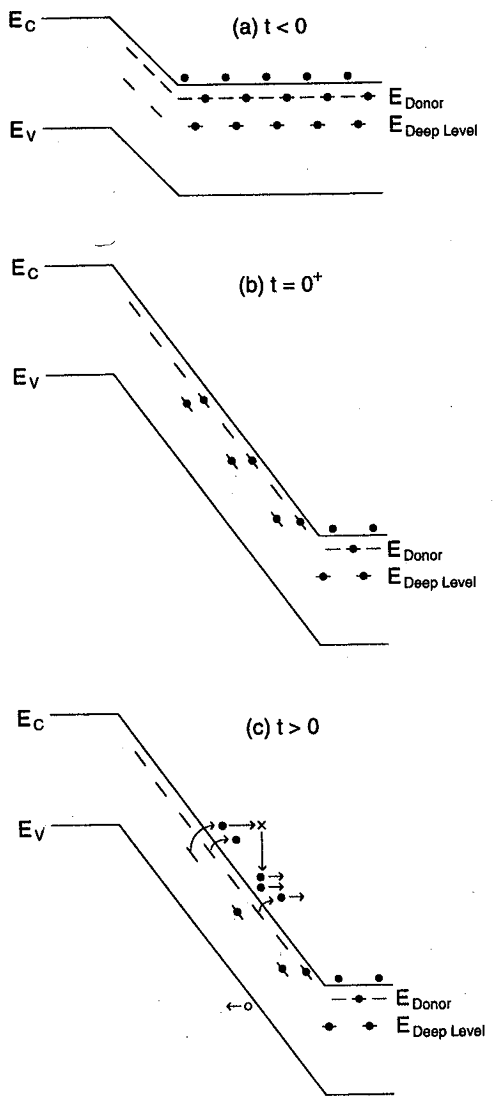

FIG. 7. Band diagrams depicting the *n* side of an arbitrary SiC diode junction (a) at zero bias, (b) with voltage applied at the leading edge of fast-risetime pulse, and (c) at a brief time following the pulse leading edge when dopants and deep levels are emitting carriers into the high-field junction depletion region.

at $t=0^+$ [Fig. 7(b)]. These carriers thermally emit into the high-field depletion region at the worst time [$t>0$, Fig. 7(c)]. The injection of carriers into the high-field region produces an undesired current surge that fails the diode.

At high enough bias levels, this mechanism is inferred to be a current filamentation mechanism, since the devices failed as short circuits and post failure inspections showed highly localized damage within the bulk diode area (Fig. 5). As discussed by Ridley[13] and others,[14] current filamentation occurs when a semiconductor exhibits S-shaped negative differential conductivity (SNDC). If a semiconductor material has a negative temperature coefficient of breakdown voltage, any localized temperature increase that occurs within the breakdown-biased junction will cause a localized current increase or hot spot. The current increase feeds back and causes even more localized and intensified heating. The process escalates until the material very rapidly overheats and fails catastrophically by shorting the junction. The notion that carrier emission from deep levels and frozen-out dopants can lead to SNDC, negative temperature coefficient of breakdown, and catastrophic current filamentation failure has been previously put forth in the literature.[13,14,20–22] Since carrier emission increases with temperature, it is possible to envision filamentation when trapped carriers emit directly into the high-field region of a near-breakdown biased junction. Localized heating at a hot spot would cause remaining trapped carriers to emit even faster, causing more current, and impact ionization at a junction hot spot. Even though a more rigorous examination of this phenomenon is clearly in order (such as high-field transport modeling), this initial speculative hypothesis can nevertheless serve as a starting point for more comprehensive investigations into the observed fast-risetime pulse breakdown instabilities.

The catastrophic filamentation failure mechanism does not take place in the steady state case, because the bias is gradually increased over a long enough time period (~16 ms on the curve tracer) that most carrier ionization takes place in a gradual fashion near the low-field edge of the expanding depletion region in relative sync with the bias signal. This more orderly and gradual discharge of trapped carriers generates negligible current and heating, so that the device retains its good low-leakage characteristics shown on the curve tracer until the dc breakdown voltage is reached. The fact that the diodes were so well-behaved when dc tested suggests that leakage effects from crystal defects and junction perimeter sidewalls may not be major factors in the anomalous pulsed-bias breakdown.

C. Prospects for reliably stable SiC breakdown

For the proposed physical mechanisms discussed above as the primary cause of the observed unstable SiC breakdown behavior, the instability may not necessarily be inherent to all SiC devices. The elimination of trapped carrier emission processes should result in reliable behavior from devices when they are free of crystal defects. Carrier emission from deep levels will hopefully be eliminated by improvements to epitaxial crystal growth technology. Carrier emission from dopant sites may also need to be minimized by choosing dopants with the lowest ionization energy levels. Since conventional silicon dopants are completely ionized over the entire U.S. military specification temperature range (−55 to +125 °C), carrier emission from dopant sites has never been an important mechanism in the high-field behavior silicon junctions. However, in wide-bandgap semiconductors such as 4H- and 6H-SiC, a significant percentage of dopants are frozen out around room temperature, so that carrier emission from dopant sites can be the cause of unstable breakdown behavior. Since percent ionization increases as doping decreases, SiC devices with lighter dopings than those employed in this work are more likely to exhibit stable reverse breakdown behavior, if crystal defects and deep levels are sufficiently low.

We are undertaking further experimental and theoretical studies to quantitatively ascertain the conditions under which

4H- and 6H-SiC junctions exhibit stable reverse breakdown behavior.

IV. CONCLUSION

The importance of this work is best summarized by the contrasting pulse-testing results between silicon and SiC diodes that exhibit comparable breakdown voltages of ~150 V when dc characterized (Sec. II C). When subjected to fast-risetime bias pulses, the SiC diode fails before a pulse amplitude of 100 V is reached, while the silicon diode can withstand pulse amplitudes of over 225 V. We have shown that the safe reverse voltage rating of a SiC rectifier should not be solely based upon its curve-tracer measured reverse knee voltage. If SiC power devices are to replace silicon devices in power system circuits, the unreliable breakdown behavior reported in this article must be eliminated. The regime over which SiC power devices exhibit stable breakdown properties will likely be significantly smaller than the temperature-doping space over which silicon power devices are known to be stable. While a smaller doping-temperature design region should not prevent the realization of SiC power electronics, it is an additional reliability constraint that must be taken into account when designing SiC-based power systems.

ACKNOWLEDGMENTS

The authors would like to gratefully acknowledge enlightening discussions with Professor Jim Parsons of Oregon Graduate Institute and Professor Mike Mazzola of Mississippi State University. We would also like to acknowledge the technical assistance of Carl Salupo, Joseph Flatico, Glenn Beheim, Luann Keys, and Andrew Trunek at NASA Lewis Research Center.

[1] M. Bhatnagar and B. J. Baliga, IEEE Trans. Electron Devices **40**, 645 (1993).

[2] B. J. Baliga, Proc. IEEE **82**, 1112 (1994).

[3] L. W. Ricketts, J. E. Bridges, and J. Miletta, *EMP Radiation and Protective Techniques* (Wiley, New York, 1976).

[4] *EMP Engineering and Design Principles* (Bell Laboratories, Murray Hill, NJ, 1984).

[5] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (Wiley, New York, 1981).

[6] Cree Research Inc., 2810 Meridian Parkway, Suite 176, Durham, NC 27713.

[7] J. A. Powell, L. G. Matus, and M. A. Kuczmarski, J. Electrochem. Soc. **134**, 1558 (1987).

[8] D. J. Larkin, P. G. Neudeck, J. A. Powell, and L. G. Matus, Appl. Phys. Lett. **65**, 1659 (1994).

[9] J. A. Powell, D. J. Larkin, and P. B. Abel, J. Electron. Mater. **24**, 295 (1995).

[10] S. Wang, M. Dudley, C. H. Carter, Jr., and H. S. Kong, in *Diamond*, SiC and Nitride Wide Bandgap Semiconductors, edited by C. H. Carter, Jr., G. Gildenblat, S. Nakamura, and R. J. Nemanich (Materials Research Society, Pittsburgh, PA, 1994), Mat. Res. Symp. Proc., Vol. 339, pp. 735–740.

[11] J. A. Edmond, D. G. Waltz, S. Brueckner, H.-S. Kong, J. W. Palmour, and C. H. Carter, Jr., in *Trans. 1st International High Temperature Electronics Conference* (Albuquerque, NM, 1991), pp. 207–212.

[12] J. W. Palmour, J. A. Edmond, H. S. Kong, and C. H. Carter, Jr., in *Silicon Carbide and Related Materials: Proceedings of the Fifth International Conference*, edited by M. G. Spencer, R. P. Devaty, J. A. Edmond, M. A. Khan, R. Kaplan, and M. Rahman (IOP, Bristol, UK, 1994), Institute of Physics Conference Series, No. 137, pp. 499–502.

[13] B. K. Ridley, Proc. Phys. Soc. **82**, 954 (1963).

[14] M. P. Shaw, V. V. Mitin, E. Scholl, and H. L. Grubin, *The Physics of Instabilities in Solid State Electron Devices* (Plenum, New York, 1992).

[15] N. G. Hingorani, IEEE Spectrum **32**, 41 (1995).

[16] M. Ruff, H. Mitlehner, and R. Helbig, IEEE Trans. Electron Devices **41**, 1040 (1994).

[17] G. Pensl and W. J. Choyke, Physica B **185**, 264 (1993).

[18] J. Schneider and K. Maier, Physica B **185**, 199 (1993).

[19] M. S. Mazzola, S. E. Saddow, P. G. Neudeck, V. K. Lakdawala, and S. We, Appl. Phys. Lett. **64**, 2730 (1994).

[20] E. Scholl, Z. Phys. B **48**, 153 (1982).

[21] A. A. Lebedev, A. M. Strelchuk, S. Ortolland, C. Raynaud, M. L. Locatelli, D. Planson, and J. P. Shante, Proceedings of the Sixth International Conference on Silicon Carbide and Related Materials, Kyoto, Japan, 18–21 September 1995 (unpublished).

[22] N. Holonyak, Jr., Proc. IRE **50**, 2421 (1962).