NASA Contractor Report 204132

System-Level Integrated Circuit (SLIC) Technology Development for Phased Array Antenna Applications

John Windyka and Ed Zablocki
Sanders
Nashua, New Hampshire

July 1997

Prepared for
Lewis Research Center
Under Contract NAS3–26394

National Aeronautics and
Space Administration

Table of Contents

List of Illustrations

List of Illustrations - Continued

List of Illustrations - Continued

List of Tables

1. EXECUTIVE SUMMARY

Introduction

While the theory of operation of phased array antennas has been known for many years, the actual hardware implementation and successful demonstration of arrays, especially in the K band and above, has been a significant technical challenge. Several factors have impeded array development, including lack of effective packaging and MMIC integration technologies, and generally the need to place (and operate) large amounts of complex circuitry in a very small volume. Furthermore, MMIC device variations due to temperature fluctuation, aging, and fabrication inconsistency presently require that significant amounts of support circuitry be included in the array electronics to maintain proper operation of each element.

> *The System-Level Integrated Circuit (SLIC) Development Program addressed many of these issues by creating a new type of integrated circuit that includes support and interface circuitry merged directly with RF components.*

Several constraints were applied to the design of the SLIC module to focus on a configuration generally representative of future phased array antenna structures. This program has demonstrated a direct path to integrating the SLIC MMIC into a compact, multi-layer structure, in this case configured for use as a two-by-four element phased array module.

> *The SLIC MMIC and module are the building blocks from which larger array antennas, existing as n x n elements, can be assembled for use in space, airborne, and terrestrial communications applications.*

Results

The System Level Integrated Circuit Program demonstrated significant technological advancements required for K Band downlink phased array development. The SLIC module shown in Figure 1 applied several unique technologies to achieve ultra-thin K Band phased array building blocks that have built-in calibration and control.

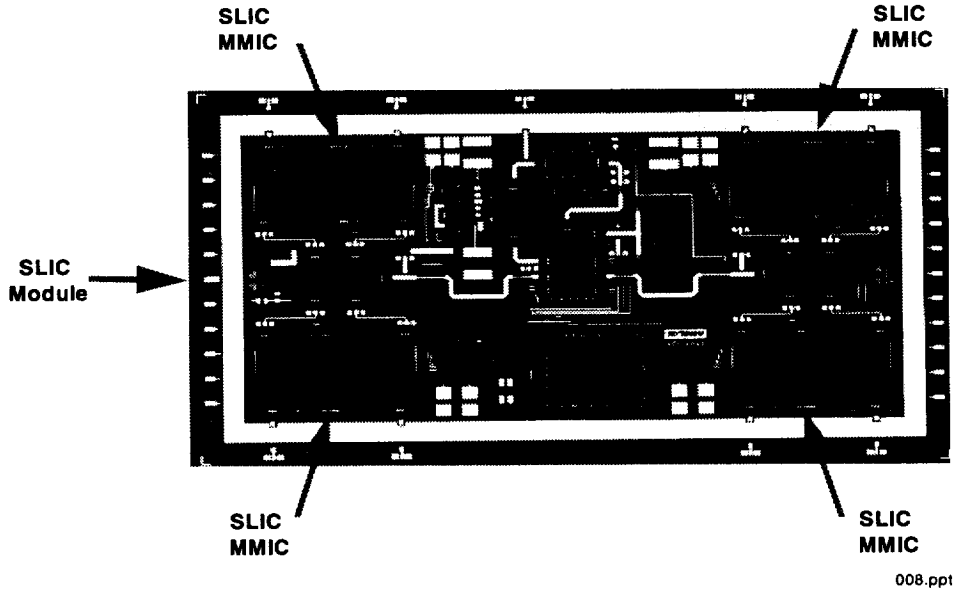


Figure 1. 2 x 4 SLIC Module, Utilizing Four Dual-Channel SLIC MMICs and Integrated Using MHDI

As can be seen in Figure 2, each module contains 4 highly-integrated dual-channel MMICs (Figure 3, SLIC MMIC) each of which have two 3-bit phase shifters, two analog attenuators, shift registers for control data transmission for phase adjustment, an analog automatic gain control, and status monitoring circuitry. RF and control signals are fed to the module via a single photonic link. This combined signal is detected using a PIN diode in the module and subsequent circuitry separates the RF and control signals. The RF signal is amplified and split eight ways to feed the four dual-channel RF MMICs. At the output of each channel on the MMIC, a peak detector samples the output signal level which is in turn fed back to the on board AGC circuitry. The measured signal level is compared to a preset desired level and the attenuator setting is automatically adjusted to retain a constant output.

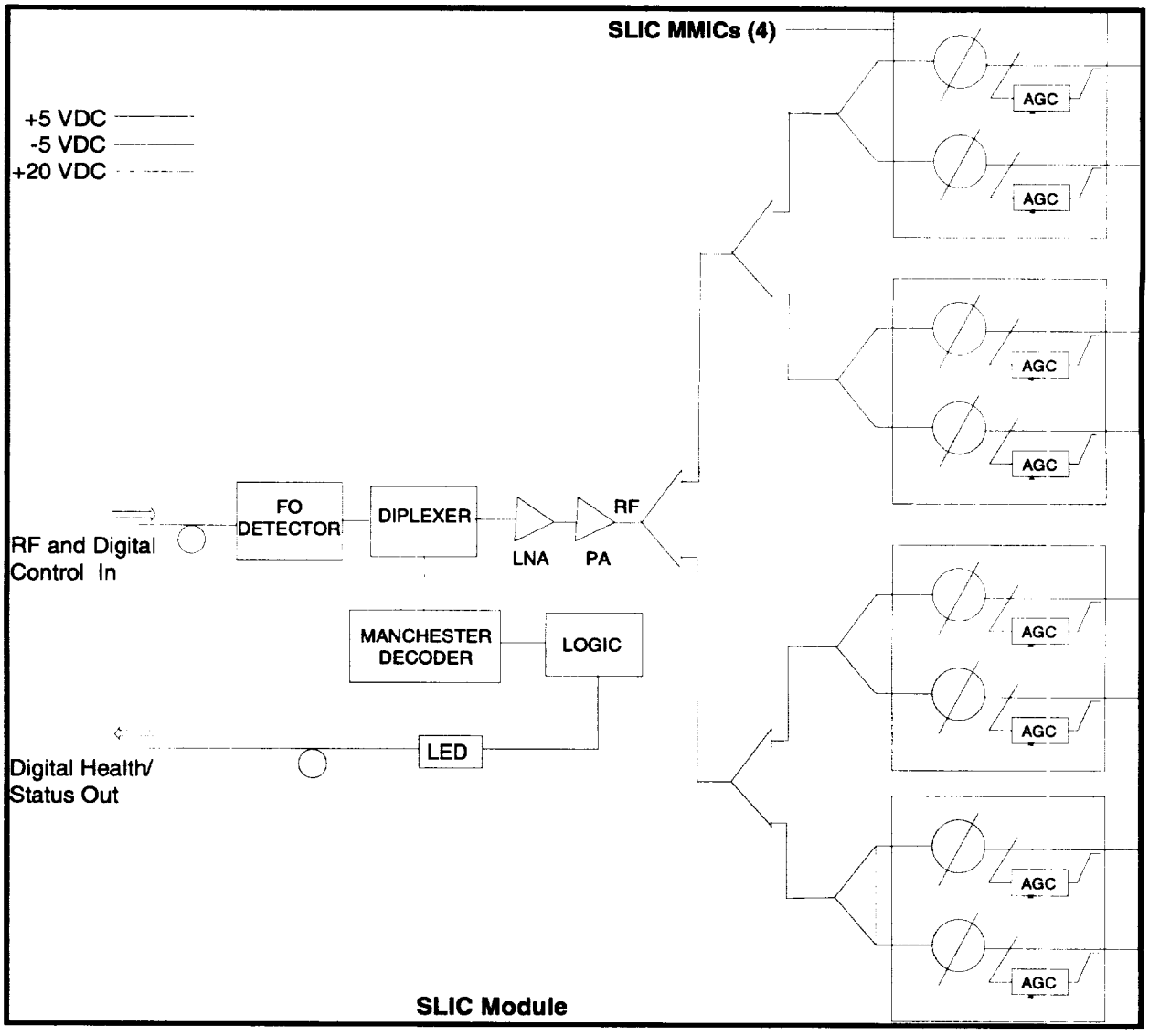


Figure 2. SLIC Module Block Diagram

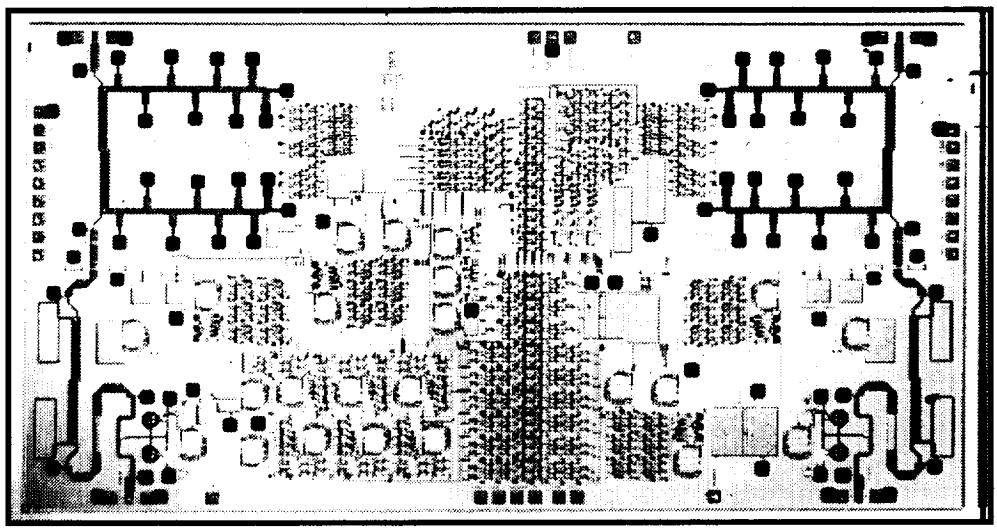


Figure 3. SLIC MMIC

These components are integrated into an 8-element tile module using our unique Microwave High Density Interconnect (MHDI) process which is the enabling interconnect technology leading to K Band tile based phased arrays with the desired level of calibration and control. The modules and MMICs successfully demonstrated the desired built-in test and calibration capability. Shown in Figure 4 is the automatic gain control (AGC) function of the SLIC Module. RF input level to the module was varied over a 8 dB range with the resulting module output power automatically compensated to stay constant within 0.2 dB. Though SLIC Module performance was excellent, overall fabrication yield was lower than expected.

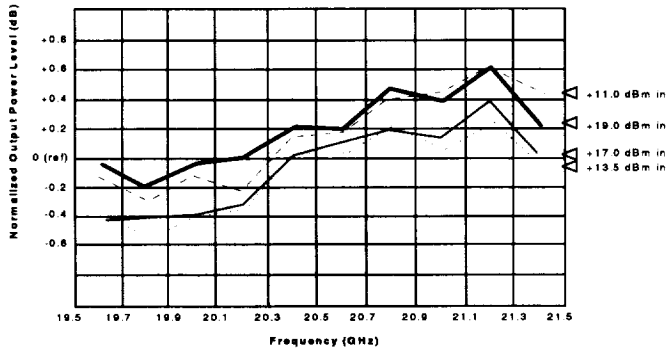


Figure 4. SLIC Module Automatic Gain Control Performance Data

Program Chronology

The SLIC program timeline is shown in Table I. Many program highlights, spanning 5 years of activity, have been included.

Table I. SLIC Program Timeline

YEAR	QUARTER	ACTIVITY	HIGHLIGHT(S)
1992	Q2	Program Start Technology Demo	• Program plan approved • Successful demonstration of artificial delay line (ADL) phase shifter
	Q3	System Tradeoff Study Preliminary Circuit Design	• System trade study begun • Phase shifter and attenuator design completed and modeled • Divider interface circuit (DIC) added to design • Digital/analog designs started
	Q4		• TriQuint added to team for foundry services • GE CR&D added to team for High Density Interconnect (HDI) capability • All SLIC MMIC designs completed • RF peak detector design completed • DIC design nearly complete
1993	Q1		• Layout verification of schematic for SLIC MMIC complete • SLIC module breadboard issues worked with CR&D • At NASA review - *change frequency of operation from 32 GHz to 20.1-21.2 GHz*
	Q2		• Redesign of all MMICcs for K band operation completed • DIC design completed • All digital/analog/RF design completed
	Q3		• System trade study completed

	Q4	Breadboard Development Package, test fixture, and controller development	• Devices received from triquint
			  • good RF performance
			  • *serious problems with digital circuitry*
			• SLIC module layout underway
			• All MMIC and module controller hardware and software completed

1994	Q1	Final Circuit Design	• Redesigned test elements provided to TriQuint for processing • SLIC module design continuing
	Q2		• Test elements received from TriQuint • SLIC module design completed
	Q3	SLIC Fabrication	• Test elements fully tested • SLIC MMIC redesign nearly completed • SLIC module in fabrication
	Q4		• SLIC MMIC tape transmitted to triquint • SLIC module received and undergoing evaluation • Optical link demonstrated
1995	Q1		• MMICS received and test • Unexplained low yield of devices • Module substrates released for assembly
	Q2		• MMICs tested - yield for 3 modules • Modules assembled for MHDI • MHDI underway
	Q3		
	Q4	Performance Testing and Analysis	
1996	Q1		• SLIC modules tested over temperature
	Q2		• Test data evaluated
	Q3		• Final report
	Q4		

Each phase of the program produced tangible results:

Task 1 - Trade Study	• Module requirements defined
	• Module architecture established
	• MMIC and photonics requirements allocated
Task 2 - Detailed Design	• MMICs, module and photonics interface designed
Task 3 - Breadboard	• First generation MMICs fabricated characterized
	• Photonics interface demonstrated
Task 4 - Design Update	• GaAs digital circuits refined
Task 5 - Module Development	• Fully functional SLIC Modules assembled and tested

In summary, the System Level Integrated Circuit Program successfully demonstrated methods of integration leading to viable spaceborne K band downlink applications. Very high levels of on-chip digital and analog control and calibration for the phase/gain control function of the array was successfully demonstrated leading to significant size reductions while providing performance enhancements for long space mission applications. Integrating multiple MMICs along with supporting control and distribution elements into a single ultra-thin tile module using the MHDI process represents the state-of-the-art design and processes that will enable a new generation of high bandwidth communications antennas that are affordable and easily integrated into a wide range of host platforms.

2. SYSTEM LEVEL INTEGRATED CIRCUIT DESIGN

In this section, Sanders establishes the relationship between array performance requirements and subarray packaging and subarray performance requirements. Next we disclose the allocation of these requirements to functional blocks.

2.1 ARCHITECTURE

The next several sections provide a context for our selected approach. The titles and topics of these sections are:

- GOALS AND ADVANTAGES OF THE SLIC APPROACH

  Presentation of selected packaging approach.

- SLIC MODULE LEVEL OF INTEGRATION

  Evaluation of radiating element packing density and influence on efficient utilization of available space.

- IMPLICATIONS OF ARRAY SCAN REQUIREMENTS ON SLIC MODULE IMPLEMENTATION

  Evaluation of the number of radiating elements and element spacing on array side lobe levels and grating lobes. A review of array scan angle requirements.

- ARRAY PERFORMANCE REQUIREMENTS

  Presentation of summary performance levels.

GOALS AND ADVANTAGES OF THE SLIC APPROACH

Recent advances in the state-of-the-art in MMIC technology, photonics and advanced packaging present a visible path to the realization of high-performance, compact millimeter-wave array systems. However, array integration problems, operational and static component variations and thermal effects have impeded the insertion of these technologies into array systems. At this time, as millimeter-wave array designs begin to emerge, a system-level view is necessary for identifying a new technology base that is both reliable and adaptable, to address both the current issues in array integration and to provide a path of growth to future array designs.

Partitioning of array functions is an essential first step to establish common functional building blocks or modular components for design flexibility. Typical interelement spacing (which are driven by array scan requirements and mechanical realities) for millimeter-wave arrays are very small, and force significant array packaging designs. In addition to size constraints, the packaging is also driven by the number of functions incorporated, the precision required to maintain high performance and the retirement of thermal and reliability risks. To meet these challenges for future generations of high-performance arrays, innovative and versatile circuit integration techniques are required.

In order to transition RF MMIC technology into millimeter-wave phased array systems, two system-level design issues must be addressed at the basic circuit level:

1. Control and support circuitry must be incorporated on-chip to regulate amplitude and phase to provide reliable RF performance.

2. This circuitry must merge in a flexible, form-fit design that reduces both interconnect complexity as well as overall array complexity.

The combining of array system-level RF and control circuits onto a single MMIC is particularly attractive in achieving the goals of overhead space reduction, higher performance, reduced array weight , lower parts count and, ultimately lower cost. Integration at the chip level also makes high performance features possible within the constraints of small interelement spacing. System-level integration at the circuit level also provides for flexible building blocks for the arrays of the future, where a single circuit could conceivably contain an entire transmitter or receiver subsystem with a single fiber-optic interface.

In order to simplify and optimize array performance, SLIC functions must be integrated into a single, easily inserted circuit that is fabricated using a technology that provides excellent performance and provides for future enhancements in advanced applications. Microwave High Density Interconnect (MHDI) technology has been chosen for SLIC component integration on the basis of superior electrical performance, ability to optimally integrate SLIC functions, module yield, recurring cost, and superior thermal performance characteristics.

MHDI technology is a leveraging technology for meeting the SLIC Requirements.

SLIC MODULE LEVEL OF INTEGRATION

A subarray SLIC Module approach offers significant advantages over a single-element SLIC Module by reducing the number of interfaces the RF or optical signals must traverse and by sharing appropriate functions between elements to more efficiently use available area.

Effects including packaging loss, VSWR, and unit-to-unit repeatability are reduced by minimizing the number of package and feedthrough interfaces the RF or optical signal must undergo. In addition, a subarray SLIC reduces overall array complexity by reducing the number of package walls, and providing the potential to share (and therefore reduce size and/or quantity of) control, monitoring, feedback, and optical interface functions. The only effect that might be detrimental with increased SLIC element integration is package resonance. However, Sanders' extensive experience with multi-element subarray packages shows that this effect can be overcome by careful package design. Elimination of circuit interconnect wire bonds, as is possible with MHDI technology, improves isolation by reducing discontinuities and high SWRs--a dominant source of cavity resonances.

A subarray SLIC allows more efficient use of limited millimeter-wave array spacing. Figure 5 displays packaging efficiency of a SLIC subarray in terms of the ratio of the available circuit area in the package to element area. As can be seen in the illustration, 70% of the available array area is used for package walls and associated bond pads if a conventional (single element) hermetic, ceramic package approach was used to package SLICs. On the other hand, too high a level of integration can lead to decreased yield resulting in higher cost.

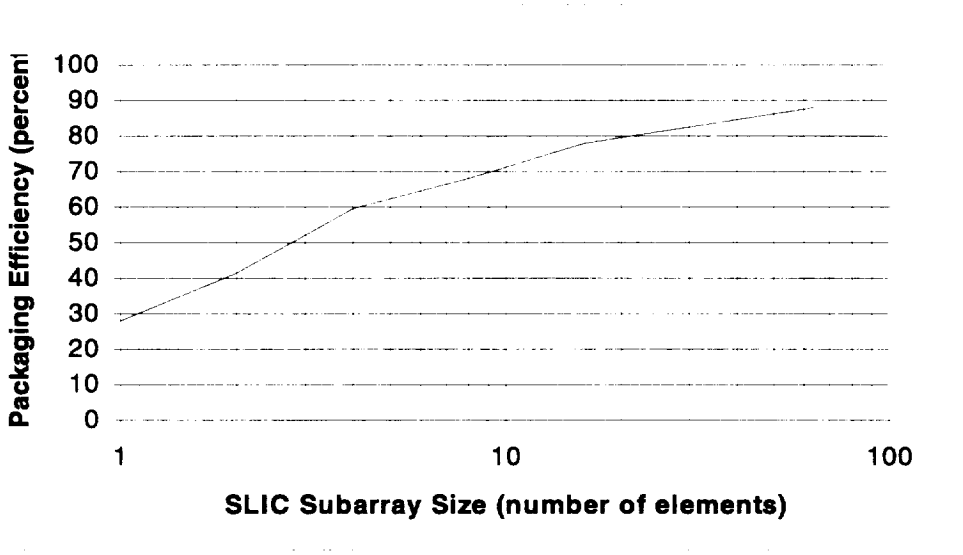


Figure 5. SLIC Packaging Efficiency SLIC Module (Subarray) Size

An 8-element per SLIC Module subarray has been selected because it provides an optimal balance between SLIC area packaging efficiency and SLIC package yields.

IMPLICATIONS OF ARRAY SCAN REQUIREMENTS ON SLIC MODULE IMPLEMENTATION

Many key RF component requirements are driven by array performance requirements. Several requirements are directly related to the overall array size into which the SLIC Module has been inserted. In order to establish derived requirements, two types of array systems are examined:

1. A 96-element (8x12) array with elements on a square lattice (which represents our approach).

2. An infinite array with elements on a square lattice (which represents the limiting case).

For a given array scan requirement, the available area per element diminishes as $1/f^2$ (where f = frequency) resulting in approximately 0.2 in^2 at 30 GHz. Figure 6 shows element spacing at 21.2 GHz (upper band edge) for both our 8x12 array and an infinite array as a function of scan angle.

Our baseline system uses a square grid with an element spacing of 0.33 in. (0.59l at 21.2 GHz), allowing for grating-lobe-free scan of +28.5 degrees. The same chart yields 43.5 degrees for the infinite array. (Grating lobe-free scanning is defined to here to be the extent to which the main beam may be steered until the null of the first grating lobe is positioned at the edge of visible space. In this sense, the infinite array defines the upper bound on the grating-lobe-free scan region.)

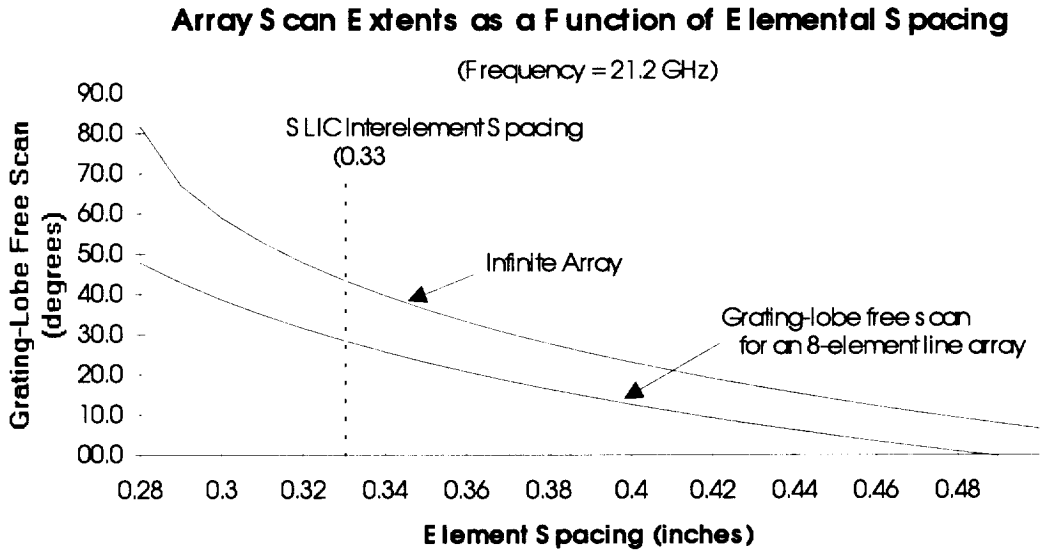


Figure 6. Grating-Lobe-Free Scan Coverage

The corresponding 3 dB broadside beamwidth of the 8 x 12 array in the narrowest aperture dimension as a function of the interelement spacing is illustrated in Figure 7.

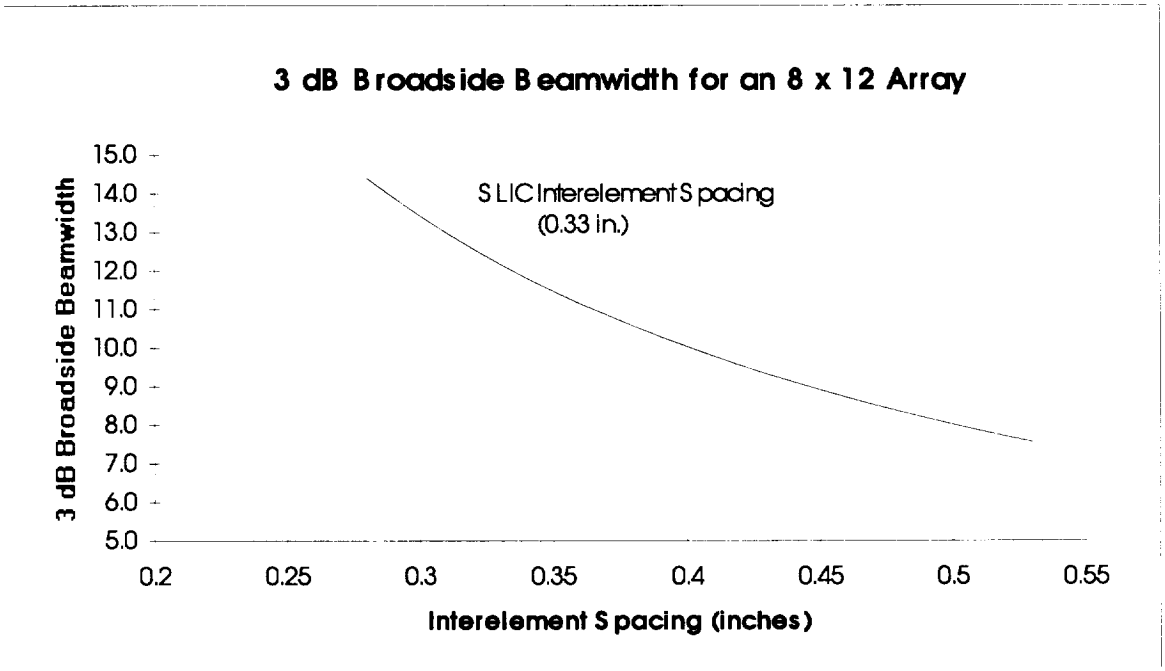


Figure 7. Broadside Beamwidth

The broadside 3-dB beamwidth for the baseline SLIC is 12.6 degrees for the 8-element dimension of an 8 x 12 array.

Amplitude and phase tracking requirements are driven largely by radiated power and beam shape characteristics. For array applications where sidelobes are relatively unimportant, allowable elemental phase and amplitude errors are dictated by loss of antenna directivity. Hence, we shall focus on this array characteristic as a driver for phase shifter and attenuator system requirements.

ARRAY PERFORMANCE REQUIREMENTS

SLIC performance requirements (as defined within Attachment B of NASA's Statement of Work, System Level Integrated Circuit Development Program) have been summarized in Table II. This table only includes NASA specified requirements addressing SLIC performance.

Table II. SLIC Performance Requirements

ITEM	REQUIREMENT	LIMIT
A	Operating Frequency and Bandwidth	20.2 GHz to 21.2 GHz. or higher
B	RF Insertion Loss	< 8 dB for any and all phase states, variation <0.75 dB across the band
C	RF Insertion Loss/gain Control	Shall not vary by more than 1 dB to any change in phase state.
D	RF Impedance	50 ohms
E	Return Loss	<-18 dB
F	Phase Shift States	Over a scan range of +/- 20 deg's in 5 deg. steps, beam steering in azimuth and elevation (capable of being randomly selected)
G	Phase Shift Repeatability	Within 5 electrical degrees
H	Phase Shifter Response Time	< 1 microsecond
I	RF Power at Output of Phase Shifter	10 mW CW
J	Configuration	SLIC shall be designed for TRANSMIT only, {fundamental design should be compatible with RECEIVE and TRANSMIT operation}.
K	Phase Shifter	Full monolithic construction, no discrete components, no wire bonds, no off chip impedance matching.
L	SLIC Circuit	Individually controllable, addresses if appropriate, shall be permanent
M	SLIC Devices	Designed and fabricated using standard processes for passivation and protection.
N	Fabrication and Process	< $200 (REF. 1992) for >5000 Piece quantities.

2.1.1 SLIC Module

2.1.1.1 Performance Requirements

The primary requirement of this program is to develop an advanced integrated circuit that merges RF MMIC technology with control, support and interface circuits to facilitate integration into compact, lightweight, reliable phased array antennas. We are required to provide this capability in the 20.2 - 21.2-GHz downlink band, and we have selected two packaging techniques to realize these requirements:

1. Integrate MMIC-level digital and analog control functions on the same chip with the RF circuitry, using innovative GaAs MMIC design techniques to combine these features.

2. Integrate subarray-level digital, analog and RF functions in a compact form, with the best chip technology for each, using Microwave High Density Integration (MHDI) process.

PRIME POWER

An important objective from the standpoint of physical interfaces and prime power requirements is to minimize the number of prime power supply voltages required. Multiple voltage supply requirements lead to extra bulky interfaces and added size, weight and complexity to the prime power supply. Minimizing the number of DC interconnections required by the SLIC Module is a high-priority goal for this program. The results of our trade study are defined in Table III.

Table III. SLIC Prime Power Requirements

COMPONENT	VOLTAGE, CURRENT, POWER REQUIREMENTS FOR COMPONENT	TOTAL POWER REQUIREMENT FOR COMPONENT PER SLIC MODULE
SLIC MMIC Analog and Digital Circuitry	+5V / 25 mA / 125 mW -5V / 25 mA / 125 mW	+5V / 100 mA / 500 mW -5V / 100 mA / 500 mW
RF Amplifiers: RF Driver Amp Power Amp	 +5V / 30 mA / 150 mW +4V / 750 mA / 3000 mW	 +5V / 30 mA / 150 mW +4V / 750 mA / 3000 mW
Optical Detector	+20V / 10 mA / 200 mW	+20V / 10 mA / 200 mW
SLIC Divider Interface Chip	+5V / 5 mA / 25 mW -5V / 5 mA / 25 mW	+5V / 5 mA / 25 mW -5V / 5 mA / 25 mW
Manchester Decoder	+5V / 10 mA / 50 mW	+5V / 10 mA / 50 mW
	SLIC Module Totals	+5V / 375 mA / 3725 mW -5V / 105 mA / 525 mW +20V / 10 mA / 200 mW
	SLIC Module Total Prime Power Requirement:	**4450 mW**

For this power supply configuration, the SLIC module requires a total of 4.45W. The +5V rail requires 84 percent of the total power requirement. Only 4.5 percent of the total power is required by the +20V rail.

PHASE SHIFTER REQUIREMENTS

The following specifications outlined in the Table II, SLIC Performance Requirements, relate directly to the phase shifter:

1. The SLIC devices shall operate over a continuous 1-GHz wide RF band.
2. The phase shifter shall be required to provide the capability to steer the antenna radiation pattern (main beam) over a scanning range of ±20 degrees from broadside in at least 5 degree steps. The beam steering angles shall be variable in 2 dimensions.
3. The phase shifter shall be capable of providing the selected phase delay to within 5 electrical degrees each time the state is selected.
4. The phase shifter shall be capable of switching between any two delay states in no more than 1 msec.
5. The phase shifter shall be capable of providing 10 milliwatts of CW RF power at its output.

Granularity of beam steering for large arrays (~100 or more elements) is dictated by the effective number of elements in the projected plane of the steering angle. For the 8 x 12 array on a 0.33" grid, the maximum effective element spacing in any given steering direction is 0.33", or 0.59l. For steering in the direction of the narrowest direction of the array, the number of elements is 8, and the largest effective interelement spacing is realized (0.59l). Based on the work by Hatcher,[1] Table IV defines the beamsteering granularity for the array in this dimension based on phase shifter quantization of from 2 (2 states) to 6 (64 states) per element.

Table IV. Array Beamsteering Granularity For An 8-Element Array

N NUMBER OF PHASE SHIFTER BITS	DQ_1 FIRST BEAM LOCATION OFF BROADSIDE	$\bar{D}Q$ AVERAGE BEAMSTEERING POSITION GRANULARITY
2	1.13 Degrees	0.75 Degrees
3	0.57 Degrees	0.38 Degrees
4	0.28 Degrees	0.19 Degrees
5	0.12 Degrees	0.08 Degrees
6	0.08 Degrees	0.05 Degrees

[1] B.R. Hatcher, "Granularity of Beam Positions in Digital Phased Arrays", *Proceedings of the IEEE*, Vol. 56, No. 11, November 1968, pp.1795-1800

The first beam position is the largest beamsteering step for ideal arrays, and should be used here to define the beamsteering granularity. The average granularity is statistically 2/3 that of the first beam position (see Hatcher). For the cases of 2 to 6 phase shifter bits, we can exceed the beamsteering granularity requirements by factors of 6 to 100.

Phase shifter components typically influence the directivity of the array system in two respects. First, the quantization of the required phase shift and the limitation this imposes on the ability to approximate the exact phase requirement for each element results in the directivity loss identified in Figure 8. This is a direct function of the number of phase states each element can realize (which is directly related to the number of phase shifter control bits).

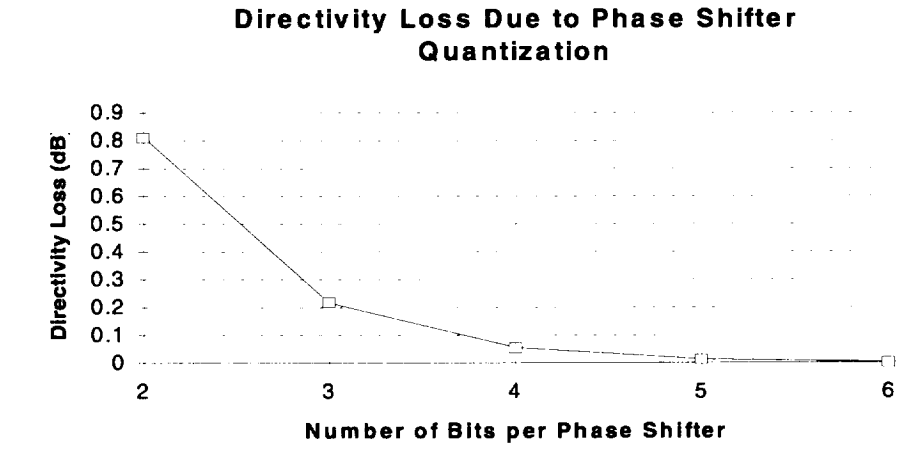


Figure 8. Directivity Loss

Second, error in the accuracy of the phase shifter elements to accurately realize a required phase shift also manifests itself in a loss of array directivity as shown in Figure 9. This is not a function of the number of bits; it is a function of the RMS phase error of each element.

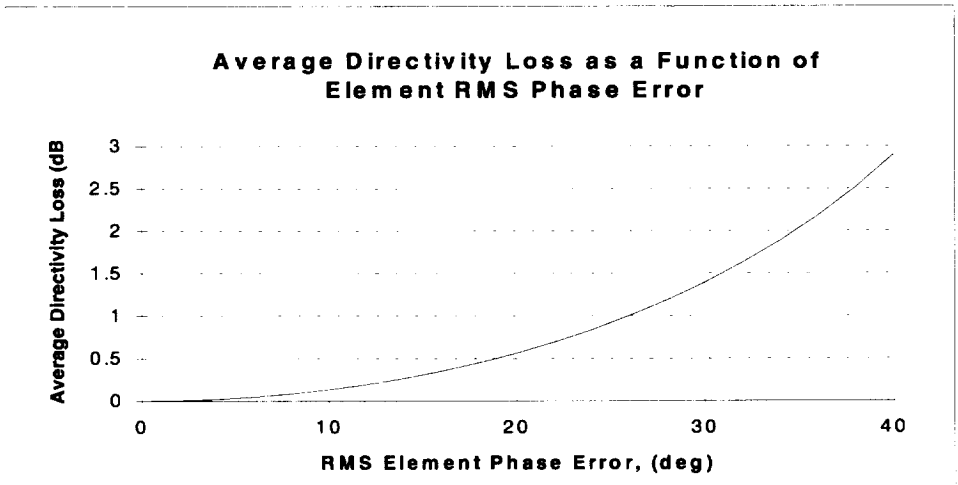


Figure 9. Average Directivity Loss

Another criterion which may be used to set the number of phase shifter bits is the average sidelobe level (SLL) which results from phase shifter quantization. Figure 10 presents the average SLL which results when the error between the required phase shift of element i and the actual phase setting is a random variable with a uniform distribution over the interval of phase corresponding to the LSB phase.

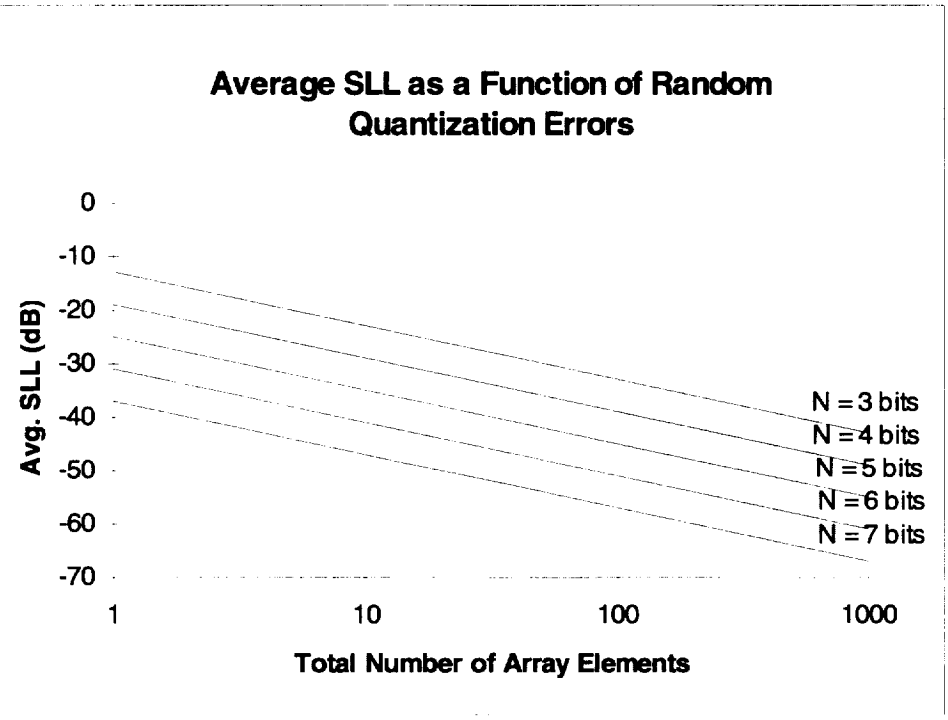


Figure 10. Average SLL

However, since no requirements have been placed on the size of the array or the required SLLs, this information does not provide a discriminant for the choice of a phase shifter. For array systems, particularly those requiring low sidelobes, this information is of critical importance.

For this program, we have selected our proven 19-22-GHz 3-bit artificial delay-line (ADL) phase shifter design to be fabricated with TriQuint's QED/A process. This phase shifter component can meet or exceed all of the specifications which directly relate to it. The specified and projected performance of the SLIC phase shifter is indicated in Table V.

Table V. Specified Performance For Phase Shifter

REQUIREMENT	LIMIT
Frequency	> 20 GHz (BW = 1 GHz)
Loss (Maximum)	8 dB
D Loss Over Frequency (Maximum)	0.75 dB
D Loss Over Phase State (Maximum)	1 dB
Return Loss (Z_0 = 50W)	18 dB
Phase Increment	Proposed 45 degrees
RMS Phase Error	Proposed 6.7 degrees
Maximum Power	10 dBm

When inserted into the 96-element (8 x 12) subarray on a 0.33" square lattice element spacing, the performance levels of Table VI are expected.

Table VI. Array Performance Metrics

PARAMETER	LIMIT
Largest Beamsteering Granularity	0.57 degrees
Directivity Loss due to Phasor Quantization	0.22 dB
Directivity Loss due to RMS Phase Error	0.06 dB
Maximum 3 dB Broadside Beamwidth	12.6 degrees (no element pattern)

VARIABLE ATTENUATOR REQUIREMENTS

Several system-wide requirements flow down to the variable attenuator:

1. All SLIC devices must operate over a continuous 1-GHz wide RF band.

2. The phase shifter shall be capable of providing the selected phase delay to within 5 electrical degrees each time the state is selected. Therefore, the effect of the variable attenuator on the phase shift of the SLIC channel must be minimized.

3. The phase shifter shall be capable of providing 10 milliwatts of continuous-wave RF power at its output. This requires the variable attenuator to not only accommodate this power level, but to also be able to dissipate the power level when set to an attenuation of at least 10 dB, or 9 mW. If the variable attenuator is used to "turn the element off", it must be capable of dissipating the full 10 mW.

These requirements shall be imposed on the variable attenuator design.

There are two ways to view the necessity and operation of the variable attenuator and its function in the larger role of the AGC loop:

1. To compensate for operational gain variations for the individual channel of which it is a member. These gain variations may be a function of:
    - phase shifter state-to-state gain variations,
    - power amplifier (if included) variations due to varying drive level,
    - thermally-induced RF component gain variations, or
    - RF component aging effects during the mission.
2. To compensate for element-to-element (channel-to-channel) gain mismatch. These gain variations may result from:
    - MMIC processing variations (particularly for amplification devices),
    - component aging differences from channel-to-channel,
    - component interconnect variations from channel-to-channel, and
    - beamformer loss variations from channel-to-channel.

Furthermore, the variable attenuator may be used to "fine-tune" or even provide for an array taper to provide beam shaping by using the programmable power set point adjustment on the AGC loop. It is probably more advisable to provide the taper control in another part of the system and use the attenuator for "fine tuning" of the taper, because significant tapers are required for low-sidelobe applications. When the signal is to be attenuated to a large degree, the power which must be dissipated in the load resistors of the attenuator becomes significant, leading to higher temperatures within the subarray assembly and needless prime power waste. Table VII illustrates the range and type of variations which could be compensated with the AGC loop and attenuator.

Table VII. SLIC System Gain Error Sources

ERROR ELEMENT	TYPE (OPERATIONAL/ STATIC)	EXPECTED VARIATION RANGE	TOTAL EXPECTED VARIATION RANGE
Phase Shifter State-to-State Variations	Operational	+/- 0.5 dB	1.0 dB
Power Amp Gain Variation Due to Temperature Changes	Operational	0.01 dB/DEG C +/- 1 DB over +/- 50 DEG C Range	1.0 dB
Component Aging (with power amp)	Operational		2.0 dB
Power Amplifier Variations Due to Drive Level Variations	Operational		1.0 dB
Phase Shifter MMIC Processing Variations	Static	+/- 0.5 dB	1.0 dB
Power Amplifier MMIC Processing Variations	Static	+/- 1.0 dB	2.0 dB
HDI Processing Variations	Static	+/- 0.25 dB	0.5 dB
Variable Attenuator MMIC Processing Variations	Static	+/- 0.5 dB	1.0 dB

The total operational variations for a single SLIC channel are on the order of 5 dB (+/-2.5 dB), while static (channel-to-channel and non-varying) variations are on the order of 4.5 dB. In order to compensate for all of these error sources, a total dynamic range of 9.5-10.0 dB is required of the (continuously variable) analog attenuator.

The operational variations will dictate the dynamic range requirement of the analog AGC loop (this loop includes not only the attenuator itself, but also the differential amp, sense coupler and peak detector). The other variations (static) can be accommodated through the use of the power set point in order to provide an optimum level for each channel about which the operational variations will occur. Provision of several power set points could allow the AGC loop to be set to a range which will optimize the sensitivity of the loop.

Another trade which could be examined is that of the number of bits required in the control of the power set point. This parameter is, however, dominated by the device characteristics in that the minimum dependable voltage reference is limited to about 40 mV. This limitation forces a limit to the number of reliable bits to six over a voltage range of 2.5 volts. Therefore, a 6-bit control DAC will be used for programming the power set point. Figure 11 illustrates the portions of the AGC pertinent to this discussion.

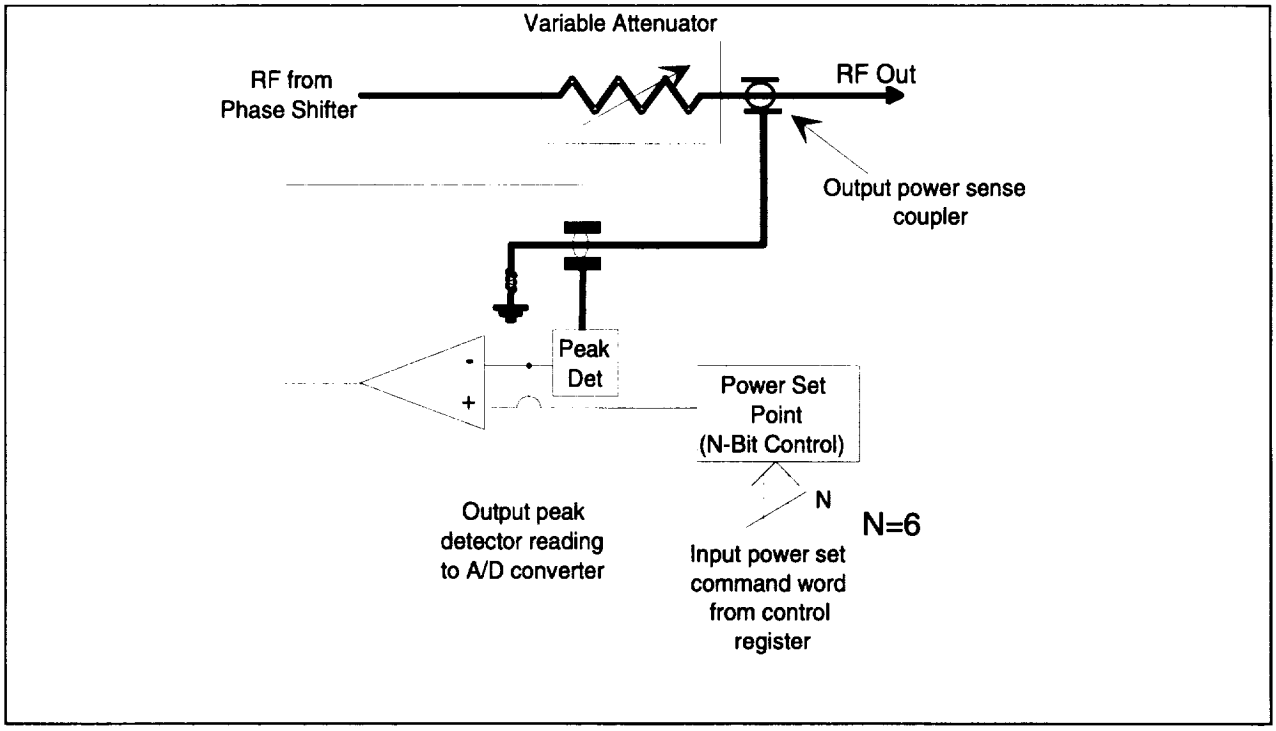


Figure 11. Basic Structure Of The AGC/Power Set Loop

As mentioned in the previous discussion, the analog portion of the AGC loop (sense coupler, peak detector, analog differential amplifier and variable attenuator) shall be held accountable to provide at least 4.5 dB of operational dynamic range, independent of the power set point. The power set point control should be capable of shifting this dynamic range into a range which has been precalibrated or adjustment by the controller in order to provide optimum operation for that channel. We would like to have states which accommodate driving the variable attenuator to a maximum ON condition, a maximum OFF condition, and states in between in order to accommodate calibration of the array, minimization of array output on an elemental basis, and multiple set points. Furthermore, we would like the intermediate states to be more dense in the higher power states, allowing for finer control near high power output levels, since we anticipate that the majority of the loop operation will occur in this range. This will allow us to realize optimal efficiency and prevent the "dumping" of excess power.

During the design process of the analog attenuator, measured FET device data has been used in a microwave circuit simulator package to characterize the attenuation response of the attenuator block. The projected attenuation characteristic has been fit to a 9-term polynomial expansion approximation, shown in Figure 12.

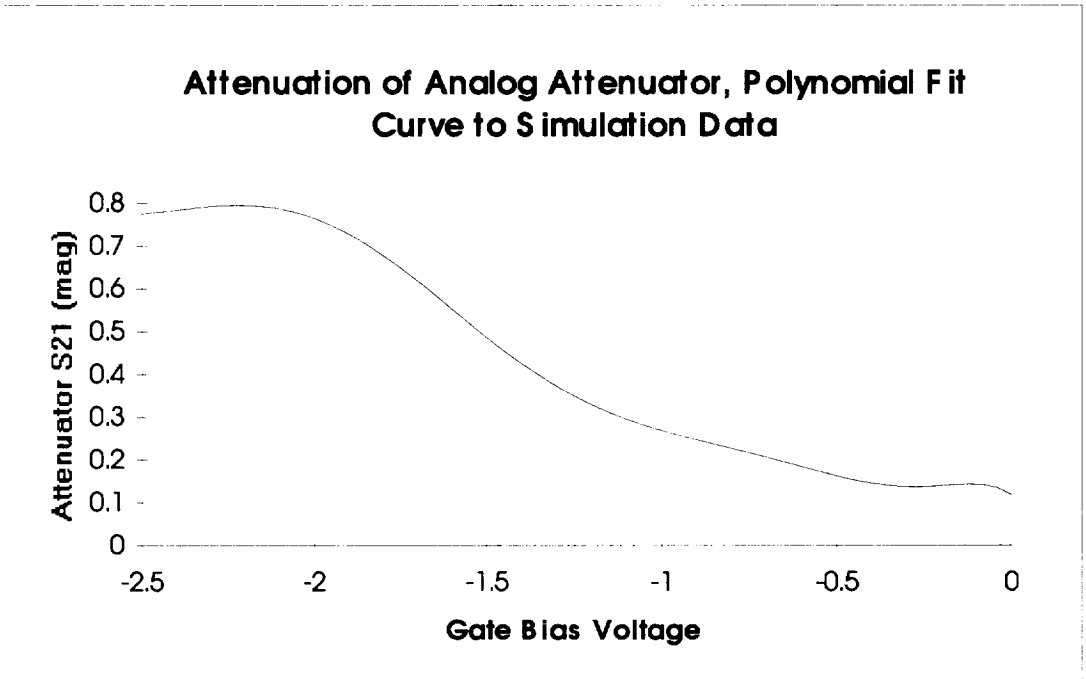


Figure 12. Attenuation of Analog Attenuator

Figure 13 shows the simulated attenuation of the subsystem as a function of DAC state. The attenuation provides a monotonic attenuation curve from a minimum attenuation of about 2.2 dB (state 63) to an attenuation of about 17.25 dB (state 9). The nearly linear characteristic of this curve, particularly at the lower attenuation states, is important to ensure the stability of the closed-loop gain control subsystem.

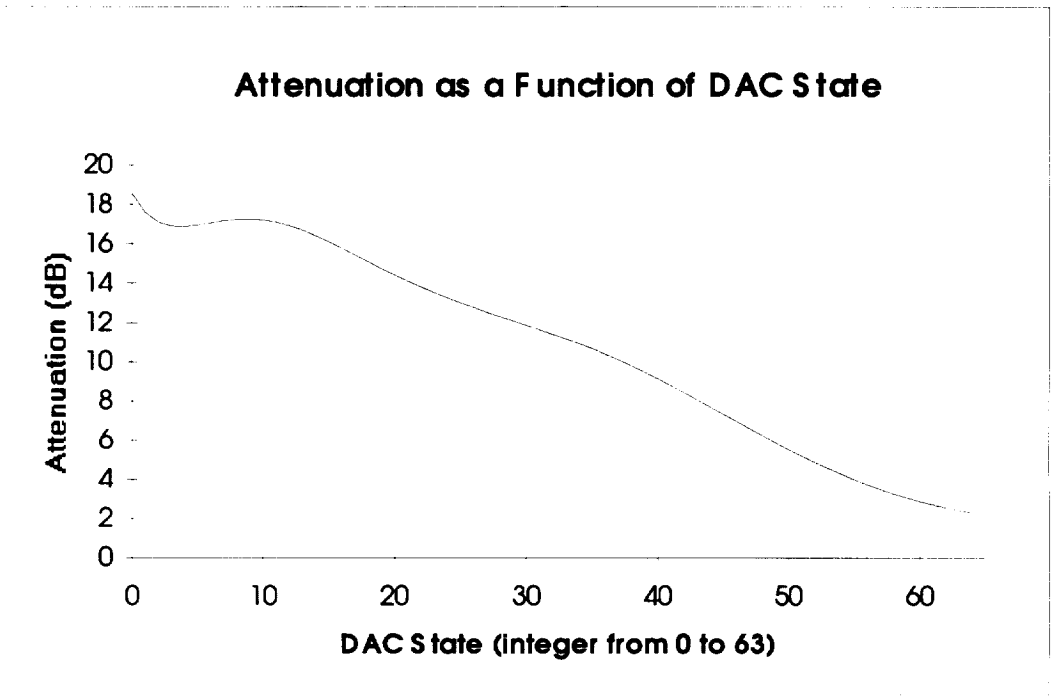


Figure 13. Attenuation Control

2.1.1.2 Functional Allocation

SLIC FUNCTIONAL OVERVIEW

A single SLIC subarray package contains the RF, control and performance monitoring subsystems for eight RF channels. It requires only two fiber-optic interfaces and three bias interfaces {redundant voltage interconnections have been provided to facilitate troubleshooting and debugging efforts so that a total of eight bias interconnections are shown in block diagrams of the SLIC Module}. One fiber-optic interface carries the RF and digital control inputs to the SLIC subarray; the second provides a digital status/health return link. These fibers provide a flexible, lightweight interface system for the subarray.

The SLIC subarray is a subarray construct suitable for use as a building block for a "tile" construct phased array antenna. The subarray which has been developed is for a transmit system, and contains channel-level signal phase and amplitude control. In addition, the subarray incorporates amplitude control, amplitude compensation for thermal effects, bias regulation, power conditioning and performance monitoring circuitry on a channel-by-channel basis.

COMPLETE SLIC SUBARRAY SYSTEM

The subarray system developed under this effort has internal power amplifiers which provide the ability to compensate for preceding power amplification stages. Figure 14 shows a functional block diagram of the 8-element SLIC subarray system. The SLIC subarray package boundaries are denoted by the dashed line; components located outside this boundary are not contained within the SLIC package. The chip-level components are shown as shaded boxes, and are interconnected by the MHDI process.

RF and digital control signals are brought into the SLIC subarray package via a single optical fiber and are detected by an Epitaxx InGaAs p-i-n photodetector diode (marked "Detector" in the architecture drawings).

The detector output is passed to the Divider Interface Circuit (DIC) MMIC, which is a GaAs MMIC incorporating an RF/digital diplexer, power amplifier interface, a single RF power divider and detection/conditioning circuitry for the subarray input digital control signals.

The RF signal is passed from the DIC MMIC to a pair of 1:4 RF power divider chips, which in turn pass the divided RF to the SLIC MMIC inputs. These divider chips each contain three 1:2 RF power dividers, implemented on GaAs to provide extremely compact power division resulting in smaller subarray module sizing requirements. The dual-channel SLIC MMICs then condition the RF as desired, and the RF outputs are taken and directed to the outside of the module package. Coplanar probe pads are provided as exterior RF interfaces, providing the capability of de-embedded measurements.

RF sense couplers are implemented on the SLIC MMIC in order to feed RF amplitude sense signals back to the AGC loop. These couplers are designed to have a low level of coupling, in order to minimize their effect on the transmitted signal power. Since the RF level at each MMIC output is sufficiently high due to the inclusion of the power amplifiers, the RF sense couplers are implemented on the SLIC MMIC rather than outside the module package. In the final system implementation these sense couplers would be located after the transmit amplifier just prior to the antenna element.

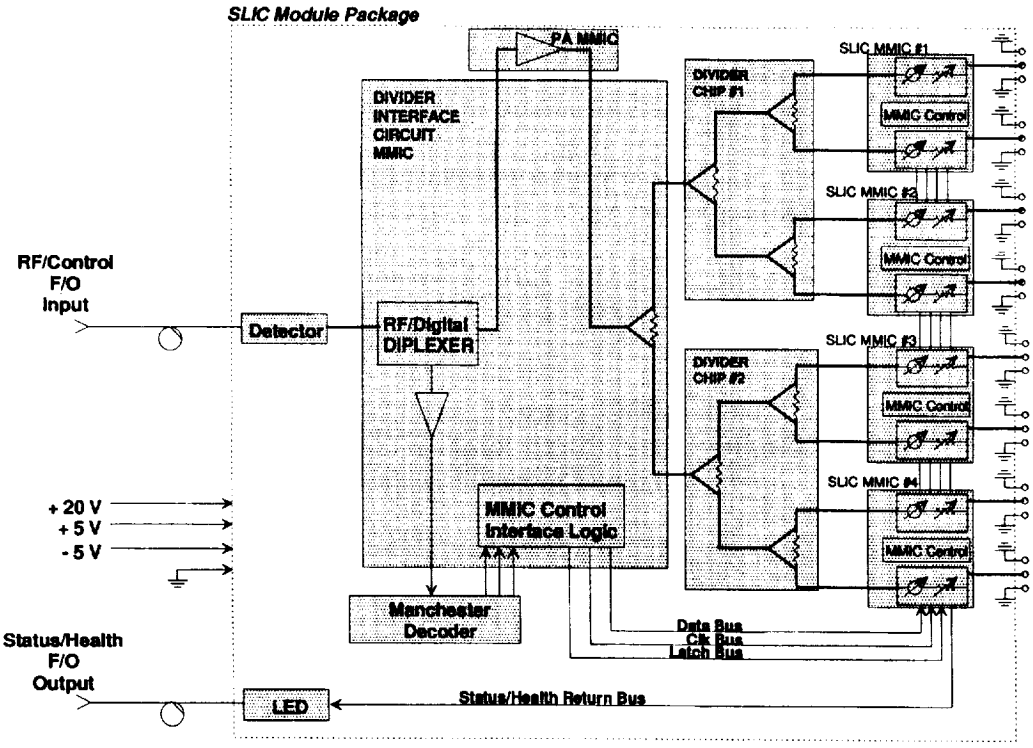


Figure 14. SLIC Module Functional Block Diagram

2.1.2 SLIC MMIC

As can be seen in the idealized SLIC Module layout, provided in Figure 15, the SLIC MMIC is the most dominant contributor to the SLIC Module implementation.

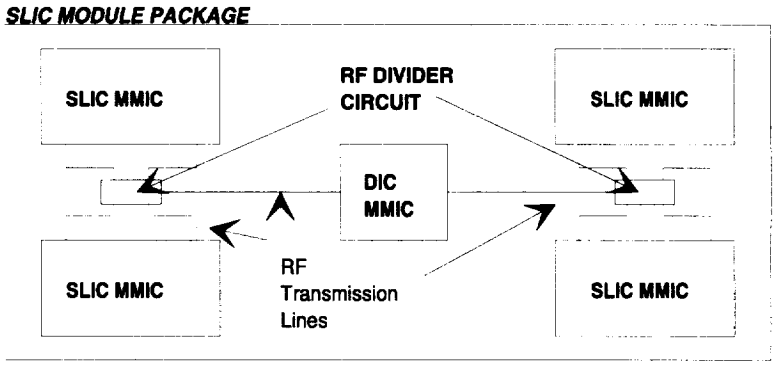


Figure 15. SLIC Module Layout

SLIC MMIC architecture is shown in Figure 16. The SLIC MMIC combines RF, analog and digital circuitry on the same MMIC, providing all interface, control and performance monitoring circuitry for each of two channels.

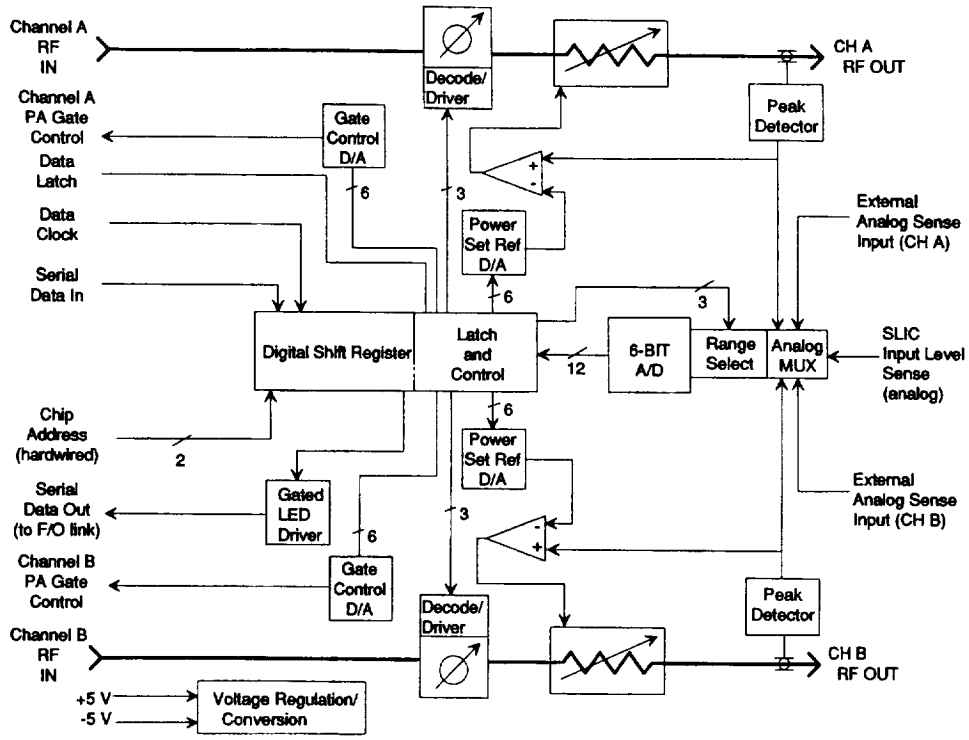


Figure 16. SLIC MMIC Functional Block Diagram

RF transmission lines are shown in bold, to distinguish them from analog and digital lines. In order to reduce the total size required for implementing the MMIC in an 8-element subarray package, two RF channels have combined onto a single MMIC, sharing relevant control and monitoring circuitry where possible. This dual-channel approach reduces the total GaAs dedicated to implementing eight channels by more than 30%--a significant cost and module space savings.

Two separate RF channels are shown which share shift register, latch and control, analog-to-digital (A/D) converter and MUX subsystem and voltage regulation and control subsystems. As the MMIC design progressed, we found that the shift register/latch and A/D subsystems accounted for nearly half of the total MMIC space dedicated to digital functions.

SLIC MMIC RF SUBSYSTEMS

On the SLIC MMIC, there are three major RF components:

1. 3-bit Artificial Delay-Line (ADL) phase shifter,
2. Analog-controlled variable attenuator, and
3. RF peak detector, which provides an analog output in response to the peak of the RF signal applied at its input.

The 3-bit ADL phase shifter provides a 335 degree phase shift capability, in 45 degree incremental phase steps. The heart of the phase shifter is an artificial delay line which behaves as a transmission line with

an electronically switchable path length. The ADL phase shifter will realize the desired phase shift in a much smaller physical area than conventional switched-line phase shifters and with lower insertion loss.

Figure 17 illustrates in greater detail the principal behind the artificial delay line (ADL) reflection-type phase shifter. The phase shifter circuits are comprised of shunt FET devices used as switch elements separated by a series of microstrip lines. Source-to-drain capacitances of pinched-off FETs and the inductances of the series microstrip lines form an artificial transmission line. The effective impedance of the artificial transmission line is determined by the characteristics of the series microstrip lines (impedance and electrical length) and the FET off-state capacitance. If the gate of a shunt in one segment is provided with 0V bias, the resulting low on-state resistance of the FET presents a highly reflective (nearly short circuit) low impedance to the previous segments. The phase of the reflected power, resulting from propagation over a physical distance to the reflective termination and back again at a given phase velocity, determines the shift in phase.

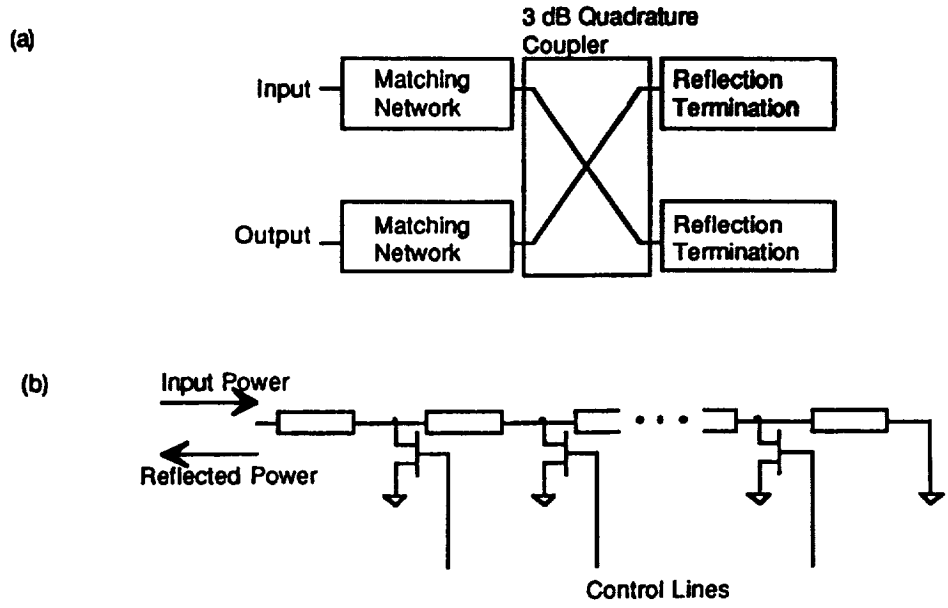


Figure 17. SLIC MMIC Artificial Delay Line Block Diagram

The ADL approach requires a minimum of eight (2^3) segments, and thus eight control lines, for a 3-bit phase shifter. This provides phase state coverage from a reference phase (0^o) to 335^o relative to the reference phase in 45^o increments.

The analog attenuator is a reflection-type attenuator, and is depicted schematically in the box in Figure 18. The circuit provides up to 11 dB of attenuation range by changing the amount of RF absorption in the terminations of a quadrature 3-dB coupler. The amount of negative bias voltage supplied to the gates of the FETs sets the conduction level of their RF paths from drain to source. When the FETs are pinched

off, a microstrip line provides a resonance which is seen by the coupler ports as a highly reflective termination, and the power is reflected back to the coupler and passed along to the output in the circuit. When the FETs are turned on and conduct, the power is shunted around the resonant line and dissipated in the termination resistances.

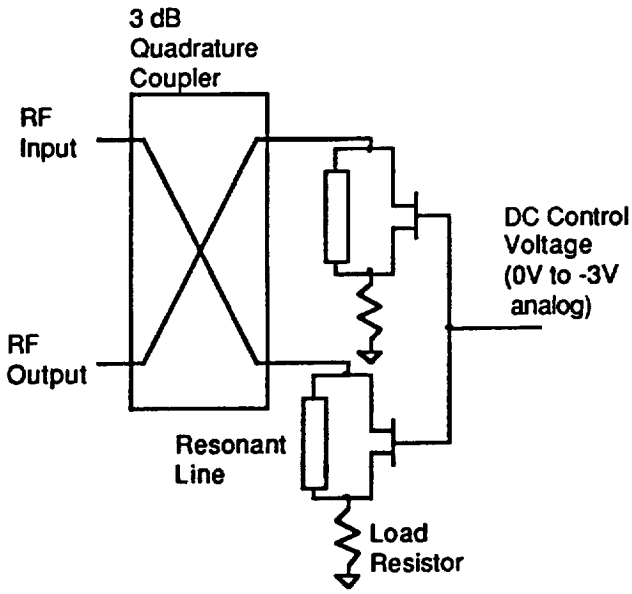


Figure 18. SLIC MMIC Analog Attenuator Block Diagram

The RF peak detector circuit is crucial to the AGC/compensation loop. The RF portion of the circuit is the RF level sensor. The RF level sensor is a voltage doubler which uses the RF swing to pump charge onto a hold capacitor proportional to the peak-to-peak swing. The voltage on this capacitor (which varies with the amplitude envelope of the RF signal) is sensed and compared against an accurate (programmable) reference voltage to derive an error signal for the AGC loop. The error signal is amplified and applied to the analog attenuator, thus applying an RF gain control. This (peak detector) circuit is extremely compact, and occupies very little GaAs space on the chip.

In order to accomplish compensation of RF power output level variation with MMIC temperature, some method of eliminating temperature-induced variation is required. This feature is provided in the RF level sensor circuit. A schematic description of the temperature invariant RF level sensor is shown in Figure 19.

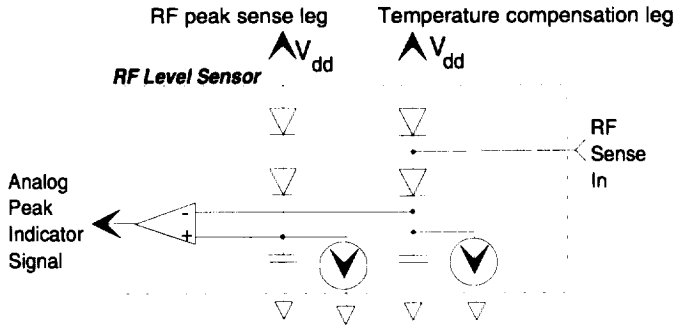


Figure 19. RF Level Sensor Schematic

A second independent hold capacitor subcircuit provides a reference voltage for a differential amplifier. Then, as the rectifier diode performance drifts with temperature, the differential amplifier provides cancellation using common mode gain and the tracking performance of the reference diode. Although there is some conductivity change in the diodes with respect to temperature, their resistivities are very small compared to the impedance of the charging capacitors at the RF frequency, and the change is negligible.

2.2 COMPONENT DEVELOPMENT

Figure 20 illustrates the GaAs devices populating a single SLIC Wafer. All elements were designed and developed for use on the SLIC program.

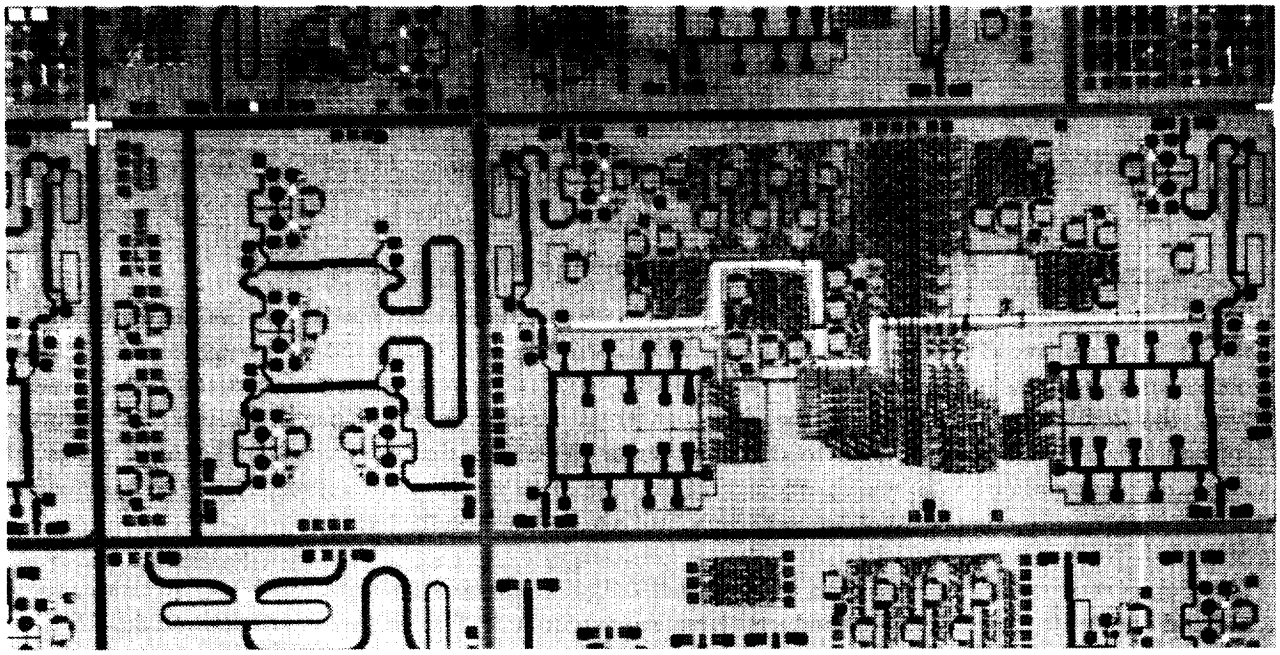


Figure 20. SLIC Wafer

Depicted in the photograph are: the SLIC MMIC, the Divider Interface Chip (DIC), the DIC RF Divider, the Phase Discriminator, and a variety of other test elements.

In the following sections we provide detailed descriptions for the circuits and assemblies developed for use on this program.

2.2.1 SLIC MMIC Design

The SLIC MMIC implements several different functions identified in the module block diagram. RF elements (phase shifter, attenuator, peak detector), analog components (op amp's), as well as digital control elements (shift register, Analog to Digital Converter, Digital to Analog Converter) have been implemented using GaAs devices. Figure 21, CALMA plot of the SLIC MMIC, has been provided to illustrate the levels of integration achieved within the SLIC MMIC.

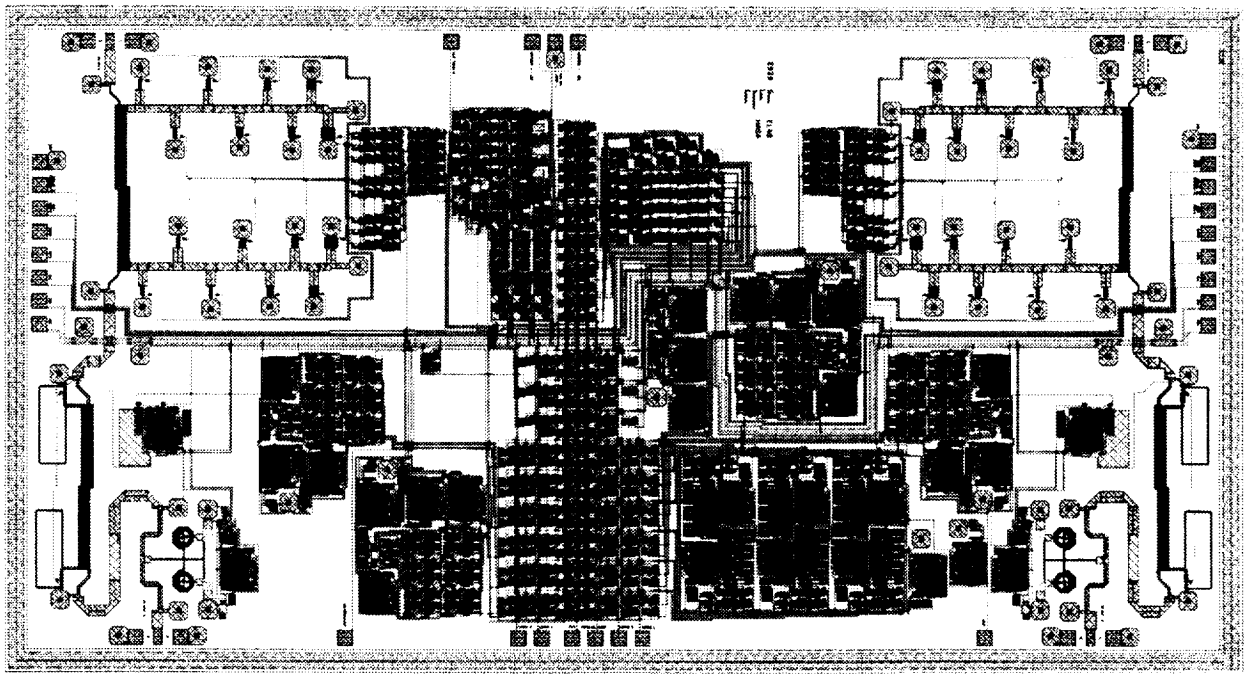


Figure 21. SLIC MMIC CALMA Plot

2.2.1.1 RF Functions

Each SLIC MMIC incorporates three RF functions: phase shift, attenuation, and peak detection. Implementation information for each circuit is provided in the next few paragraphs.

2.2.1.1.1 Phase Shifter

Figure 22 provides a detailed illustration of the artificial delay line phase shifter developed for the SLIC Program.

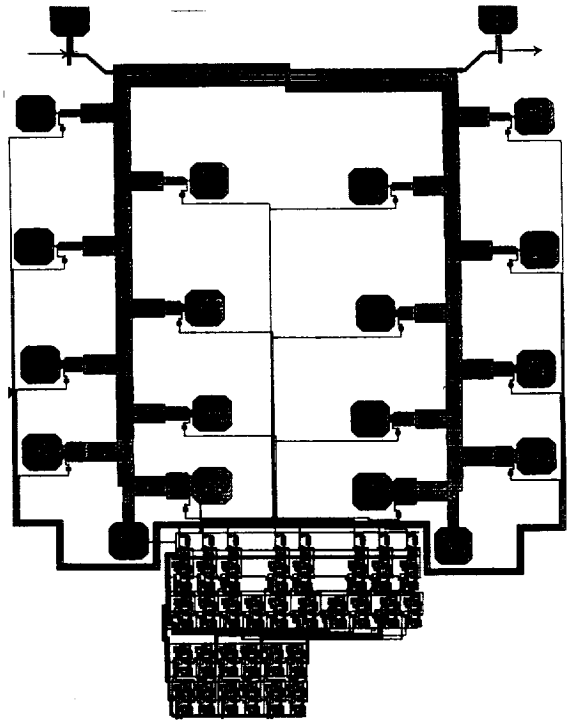


Figure 22. SLIC MMIC Phase Shifter Implementation

The first line plot, Figure 23, shows the excellent performance of the phase shifter in terms of relative phase shift for all eight states. As can be seen in the plot, the relative phase shift of 45° is maintained over a 2-GHz band (19.5 to 21.5 GHz). The second line plot, Figure 24, illustrates the exceptional insertion loss performance of the phase shifter. Insertion loss varies from -4.5 to -6.5 dB over all phase shifter states for the same 2-GHz band.

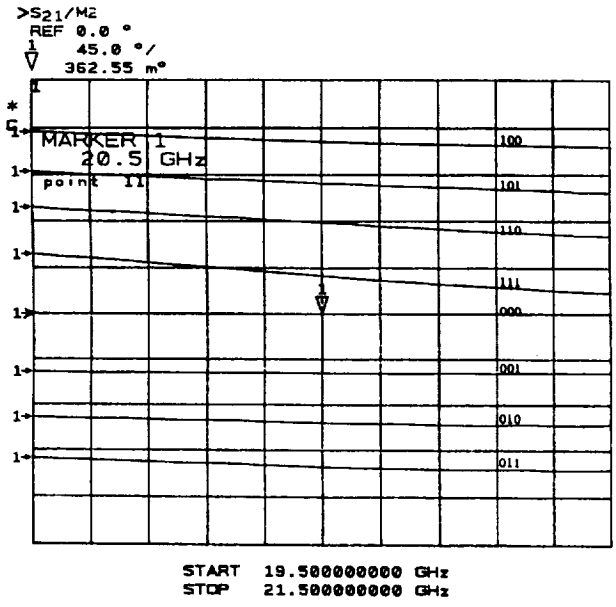


Figure 23. SLIC MMIC Phase Shifter Performance Data - Relative Phase Shift

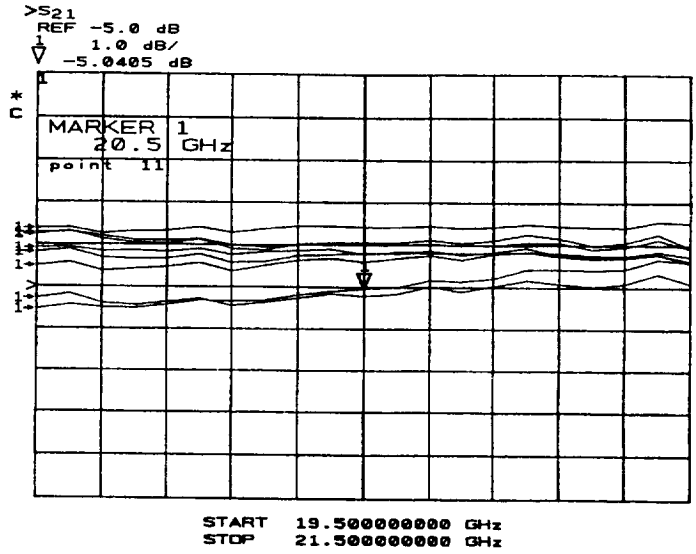


Figure 24. SLIC MMIC Phase Shifter Performance Data - Insertion Loss (S_{21})

Provided below is a return loss measurement of the SLIC MMIC phase shifter: Figure 25 shows the device input and output match versus device state 111. The input match is better than 2:1 over our entire band of specified performance.

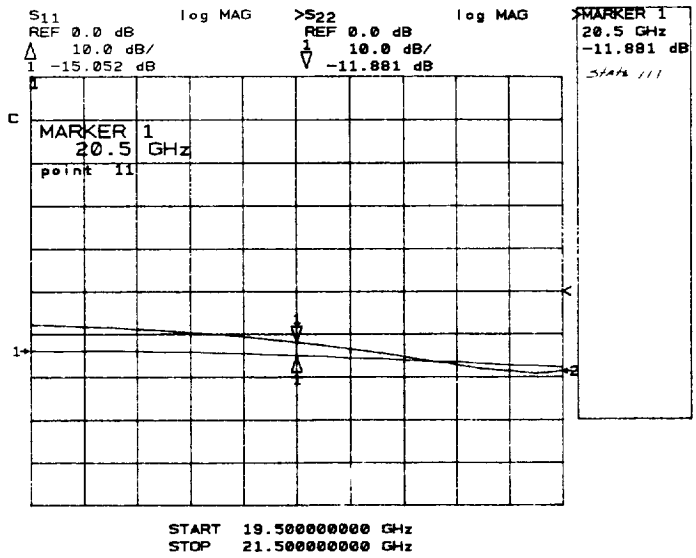


Figure 25. SLIC MMIC Phase Shifter Performance Data - Return Loss (S_{11}) Vs. Phase State (111)

All of the test data collected for the SLIC MMIC phase shifter demonstrate exceptional performance characteristics. The MMIC was a first pass success and achieved high yields on all lots - 70 to 80 %.

2.2.1.1.2 Attenuator

Figure 26 provides a detailed illustration of the analog attenuator circuit developed for the SLIC Program.

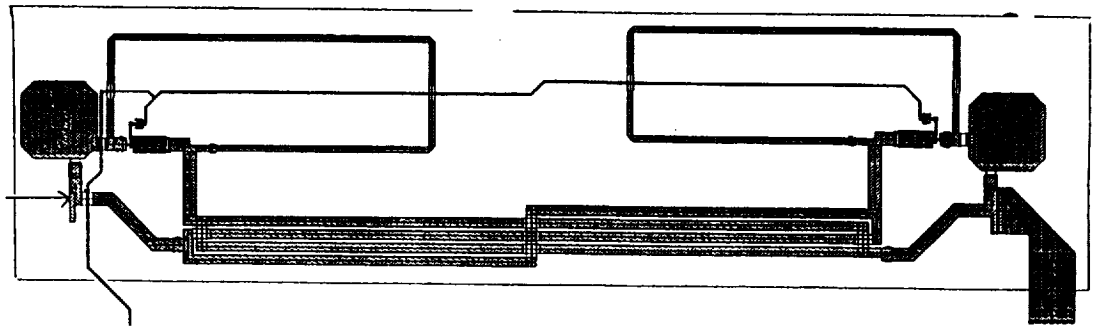


Figure 26. SLIC MMIC Attenuator Implementation

The next two plots help to delineate attenuator performance. The first plot, Figure 27, shows that the attenuator provides 20 dB of attenuation for a 2-volt gate voltage range with a minimum insertion loss of 1.5 dB. The second plot, Figure 28, illustrates the very small phase shift (approximately 5^0) realized over the entire used attenuation range (from -0.5 to -1.5 volts)(Note: 0.0V curve is shown for reference only.). This is a key factor in the calibration of a phased array module since amplitude corrections can be made without perturbing phase and hence beam control.

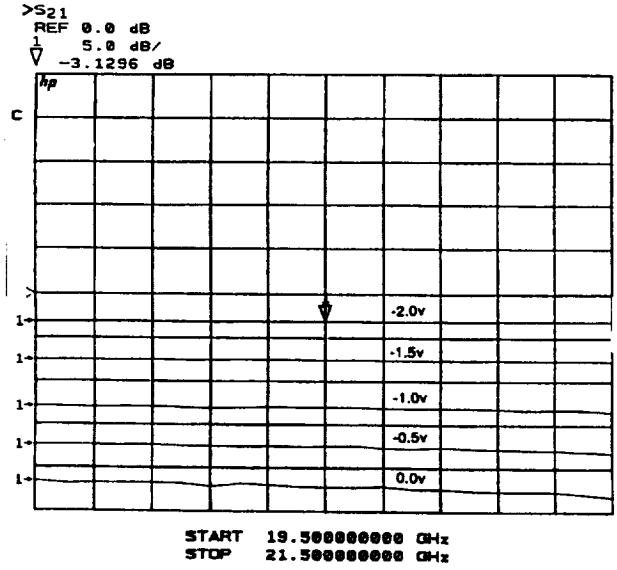


Figure 27. SLIC MMIC Attenuator Performance Data - Attenuation Range

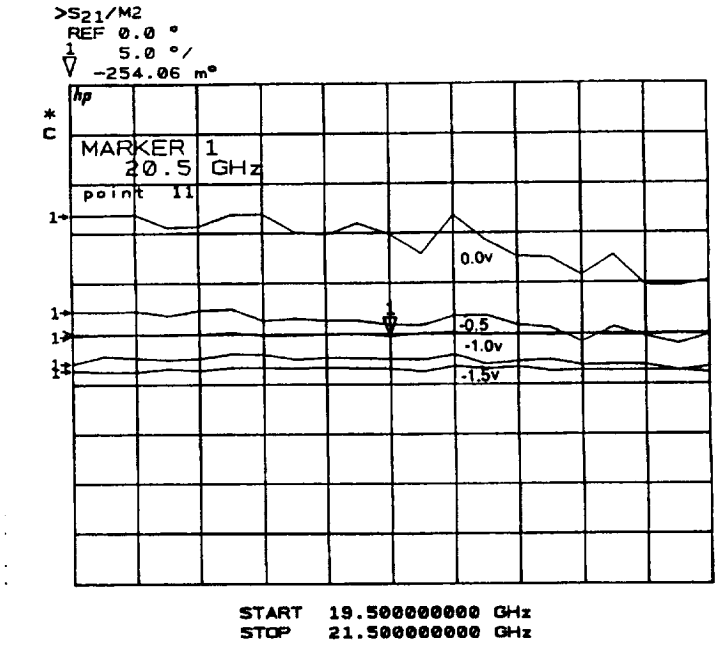


Figure 28. SLIC MMIC Attenuator Performance Data - Phase Shift

The overall return loss of the analog attenuator is very good. Figure 29 shows the return loss to be better than -11 dB for all gate voltages over a 2-GHz band (19.5 to 21.5 GHz). The second line plot, Figure 30, shows the attenuator return loss to be better than -15 dB (at a fixed gate voltage) over a 10-GHz band.

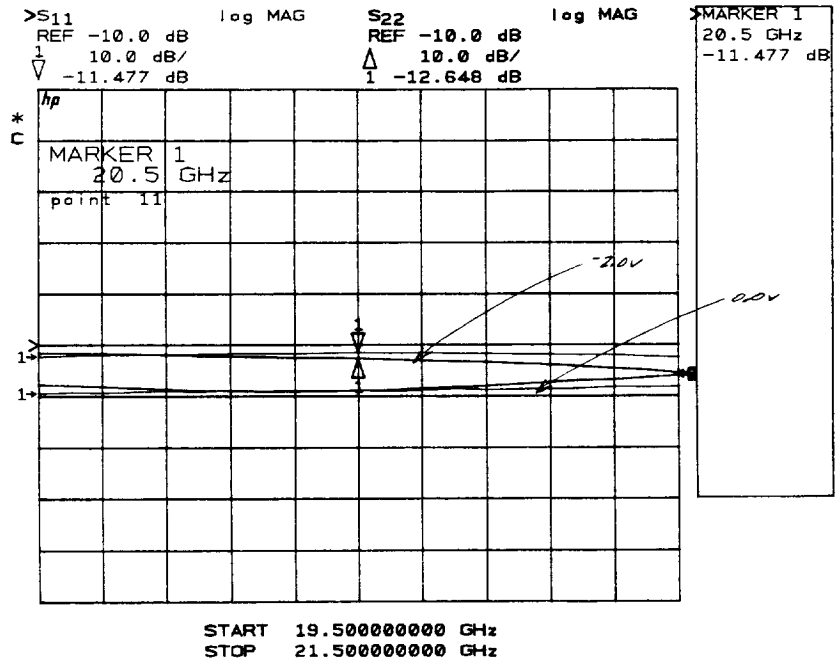


Figure 29. SLIC MMIC Attenuator Performance Data - Return Loss (S_{11}) Vs. Voltage

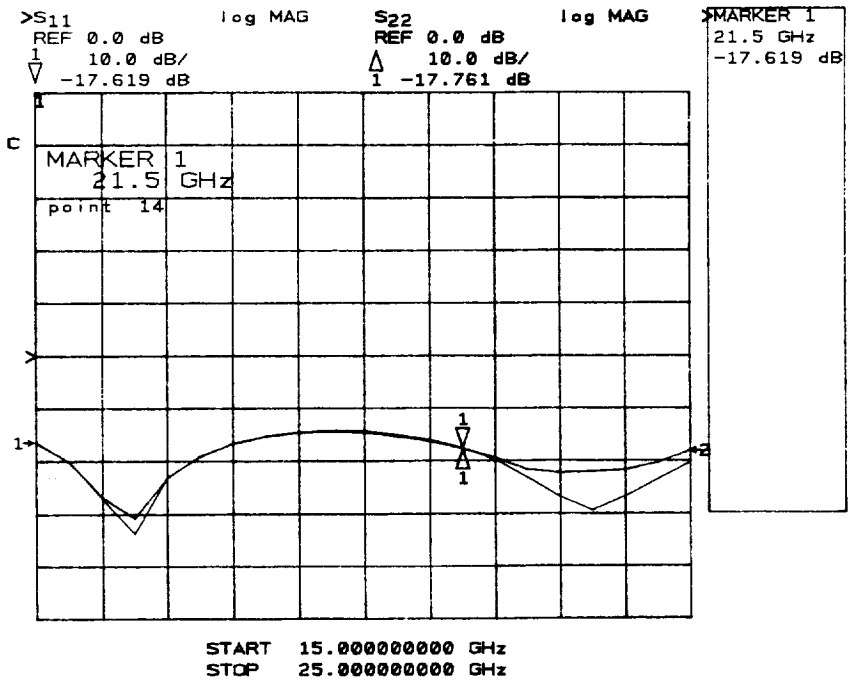


Figure 30. SLIC MMIC Attenuator Performance Data - Return Loss (S_{11}) Vs. Frequency

All of the test data collected for the SLIC MMIC attenuator show it to be a good design with high performance characteristics.

2.2.1.1.3 Peak Detector

An illustration of the peak detector circuit implementation is provided in Figure 31. Details of its function are described under the section on the AGC which follows.

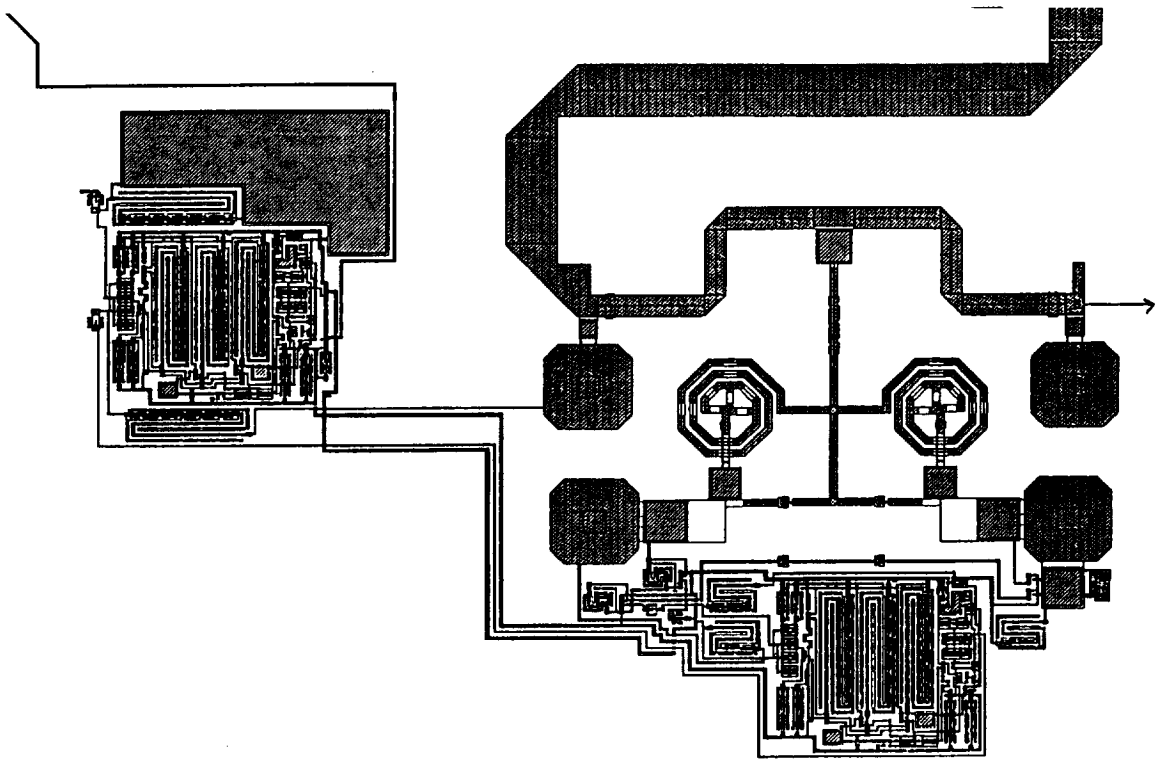


Figure 31. SLIC MMIC Peak Detector Implementation

The test data provided in Figure 32 clearly illustrates that the peak detector design provides excellent input and output match characteristics with both achieving better than -12 dB return loss. Insertion loss measurements indicate less than 0.8 dB of loss in our band of interest.

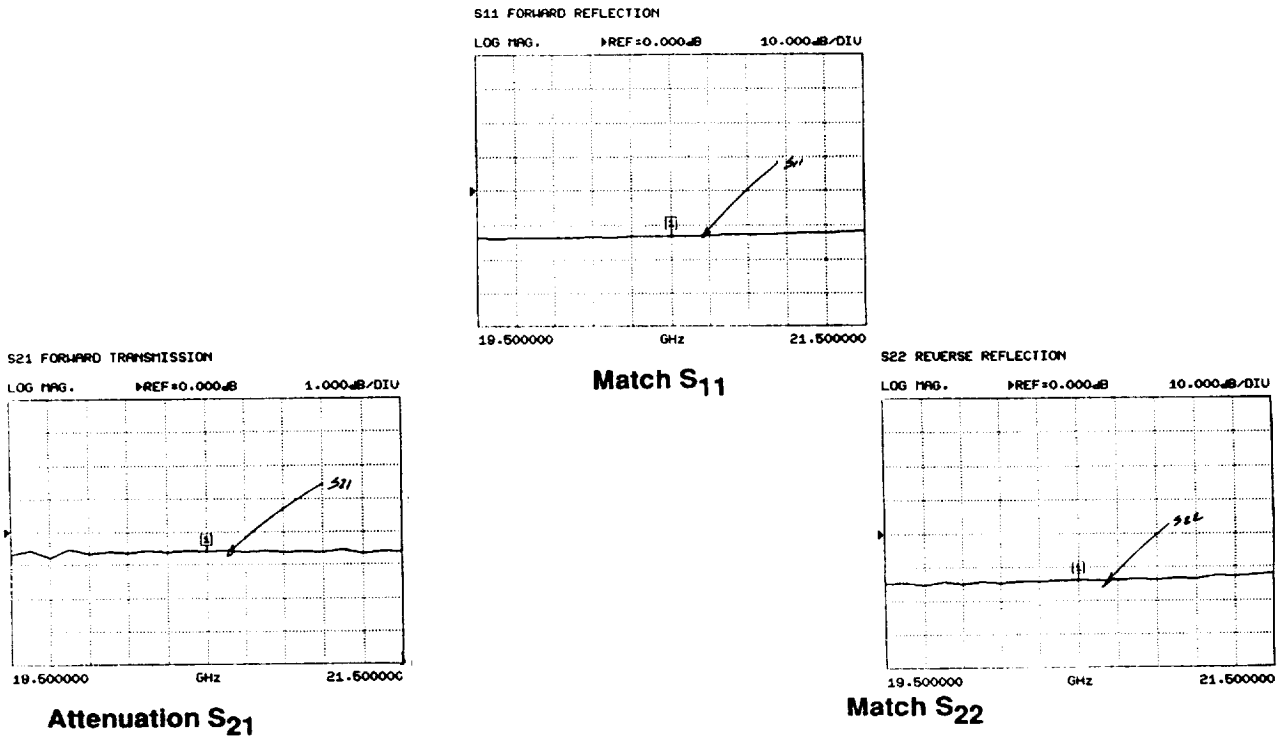


Figure 32. SLIC MMIC Peak Detector Performance Data

2.2.1.2 Control Functions

The next two sections provide detailed explanations for the controlling functions provided by both the analog and digital portions of the SLIC MMIC.

2.2.1.2.1 Automatic Gain Control

SLIC MMIC ANALOG SUBSYSTEMS

Analog subsystems are involved in:

1. AGC control loop
2. Temperature compensation loop
3. Generation of programmable reference voltages
4. Signal inputs to Manchester decoder or from Manchester encoder

A simplified system view of the AGC loop is shown in Figure 33, the components involved in this control loop are the variable attenuator, RF sense coupler, RF level sensor, the differential amplifier and the power level set reference voltage, V_{ref}. A small amount of the RF MMIC output power is coupled back to the MMIC from the RF sense coupler, which is located off-chip. The RF level sensor provides a voltage which is proportional to the MMIC RF power output. This voltage is an analog signal voltage, which is compared to the programmable reference voltage, V_{ref}, which is proportional to the power set point. The output of the differential amplifier is then used as the control voltage for the FET gates in the variable attenuator, and the RF attenuation is adjusted accordingly. The response of the AGC loop can be adjusted by proper adjustment of the time constants in the RF level sensor such that the response is much slower than an RF cycle time, but high enough to ensure a desired compensation response for RF power leveling. The RF level sensor acts as a voltage doubler which uses the RF swing to pump charge onto a hold capacitor. The clamped voltage on the capacitor is proportional to the RF amplitude. A constant-current source is placed in parallel with the capacitor to provide a controlled rate of capacitive discharge, thus controlling the response of the analog AGC loop.

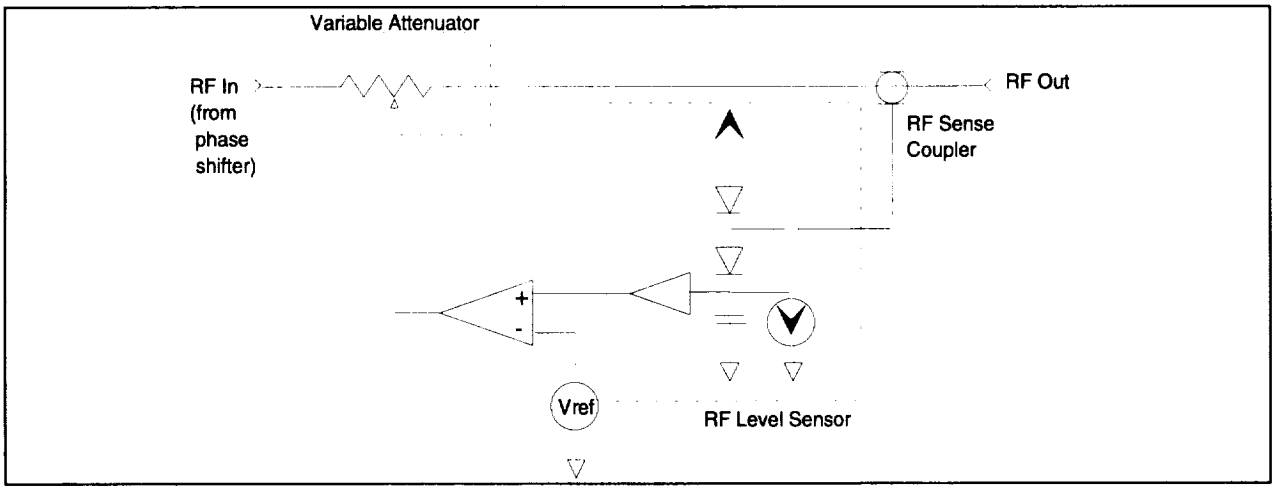


Figure 33. Simplified Schematic of AGC Control Loop

Successful implementation of the programmable AGC loop requires that an accurate, programmable voltage reference is available. Therefore, a 6-bit programmable voltage supply was implemented, providing 16 different programmable voltages over a 0 - -2 volt range. This enables 64 different AGC level settings. For each of these settings, the AGC loop provides compensation for phase shifter state-to-state amplitude variation, amplifier variations, and temperature effects on gain.

Still another analog subsystem is that of the control baseband signal transfer between the Manchester encoder/decoder and the photonic transducers. These signals are 0.5 - 1.0 MHz bi-polar digital signals. A low-pass filter is required for the photonic detector output to pass the digital control information to the Manchester decoder and block the RF. This low-pass filter is of simple design and was implemented on the DIC chip. Since the digital signal is a bi-polar, NRZ (Non-Return to Zero) type, there is ideally no DC component in the signal. Any DC which might be present would indicate a state-to-state level imbalance.

Test data of closed loop performance (of the entire module) is provided in Figure 34.

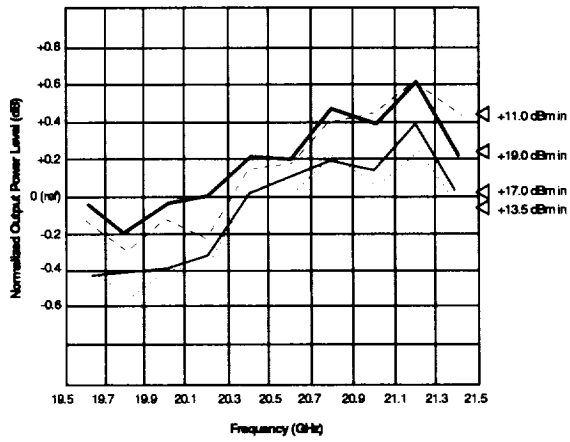


Figure 34. SLIC MMIC Module Closed Loop Gain Control Performance

This test data shows that the loop successfully compensates for eight dB of external power variation to within +/- 0.2 dB over our frequency band of interest. To test this performance, two sets of experiments were performed. In the first, the attenuation level was fixed in the middle of the AGC range and the phase shifters were changed. On the phase shifter alone the gain varied by greater than +/- 0.5 dB while with the AGC active, the state to state variation was only +/- 0.2 dB. Coupled with the low incidental phase shift of the attenuator, this leads to outstanding phase and amplitude uniformity. The second experiment involved the variation of input drive level to the unit. Input signal varied over an eight dB range with the output remaining constant within 0.2 dB. This is a fully linear system at this point and demonstrates the ability to correct for extreme variations in array drive signal. This will allow the maintenance of an excellent constant drive to the final amplifier which will maintain outstanding system linearity.

2.2.1.2.2 Control Interface

SLIC MMIC DIGITAL SUBSYSTEMS

A number of digital subsystems have been incorporated directly on-MMIC in order to reduce the number of module interconnects, enhance and increase the control features and facilitate a significant shrinkage of the module. A block diagram overview of the SLIC MMIC digital subsystems is shown in Figure 35.

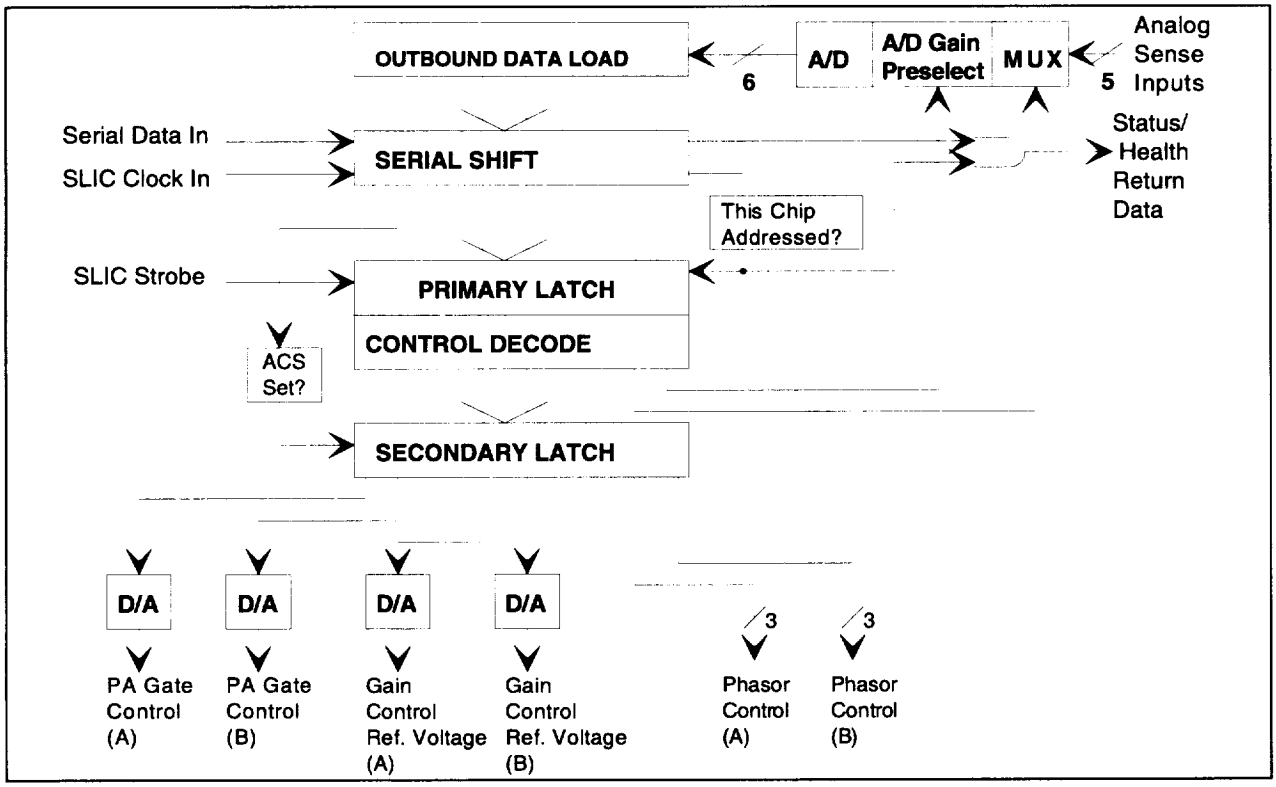


Figure 35. SLIC MMIC Digital Subsystems

Control data for each SLIC MMIC is passed in over the Serial Data In line while the SLIC Clock In line provides an active clock. When the data transaction is complete, the SLIC Strobe line is pulsed, Signaling the completion of the transaction. During the incoming data transfer, one of the four SLIC MMICs is simultaneously shifting status and health information out via the Status/Health Return Data line. The SLIC MMIC that transmits this data is the MMIC which was addressed on the previous data transaction.

Once the incoming data is loaded into the serial shift register, the address bit field is checked to determined whether the data word is intended for that particular chip. If the address bits match the hard coded address of the chip, the data is latched into the primary latch upon receipt of the SLIC Strobe. The Status/Health bit fields are then decoded to determined which status/health information will be requested from this chip at the next data transaction and the proper commands are forced upon the A/D gain preselector and the A/D MUX.

The SLIC phasor and/or attenuator states may be set up and changed on a one-by-one basis, or they may be set up one at a time and all switched together by using the All Chips Switch (ACS) discrete bit in the control word. In the SLIC control architecture, the ACS bit must be set in order to latch the D/A (gain and power conditioning controls) and phasor controls to the elements themselves, thereby activating the settings. The ACS bit is always checked and acted upon, regardless of the address setting in the control word.

When a particular status/health information request has been made of a particular MMIC, (only) that MMIC will transmit the requested data on the Status/Health Return Data bus on the next transaction. The status/health request is decoded if that MMIC is addressed, and the A/D gain preselect and MUX setting are adjusted to measure the proper voltage. The outbound data register is continually monitoring the "free-running" A/D readings, and a trigger signal (not shown) latches the data into the serial shift register for transmission out on the next data transaction. This trigger signal is derived (delayed) from the SLIC strobe in such a way that the system is allowed to settle from possible phase and/or gain setting changes before the A/D reading is taken on that channel.

The SLIC input control word fields are shown in Figure 36, and the SLIC Status/Health output data word is shown in Figure 37.

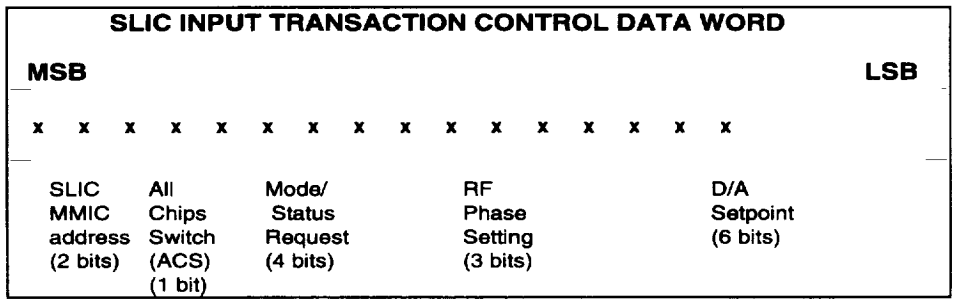


Figure 36. SLIC MMIC Control Word Definition.

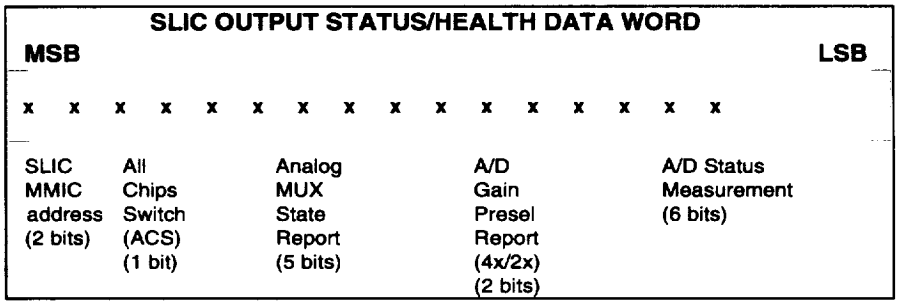


Figure 37. SLIC MMIC Status/Health Data Word Definition.

The BIT field interpretations for the SLIC MMIC input control word are shown in Table VIII.

Table VIII. SLIC MMIC Data Word BIT Definitions.

BIT FIELD	SETTING	COMMAND
SLIC MMIC Address	00	SLIC MMIC #1 is data target
	01	SLIC MMIC #2 is data target
	10	SLIC MMIC #3 is data target
	11	SLIC MMIC #4 is data target
All Chips Switch	0 / 1	0-No action, 1-Act on settings
Mode/Status Request	0 (0000)	No Operation
	1 (0001)	Test and Calibration (external interface pad)
	2 (0010)	MMIC Output RF Amplitude Channel A
	3 (0011)	MMIC Output RF Amplitude Channel B
	4 (0100)	Analog Input Channel A (off-chip sensor interface)
	5 (0101)	Analog Input Channel B (off-chip sensor interface)
	6 (0110)	No Operation
	7 (0111)	No Operation
	8 (1000)	Latch Phasor/RF Attenuator Channel A
	9 (1001)	Latch Phasor/RF Attenuator Channel B
	10 (1010)	Latch Power Amp Gate Bias Set-Point Channel A
	11 (1011)	Latch Power Amp Gate Bias Set-Point Channel B
	12 (1100)	Switch ADC 2x Preselect Gain ON
	13 (1101)	Switch ADC 4x Preselect Gain ON
	14 (1110)	Switch All ADC Preselect Gain Multipliers OFF
	15 (1111)	No Operation
RF Phase Setting	0 (000)	0 degree phase setting
	1 (001)	45 degree phase setting
	2 (010)	90 degree phase setting
	3 (011)	135 degree phase setting
	4 (100)	180 degree phase setting
	5 (101)	225 degree phase setting
	6 (110)	270 degree phase setting
	7 (111)	315 degree phase setting
D/A Setpoints	(000000 - 111111)	

The BIT field interpretations for the SLIC MMIC output status/health data word are shown in Table IX.

Table IX. SLIC MMIC Status/Health Data Word BIT Definitions.

BIT FIELD	SETTING	COMMAND
SLIC MMIC Address	00	SLIC MMIC #1 is data source
	01	SLIC MMIC #2 is data source
	10	SLIC MMIC #3 is data source
	11	SLIC MMIC #4 is data source
All Chips Switch	0 / 1	0-No action requested, 1-Act on settings requested
Analog MUX State	10000	MUX setting: Test/calibration, SLIC input level
	01000	MUX setting: On-chip level sensor, Channel A
	00100	MUX setting: On-chip level sensor, Channel B
	00010	MUX setting: Analog Input (off-chip sensor), Channel A
	00001	MUX setting: Analog Input (off-chip sensor), Channel B
A/D Gain Presel State	00	No preselect gain employed
	01	2X preselect gain employed prior to A/D
	10	4X preselect gain employed prior to A/D
	11	8X preselect gain employed prior to A/D
A/D Status Measurement	(000000 - 111111)	Binary measurement data from 6-bit A/D

2.2.1.3 Foundry Experience/Results

Four wafers were probed for functionality and binned into six different classes of operation. These bins are identified and defined in Table X.

Table X: Wafer Probe Bin Definitions

BIN	DESCRIPTION	FAILURE
X	Non-functional Die; unable to Load and Read shift register with simple alternating one's and zero's pattern	Shift Register Failure
A	Bin: Load and Read Shift Register with simple alternating one's and zero's pattern, Shift Register functional. Control Word Response (Bits 15-6) Output incorrect	Control Word Failure
B	Bin: Load and Read Shift Register with simple alternating one's and zero's pattern, Shift Register functional. Control Word Response (Bits 15-6) OK, but A/D Status Measurement of Control Word (Bits 5-0) output incorrect. PA Gate Control verification with oscilloscope for both Channels "A" and "B" failed to respond	Both A/D Status Measurement and D/A Channel "A" and "B" Failure
C	Bin: Load and Read Shift Register with simple alternating one's and zero's pattern, Shift Register functional. Control Word Response (Bits 15-6) OK, but A/D Status Measurement of Control Word (Bits 5-0) incorrect. PA Gate Control Verification with oscilloscope for CHANNEL ÌB" failed to respond, but CHANNEL ÌA" responded with a increasing value with increase in D/A Input Setpoint (Bits 5-0)	A/D Status Measurement and D/A CHANNEL ÌB" Failure.
D	Bin: Load and Read Shift Register with simple alternating one's and zero's pattern, Shift Register functional. Control Word Response (Bits 15-6) OK, but A/D Status Measurement of Control Word (Bits 5-0) incorrect. PA Gate Control Verification with oscilloscope for CHANNEL ÌA failed to respond, but CHANNEL ÌB responded with a increasing value with increase in D/A Input Setpoint (Bits 5-0)	A/D Status Measurement and D/A CHANNEL ÌA" Failure
E	Bin: Load and Read Shift Register with simple alternating one's and zero's pattern, Shift Register functional. Control Word Response (Bits 15-6) OK, but A/D Status Measurement of Control Word (Bits 5-0) incorrect. PA Gate Control Verification with oscilloscope for both CHANNEL ÌA and CHANNEL ÌB responded with a increasing value with increase in D/A Input Setpoint (Bits 5-0)	A/D Status Measurement Failure

Only Die binned "B", "C", "D" or "E" were chosen as candidates for RF Testing. RF Testing was done using an HP 8510 and digital control card in PC for Digital Control. RF test status has been provided in Table XI.

Table XI. SLIC MMIC Yield Analysis

TRIQUINT Wafer Lot#: GS-3125-AW; Run ID: 4823 and 4951
Using Short Test and Scope Verification(SLICXX.SET)
There are 72 candidates per wafer

		Digital Test Results						B&C&D&E		RF Test FAILED						
Wafer		Test FAILED by Bin						Die	Yield	Die	Phase Shifte		AGC Control		RF	Total
Number	VSS/VDD	"X"	"A"	"B"	"C"	"D"	"E"	Total	Data	Tested	"A"	"B"	"A"	"B"	Pass	Yield	Yield
11346	-5V/+5V	18	29	5	5	5	10	25	34.7%	17	0	1	9	10	3	17.65%	4.2%
12400	-5.5V/+5V	16	10	6	7	8	25	46	63.9%	19	1	0	13	12	2	10.53%	2.8%
12403	-5.5V/+5V	10	14	5	4	10	29	48	66.7%	15	0	0	6	8	5	33.33%	6.9%
12404	-5.5V/+5V	13	11	0	5	8	35	48	66.7%	45	2	2	22	18	15	33.33%	20.8%
	Tested	288	231	167	167	167	167			96	99	99	99	99			
	Failed	57	64	16	21	31	99				3	3	50	48			
	Failure YIELD	20%	28%	10%	13%	19%	59%				3%	3%	51%	48%			
				Possible Candidates:				167	57.99%			Possible Candidates:			25	26.04%	8.68%

"X" Bin Tests Results= Shift Register(SR) Fails
"A" Bin Tests Results= SR OK, Control Word Fails
"B" Bin Tests Results= SR OK, A/D Value Fails, D/A(Ch A & B) Fails
"C" Bin Tests Results= SR OK, A/D Value Fails, D/A(Ch A): OK or Value, D/A(Ch B) Fails
"D" Bin Tests Results= SR OK, A/D Value Fails, D/A(Ch A): Fails, D/A(Ch B) OK or Value
"E" Bin Tests Results= SR OK, A/D Value Fails, D/A(Ch A & Ch B): OK or Value

2.2.2 Divider Interface Circuit Design

DIVIDER INTERFACE CIRCUIT (DIC) MMIC DESCRIPTION

There are a number of functions within the SLIC module which are required on the subarray level which would be redundant if implemented on each SLIC MMIC. These functions include:

- Diplexing RF and digital signals entering over the input optical link
- Sensing the module input RF level delivered by the optical link
- Providing a 12-MHz free-running clock for the Manchester Decoder chip
- Providing level-shifting for digital signals between the Manchester decoder and the SLIC MMICs
- Providing properly timed latch signals and data shift clock signals for the SLIC MMICs
- Providing an RF interface for a power amplifier to boost RF signal level
- Providing a compact RF power divider to run RF in each direction in the module from the center

To accommodate these features, a separate chip called the Divider Interface Circuit MMIC was designed and developed. Implementing these features on a single GaAs MMIC freed up significant module floor space for other functions. The device is located in the center of the SLIC subarray. The DIC MMIC is based on the same process as the SLIC MMIC; these chips are fabricated together on the same wafer in the TriQuint QED/A process.

A simple block diagram in Figure 38 illustrates the functions incorporated on the DIC MMIC.

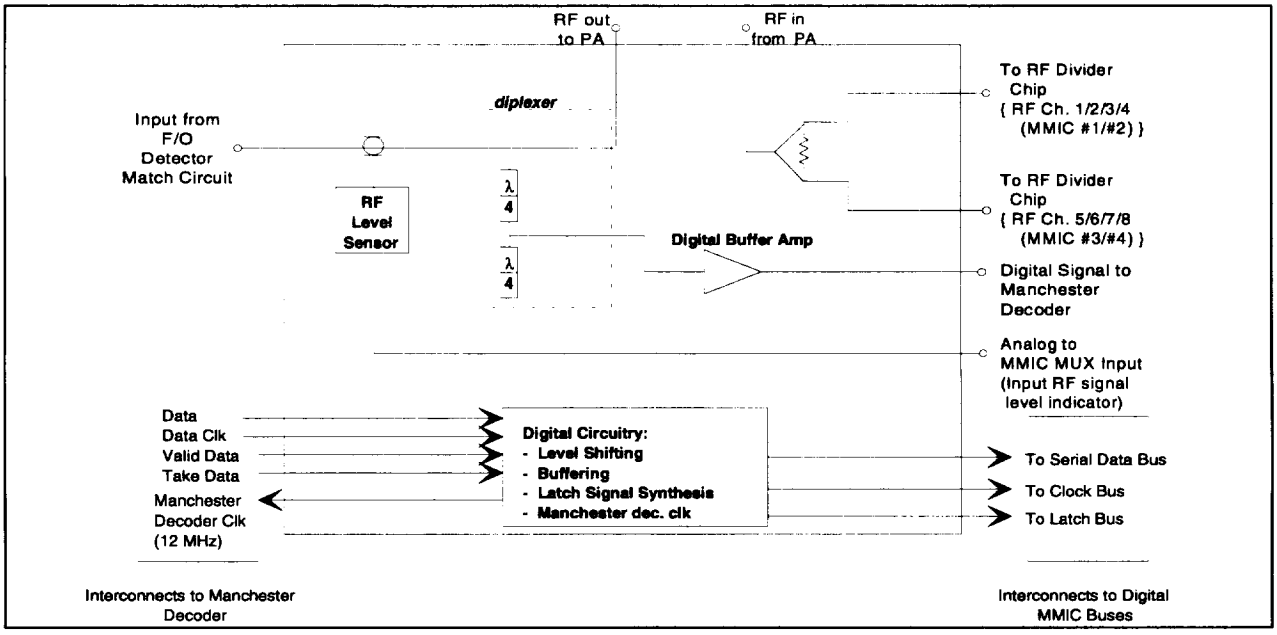


Figure 38. SLIC Divider Interface Circuit MMIC Functional Block Diagram

Figure 39 is a picture of the actual DIC MMIC device developed and fabricated on this program.

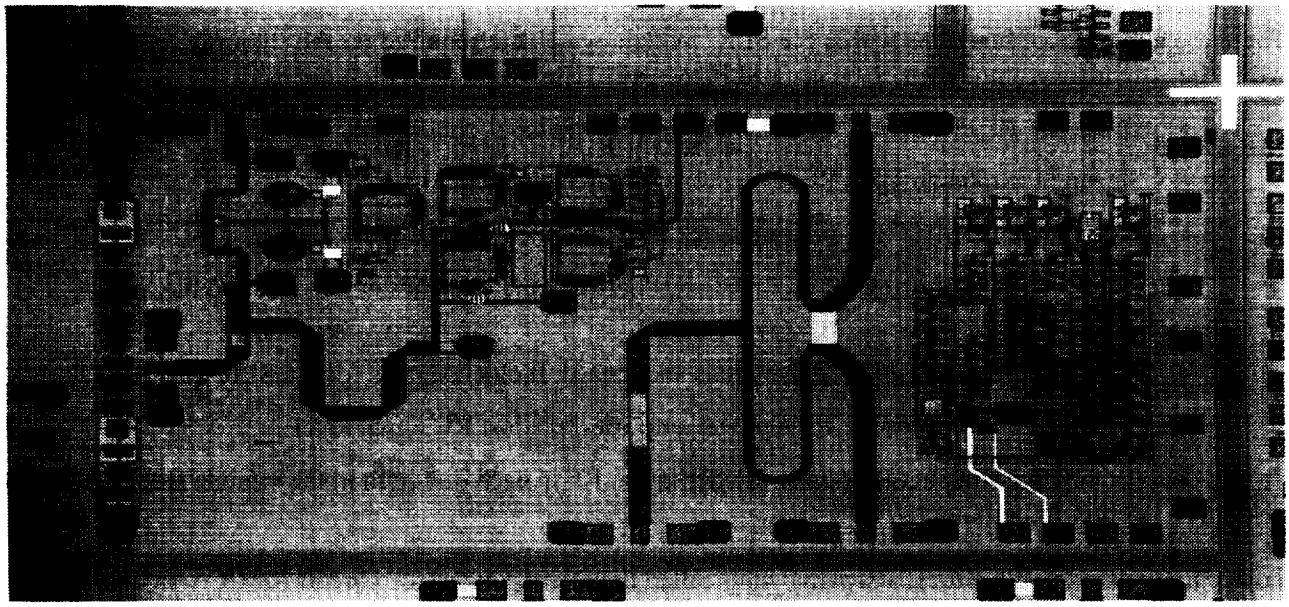


Figure 39. SLIC Divider Interface Circuit MMIC

Provided in Figure 40 is the Calma Plot for the DIC MMIC.

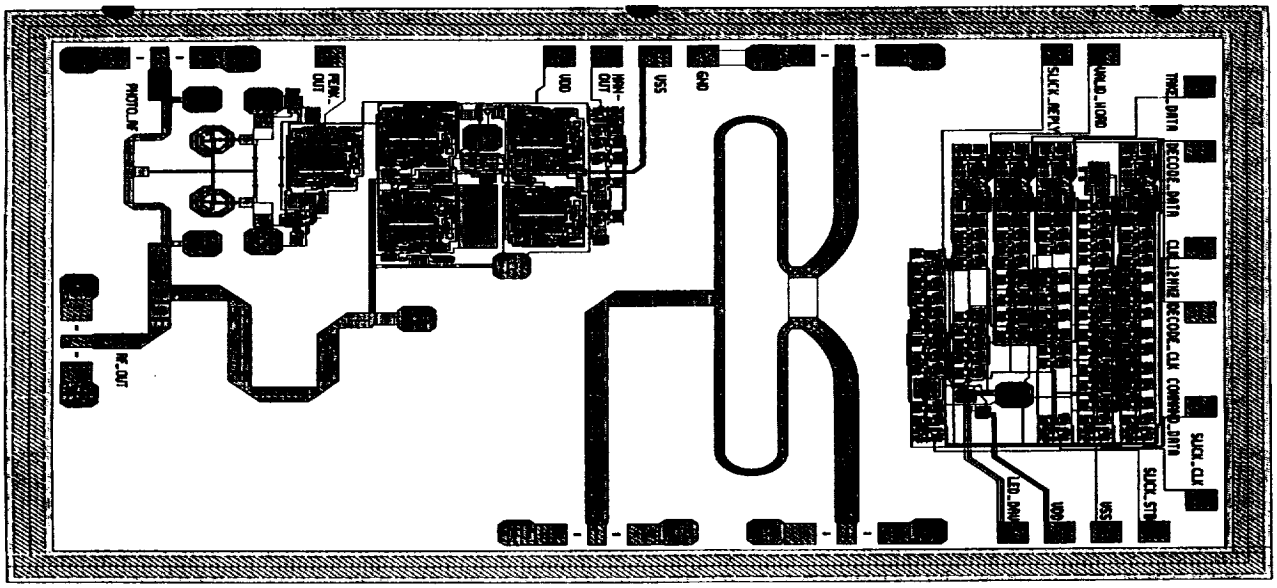
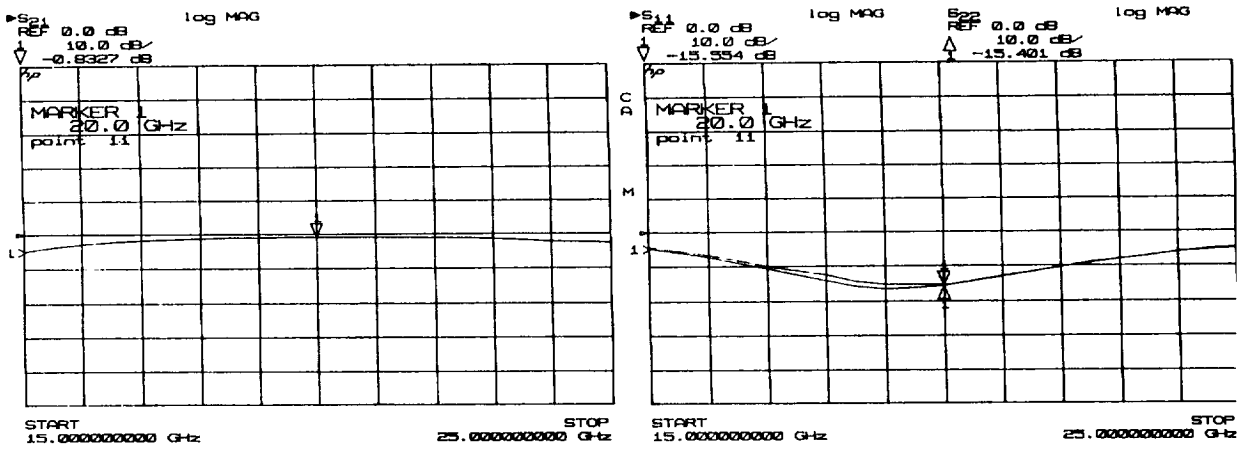


Figure 40. Divider Interface Circuit Line Plot

Figure 41 presents insertion loss and return loss performance data for the Diplexer implemented on the DIC MMIC. As can be seen from the line plots, insertion loss is low and the match is good.



Attenuation S_{21} **Match S_{11}, S_{22}**

Figure 41. Divider Interface Circuit MMIC RF Performance

RF DIVIDER CIRCUIT DESCRIPTION

Figure 42 shows an approximation to the SLIC module layout, where the MMICs and RF transmission lines associated with the RF subsystems are depicted. The divider interface circuit MMIC provides one level of RF power division, and connects to transmission lines which run to each end of the SLIC subarray package.

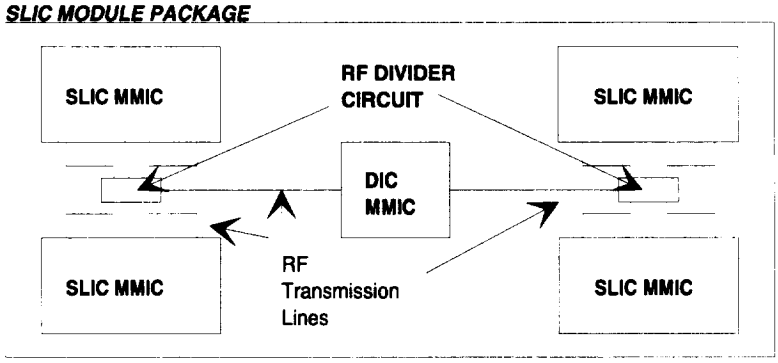


Figure 42. Approximation of SLIC Module Layout

Since the SLIC MMICs have separate input interfaces for each channel, a 4-way RF power divider is required at each end of the module. There are a number of ways that this division could have been implemented, including:

- Printing the divider on the module package base substrate (Aluminum Nitride).
- Implementing the divider in HDI between the MMICs.
- Designing a second SLIC MMIC which could carry the divider on one side of the module.
- Providing all (or part) of the RF power division on the DIC MMIC and running more than one transmission line out to the SLIC MMICs.
- Designing a small GaAs drop-in chip providing circuitry for a 4-way divider.

We elected to design a small GaAs drop-in chip to provide a 4-way divider. This approach is attractive because it is extremely compact, well-phase balanced to the SLIC MMIC inputs, and the chips can be fabricated to a high degree of accuracy. Since only one long transmission line runs to each end of the module, the risk of coupling between multiple transmission lines is minimized. This RF divider circuit is also implemented in the TriQuint QED/A process, and is fabricated on the same wafer as the SLIC MMIC and the Divider Interface Circuits. Since the divider contains only passive structures, it represented a very low-risk in development.

A simple functional diagram of the RF divider circuit is shown in Figure 43.

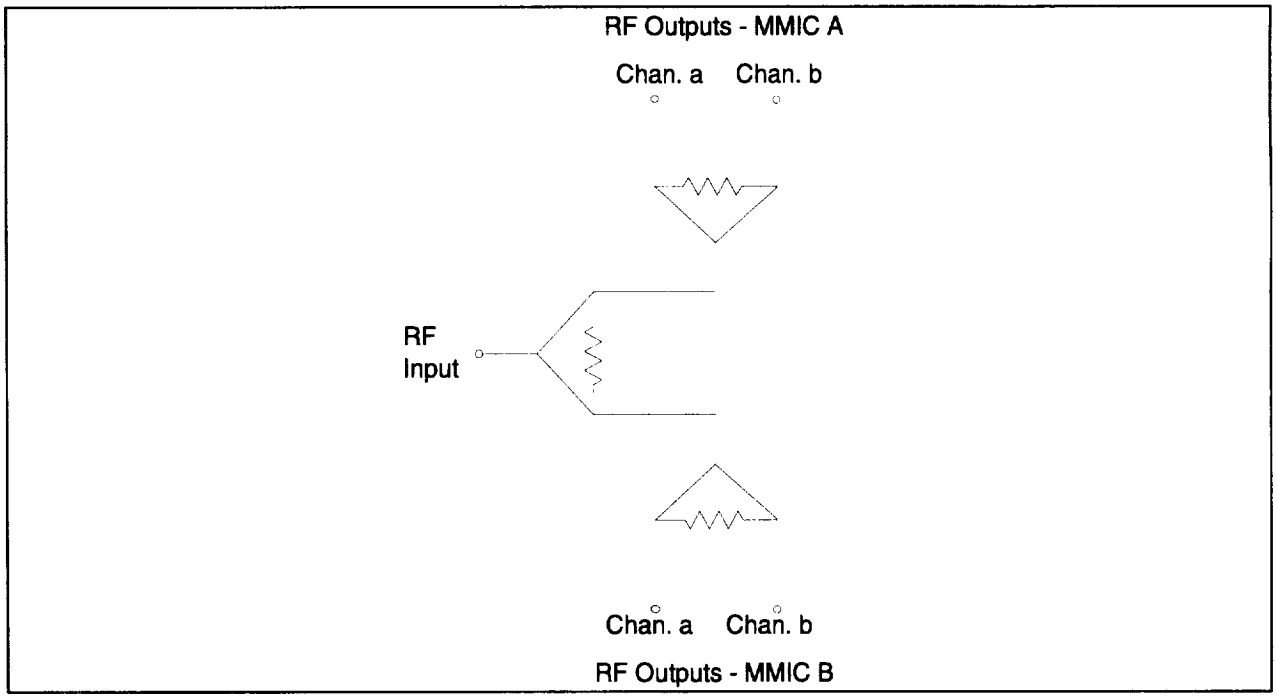


Figure 43. SLIC RF Divider Circuit Functional Schematic

Figure 44 illustrates the GaAs MMIC implementation of the RF Divider circuit.

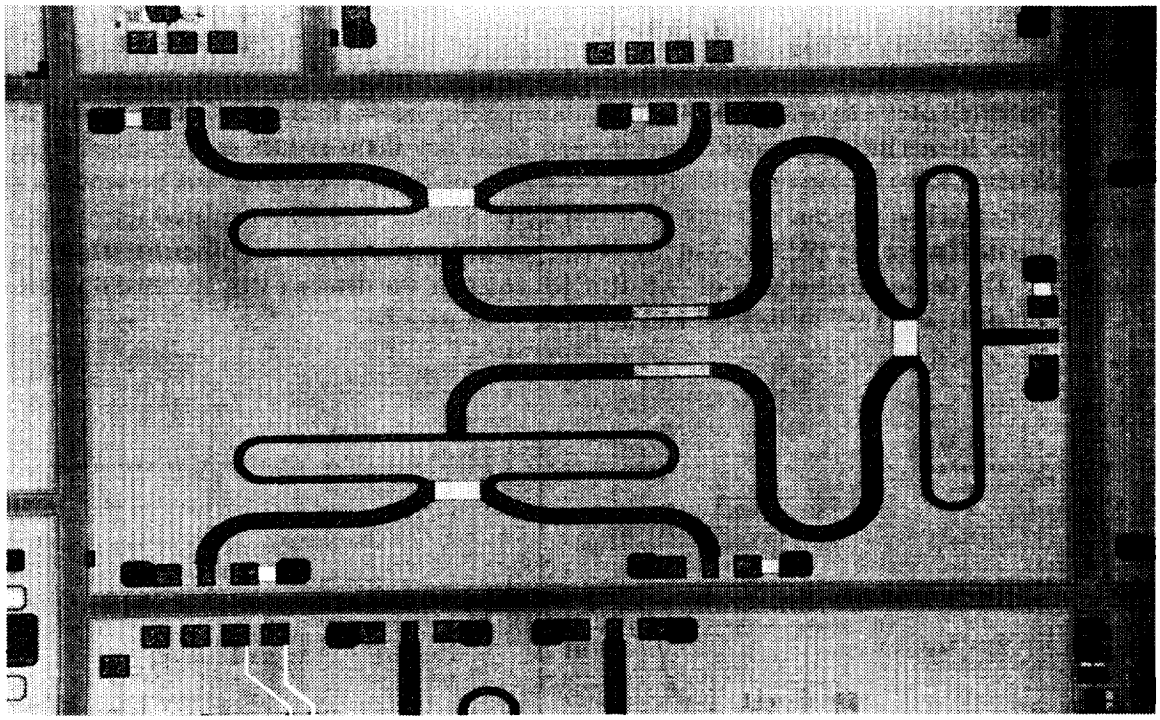


Figure 44. SLIC RF Divider MMIC

Figure 45 illustrates performance data for the RF Divider circuit. Return loss is better than -25 dB at the input and -20 dB at the output. Insertion loss is no worse than -8.5 dB in our specified band of operation.

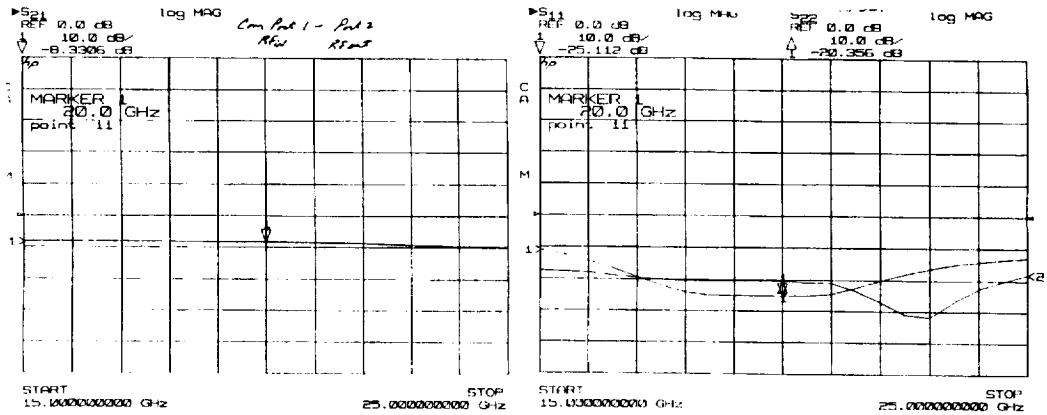


Figure 45. SLIC RF Divider Circuit Performance Data

2.2.3 Fiber Optic Link Design

FIBER-OPTIC SUBSYSTEM

The SLIC subarray uses a two-fiber architecture, shown in Figure 46, to achieve a high-fidelity fiber-optic interface. In this interface architecture, the low-frequency status signals are generated using light emitting diodes (LEDs) for high reliability and low cost. The 20 to 22-GHz RF link presented a greater challenge. For this link external modulation was selected because directly modulated semiconductor lasers are too inefficient to yield high-fidelity fiber-optic link performance at millimeter-wave frequencies. The demonstration goal of -9.5 dBm RF output at the detector was successfully met using an AMOCO laser, an AT&T modulator, and an Epitaxx photodiode.

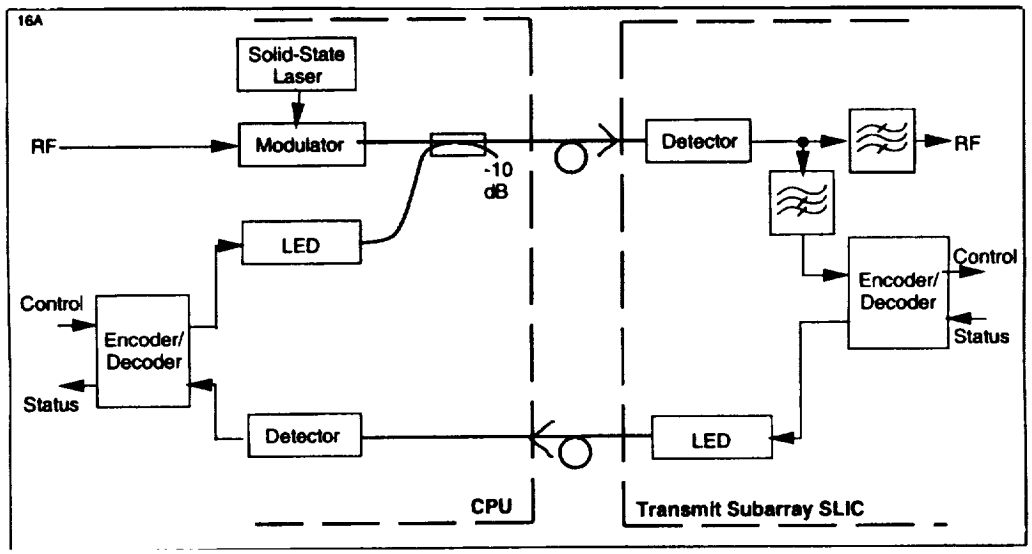


Figure 46. SLIC Module Fiber Optic Interface Block Diagram

The solid-state laser and electro-optic modulator used to create the RF-modulated optical signal were originally procured for a microwave photonics IRAD program. The solid-state laser is a Nd:YAG device manufactured by AMOCO. It emits 75 mW of l=1.3 mm light into a single-mode fiber pigtail. The modulator is a Mach-Zender interferometric directional coupler with optical waveguides created by T-doping a $LiNbO_3$ substrate. It also has a four-section traveling-wave electrode structure for matching the millimeter-wave phase velocities of the electronic and optical signals. Sanders (formerly Martin Marietta Electronics Laboratory) and AT&T Bell Laboratories jointly developed this modulator.

The photodetector is an InGaAs p-i-n device selected for its high responsivity at 20-22 GHz of 0.6 A/W or greater, its low photodiode reverse-bias resistance (5-10W), and its ability to withstand high current densities of at least 10 mA. The RF performance of the device we selected as part of an extensive evaluation effort is illustrated in Figure 47. Figure 48 shows the cross-section of the p-i-n photodiode monolithically interconnected to the HDI impedance-matching circuit.

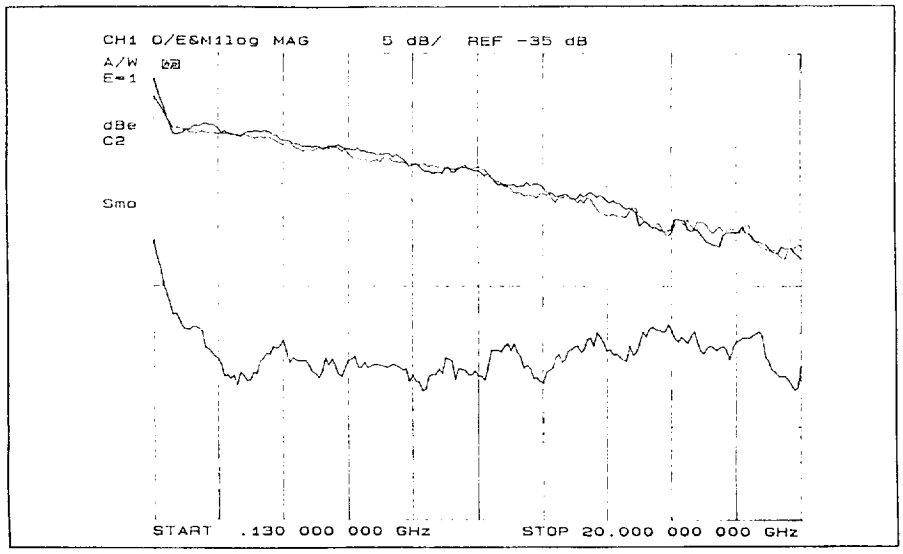


Figure 47. Detector Diode Response Versus Frequency

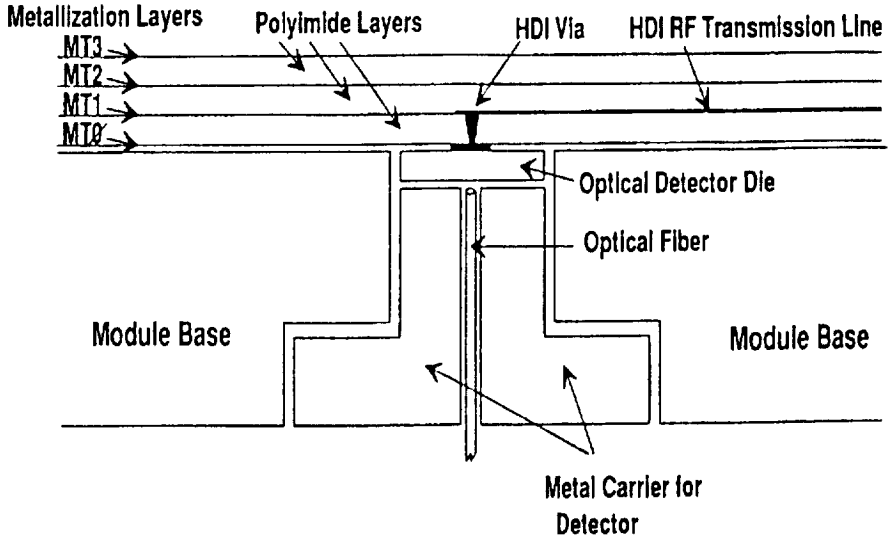
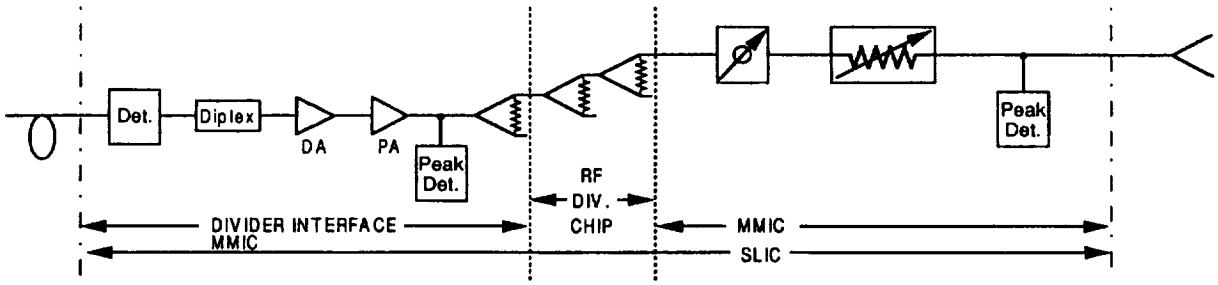


Figure 48. Detector Diode Mount Cross Section

The cross-section illustrates the via hole that connects the conducting contact on top of the detector chip to the top of the HDI substrate where the waveguides reside. It also shows the method by which Sanders is accomplishing optical alignment of the fiber's 8-mm core to the detector's 25-mm active region. The detector die sits in a well, as shown, such that its top contact lies in the same plane as the surface of the silicon substrate, and its photosensitive backside is accessible through an aperture drilled in the substrate. Since the target photodetector is larger than the fiber core in which the nearly collimated light propagates, fiber-to-detector coupling efficiency of 95% is obtained, with only 5% lost due to reflections at the fiber/air interface.

The SLIC power budget requires -9.4 dBm RF output from the photodiode, shown opposite the "F/O Detector" entry in Figure 49. SLIC Channel RF Power Budget. We achieved -9.5 dBm output by careful tuning of the optical polarization at the input to the modulator using an AT&T torsion fiber polarizer.



RF Component	Component Gain (dB)	Power at Output (dBm)
F/O Detector	–	-9.4
Detector Match	-0.5	-9.9
Diplexer/DC Block	-0.9	-10.8
Driver Amplifier	19	8.2
Power Amplifier	18	26.2
Power Divider #1	-4.2	22.0
Power Divider #2	-4.2	17.8
Power Divider #3	-4.2	13.6
Phase Shifter	~6.0	7.6
Variable Attenuator	~2.0	5.6
RF Level Sensor	~1.0	4.6

Figure 49. SLIC Channel RF Power Budget

The polarization of the light's E-field at its launch into the Mach-Zender modulator must be matched to the RF E-field. Increased optical power was useful in reducing net RF loss only up to about 20 mW. Greater intensities created anisotropies in the Faraday coupling coefficient, or electro-optic coefficient, of the $LiNbO_3$ crystal that governs the efficiency of the modulator. The anisotropies took several days to relax, frustrating the test procedure. To avoid testing delays we settled on 15 mW optical input power, only 15% of the laser's capability. The link output power at the high end of the band was measured at -9.5 dBm. This result is found by adding a cable-loss correction of 5.33 dB to the marker readout of -14.83 dBm in Figure 50. The three curves in Figure 51 show how the output match of the photodiode changes with the applied voltage across it. The -9.5 dBm result was taken at 20V, and was considered to be compliant with the power budget requirements in Figure 49. SLIC Channel RF Power Budget in spite of a slight fall-off of 3 dB at the low edge of the band.

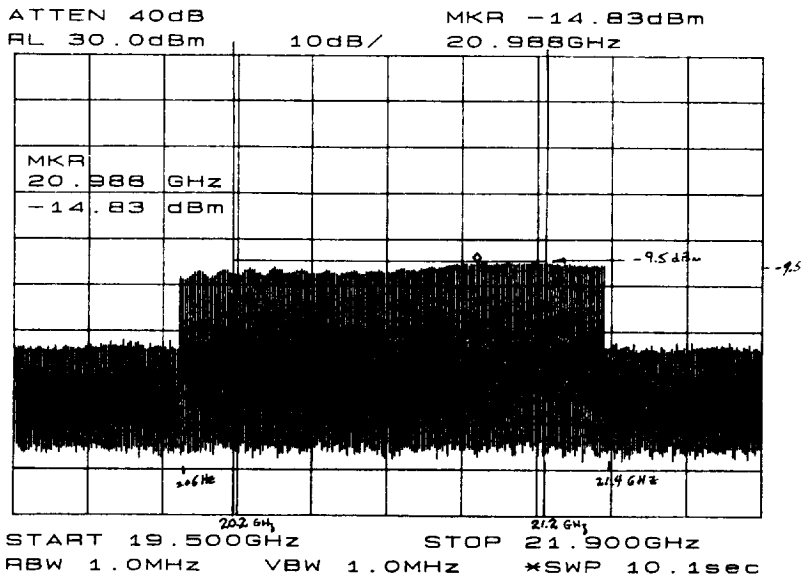


Figure 50. FO Link RF Power Performance

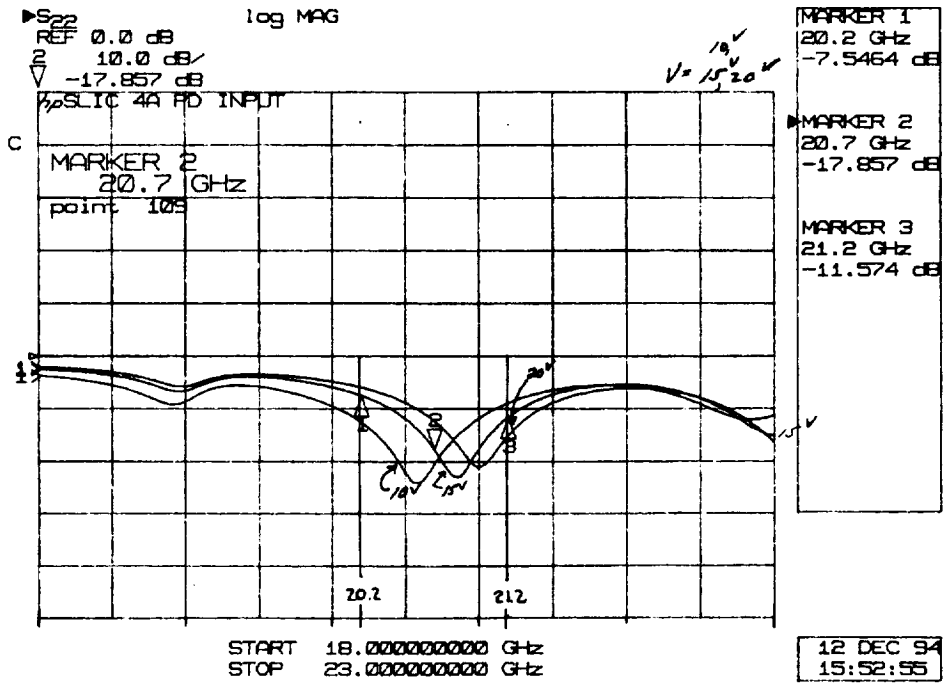


Figure 51. FO Link Output Match

The EHF interface to the eight-element subarray uses an InGaAs p-i-n photodiode detector that is connected using HDI. In addition to permitting low-loss impedance matching and very efficient optical coupling techniques, HDI has the flexibility to accommodate any backfacet-illuminated detector. Thus candidate devices could be selected on the basis of performance alone, then monolithically interconnected to the HDI matching circuit, avoiding bond wires that would degrade the available transducer gain.

Difficulties were observed in the optical link after MHDI processing. Several modules had short circuits while others appeared to be resistive. Failure analysis identified the root cause to be the laser drilling of the MHDI kapton layer to allow contact with diode bond pad. For example, Figure 52 illustrates the damage to a photodiode during the kapton laser drilling operation. An effort to modify the MHDI process to accommodate small, thin metal pads, like those found on photodiodes, would have been outside of the scope of this contract. Instead, a work-around technique allowed the diode to be added after MHDI processing, using a single wire bond.

Figure 52. Representative Detector Damage

Detector impedance matching is accomplished using a circuit topology realized in HDI. Figure 53 is an expanded photograph of the HDI detector matching circuit, which was designed using the Super Compact CAD tool and an accurate millimeter-wave equivalent circuit model of the photodetector. The circuit model was developed from the intrinsic one-port scattering parameter of the device, which had been determined by de-embedding the two-port scattering parameters of a calibrated test fixture from the measured reflection coefficient of the device in that fixture.

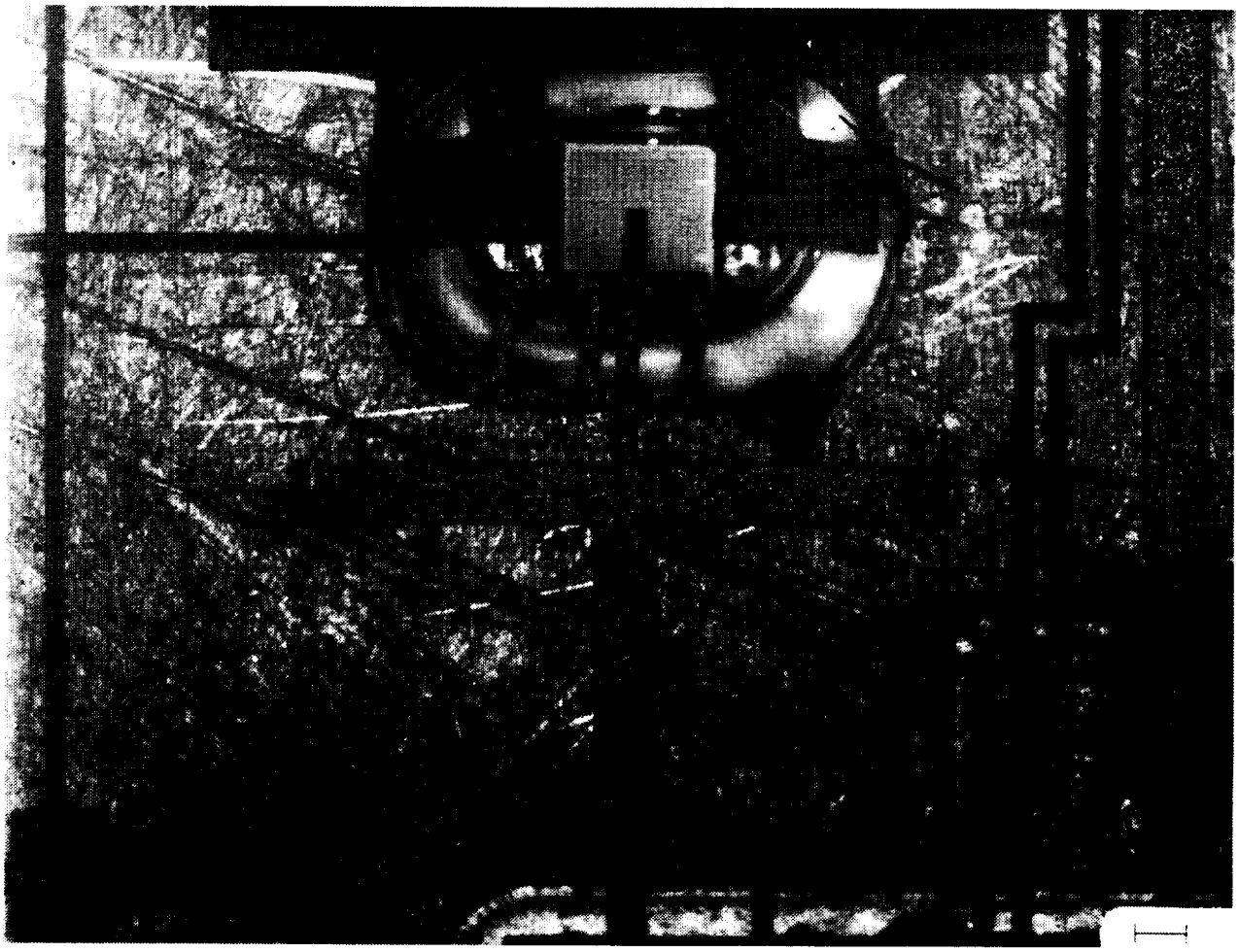


Figure 53. Detector Diode with HDI Matching Network

Figure 54 shows the schematic for the impedance matching circuit, while Figure 55 shows the predicted return loss of the selected InGaAs p-i-n photodetector impedance-matched in this fashion. The magnitude of the return loss is better than -15 dB across the frequency band (20.2 to 21.2 GHz), and, since no resistive elements are used in the matching network, the transducer gain will be maximum across this frequency band.

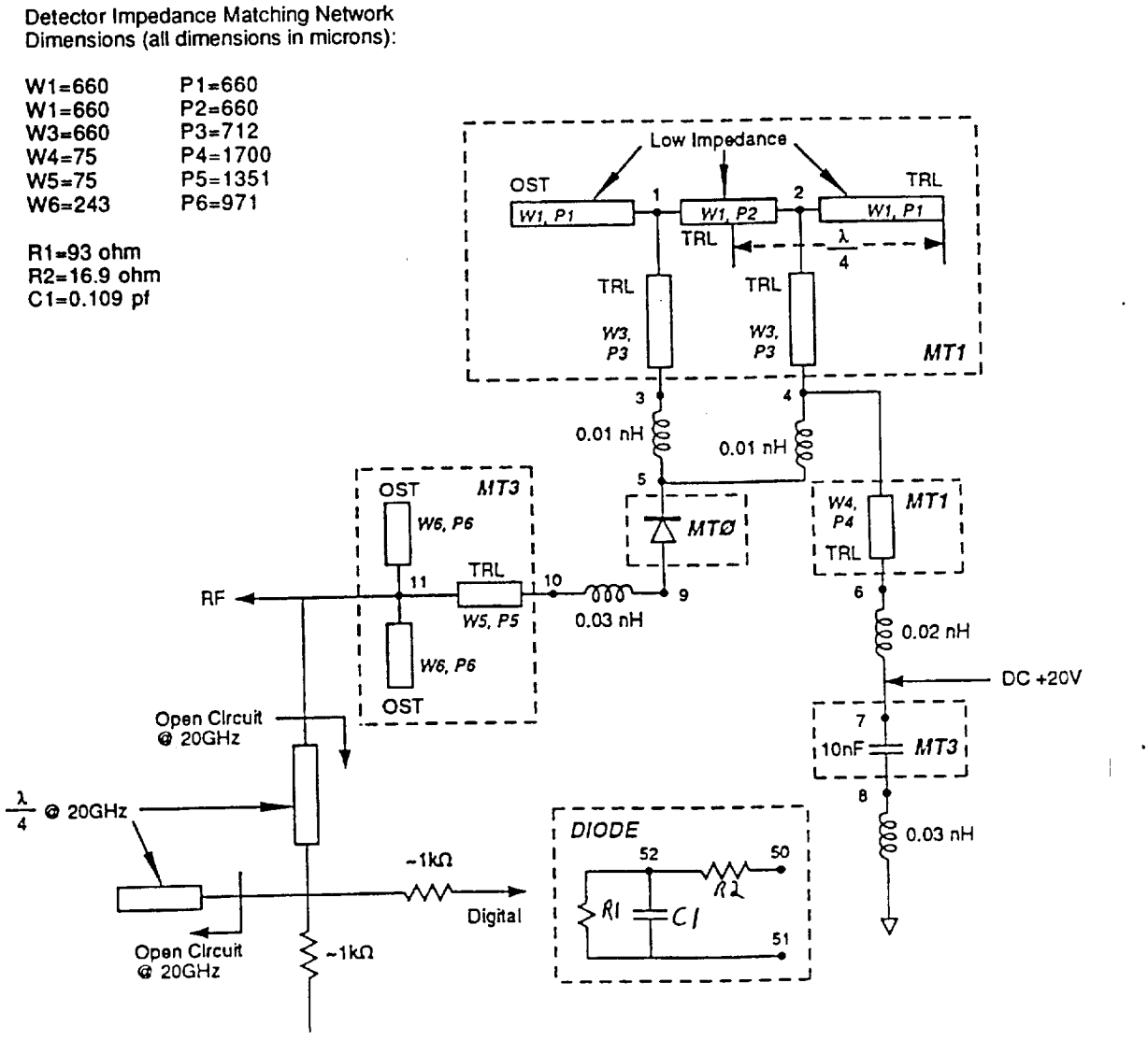


Figure 54. Impedance Matching Circuit Schematic

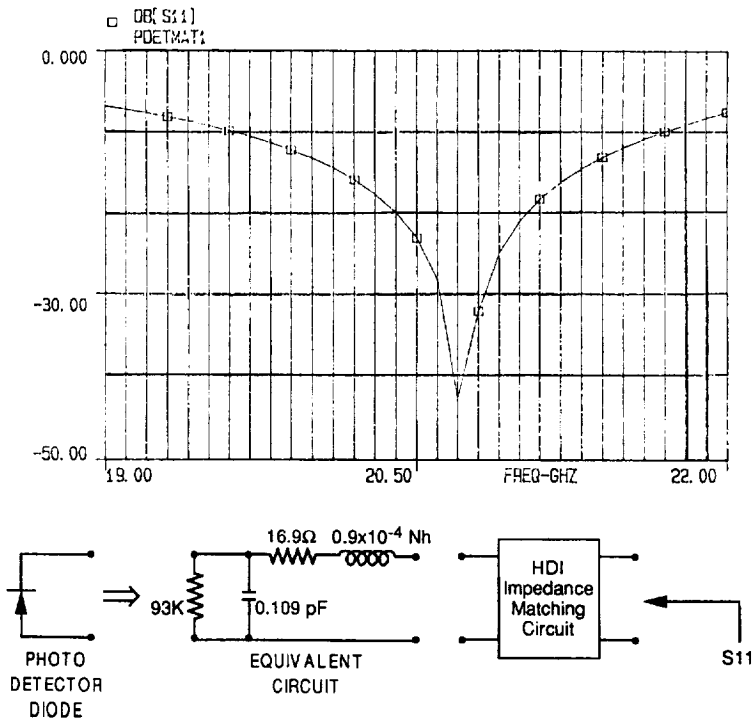


Figure 55. Impedance Matching Circuit Performance Data

Attaining the -9.5 dBm output power goal from the high-fidelity optical link module was important for the SLIC program as well as for HDI technology. The ability to combine the low cost capability of HDI with the low weight and RF immunity advantages offered by optical fiber represents a milestone for future airborne systems.

2.2.4 Commercial-Off-The-Shelf Components

In a few instances, when suitable off-the-shelf components were identified and could meet the rigorous performance and packaging requirement of the SLIC program, they were used. Two such cases are: the Manchester decoder and the RF power amplifier. These are discussed in greater detail below.

2.2.4.1 Manchester Decoder

This is a conventional off-the-shelf Silicon component provided by Harris Corp.

2.2.4.2 RF Elements

POWER AMPLIFIER MMIC DESCRIPTION

The amplifier MMIC chosen for this program, shown in Figure 56, is an existing design developed for the 20-GHz PHEMT Amplifier program.

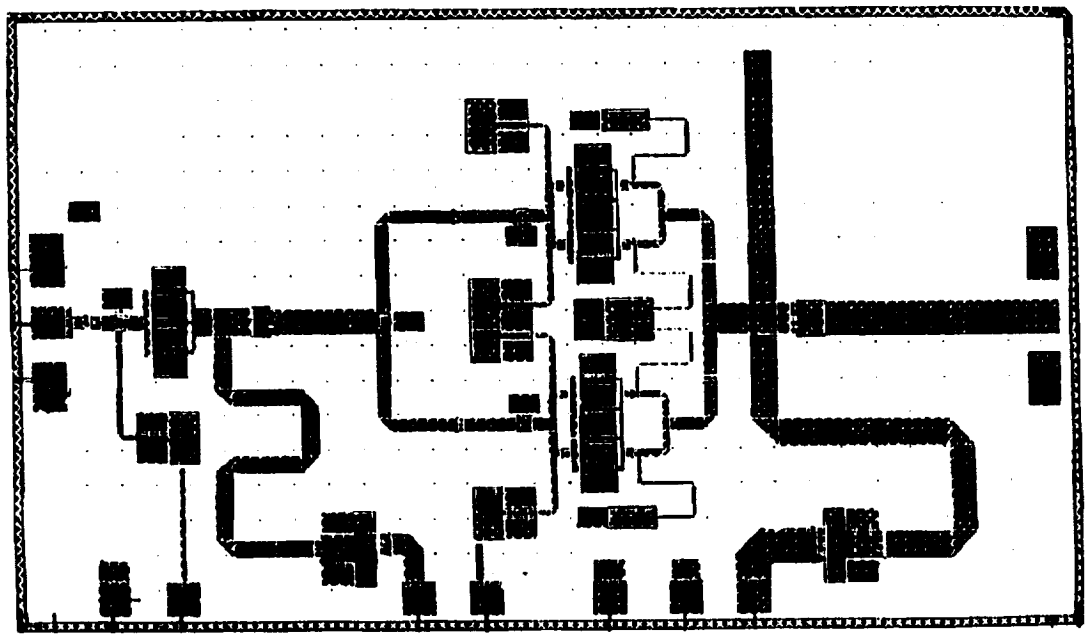


Figure 56. 20-GHz PHEMT MMIC Amplifier CALMA Layout

The power amplifier provides some of the gain to overcome optical RF link loss and to provide RF levels in the SLIC which are within the sensitive region of the RF power sensors in the gain loop. No off-chip input matching structures are required for the 2-stage PHEMT amplifier. The amplifier has a demonstrated 12 dB gain at 20 GHz. It is capable of 24 dBm of output power while attaining a 15 percent efficiency. Its compact size (2.12 x 1.74 mm) provides a minimal impact to overall module size.

Figure 57 illustrates test data collected on the K Band MMIC Amplifier. Test results for RF output power and power added efficiency have been provided.

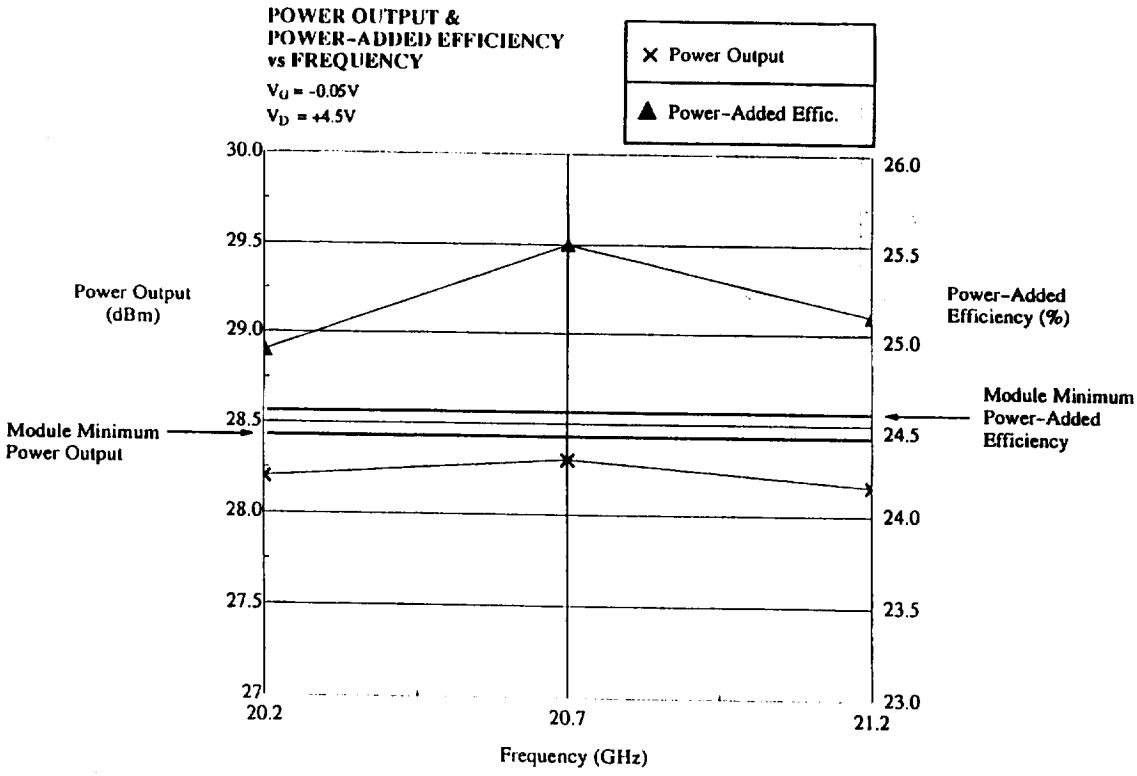


Figure 57. 20-GHz 0.75W MMIC PA Test Results

2.3 MODULE DEVELOPMENT

Illustrated in Figure 58 is the final version of the design drawing for the SLIC Module. This drawing was produced on a Mentor Hybrid Station. Extensive training was required to develop this design capability.

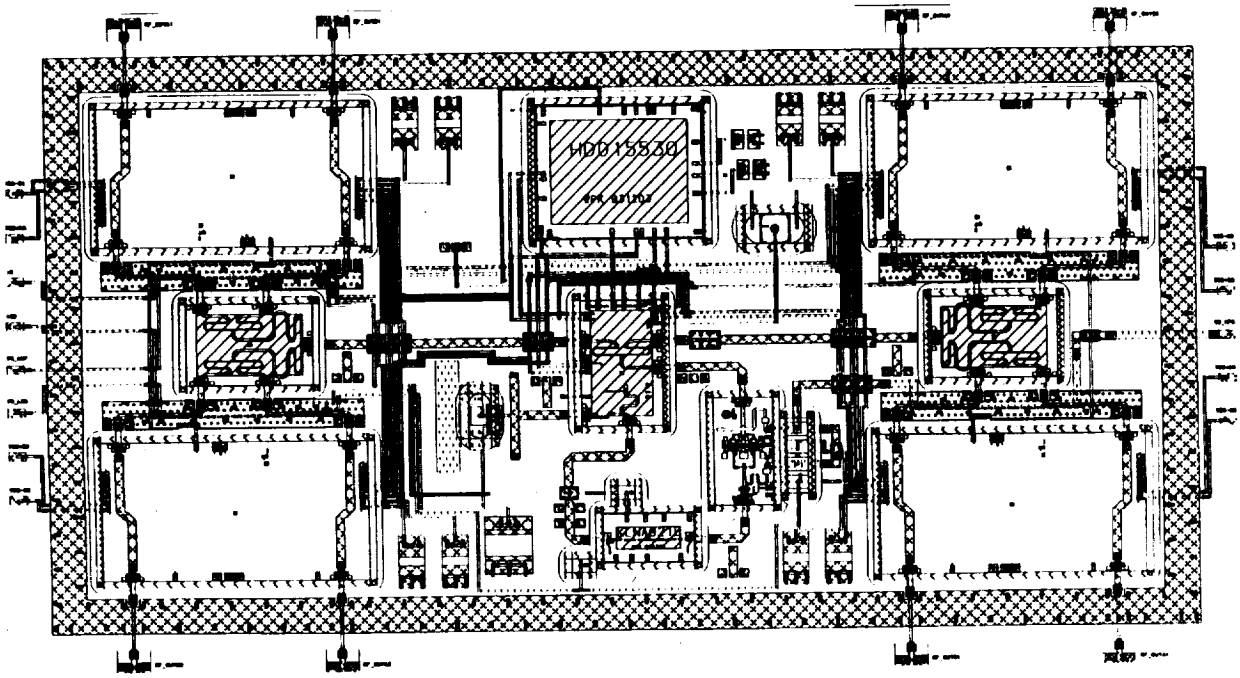


Figure 58. SLIC Module

Figure 59 demonstrates the partially populated product as developed from the design documentation.

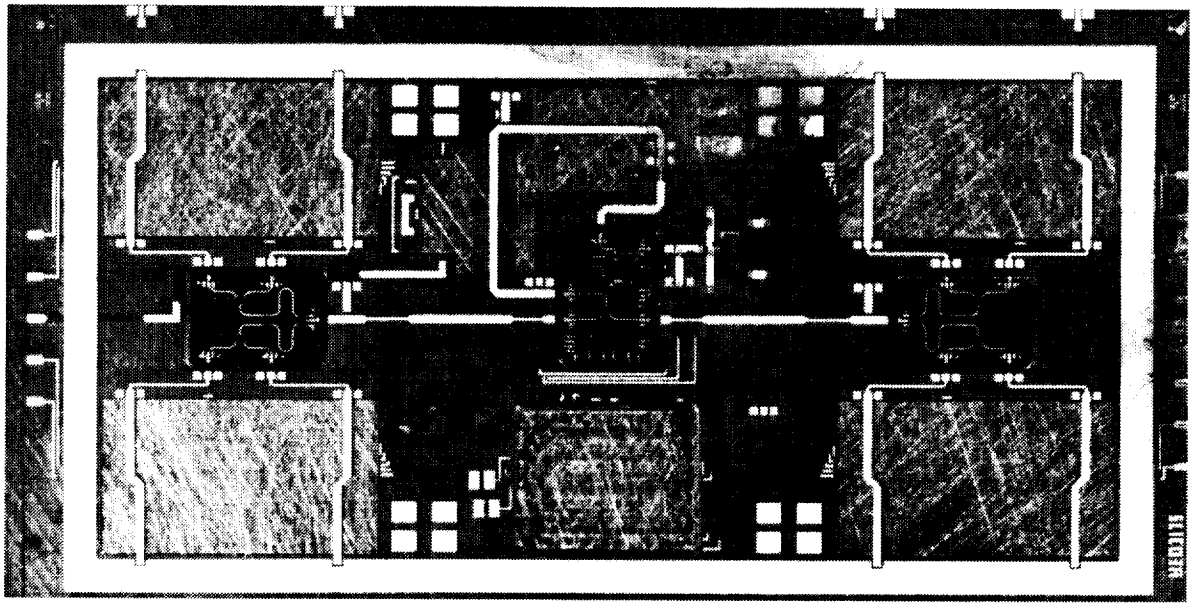


Figure 59. SLIC Module Substrate with GaAs Dividers and DIC MMICs

During the course of the SLIC program, ten modules were built [two mechanical models and eight functional units]. All eight functional units were tested on the ANA and the power bench. Several of the modules were fabricated with SLIC chips that had both A and B channels functional. These chips were selected so that when integrated into the SLIC Module the center four elements of the 8-element module would contain functional channels.

The remainder of the modules had SLIC chips with just a single channel functional. In addition, only a few modules were built with the fiber optic interface.

OBSERVATIONS/TEST RESULTS

The following observations were made during the test of the units:

- A fiber optic cable was successfully aligned with the photo detector diode [mounted in its pedestal]. This alignment was accomplished by monitoring the diode current when illuminated from a cable attached to the backside of he module baseplate.

- Although RF performance was excellant, overall MMIC yield was lower than expected due to problems with digital sections of the chip. Voltage drops across the chip, low logic noise margins, and high power consumption could have been corrected with additional iterations of the design.

- Various degrees of delamination of the Kapton from the silvar baseplate was present after HDI processing. For the most part, this delamination occurred outboard of the module seal ring and became worse as the temperature of the module was increased. For this reason, the

temperature range used in testing was limited to $\leq 50^{\circ}$ C. The delamination did not prevent the testing of the modules on the probe station. This delamination is an anomaly associated with adhesion to Silvar while in an operational design either Alumina, Aluminum Nitride or Aluminum Silicon Carbide would be used. None of these substrates has shown any delamination problems with MHDI. Silvar has been used successfully with MHDI and was used in this application as a cost savings.

- In order for the AGC loop on the SLIC chip to function properly, a power level of approximately +10 dBm or higher was required at the input to the chip. It was found during the test of the module that the amplifier chosen as the KPA driver did not have sufficient output power. This necessitated module rework so that an external source could be used as a driver. When this was completed, the drive levels to the SLIC chip were high enough for proper operation of the AGC loop.

- The data in the accompanying figures are provided to illustrate SLIC chip and KPA operation in the AGC loop.

- Figure 60 demonstrates the operation of the major attenuation states at a power level of +10 dBm at the input of the KPA. With a saturated gain of approximately 12.5 dB from the amplifier and a loss of 12.6 dB through the Wilkinson power dividers, the drive level at the SLIC chip input is +10 dBm. Figure 61 shows that with the attenuator preset in the 001000 state [mid-range], the AGC loop maintains an output level from the SLIC chip within 0.4 dB while the drive level to the KPA varies over a 10 dB range.

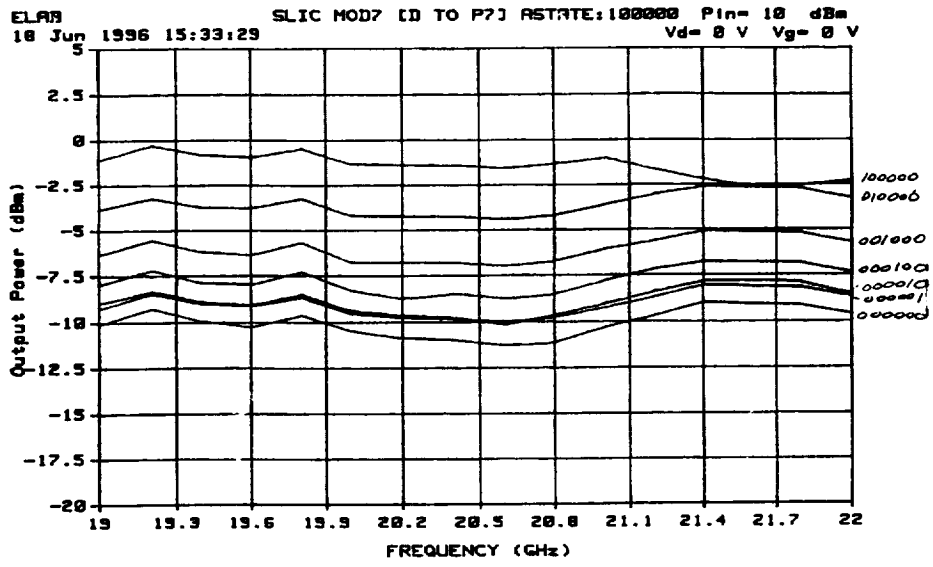


Figure 60. SLIC Module Performance Data

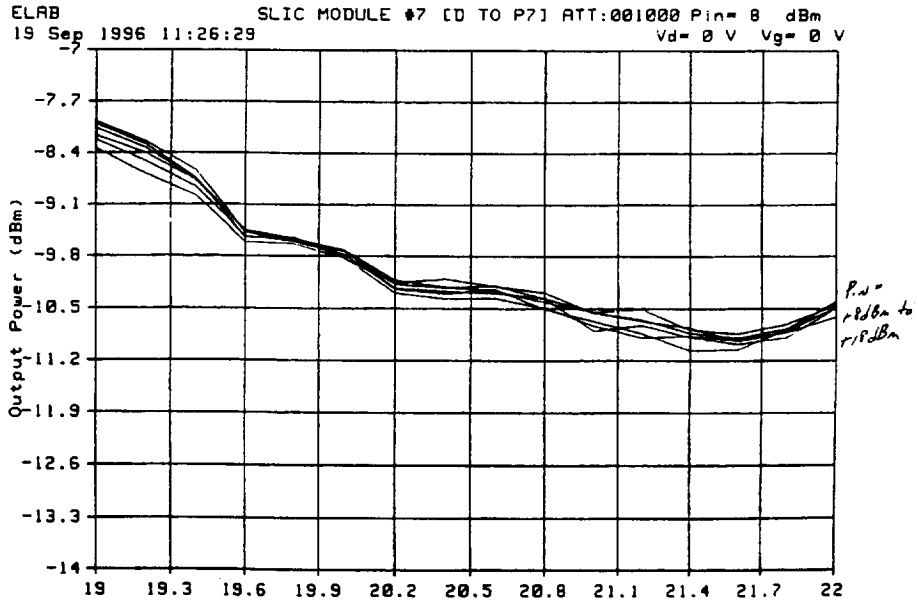


Figure 61. SLIC Module Performance Data

- There remains several unanswered questions concerning the operation of the modules after the completion of the HDI process. The modules were populated with functioning SLIC chips [wafer tested] and after HDI processing the attenuator ceased to operate while the phase shifter operated as expected. This condition was observed on several modules. In addition, one or two KPA chips did not function [no gate control] after HDI processing. One of these modules has been de-pelted and ablated and a scanning electron microscope (SEM) analysis of the SLIC chip has been undertaken to find any possible damage caused by the HDI process. The digital portion of the SLIC chips was not capped and there is a possibility that air bridges were damaged. The KPA chips were not tested prior to assembly, so there is a chance that the modules with non-operating KPA's were equipped with defective units. It is difficult to do a visual inspection on suspected damaged chips unless the KAPTON is ablated. It was easier to replace the defective KPA chips by performing surgery and then retesting.

- The SEM analysis of the de-pelted, ablated, defective SLIC chips mentioned above has been completed. The photographs shown in Figure 62 and Figure 63 show two problem areas. These areas were characteristic of areas all over the chip. The SEM photographs show that there are interconnect lines that are shorted. This damage must have taken place after wafer testing since the chips were functional when tested on wafer. The shorted or damaged interconnects would explain the problems observed at module test. A remaining task is to provide an explanation for the cause of the damage. The chips could have been damaged in handling after dicing, during the module assembly process, or during HDI processing. HDI processing has not historically shown problems with air bridges, unless the bridges were extremely long. This fact was known during the MMIC design phase and care was exercised to insure that the maximum air bridge lengths used complied with the HDI process. Other modules have been fabricated using similar numbers of air bridges and have not failed. At this point it is impossible to determine whether there was a perturbation on this specific HDI run or whether the chips were damaged in handling following wafer test.

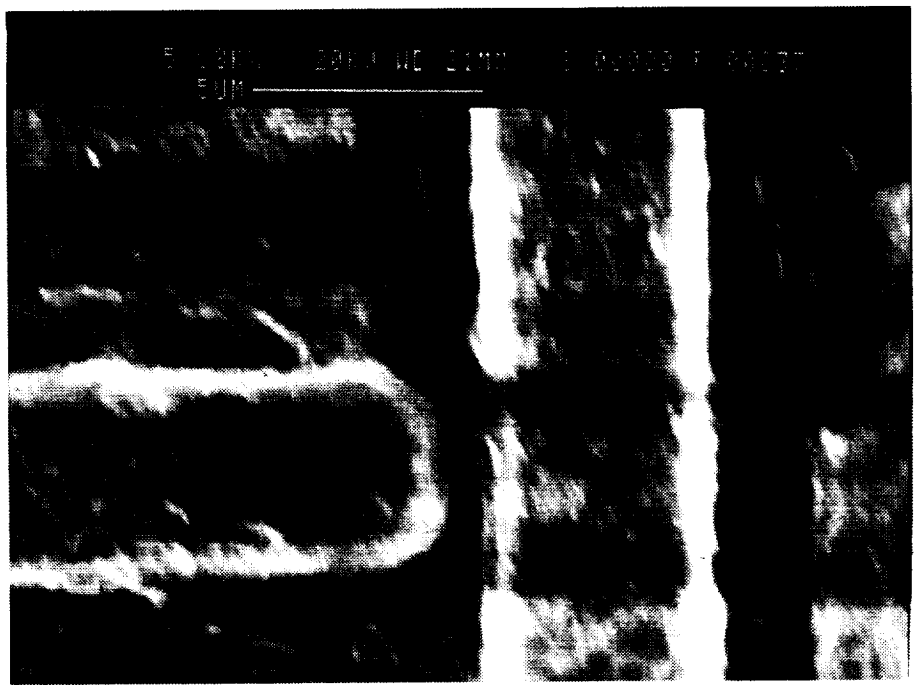


Figure 62. SLIC Module Failure

Figure 63. SLIC Module Failure

3. ALTERNATIVE ARCHITECTURE

The System Level Integrated Circuit Program demonstrated significant technological advances required for the development of a K Band downlink phased array. The SLIC module shown in Figure 64 applied several unique technologies to achieve ultra thin K-Band phased array building blocks that have built-in calibration and control.

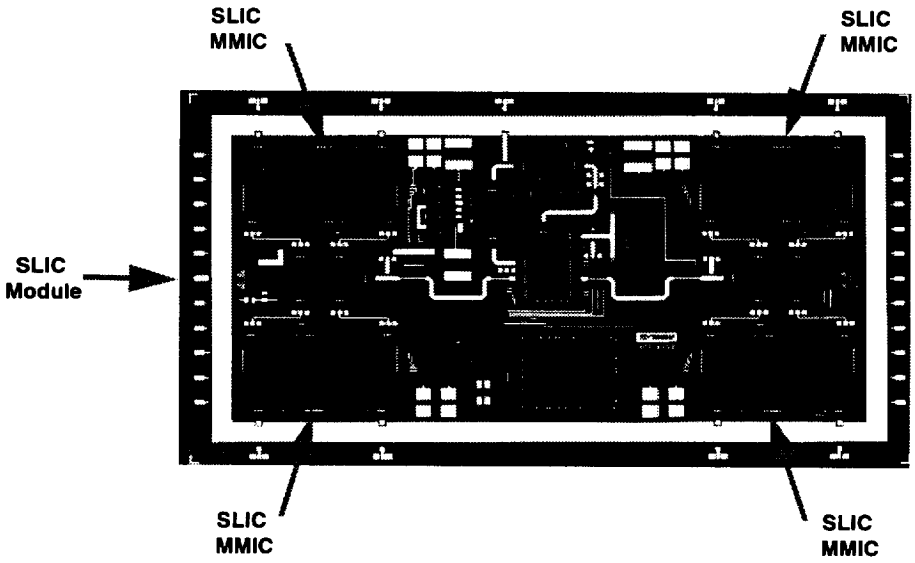


Figure 64. SLIC Module

The modules and MMICs successfully demonstrated the desired built-in test and calibration capability as well as superb automatic gain control as shown in Figure 65.

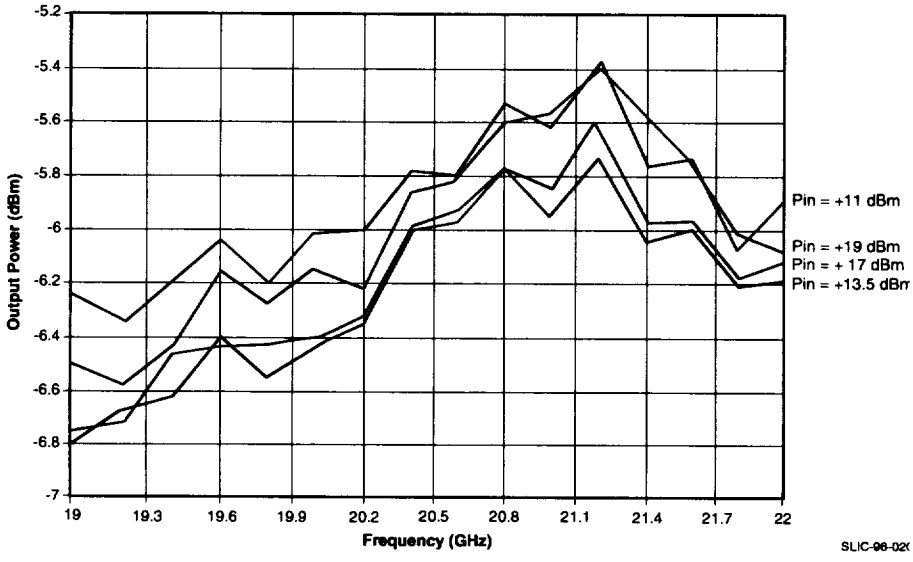


Figure 65. SLIC Module Performance Data

Though performance was excellent, yield was lower than expected. In addition, some physical and functional attributes of the SLIC module did not lend themselves to a practical phased array implementation. In particular low yields for the SLIC MMIC, the fragile module photonics interface, and the lack of a final RF power amplifier effectively precludes the use of the SLIC Module in a spaceborne phased array.

In the next two sections we detail proposed modifications to the SLIC Module Architecture to enhance yield and promote robust array operation.

3.1 MODIFIED REQUIREMENTS

In our original trade analysis for the SLIC MMIC module we arrived at a 2 by 4 radiating element configuration. In retrospect, this subarray selection unduly placed a premium on module floor-space and consequently had great influence on MMIC levels of integration. In light of these low yields, we have revisited this fundamental question of optimum building block size and determined 16 elements in a 4 x 4 grid sharing a single controller to be a better choice. This "Multipac" configuration best provides the necessary packaging overhead and yet results in a module complexity that has been demonstrated (with high yield) on our previous space based phased array MHDI beamforming modules.

Here are a few benefits of this selection:

- To accommodate the reduced area and increased RF circuitry while retaining the full AGC functionality, the elemental controllers must be replaced with a single module level controller that will sequentially calibrate each of the modules in the Multipac thus *reducing the amount of duplicated circuitry.*

- By using a single module level controller, we no longer are driven to use device technologies compatible with RF MMIC processes, hence a GaAs based controller is not required because a silicon based design is compatible. Not only will this reduce program risk since available control circuits can be used, *it will reduce controller power requirements by a 10:1 ratio* compared to the GaAs approach.

- The SLIC module does not contain the final transmit amplifier required for this application. Much of the area in the current SLIC design is consumed with the elemental control circuits that are located on each dual channel MMICs. By increasing array size *RF power amplifiers can be included in the subarray.*

In addition, the requirements for the photonics interface as well as antenna element spacing have been revisited:

- The SLIC module also employed a photonic link which was successfully demonstrated, however its relatively large size, high insertion loss and technical/cost immaturity at K Band leads us to recommend the delay of its insertion into a full array design.

- Finally, the element pitch in the SLIC module was designed for a +/- 20 degree scan increasing available component area. For a larger scan requirement (which is likely for low earth orbiting applications) the elements must be separated by smaller fractions of a wavelength to eliminate grating lobe formation.

PROPOSED ALTERNATIVE ARCHITECTURE

Sanders' proposed architecture has been developed as part of a systematic process in which NASA defined requirements have been allocated to functional blocks. Using recently gained knowledge from the System Level Integrated Circuit (SLIC) Program, these functional blocks have been organized in a manner that not only ensures compliance with defined performance objectives but optimizes implementation tradeoffs so as to improve the practical realization of the phased array antenna.

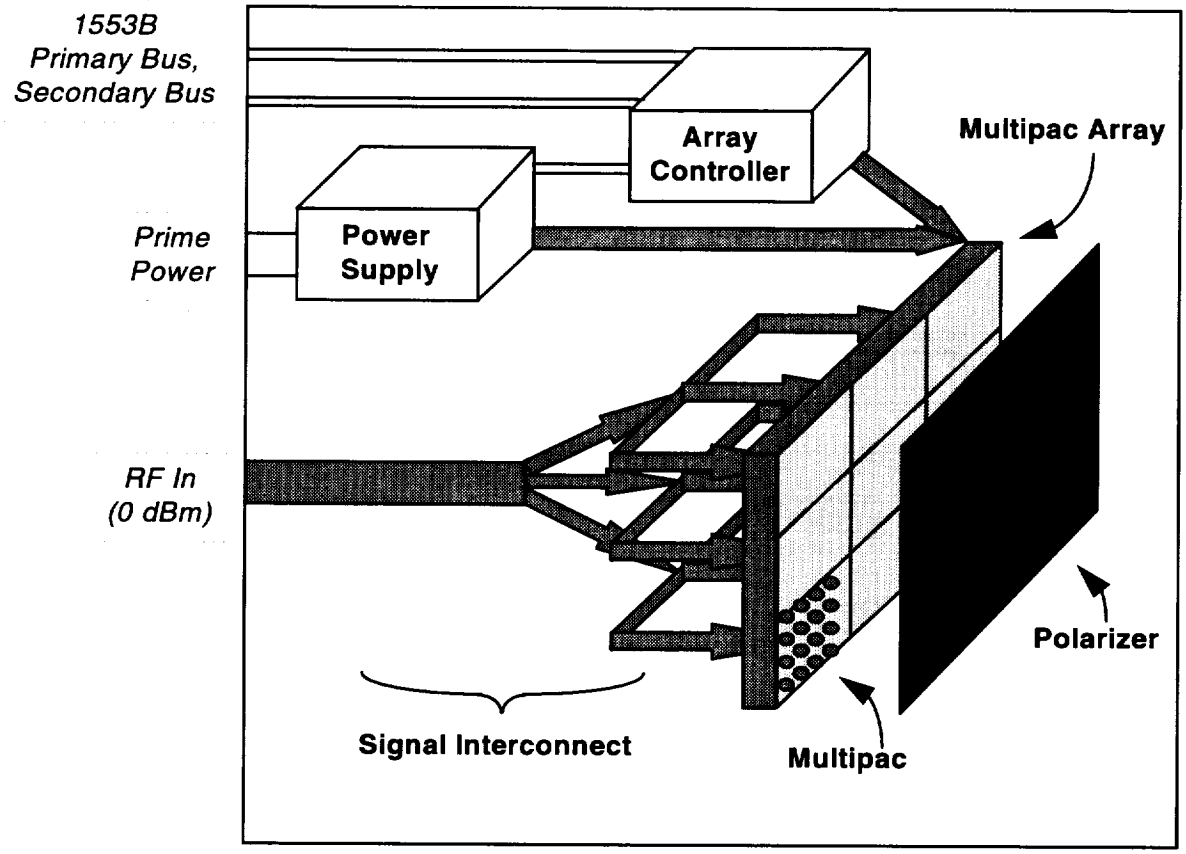


Figure 66. Phased Array Antenna Functional Block Diagram

Illustrated in Figure 66 is Sanders proposed implementation: a 144-element array implemented in a 3 by 3 Multipac configuration. Each Multipac block:

- is identical in implementation,
- contains a 4 by 4 antenna element array (utilizing nominal l/2 spacing),
- has integral RF power amplifiers, phase shifters and attenuators,
- has an automatic gain control (AGC) for temperature compensated amplitude control,
- has the circuitry necessary to provide phase control,
- has control over each individual element so as to perform calibration or diagnostic functions.

Right hand circular polarization is achieved with a polarizer external to the Multipac array. Overall antenna control is maintained with an array controller which interfaces to individual elements as well as external systems. Distribution of RF, DC and control signals is accomplished via a novel heatsink/distribution network on the backside of the array. A power supply converts prime power to forms suitable for MMIC, analog and digital devices. A total of approximately 150 Watts of power will be required by the array: 144 Watts allocated to RF functions and 6.3 Watts allocated to control functions.

MULTIPAC ARRAY

Array Size Tradeoff - To achieve a 30 dBW EIRP, a tradeoff analysis between the number of elements in the array and power per element is required. Lower power elements require larger arrays but the total power per array is reduced. With higher power transmitters, the array requires fewer elements but creates a higher thermal load. Figure 67 presents the tradeoff in EIRP versus the number of array elements for various transmit power levels. The assumptions made in this curve are summarized in Table XII.

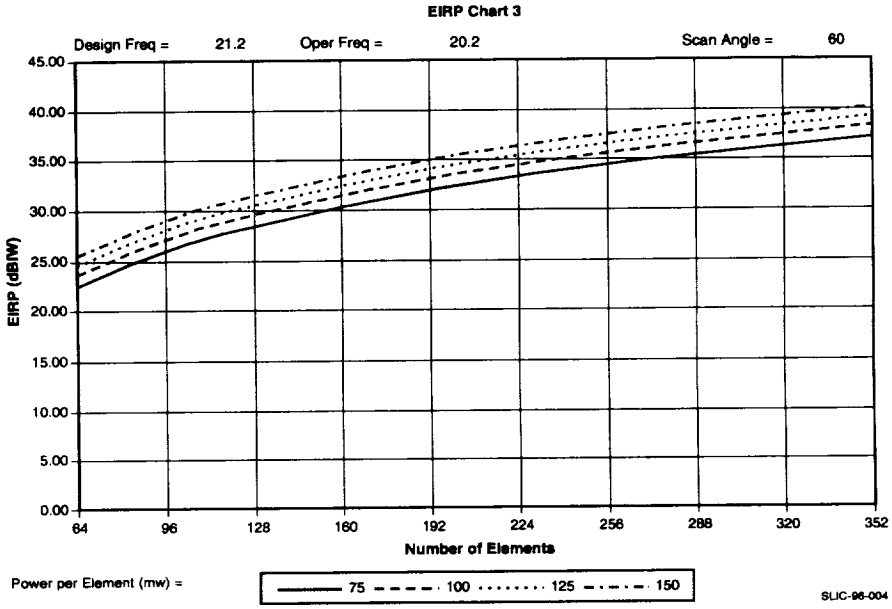


Figure 67. Array Size Vs. RF Power

With a 75 mW transmitter a 30 dBW EIRP is achieved with a 160-element array (includes 0.4 dB margin). With 125 mW an EIRP of 31.7 dB is achieved with 144 -elements providing design margin. Our design will be based on a 144-element array since even with a 100 mW amplifier an EIRP of 30.7 dBW is achieved still providing margin and thus reducing risk.

The 144-element array is comprised of nine 16-element Multipacs arranged in a 3 Multipac by 3 Multipac grid . Since the array will be designed with an excellent heat sink directly on the back of the Multipac, heat can be readily removed. Even assuming a low efficiency of 10 %, the total heat load is 1 watt per element spread over a 3.6 x 3.6 inch area which is compatible with our thermal design.

Table XII. Multipac Array Assumptions

Array Parameter	Value
Losses After Power Amplifier	1.1 dB
Radiator Efficiency	0.7 dB
Amplitude/Phase Error	0.5 dB
Polarization Mismatch	0.25 dB
Active Mismatch	0.5 dB
Scan Loss at 60 degrees	4.5 dB

ARRAY/MULTIPAC CONTROL

Array Control - Maintaining continuity with the control architecture developed on the SLIC Program, SLIC Based Phased Array control is accomplished with two levels of circuitry. As shown in Figure 68, there is a single Array Controller for overall control and a Module Controller in each of the Multipacs for local control.

The Array Controller communicates with the On-Board Computer (OBC) via a MIL-STD-1553 data bus. The Array Controller receives direction cosines from the OBC, from which required phase settings for each element of each module is computed. This data is serially transferred (as it is computed) to each Multipac module controller. After all data is loaded, it is transferred to the phase shifters. The On Board Computer is capable of adjusting every attenuator setting, and Power Amplifier Bias point over the same interface. Power Amplifier RF level and temperature data are also available via this interface.

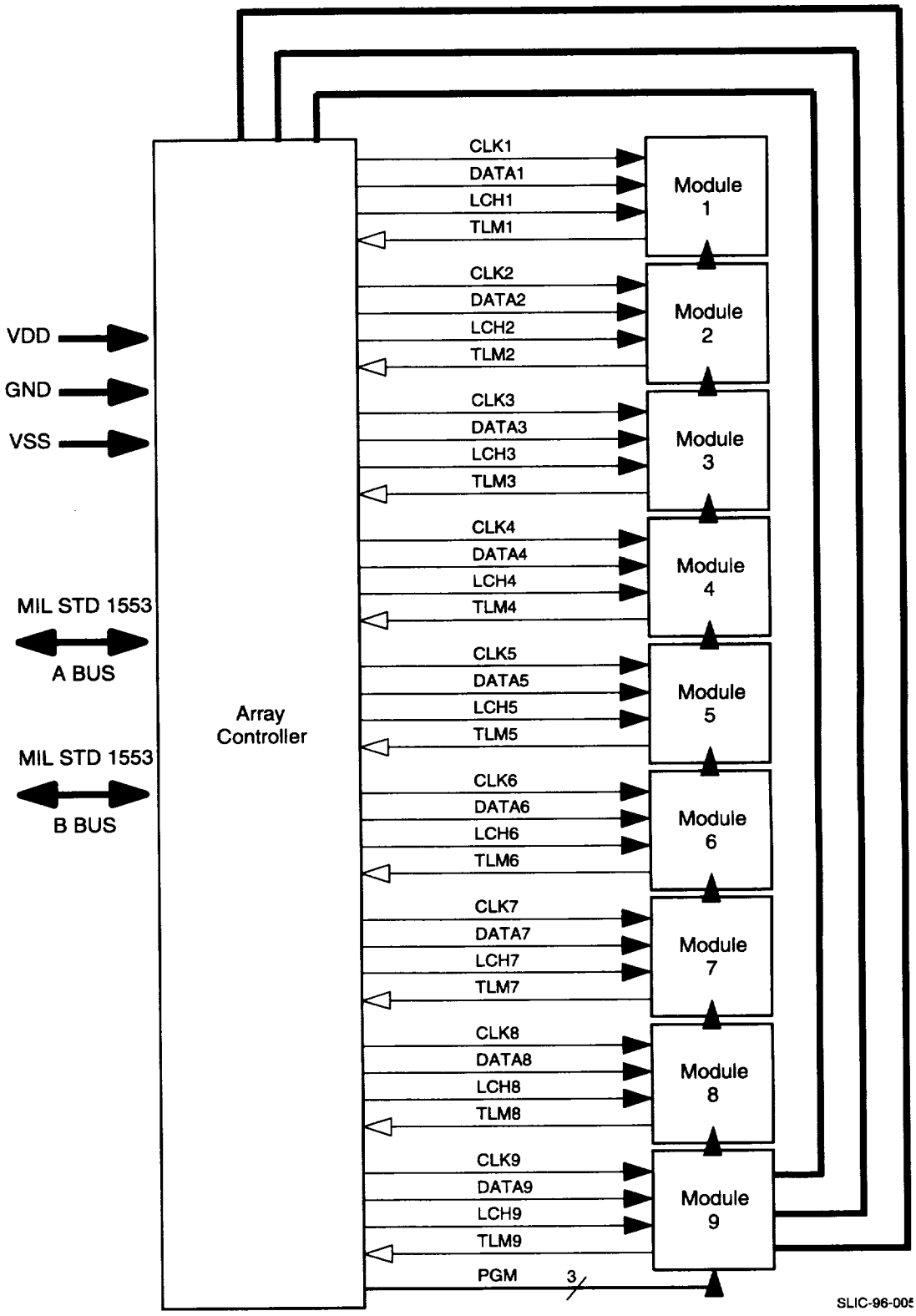
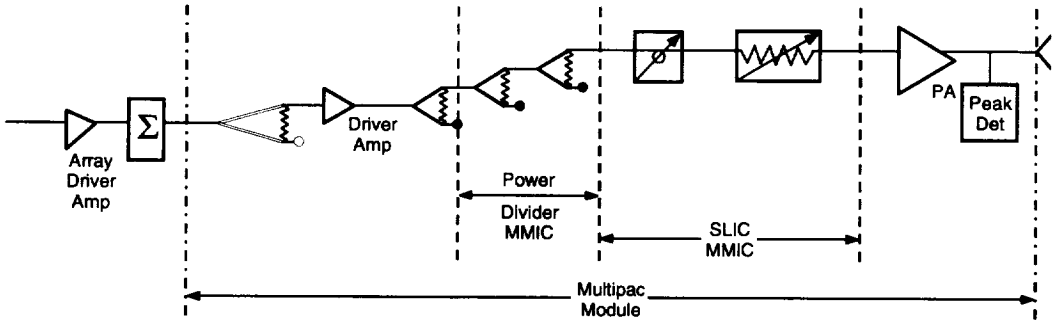


Figure 68. Array Controller Signal Distribution

ARRAY RF ARCHITECTURE

Figure 69 illustrates our proposed RF architecture for the Multipac Array. The architecture is essentially the same as was used and proven on the SLIC Program. As a result, we see no reason to evaluate alternative architectures at this juncture. Implementation differences have arisen because of a change in the number of radiating elements per Multipac and the elimination of a photonic interface.



Component	Gain / Loss (dB)	Power Level at Output (dBm)
**Array Driver Amp	30	30
Array RF Distribution Net	-11.6	-18.5
Power Divider #1	-4.2	14.3
Driver Amp	10	+24.3
Power Divider #2	-4.2	+20.1
Power Divider #3	-4.2	+15.9
Power Divider #4	-4.2	+11.7
Transmission Line	-0.7	+11
Phase Shifter	-6	+5
Attenuator	-5	0
Power Amp	+21	+21
*Peak Detector	-1.0	-20

Multipac Module

* **Note:** Attenuator is set at -3 dB loss, in order to provide for an up or down movement in its setting
** **Note:** Assume 0 dBm at Array Drive Amp Input

SLIC-96-007

Figure 69. Multipac Single Channel RF Architecture

Each of the modules within the Multipac array is fed from a common Array Driver Amplifier via an Array RF Distribution Network. The Array Driver Amplifier boosts the RF power level prior to splitting it nine ways. In addition, the amplifier provides an excellent match for the antenna array and serves to isolate the input from elements downstream.

Each of the nine Multipac modules have integral driver amplifiers and power distribution networks. The driver amplifiers serve the same purpose as the Array Driver Amplifier, to boost RF power levels prior to splitting. The power splitters feed RF to 16 separate channels. Each of the 16 channels on the Multipac has its own phase shifter, attenuator and power amplifier.

3.2 MODIFIED IMPLEMENTATION

MULTIPAC DESIGN

Each Multipac is 1.2 x 1.2 x 0.1 inches and contains all the electronics required to support 16 radiating elements, including power amplifier and phase shifter MMICs, power dividers, and control ICs. Sixteen stacked patch radiating elements are arranged 4x4 at a spacing of 0.3 inches, fixing the size of the Multipac in those dimensions to 1.2 inches. In addition to 22 GaAs MMICs, each Multipac will contain at least 49 silicon control die to provide SLIC functionality. Figure 70 shows the plan view of the Multipac indicating the circuit density. Multipac building blocks will be used to build up a thin phased arrays which will take minimal real estate on the host spacecraft.

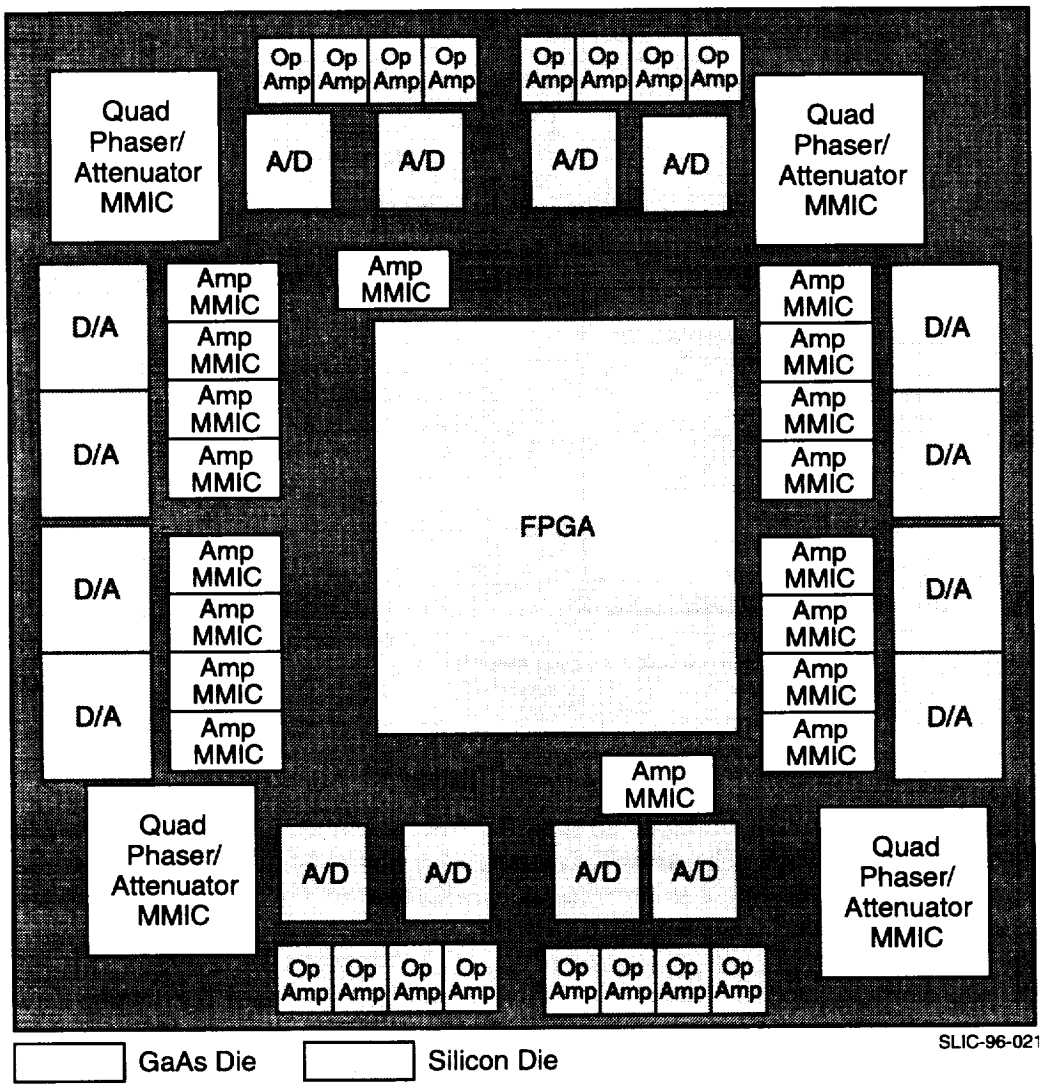


Figure 70. Plan View of the Multipac

The yield on these modules is expected to increase dramatically compared to the SLIC modules since many of the components, in particular the Silicon control chips, are more robust than the TriQuint analog/digital elements. Long air bridges on the TriQuint control elements makes them more susceptible

to crushing, greatly reducing yield. All of the RF functions are designed compatible with MHDI rules and will be high yield as proven on our MHDI beamformer modules for our commercial satellite and for SHF military satellite applications. Figure 71 shows the SHF beamformer module developed for Rome Laboratory were 16 gain and phase control MMICs where integrated with 34 silicon chips with yields of 100% at the module level.

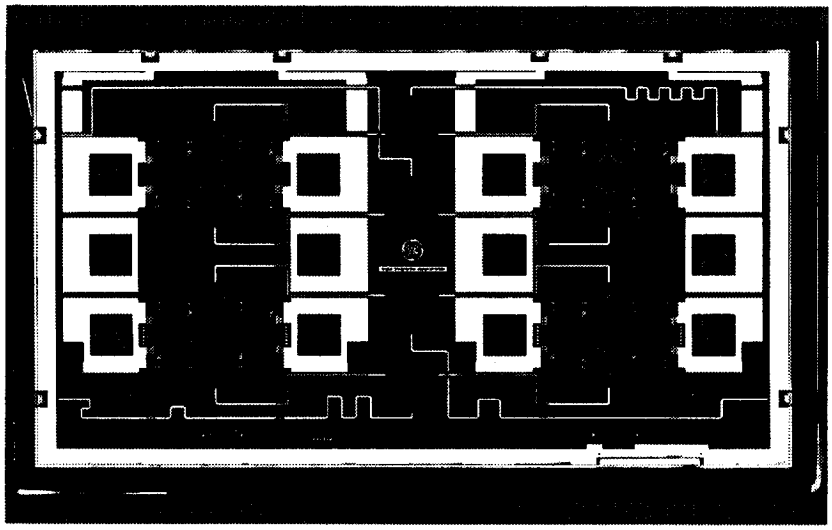


Figure 71. MHDI Beamforming Matrix Module

Several DoD-funded programs have demonstrated high yield on modules with the complexity level of the Multipac. A C-band MHDI T/R module program demonstrated >80% yield at first turn-on with no rework for about fifty modules. A later X-band MHDI T/R module program demonstrated 90% yield at first turn-on with no rework for about twenty modules containing 8 GaAs MMICs, 3 silicon ICs, and 13 chip resistors and capacitors. These programs showed that module yield is dependent on GaAs MMIC yield. "Known good die" make good high-yield modules.

Multipac Substrate - The 16-element thin tile Multipac will be constructed on substrate which will hold components in place and provides vertical interconnect so that RF, DC, and control signals can be fed into the bottom of the Multipac. This will enable Multipacs to be placed closely together in the array, preserving the critical element spacing. The substrate will also provide the thermal path from the active circuits to the array heatsink, so a thermally conductive material is indicated. We believe a co-fired aluminum nitride material is the best choice for substrates.

Multipac Fabrication - The tile Multipac will be fabricated using Microwave High Density Interconnect (MHDI). MHDI is a high yield interconnect process that has been proven for high performance electronic uses through 60 GHz. MHDI is a Polyimide multi-layer interconnect process that routinely achieves a 2:1 size reduction on digital and RF circuitry compared to more conventional interconnect technologies. Replacing wire bonds with MHDI vias through 1 mil Kapton Polyimide film, provides excellent low inductance connections between MMICs with a return loss of 30 dB at 40 GHz. MHDI also provides controlled impedance transmission lines that extend directly over the MMIC bond pad, resulting in excellent lot-to-lot repeatability. This eliminates the variations in MMW performance seen with variable lengths and heights of wire bonds. Additionally MHDI is a planar process which constrains the field in the dielectric, resulting in reduced circuit-to-package coupling effects, unlike wire bonding. Also MHDI is compatible with diverse component technologies eliminating the need to custom design elements for module insertion. Placement of an air gap over critical RF elements on the MMIC will

ensure they are not affected by the presence of the dielectric. Importantly, it allows us to place a ground plane over the MMICs shielding them from the layers above enabling the direct integration of the radiating elements.

MHDI is also a batch manufacturing process where multiple modules are fabricated simultaneously on a single wafer as shown in Figure 72 where two beamformer modules and a number of power modules are fabricated on a single 6-inch wafer. Semiconductor style interconnect and testing will lead to reduced assembly and test costs. For the SLIC based array, 16 of our 16-element Multipacs will be integrated on a single wafer.

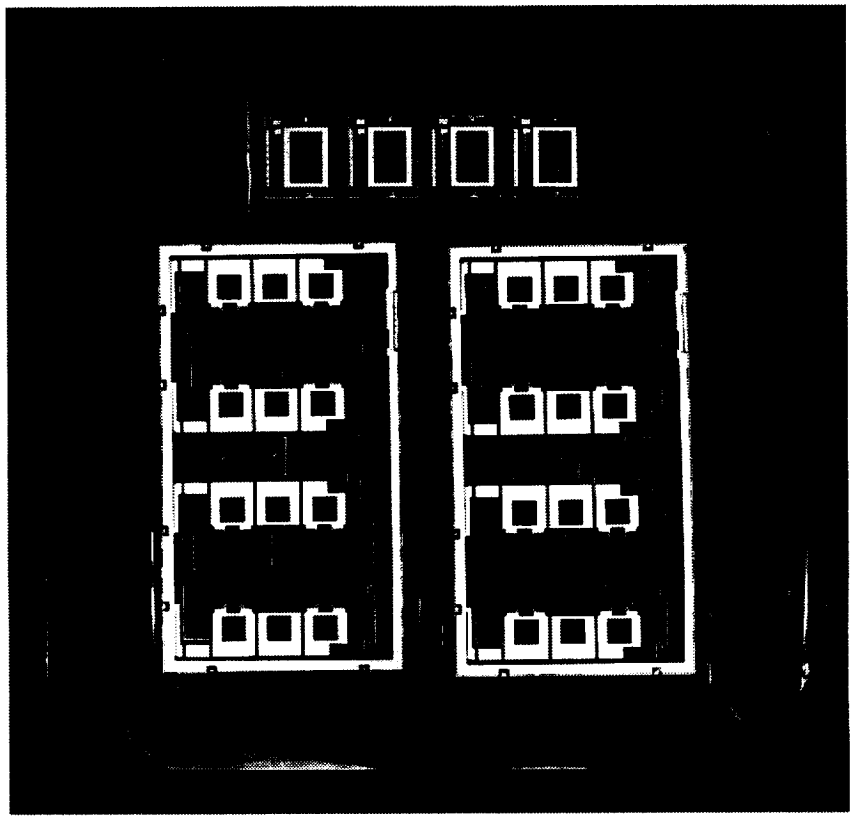


Figure 72. Batch Manufacturing MHDI Modules

Stacked Patch Radiating Elements - The Multipac fabrication process will include direct attachment of radiating elements to the top surface of the MHDI. This batch process will fabricate many array elements simultaneously to preserve low production cost on the complete Multipac. On our 1996 IRAD program, GE CR&D has developed a process for the attachment of radiating elements on the top side of the MHDI module. Solder-bumps are applied to the MHDI and using automated pick and place equipment the stacked patch element is located and aligned with the bumps so when heated the connection form the module to the driven patch is made. Figure 73 shows the results of this development on a test circuit. These were sample patch designs to verify the process.

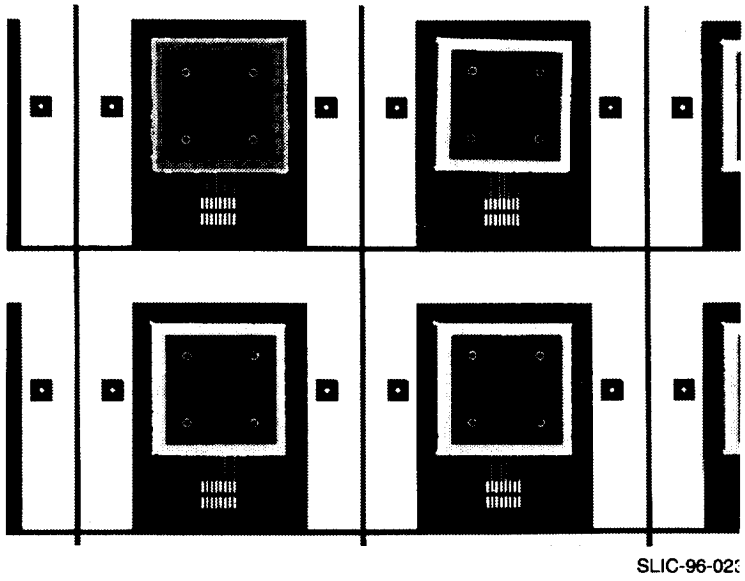


Figure 73. Stacked Patch Process Development

Multipac Test - Completed Multipacs will undergo RF test to ensure they are good prior to integration into the array. Multipacs are 16-element sub-arrays at this point with one RF input and sixteen radiating elements at the output so testing will be done in an antenna range. The electronics behind each element will be checked out individually, then the entire Multipac will be exercised functionally.

The key elements of the Multipac fabrication include:

- Procurement of thin Multipac substrate with integral vertical feed-throughs.
- Attachment of known good MMICs onto shims that form the DC ground and thermal path.
- Automated pick and place of the die/shim onto an adhesive on the Multipac substrate.
- Application of the 3-layer MHDI process to form a 16-element Multipac.
- Radiating elements are attached to the top surface of the completed MHDI Multipac.
- Individual Multipacs are RF tested to select known good Multipacs
- Known good Multipacs are ready for array integration and test.

ARRAY DESIGN

Array Size - For a 155 Mbps application, 144 elements (nine Multipacs) provides a 30 dBW EIRP with some margin. However the baseline concept is readily expandable to 622 Mbps and beyond by increasing the number of Multipacs. The larger array requires no changes to the Multipac building block, but does require a larger structural/thermal frame and a bigger signal distribution manifold which are simple extensions of the baseline.

Array Mechanical Configuration - There are two major parts of the array in addition to the Multipacs, the structural/thermal frame and the signal distribution manifold. The structural/thermal frame has two functions; it must hold the Multipacs in a mechanically rigid lightweight holder which will allow Multipacs to be removed for repair. It also must provide an excellent thermal path to the back of the array.

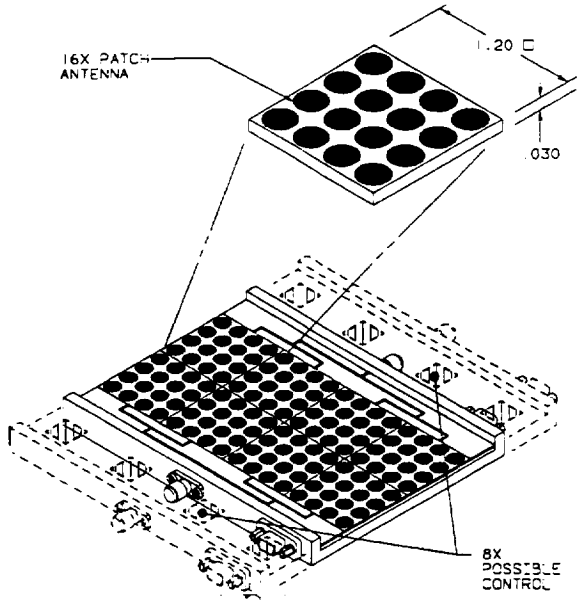
The signal distribution manifold must route RF to each of the nine Multipac inputs. Feedthroughs in the Multipac substrate feed the RF input signal, the control signals and the DC power from the frontside to the back where the connections to the distribution substrate are made. It is assumed that a lightweight planar medium such as multi-layer Duroid would be a good candidate for this function. Outputs of the nine-way RF signal distribution manifold would be wire-bonded to the RF input on the back of each Multipac. The signal distribution manifold must also carry DC and control signals to each Multipac. A planar flex interconnect would be wire-bonded to Multipac inputs to achieve this function. The signal distribution manifold must be carefully designed to work with the structural/thermal frame so that reparability is maintained and the array has a good thermal path to the back cover.

Array Assembly - SLIC Based Phased Arrays will be built using only known-good Multipacs.

Key elements of the assembly of the array include:

- Nine known-good Multipacs are inserted into a 3x3 frame
- Nine-way RF divider manifold is attached
- DC/Control harness is attached
- Array structure, which is also the major heatsink,
- Array is tested, if any Multipacs are found to be bad the assembly process is reversed and the bad Multipac is replaced

An alternate configuration has also been developed as shown in Figure 74 that eliminates the need for the RF and control to be fed from the backside of the Multipac. The Multipacs are configured in a 2 x N arrangement with RF power dividers and possibly control circuits located on distribution boards along the two long sides of the array. I/Os on the sides of the Multipac are wirebonded to these distribution boards resulting in a easily constructed and repaired design. The alternate configuration allows us to place some of the control electronics on the sides of the array and not in the Multipac in the event that the complexity grows beyond the current projection. The only negative of this approach is the limitation of the array configuration to a 2 x N array which means to increase data rate, the array can only grow in one dimension resulting in narrower beams. The 30 dBW requirement can be met with a 2 x 4 or more conservatively a 2 x 5 configuration. This is not a problem from the beam pointing perspective since the controller can update the beam position much faster than the specified beam update rate allowing us to change position even with the narrower beam.

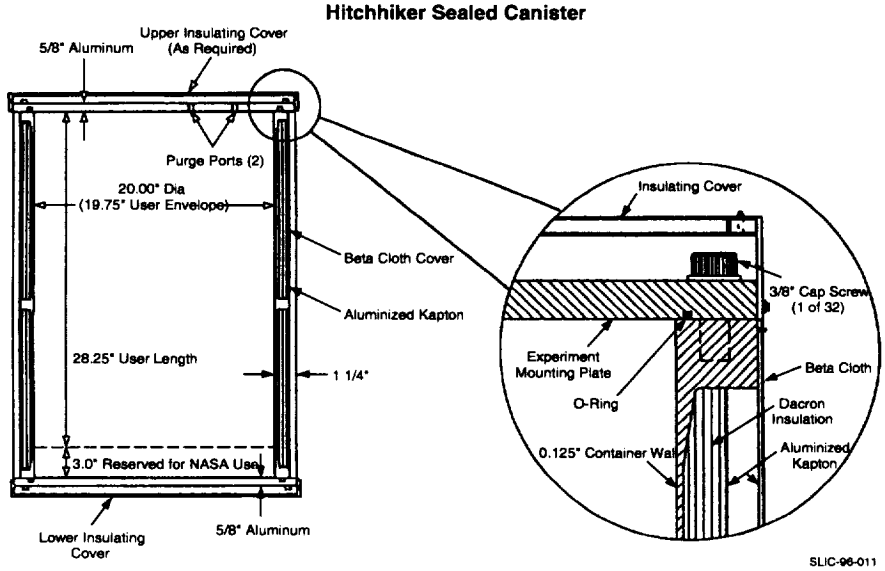


This configuration greatly reduces array integration complexity and forms our risk mitigation.

Figure 74. Alternate Array Configuration

Array Integration - The array design is compatible with integration requirements for a NASA Class D space experiment. Figure 75 and Figure 76 depict the array in the cargo bay of a space shuttle. NASA would be responsible for defining the interface requirements for the array, both mechanical and electrical. Our design assumes that the "Get Away Special (GAS)" canister provides a controlled electrical, thermal, and atmospheric environment.

In addition to the SLIC Based Phased Array, the GAS canister would have to contain array control electronics for interfacing with the space shuttle payload as well as possible power conditioning electronics.



The GAS canister will provide a benign environment for all interfaces to the shuttle payload.

Figure 75. Sealed Canister

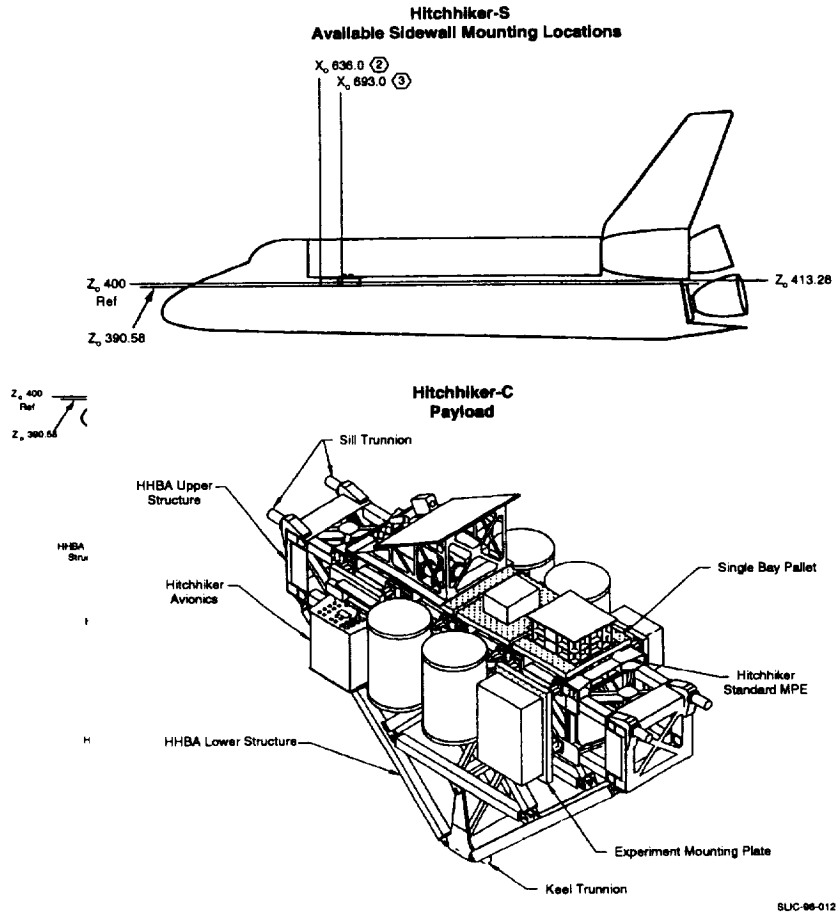


Figure 76. Space Shuttle Experiment Payload

ACTIVE ARRAY CONTROL DESIGN

The alternative control architecture is very similar to that developed on the SLIC program. The main differences are implementation driven. Control for the Active Downlink Array will be accomplished by two levels of circuitry. As shown in Figure 77, there will be an Array Controller, which will communicate with the On-Board Computer (OBC) via a MIL STD 1553 data bus. The maximum beam update rate of two beams per second can easily be accomplished over the MIL STD 1553 bus. The Array Controller receives direction cosines from the OBC, and computes the desired phase settings for each element of each module. This data is transferred as it is computed to each module, n, over a serial data line using signals CLKn and DATAn. When all the data has been loaded, it is transferred to the phase shifters when LCHn occurs. The On Board Computer can also adjust every attenuator setting, and Power Amplifier Bias point over the same interface. Each Power Amplifier RF level and temperature can be read back over the telemetry lines, TLMn. The Array Controller also receives prime power from the spacecraft, and conditions it to drive the nine modules with +5V, GND, and -5V. The +5V and -5V will be distributed via a busbar matrix embedded in the array. The entire metal heat sink structure will provide electrical and chassis ground.

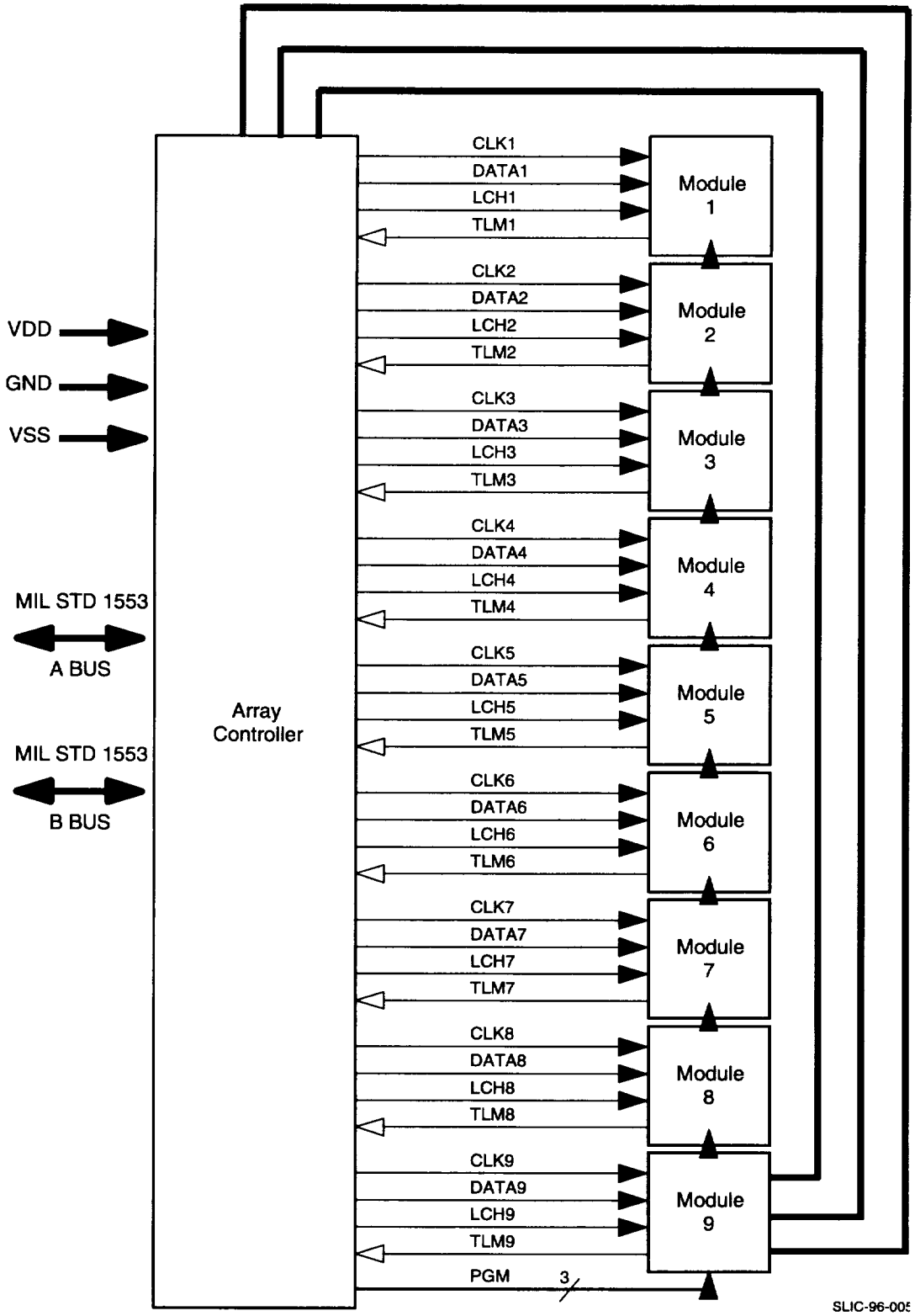


Figure 77. Array Control Architecture

Module Control - Our plan for module level control is to build on the successful portions of the SLIC program, while replacing the risky portions with off-the-shelf circuitry wherever possible. The successful portions of SLIC included the phase shifter and attenuator, as well as the AGC loop coupled to the RF detector. Our desire for the Active Downlink Array, however, is to monitor the RF power out of the Power Amplifier, which was not included in the SLIC MMIC. We believe the lowest risk approach to building a full-up array involves sharing the module control function among a set of sixteen elements. Figure 78 shows the module architecture.

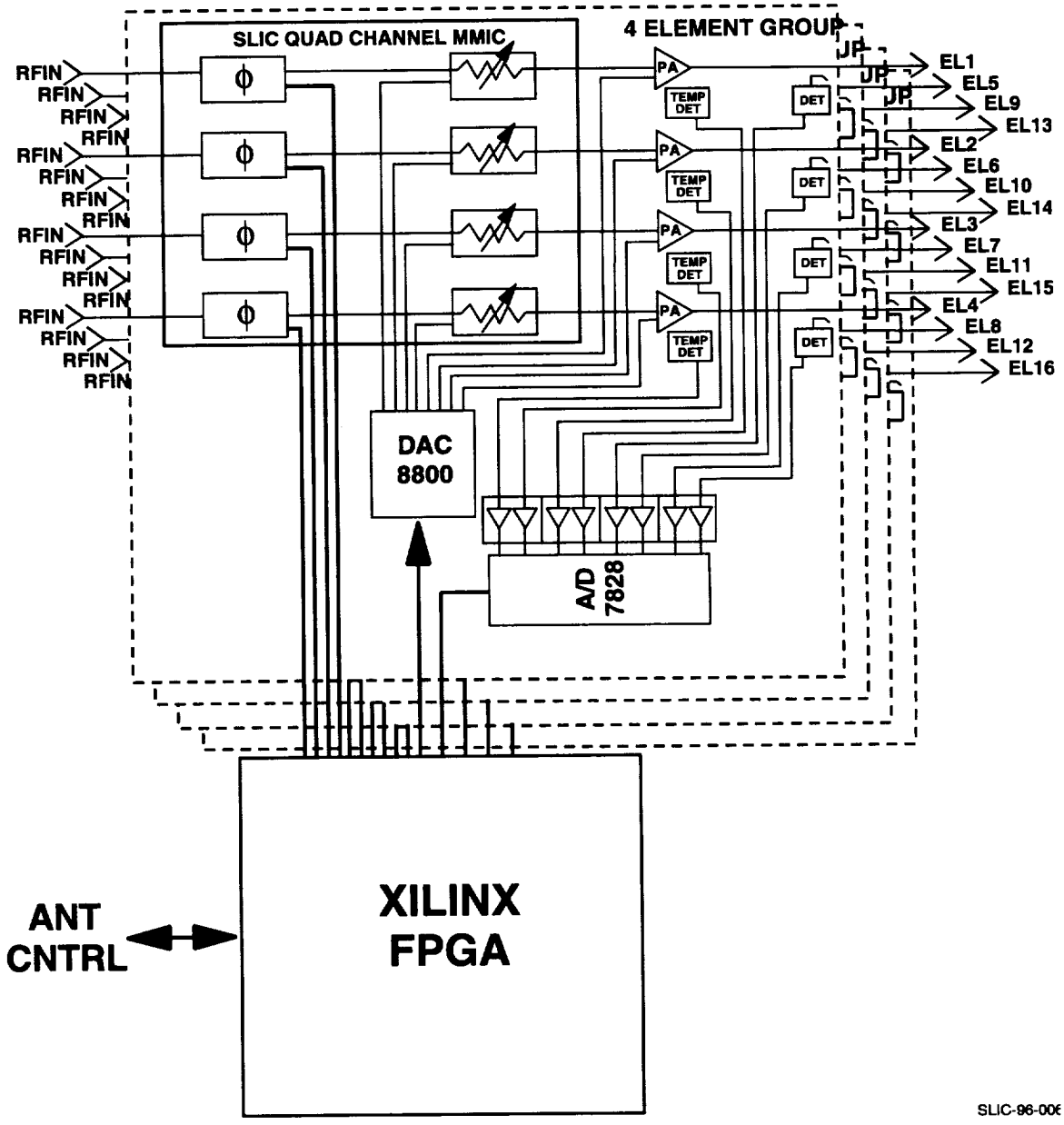


Figure 78. Module Controller Architecture

Each group of four elements has a Phase Attenuator MMIC, which will consist of four phase shifter attenuators lifted from the SLIC design, a Power Amplifier, a detector circuit, an octal eight-bit A/D (AD7828), an octal eight-bit D/A (DAC8800), and four dual op-amps. The detector circuit is coupled to each Power Amplifier output, and is scaled via one of the op amps to drive one channel of the A/D. A temperature sensing diode is also placed in close proximity to each Power Amplifier. Its output is also scaled via one of the op amps to drive a second channel of the A/D. One D/A channel is used to control the analog attenuator, while a second is used to set the bias point of the Power Amplifier. Each Power Amplifier can be shut off by setting its bias voltage in the "pinch-off" region of the amplifier. This would be used for calibration, or if the temperature exceeded a set threshold. The AGC loop can be set to operate either digitally, or in analog fashion. A digital loop would execute the following sequence at about a 10 Hz rate:

DIGITAL AGC LOOP

1. For n = 0, 1, 2, 3
2. Read A/D channel n (Element n output detector level)
3. Compare level to programmed allowable range (established during calibration)
4. If amplitude outside range, increment/decrement D/A n (Attenuator setting)
5. Read A/D channel n+4 (Element n temperature)
6. If temperature too high, set D/a n+4 to 0 (PA bias in "pinch-off")
7. next n

Alternatively, the D/A could be used to set a desired detector output, which would drive one input of the op amp. The other op amp input is driven by the detector output. The output of the op amp directly drives the attenuator. This creates a continuous time feedback loop, similar to SLIC, except the Power Amplifier is now in the loop. The optimum configuration could be determined by simulation and breadboarding.

The phase shifters are controlled directly by the Xilinx FPGA. Eight signals drive each phase shifter. This requires 32 wires to each quad phase/attenuator MMIC, but this should not be a problem for the High Density Interconnect (HDI) module. To minimize level shifting, the FPGA will be run at -5V, and the serial data lines to the Array Controller will be likewise. The A/Ds and D/As will similarly be biased to interface directly to the FPGA. Any required level shifting of A/D and D/A analog signals will be accomplished with the op amps.

The selected approach represents the lowest possible risk. Use of off-the-shelf A/Ds, D/As, and op amps insures known voltage levels and performance, while CMOS technology provides the lowest possible power. Xilinx Field Programmable Gate Arrays (FPGAs) are downloaded at power-up, thereby enabling modifications of the control algorithm right up to flight time. This provides a high degree of flexibility for calibration, debug, and flight worthiness. The Signal Processing Center of Technology at Sanders has been using these devices in reconfigurable computing architectures for a number of years, and therefore can assert with confidence that the desired functions will easily fit in the chosen array, and there will be no problem executing the control algorithms in the time allotted.

COMPONENT DESIGN

Quad Phase Shifter and Attenuator - The phase shifter and variable attenuator designs are directly based on the designs verified on the SLIC program. Both designs exhibit excellent performance with the phaser having an average insertion loss of 6 dB and the attenuator have a loss on < 2 dB, a 18 dB gain control range and an incidental phase change of < 5 degrees. Yield is very high on the RF functionality of the SLIC MMICs (>80%), hence we could fabricate a new MMIC with 4 pairs of phase shifters and attenuators on a single chip to facilitate the integration in the tile module and reduce the number of array components for higher module yield.

The phase shifter MMIC uses an artificial delay line approach, shown imbedded in the SLIC MMIC in Figure 79, that results in the lowest insertion loss and most compact size of any MMIC phaser concept studied. The principle of operation consists of a quadrature (Lange) coupler with identical switched artificial delay lines connected to two quadrature ports. Periodically spaced shunt FET switches on the delay line are used to control the path length on the line by selectively shorting it at different points to effect a reflection with controlled phase characteristics. The output from the phaser occurs at the normally isolated port of the Lange coupler as desired. One advantage of this design is that the impedance match is inherently good as dictated by the return loss of the Lange coupler and not the termination impedance.

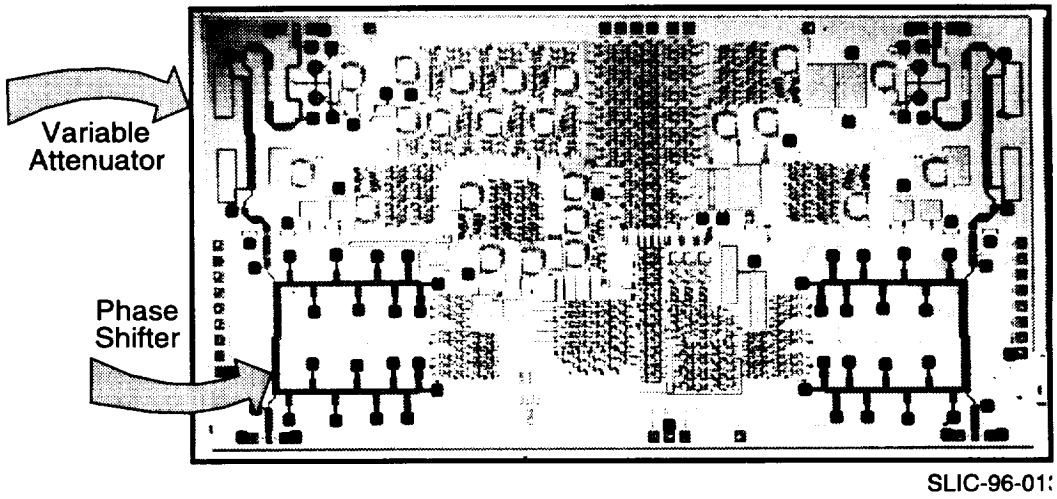


Figure 79. SLIC MMIC with Imbedded Phase Shifter and Attenuator Circuits

On the SLIC program the phaser was fabricated at the TriQuint foundry because of their low loss FET process and ability to provide integral control logic. Figure 80 shows the resulting amplitude and phase characteristics which were achieved on the first pass of the design. Average insertion loss is 6 dB with a state to state variation of +/- 0.5 dB. The phase characteristics were as expected with the linear phase shift versus frequency characteristic of a delay line phase shifter. Return loss is better than 12 dB over all states.

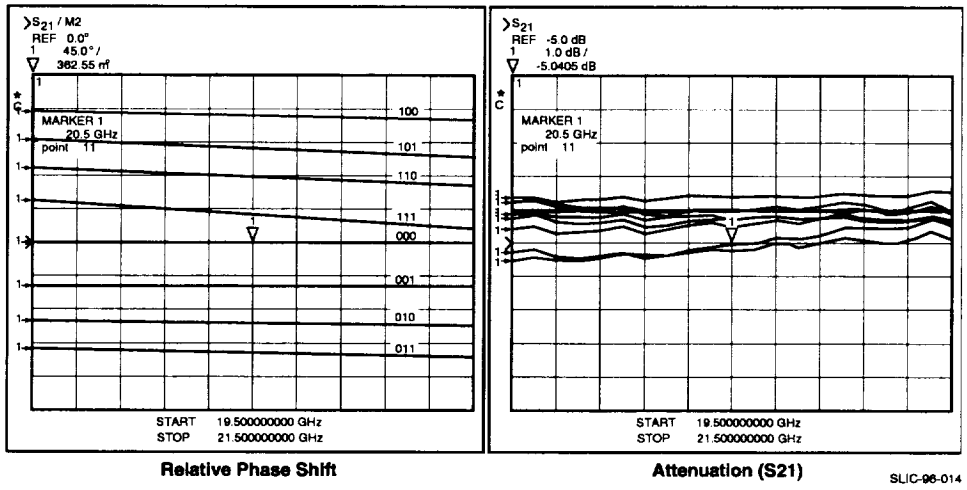


Figure 80. Phase Shifter Performance

The attenuator shown imbedded in the SLIC MMIC photo of Figure 79 is also based on the same reflection type design as the phase shifter but in this case a variable resistive load is used. Great care was taken in the design of the load to insure that as the gain is varied, there is little incidental phase change since this would adversely effect the performance or control of the phased array. An analog termination was selected for interfacing to our AGC loop. Figure 81 shows the resulting attenuation and phase characteristics. Insertion loss is less than 2 dB with a control range of 18 dB while the insertion phase varied less than 5 degrees for all ranges except the full off state which is not considered an operational state.

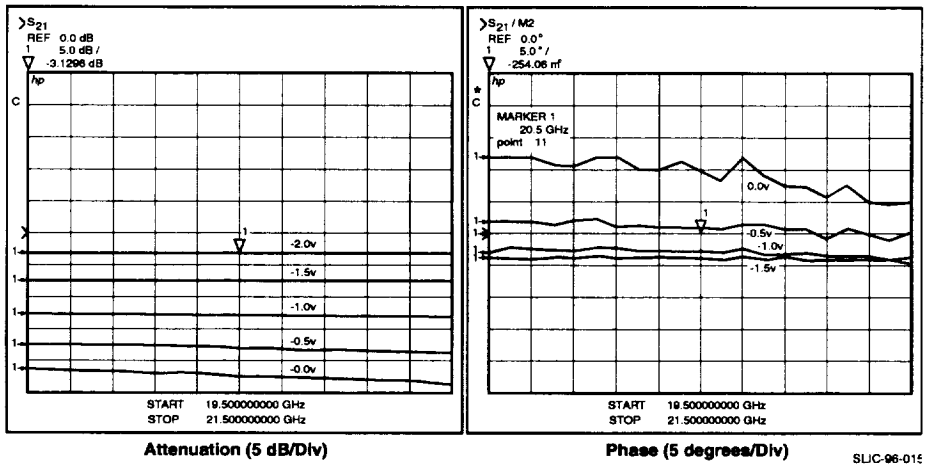


Figure 81. Variable Attenuator Performance

Both the phaser and attenuator demonstrated excellent RF yield on the SLIC program, however overall yield was reduced by the GaAs AGC control loop. Because of the high RF yield, 4 pairs of phase shifter and attenuator MMICs will be integrated onto a single chip that measures 250 x 250 mils resulting in over 160 sites on a TriQuint 4 inch wafer. This increase in integration will result in fewer array parts which will lead to higher Multipac integration yield. Minimal control logic will be included on the MMIC to reduce DC power in the array and an available shifter register chip in Silicon will be located adjacent to the MMIC.

Peak Detector - Since the peak detector design used on the SLIC MMIC functioned satisfactorily in the module, the same design will be used in a multiplex arrangement for amplitude control of all the array elements. The peak detector functions properly with the AGC when it sees RF signal levels between -5 dBm and +3 dBm. These levels were experimentally determined during bench testing of the SLIC modules. On wafer testing of the detector demonstrated an insertion loss of 0.6 dB.

Power MMIC - In order to minimize risk for the Multipac MHDI module design, an off-the-shelf power amplifier will be used at each element input. The chosen amplifier is a broadband PHEMT MMIC (Hewlett Packard HMMC-5040). The amplifier is capable of 100 milliwatts of RF output with a power added efficiency of 13% (Figure 82). To further reduce risk at the module design level, this amplifier will be tested on a single channel brassboard (wirebonded) with other Multipac circuits with emphasis placed on stability and circuit interaction. In addition, this amplifier chip will be placed on a carrier and evaluated before and after the MHDI post process is applied.

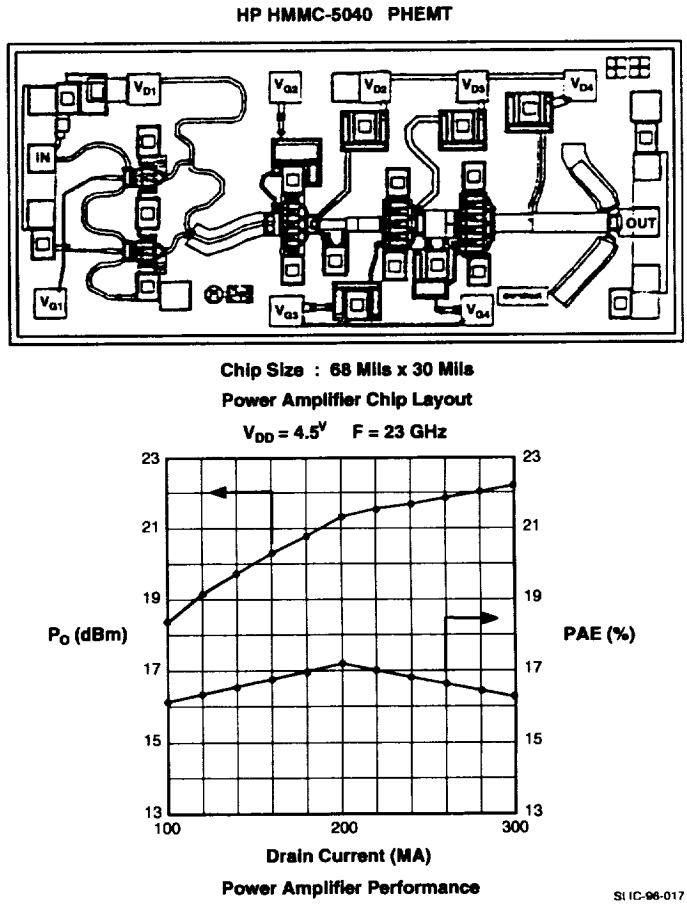


Figure 82. Broadband PHEMT MMIC

A second power amplifier MMIC is required for each Multipac module. Its function is to raise the power level in each channel, so it is placed between the first and second power divider. Two of these GaAs MMICs are required per module. The saturated output power is 25 dBm with 10 dB of gain and a power added efficiency of 18%. These amplifiers will also be evaluated before and after the MHDI post process is applied.

IRAD Power Amplifier Design - We plan to develop on IRAD a PHEMT MMIC Power Amplifier that specifically addresses the longer term requirements of space-based phased arrays as follows:

By exploiting Sanders state-of-the-art 0.15μm PHEMT technology (see Figure 83), we will provide a MMIC with the highest possible efficiency - 42% power added efficiency is projected. This high efficiency is critical in a space based array both to minimize prime power consumption and to reduce the thermal load presented by the array.

Organization	Device	Freq (GHz)	Power-Added Efficiency (%)	Power Gain (dB)	Reference
Lockheed Martin/ Lincoln Laboratory	0.15 μm PHEMT with LTG Buffer	20	63	10.5	1995 MTT Symp.
Lockheed Martin	0.25 μm PHEMT	20	55	9.5	1994 GaAs IC Symp.
Raytheon	0.25 μm PHEMT	18	50	7.0	1993 GAAs IC Symp.
Texas Instruments	0.25 μm PHEMT	20	45	7.4	1994 MTT Symp.
Lockheed Martin	HBT	18	46	6.1	Internal Data
Rockwell	HBT	18	49	6.2	1990 GaAs IC Symp.

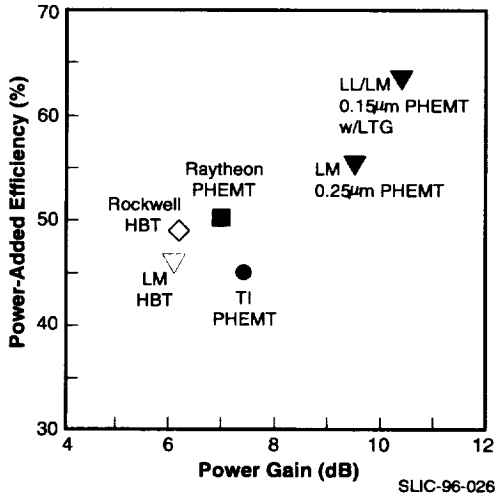


Figure 83. 0.15μm PHEMT Amplifier Technology

The high power gain of our 0.15μm PHEMTs at 20 GHz 9-11 dB compared with 6-7 dB for devices representative of the rest of the industry, allows the required amplification to be achieved with fewer stages, reducing MMIC chip size. The two-stage power MMIC we will develop will provide the same gain as a 3-stage design based on a lower performance technology.

The enhanced power MMIC will be fabricated using a proprietary gate recess process that produces exceptional uniformity in MMIC characteristics across large wafers through the use of etch stop layers and selective etchants. Excellent consistency in MMIC amplitude and phase from part-to-part is essential to effective construction and operation of the phased array.

Our IRAD activity, scheduled to begin in January 1997, will focus on the development of a 2-stage PHEMT MMIC producing 150 mW output power with 18 dB gain and 42% power added efficiency. The MMIC will be designed to operate over the 18.0-21.2-GHz band, allowing its use in NASA, military and emerging commercial satellite transmitter applications.

A detailed gain/power budget for the MMIC is presented in Figure 84. Note that a 400 μm gate width PHEMT is used in the first stage. A drain supply voltage of 4.5V is required, and the expected DC power consumption is 0.35W per chip. The predicted size of this MMIC PA is approximately 1.0 x 2.0 mm^2.

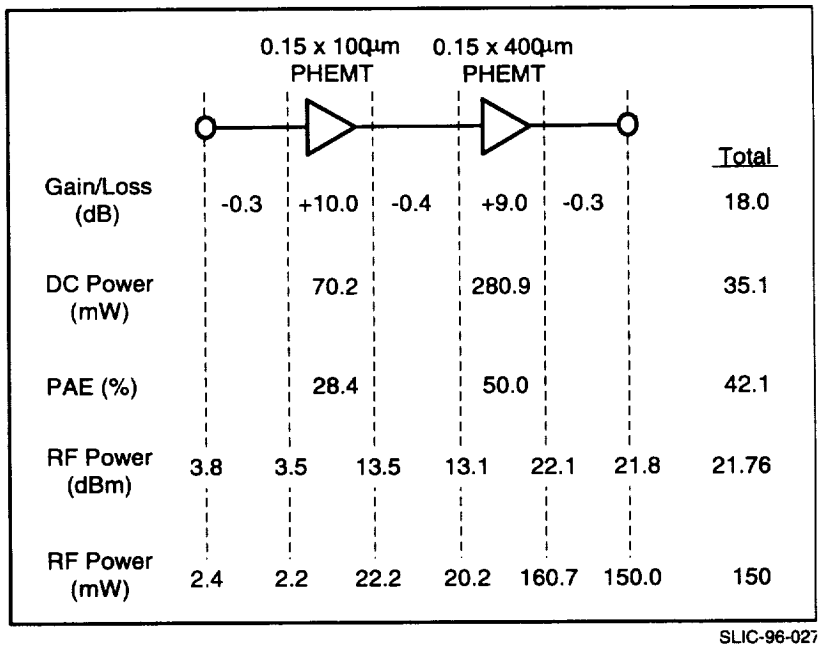


Figure 84. Gain/Power Budget

This MMIC development will require the usual two design, fab and test cycles to arrive at the final production-ready version, and we expect this to be completed by March 1998. We believe this MMIC design will meet the full objectives of NASA's 20-GHz phased array needs, including high efficiency, excellent long-term reliability, excellent repeatability and small size. The development of this enhanced MMIC leverages off a significant amount of past experience and ongoing work aimed at 20-GHz power generation for satellite applications, including the followings efforts:

Two contracts are underway to develop 20-GHz high power MMICs based on 0.15µm PHEMT technology for future SSPA applications. One program is developing a 6W narrow band MMIC design (20.2-21.2 GHz) for use in a 5W transmitter for ground-based interceptors (GBI), while the second is developing 3 and 6W broadband designs (18.0-21.2 GHz) for ultimate integration into a 60W SSPA for TWTA replacement.

Beginning in 1990, we optimized the design of our 0.25µm PHEMT for 20-GHz operation. We developed a large PHEMT device with 2W output power, 45% PAE and 9.6 dB gain, and these discrete PHEMTs have been successfully integrated into a 20W SSPA. In addition, extensive reliability testing of these devices has confirmed that reliability is consistent with long-life satellite applications.

Power Dividers - During the SLIC program the Wilkinson power divider MMICs required for a multi-channel module were designed and tested in the MHDI environment. Figure 85 is a single channel measurement of three cascaded power dividers that are interconnected by MHDI stripline/microstrip lines. The interconnect lines contained a number of transitions that were required in the module layout such as passages over RF shields on lower layers, passages under the seal ring and microstrip to coplanar lines for RF testing. At frequencies of 20 GHz, the design of these features is not trivial and the test results indicate that the power divider and transitions perform satisfactorily and are not a design risk.

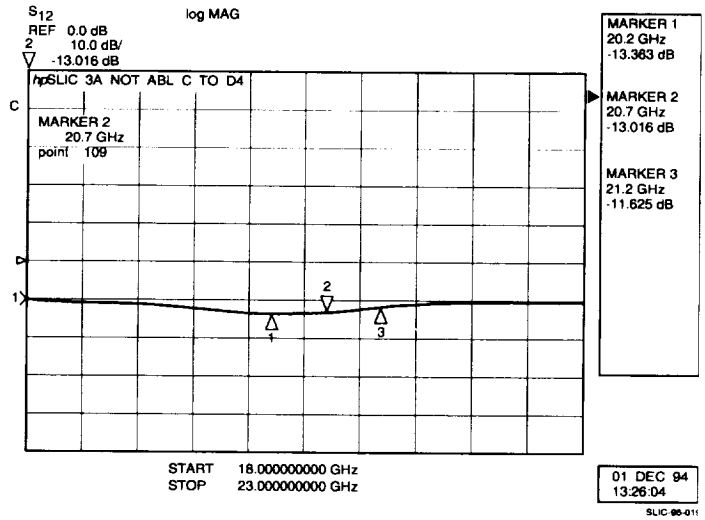


Figure 85. Single Channel Measurement

3.3 APPLICATIONS

K Band Phased arrays for high bandwidth data downlink applications are a critical step that will lead to a large family of K Band phased array products for NASA, Commercial communication and earth sensing, and DoD applications. Bandwidths of 622 MBPS from LEO satellites can be achieved with an array of only 300 - 400 elements which can readily be mounted on a wide range of platforms.

Low earth orbiting satellite platforms, in particular those used in earth science experiments, have an increasing need for the ability to provide high bandwidth data distribution of the collected data directly to users on earth. Phased arrays again are required to provide the required antenna performance in a low profile non-intrusive design that provides inertia-less beam steering as the satellite passes a users station. Data rates of 155 Mbps and 622 Mbps are standard rates identified for compatibility with emerging communications standards, while data rates of over 2 Gbps have been identified for application on enhancements to the International Space Station. These designs, based on SLIC technology are recognized by us as an important element that will be included in all future Earth Observing Satellites (EOS) as well as commercial earth sensing satellites.

Collectively, K Band phased arrays represent several $100M of potential development and production for the antennas alone over the next 5 years but importantly will leverage a systems business for satellites and communications services that is conservatively estimated at >$3B by early the year 2002. This NASA SLIC based phased array will be the pace setter in the development, demonstrating ultra-thin tile designs, built-in calibration for high performance and low cost manufacturing approaches.

The Sanders role in these programs is to be the primary supplier of MMICs, Modules, and integrated array subsystems in support of Lockheed Martin internal programs, directly to Government agencies, and importantly, as a major supplier of these components to strategic external industry partners. The newly formed Sanders Microwave Electronics Division in Nashua NH has been established as a corporate center of excellence of the development and production of the type advanced microwave and millimeter components that will be required for the development of these K Band Phased Arrays. Advanced technology coupled with a highly automated manufacturing and a disciplined quality assurance process will lead to the successful development and insertion of this product into future systems.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	July 1997	Final Contractor Report

4. TITLE AND SUBTITLE

System-Level Integrated Circuit (SLIC) Technology Development for Phased Array Antenna Applications

5. FUNDING NUMBERS

WU–632–50–5B
C–NAS3–26394

6. AUTHOR(S)

John A. Windyka and Ed G. Zablocki

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Sanders
A Lockheed Martin Company
Microwave Electronics Division
Nashua, New Hampshire

8. PERFORMING ORGANIZATION REPORT NUMBER

E–10817

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

National Aeronautics and Space Administration
Lewis Research Center
Cleveland, Ohio 44135–3191

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

NASA CR–204132

11. SUPPLEMENTARY NOTES

Project Manager, Kurt A. Shalkhauser, Communications Technology Division, NASA Lewis Research Center, organization code 5640, (216) 433–3452.

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Unclassified - Unlimited
Subject Category 32

This publication is available from the NASA Center for AeroSpace Information, (301) 621–0390.

12b. DISTRIBUTION CODE

13. ABSTRACT (***Maximum 200 words***)

This report documents the efforts and progress in developing a "system-level" integrated circuit, or SLIC, for application in advanced phased array antenna systems. The SLIC combines radio-frequency (RF) microelectronics, digital and analog support circuitry, and photonic interfaces into a single micro-hybrid assembly. Together, these technologies provide not only the amplitude and phase control necessary for electronic beam steering in the phased array, but also add thermally-compensated automatic gain control, health and status feedback, bias regulation, and reduced interconnect complexity. All circuitry is integrated into a compact, multilayer structure configured for use as a two-by-four element phased array module, operating at 20 Gigahertz, using a Microwave High-Density Interconnect (MHDI) process. The resultant hardware is constructed without conventional wirebonds, maintains tight inter-element spacing, and leads toward low-cost mass production. The measured performances and development issues associated with both the two-by-four element module and the constituent elements are presented. Additionally, a section of the report describes alternative architectures and applications supported by the SLIC electronics. Test results show excellent yield and performance of RF circuitry and full automatic gain control for multiple, independent channels. Digital control function, while suffering from lower manufacturing yield, also proved successful.

14. SUBJECT TERMS

Active phased array; Antenna; Monolithic microwave integrated circuit; MMIC; Phase shifter; Photonics; K-band; Microwave high-density interconnect; MHDI

15. NUMBER OF PAGES

90

16. PRICE CODE

A05

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	