



**PMMW Camera TRP Phase 1
Final Report
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Final Report

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1.0 Introduction

Passive millimeter wave (PMMW) sensors have the ability to see through fog, clouds, dust and sandstorms and thus have the potential to support all-weather operations, both military and commercial. Many of the applications, such as military transport or commercial aircraft landing, are technologically stressing in that they require imaging of a scene with a large field of view in real time and with high spatial resolution. The development of a low cost PMMW focal plane array camera is essential to obtain real-time video images to fulfill the above needs.

The overall objective of this multi-year project (Phase 1) was to develop and demonstrate the capabilities of a W-band PMMW camera with a microwave/millimeter wave monolithic integrated circuit (MMIC) focal plane array (FPA) that can be manufactured at low cost for both military and commercial applications. This overall objective was met in July 1997 when the first video images from the camera were generated of an outdoor scene. In addition, our consortium partner McDonnell Douglas was to develop a real-time passive millimeter wave flight simulator to permit pilot evaluation of a PMMW-equipped aircraft in a landing scenario. A working version of this simulator was completed. This work was carried out under the DARPA-funded PMMW Camera Technology Reinvestment Project (TRP), also known as the PMMW Camera DARPA Joint Dual-Use Project.

In this final report for the Phase 1 activities, a year by year description of what the specific objectives were, the approaches taken, and the progress made is presented, followed by a description of the validation and imaging test results obtained in 1997.

2.0 Annual Progress

The Phase 1 effort spanned the years 1994 through 1997. The following sections contain chronological descriptions of the specific objectives, approaches, and progress made during each year. The yearly progress was written at the conclusion of each year (1994-1997). As such, they portray the progress and plans at yearly intervals during the course of the program, and reflect the evolution of the concept towards the final configuration of the camera. In retrospect, only a few major changes took place and the bulk of the camera concept continued to the end.

2.1 Activities in 1994

2.1.1 Specific Objectives

The specific objectives for the 1994 effort were to carry out mission definition for a demonstration camera, system requirement studies, trades of subsystem design concepts, and a camera concept definition to help focus further engineering efforts.

2.1.2 Approach

The overall approach to developing and demonstrating a PMMW camera was based on designing and fabricating a Demonstration Camera that could be tested by various users interested in this technology. Special emphasis on the aircraft landing mission was given to the design and system engineering efforts, since this is one of the more stressing applications.

TRW's approach uses TRW-patented single chip W-band GaAs MMIC direct amplification and detection receiver technology. This technology enables the low cost manufacturing of the high performance large FPA needed at the heart of video frame-rate cameras. In addition to leveraging this technology, full advantage was made of a millimeter wave automated assembly line (AAL) developed at TRW to economically

assemble components for the 1040 pixel FPA to be used in the demonstration camera. Combining these advances with the years of experience TRW has gained in developing PMMW imaging sensors and systems will lead to a PMMW camera product.

The 1994 objectives were met through the completion of three tasks: Task 1) generate camera requirements generic to the different missions of interest, Task 2) provide the camera system engineering which defined the camera concept, and Task 3) address in more detail the design of the camera optics and imaging functions.

2.1.3 Progress

The 1994 PMMW camera project completed the three planned tasks. These are described below:

Task 1. PMMW Camera Requirements.

Among the many applications of the PMMW camera, the low visibility aircraft landing mission has great need for this sensor, and a high benefit-to-cost ratio is seen. We selected it as the focus of the development effort of the demonstration camera.

The aircraft landing mission requires the camera to provide the pilot with a weather penetrating image of the forward scene from final approach through touchdown, roll-out, and taxi. The camera image is to be updated at a rate sufficient to permit manual aircraft landing. The camera is to fit inside the airplane nose cone and the camera design should provide turn-key operation to alleviate pilot workload. The camera system requirements are derived in large part from the PMMW computer simulation using a standard aircraft landing scene constructed from a generic commercial aircraft landing profile. The derived camera system requirements include frequency and bandwidth of operation, camera field-of-view, camera angular resolution, contrast, sensitivity, image refresh rate, image latency, operation interfaces and environment. In addition to the functional system requirements there are requirements

related to overall product attractiveness, which include size, weight, power consumption, retrofit compatibility and cost.

In order to produce adequate system requirements, we have generated a camera operation time line for the landing mission. Starting from an altitude of 15,000 feet, the camera is turned on, well before final aircraft approach to allow for sufficient warm-up time to stabilize the electronics. At power-on the camera goes through the appropriate self-check, calibration and adjustment, both automatic and manual, and these functions are completed in such a way that the camera is ready to operate and generate images of the forward scene at a range of 5 km from the landing runway, or about one minute away from the touchdown point. From this point onward the camera will present to the pilot a continuing image until the final decision height of 200 feet. Fifteen seconds later, the aircraft will touch down, and at a convenient time later, after the taxi and parking operations are completed, the camera is turned off. Based on this mission scenario, the camera system requirements are flowed down to the various subsystems defined by their specific functions.

Task 2. PMMW Demonstration Camera System Engineering.

Based on the demonstration camera system and subsystem requirements, the system engineering effort produced a baseline camera concept that meets these requirements and that is traceable to a production camera item. Details of the camera concept are documented in the "PMMW Camera Definition" document. The summary functional schematic of the camera concept is shown in Figure 1 (this diagram corresponds to the final schematic, little changed from the first diagram in 1994). The key camera components are the 1040-pixel W-band GaAs MMIC direct amplification and detection focal plane array (FPA), an internal on-chip and external pulsed FPA calibration, an image dithering reflector, a compact dual-lens optics, and a super-resolution real-time image processing capability.

The camera subsystems consist of the optics, the image oversampling mechanism, the calibration, the FPA, the backend electronics, and the image processor. The optics subsystem defines the spatial resolution of the camera. The external calibration subsystem provides the gain calibration for the FPA receivers while the internal switched load supplies the offset calibration for the FPA receivers in order to flat-field the array signals. The dithering mirror allows the receivers to optically oversample the imaged scene by a factor of four, thus reducing the number of physical receivers by the same factor. This technique alleviates the problem of high density packaging of the FPA receivers. The FPA subsystem amplifies the broadband emissions of the scene to a level that is sufficient for detection with a diode detector. The backend electronics conditions and digitizes the receiver signals, multiplexes them, and sends them to the image processor. Within the image processor the signals are recalibrated, super-resolved and image enhanced to provide a real-time image display.

The system engineering effort also carried out subsystem concept trades which resulted in a baseline camera concept. Highlights of these trades at the subsystem level are described in the following.

Optics: The optics subsystem traded various approaches to image focusing: transmissive dielectric and constrained lens(es), reflective systems, and use of artificial dielectric optics. The concept of choice is a compact two-element tele-photo lens with good wide angle and aberration performance.

Calibration: The calibration subsystem traded the following concepts: internal on-chip monolithic integrated switchable load, external coherent source, noise source and mechanical load. The concept of choice is a combination of external pulse noise source and the internal on-chip switchable load which will provide a reliable FPA receiver gain and offset calibration.

Image Dithering: The image dithering subsystem traded a rotating offset mirror, a rotating wedge, a step/stare mirror, and electro-optical concepts like silicon light-

activated reflectors and switched polarizing grids. The concept of choice is the step and stare mirror which can provide image dithering without smearing.

FPA: The FPA subsystem trades consisted of the FPA antenna, the receiver design, and the FPA packaging. The antenna design traded between horns, dielectric end-fire, monolithic array and planar taper slotted antennas. The concept of choice is the planar taper slotted antenna on a thin dielectric substrate for low cost and ease of manufacturing. The receiver design trade involves heterodyne and direct detection with the latter being a much simpler design because no local oscillator is required, easing the packaging problem. The direct detection receiver design trade involved single and multiple chip designs. W-band technology advances have produced MMIC chip performance and yield sufficiently high to support a single chip design that will lead to a low cost receiver manufacturing process. In addition, a switched internal load is implemented on the chip monolithically to provide receiver offset calibration and to allow a synchronous detection process for higher receiver sensitivity.

Image Processing: The image processing subsystem trades focused on the implementation of proven algorithms on developed and well supported hardware. The approach for this subsystem takes advantage of the relatively low processing demands and can be readily custom-made for the camera product at low cost. A linear superresolution algorithm will be implemented on paralleled digital signal processors that are proven, well supported, and have low manufacturing cost.

Task 3. Conceptual Design of Camera Optics and Imaging Functions.

The quality of the image obtained by the camera is a function of the camera focusing element, the aperture, the type of mechanisms used to fold the optical path, and the type of image processing. The baseline optical subsystem concept is compact and provides a 15 degree by 10 degree FOV capability with an effective spatial resolution of approximately 6 milliradians. The optical elements consist of an 18 inch

diameter dual-lens front end, a high pass filter, a dithering reflector, and the FPA antenna. Real time superresolution algorithms and processors are also implemented to enhance the performance of the optical elements to achieve the 6 milliradians effective resolution.

The front end optics are made from a two-element telephoto lens. The first lens is zoned for weight reduction, and both lenses have a surface matching layer to reduce reflection loss. The lens material has low insertion loss at W-band frequencies and can be manufactured at low cost. The telephoto design excels in wide angle performance, low insertion loss, technology maturity, and low cost manufacturing.

The high pass filter design concept is a perforated conductive plate with thickness optimized for required RF interference protection. This concept excels in ease of attenuation and cut-off frequency optimization, and low cost of manufacturing.

The image dithering reflector concept is a servo-feedback voice coil step-stare reflector design providing pixel sampling of the image at four adjacent positions leading to a high quality over-sampled image with a reduction in the needed number of receivers in the FPA. This concept is also attractive because of what it provides in image quality, technology maturity, and low cost of manufacturing.

The image resolution enhancement processing concept uses a linear superresolution algorithm which will be implemented with off-the-shelf parallel digital signal processing (DSP) processors. This approach also provides quality off-the-shelf hardware support and low cost of manufacturing.

2.2 Activities in 1995

2.2.1 Specific Objectives

The specific objectives for the 1995 effort were the preliminary and final design of the camera, and the start of fabrication of the PMMW camera subsystems.

2.2.2 Approach

The 1995 objectives were met through the completion of four tasks: Task 1) generate preliminary designs for all of the camera subsystems, Task 2) validate the design concepts using proof-of-concept models and measurements, Task 3) update design concepts to define final subsystem designs, and Task 4) fabricate subsystems and tested them.

2.2.3 Progress

The 1995 PMMW camera project completed the four planned tasks. These are described below:

Task 1. Preliminary PMMW Camera Subsystem Design.

Optics: Preliminary Baseline and Backup lens designs were devised to meet the camera optics requirements. The Baseline design was based on a doublet composed of an 18" diameter convergent primary (with zoning on the periphery to reduce weight) and 12" diameter divergent secondary lens. The Backup design was a simple, low-risk, 18" diameter plano-convex lens. Rexolite was chosen as the lens material. Anti-reflection coating concepts were devised (grooved surface treatment and screen or mesh material covers).

A high pass filter (HPF) was designed, based on a conductive plate perforated with holes. The HPF location was set behind the secondary lens of the Baseline lens design.

Image Oversampling Mechanism: A preliminary design for the image oversampling mechanism was devised based on the use of speaker voice-coil drivers pushing and pulling on a reflector mounted on a stictionless pivot. An open-looped drive circuit was initially designed, controlled by an embedded microprocessor, to

generate the required step-stare motion for the reflector.

Calibration: A preliminary calibration subsystem design was developed using a combination of an external broadband (to reduce standing wave effects) noise source to illuminate the focal plane receivers, and a reference load that is electronically switched into the receiver input (in place of the signal input from the scene) using a "switching" low noise amplifier (LNA) located on the MMIC receiver chip itself. These two input noise levels provided the difference signals necessary to independently calibrate each receiver. The means to illuminate the receivers with the external noise source was also designed, based on a waveguide fed horn located on-axis immediately behind the primary lens. The radiation from this horn would be directed through the secondary lens, the HPF, and reflect off of the oversampling reflector onto the receiver antennas.

FPA: The FPA, as defined in the preliminary camera concept, is composed of three primary subsystem levels. Each level required its own preliminary design effort. These levels are: 1) the MMIC receiver chip, 2) the 1x4 Module, and 3) the 1x40 Card.

In the first iteration, two MMIC receiver chip designs were developed, one characterized by a balanced switched input (identical gains on signal input and reference load input legs) and a backup design having an unbalanced input (higher gain on the signal input leg). The unbalanced design was expected to have lower noise levels but with larger DC offsets. Both designs incorporated rapid (25 kHz) switching of the switched LNA to reduce $1/f$ noise and to potentially serve as a calibration reference level.

The 1x4 Module design includes preliminary designs for the input antenna and the Thick Film Board circuit. The input antenna baseline design was based on a Linear Taper Slot Antenna (LTSA) formed on a substrate. The Thick Film Board circuit design includes video signal amplifiers and current regulator to power the MMIC chips. All aspects of the 1x4 Module design provided for automatic assembly on the TRW

Automated Assembly Line.

The 1x40 Card was designed to support ten 1x4 Modules as well as signal processing elements of the Backend Electronics. The principal design effort involved packaging all elements within a 0.2" card thickness. In addition, adequate thermal conduction to a cooling plate was provided by a wedge-shaped interface.

Backend Electronics: The Backend Electronics preliminary design includes circuits to control and process signals from the MMIC receivers, and to provide power. The signal processing includes circuitry to synchronously detect the 25 kHz switched signals from the MMIC receivers, to filter the resultant signals, to digitize and multiplex them, and to transfer the image data to the image processor. It was decided to incorporate all signal processing circuitry into a single Hybrid component, five of them to be placed on each 1x40 Card along with a printed wire board to provide interconnection paths. An embedded processor would be used to provide smart control interface between the camera and the image processor/camera operator.

Image Processor: On the hardware side, C-40 processor boards were selected for their speed and parallel processing capability (a quad C-40 board was selected to do the super-resolution image processing in which each quadrant of the image would be ported to separate C-40 processors). These are commercial products that are well supported and have relatively low manufacturing cost. Separate boards for the system controller (Sparc system) and graphic display interface (RS-170), with associated display, memory, and other hardware were selected.

Image processing algorithms were designed to perform calibration, image upsampling, super-resolution, contrast enhancement. Preliminary versions of these algorithms were coded.

Task 2. Subsystem Design Validation using Proof-of-Concept Models.

Optics: Proof-of-concept (POC) models were built of both the Baseline and Backup lens designs. The Backup lens, with a 89 GHz source, was set up as a parallel wavefront source which allowed the verification of the design focal length. Using this source, the Baseline lens design was tested and its performance verified through measurements of the field of view, the point spread function across the image plane, and total transmission.

A grooved anti-reflection POC test article was constructed and tested. Its performance was inadequate. Various mesh materials were then tested and the performance verified through testing.

A HPF POC was built and its transmission characteristic verified at 89 GHz. The frequency cut-off of 77 GHz will be verified during final camera testing.

Image Oversampling Mechanism: A POC mechanism was built, as well as breadboard circuits containing the voice-coil drivers and microprocessor. Position transducers were installed to monitor the movement of the reflector. These were used to verify the required movement and timing of the reflector.

Calibration: A POC calibrator using a broadband noise source was set up, along with a prototype MMIC receiver containing the switched LNA reference load. Validation tests were performed to determine the accuracy and stability of the calibration scheme. These tests revealed that the internal reference load was inadequate for the purpose of generating a stable, accurate calibration point. Thermal drifts, and the difficulty of controlling them or monitoring them, made the use of the internal reference load unrealistic. Other tests using the broadband noise source indicated the soundness of requiring a broad bandwidth. Standing wave effects were significantly reduced. Finally, the design of the noise source horn and its location were verified through measurements of the resultant power distribution on the focal plane array.

FPA: A POC LTSA was built and tested independently. Once the LTSA design was updated, it was included in POC 1x4 Modules which were stacked to form a 4x4 POC subarray. These early 1x4 Modules used MMIC receiver chips with earlier designs, and POC Thick Film Boards. All assembly was performed manually for the POC. Testing of the 1x4 Modules and the 4x4 Subarray validated the independent operation of the individual receivers. However, covers for the 1x4 Module induced oscillations in the MMIC chip that limited the allowable gain. Once the MMIC chip design was finalized, newly designed 1x4 Modules were fabricated using the AAL and mounted on a POC 1x40 Card. This card also contained the POC Backend Electronics Hybrid circuits. Testing of the card is to be performed in early January, 1996.

Backend Electronics: The preliminary signal processing circuits were breadboarded and tested using early MMIC receivers. The synchronous detection circuitry functioned as planned, as well as the signal digitizer. However, tests revealed deficiencies in the filter design concept. After changes, a Hybrid circuit design was sent for prototype fabrication by a vendor, and the first 10 Hybrids were installed, along with a printed wire board, onto the POC 1x40 Card for further testing.

Image Processor: Hardware was obtained with the intent of using these as POC models that could be evaluated and eventually become the final development camera hardware. A number of boards were obtained from manufacturers as evaluation boards, allowing a downselect later. Only one board proved inadequate (the data interface board providing communication directly with the camera controller electronics).

Image processing algorithms were developed and tested on desktop SUN workstations. These algorithms were also tested with simulated inputs. Algorithms for performing calibration functions were written for the baseline calibration concept.

Task 3. Design Concept Updates and Final Design.

Optics: The only design concept update was in the choice of anti-reflection screen material to use, and an optimal mesh thickness and density was determined through testing. The final optics design is composed of the Baseline lens design, with mesh material stretched across the convex surfaces and held against concave surfaces using low loss foam inserts, with the HPF filter used behind the secondary lens.

Image Oversampling Mechanism: Position drifts and the need to null the mirror position for different camera orientations, necessitated the incorporation of the position transducers in a closed-loop control circuit configuration. This design update was validated using the POC mechanism. The final design also included the interface with the camera enclosure.

Calibration: The design of the calibration subsystem required an update to replace the use of the on-chip reference load. The updated design provides a two-level output from the external noise source, using an arrangement of attenuators, a MMIC amplifier (to boost the power output level), a PIN diode waveguide switch, and control circuitry.

FPA: The unbalanced MMIC chip design was selected after testing showed its noise performance superior to the baseline design. This finalized the circuitry required to control and power the chip. The Thick Film Board design required an update to reduce switching noise coupling to the signal line. The LTSA design was iterated and updated to maximize coupling to the optics design.

Backend Electronics: The signal processing design required one principal update, and that was the replacement of a filter circuit with an integrate/dump circuit. This gave better performance by maximizing the usage of the 10 milliseconds that each receiver has to stare at the scene (set by the image oversampling mirror step-stare motion and ultimately by the required 17 Hz image refresh rate).

Image Processor: On the hardware side, since the data interface board that was being evaluated proved inadequate, it was decided to design and fabricate a board to do the same functions using in-house expertise. In addition, this board could be built to correct various cable interfacing problems. On the software side, the calibration algorithm required an update due to the change in the baseline calibration process (using a 2-level calibration noise source).

System Engineering/Productization: Included under final design activities were various system engineering/productization efforts. These addressed the following areas related to the camera: 1) Aircraft Interface issues such as accommodation of the camera within the aircraft radome or other locations, and electrical power, 2) Camera Productization, including the generation of both a Manufacturing Plan and product Cost Model, and 3) a Cost/Benefit Analysis, with a Cost of Ownership study provided by McDonnell Douglas and a Benefit Analysis provided by an outside consultant (George Kanellis).

Task 4. Camera Subsystem Fabrication.

Optics: The Baseline lens and HPF POCs were built and shown to meet requirements. These would be used in the final camera. Mesh material was procured and is ready for final installation.

Image Oversampling Mechanism: All breadboard circuits were replaced with final circuit boards, and the final reflector mechanical mounting was fabricated, using selected parts from the POC mechanism. Fabrication of a mounting interface with the camera enclosure was also started in 1995.

Calibration: The Calibrator POC was modified to incorporate the two-level noise source scheme. The POC noise source horn and mounting was found to be adequate and will be used in the final camera. The final mounting for the calibrator components is under fabrication.

FPA: Manufacturing of the unbalanced receiver MMIC wafers began in mid April 1995. MMIC Foundry process problems caused delays which pushed projected completion of all chips into late April 1996. Production of the 1x4 Modules began in November 1995, including all the LTSA's, Thick Film Boards, but excluding the MMIC chips. The MMIC chips will be installed in 1996. Manufacturing of the 1x40 production cards would be delayed into 1996. Manufacturing of the FPA Housing, including the cooling plate requiring EDM to form the wedge-shaped interface for the 1x40 cards, was begun late in 1995 and would continue into 1996.

Backend Electronics: Fabrication of the Hybrid components was poised to begin pending test results from the prototype units mounted on the first 1x40 Card. Printed wire boards were all fabricated successfully. Layout for remaining circuit boards (for camera controller, power distribution, and data transfer functions) had begun.

Image Processor: All processor hardware except the data interface board was purchased and was being used. Layout of the data interface board was being performed at the end of 1995.

2.3 Activities in 1996

2.3.1 Specific Objectives

The specific objectives for the 1996 effort were the completion of the PMMW camera subsystems, including the first half of the FPA, and to begin integration.

2.3.2 Approach

The 1996 objectives were met through the following two tasks: Task 1) final fabrication and assembly of all subsystems, including the first half of the FPA (520 out of 1040 pixels); and Task 2) begin integration of subsystems into the Demonstration Camera.

2.3.3 Progress

The 1996 PMMW camera project completed the two planned tasks. These are described below:

Task 1. Final Subsystem Fabrication and Assembly.

FPA: The FPA is composed of three primary components or subassemblies. These are: 1) the MMIC receiver chips, 2) the 1x4 Module, and 3) the 1x40 Card.

Although production delays pushed the completion of all MMIC chips into 1997, sufficient high-performance MMIC receiver chips were produced in 1996 by the TRW MMIC foundry to populate 540 channels, or half of the full FPA. These MMIC chips, along with other components, were installed in the 1x4 Modules using the TRW Automated Assembly Line. A module without its cover is shown in Figure 2. The four MMIC receiver chips are visible as dark rectangles near the center of the figure. A total of 52 "production" 1x4 Modules were assembled and were ready for card insertion.

Early in 1996, a proof-of-concept 1x40 Card, containing the POC Hybrid circuit (described in the Electronics section) and 10 "pre-production" 1x4 Modules, was assembled and tested, and is shown in Figure 3. Revisions were made in both the card and Hybrid designs, and production of both were started in 1996. A total of 13 functional and two non-functional edge cards (with antennas only) were completed. In addition, fabrication and assembly of the FPA housing, including the cooling plate with welded fittings for cooling lines, was completed. The 1x40 Cards were mounted within the FPA housing, as shown in Figure 4. An additional 15 cards were assembled but were lacking 1x4 Modules at the end of 1996.

The POC 1x40 Card was placed at the focus of the camera optics, and hooked up to a data acquisition system to acquire a still image of a scene in a TRW parking lot using the card array in a pushbroom manner. The scene is shown in Figure 5a (visible

light photograph), and the resultant MMW image is shown in Figure 5b.

Camera Mechanical Parts: Fabrication of all elements of the camera housing was completed in early 1996. In addition, a mounting adapter plate for the camera (to interface with an azimuth-elevation platform), a support fixture for safer handling of the FPA, and a mounting bracket for co-boresighted video and still cameras were fabricated and assembled.

Optics: The anti-reflection coating developed in 1995 was installed on 3 of the 4 lens surfaces of the two lenses. Since the coating is a mesh material, it was easily stretched across the convex surfaces of the two lenses and secured. The mesh was pressed against the concave side of the secondary lens using a form-fitted piece of Styrofoam, which was itself held in place by the High Pass Filter (HPF) plate.

Image Oversampling Mechanism: Fabrication of a mounting interface for the oversampling mirror mechanism with the camera enclosure, and the final assembly of the subsystem were completed in 1996. The completed subsystem is shown in Figure 6. The mirror motion was verified by using a laser beam reflecting off of a small optical mirror mounted on the mmw reflector, and watching the reflected beam on a distant surface (a square pattern of the right dimensions was observed). EPROM burn-in of the final control program would await final testing with the camera control electronics.

Calibration: The final mounting plate for the calibrator components was fabricated, and all components were mounted onto it. In addition, the calibration control circuit and interconnecting wiring were fabricated. The calibration control circuit was tested prior to connection to the calibrator millimeter wave components, and adjustments were made to reduce transients and noise. The completed subsystem is shown in Figure 7.

Electronics: It was decided to incorporate all signal processing circuitry into a single Hybrid component, five of them to be placed on each 1x40 Card along with a printed wire board to provide interconnection paths, all of which are visible in Figure 3.

Each Hybrid processes the output signals from two 1x4 Modules. Fabrication of 150 Hybrid components was completed, and along with the printed wire boards, were mounted onto 28 1x40 Cards.

Fabrication and assembly of the remaining circuit boards for the camera control electronics (the camera control processor, power distribution, and data transfer functions) were also completed. These boards were installed within a machined aluminum enclosure, along with the DC-to-DC converters for powering all camera subsystems from a single 28VDC supply. The functionality of this package was also verified, and the completed package is shown in Figure 8.

Image Processor: Image processing algorithms to perform calibration, image upsampling, super-resolution, and contrast enhancement were written and tested on the dedicated image processing hardware. This hardware is shown in Figure 9. These algorithms were also tested with simulated inputs.

The data interface board that provides the data communication connection between the camera control electronics and the image processor, at the image processor end, was fabricated, assembled, and successfully tested.

Power Interlock: A circuit box was designed, fabricated, assembled, and tested to perform the job of controlling the primary 28V DC power supply and to shut it off in the event of coolant failure or water leaks. This circuit box was also designed to house other circuit elements, such as the "Pilot Interface" that serves as a simple, 4-button interface with the camera control software, and video time-mark generators for synchronizing the video tapes recording the image output of both the Demonstration Camera and a co-boresighted color video camera.

Instrument Rack and Cables: A dedicated instrument rack was prepared for field use and outfitted with the 28VDC power supply, two VCR's for image data recording, the image processor, two display monitors, the power interlock circuit box, and the cooler control panel. In addition, cable definition diagrams and tables were completed,

and cable fabrication was started.

Task 2. Start of Demonstration Camera Integration.

Integration of the subsystems into the final camera began with mechanical integration activities. The various camera housing parts were initially fit checked. Then a sheet-like microwave absorber was epoxied onto the interior surfaces of the various camera housings, and on other internal structures, to reduce stray reflections.

The two lenses were mounted onto the optics housing, and the spacing between them was set to the design value, which had been verified during earlier lens testing. The calibration horn was also installed within the optics housing. The calibration subsystem was then fit checked with the optics housing and waveguide feedthrough.

Electronics integration was begun at the end of 1996 between the camera control electronics and the image processor. Hardware/software de-bugging took place to attain successful transfer of commands and simulated data. Integration and testing with the other subsystems was slated to begin in 1997.

2.4 Activities in 1997

2.4.1 Specific Objectives

The specific objectives for 1997 were the completion of all subsystems, the completion of the camera integration, and the completion of the validation tests of the Demonstration Camera (with the full FPA). In addition, another objective for 1997 was the completion of the McDonnell Douglas flight simulator.

2.4.2 Approach

The 1997 objectives were met through the following five tasks: Task 1) complete the fabrication of the final set of MMIC receiver chips for the FPA, Task 2) complete the

second half of the FPA, Task 3) complete the integration of the full FPA into the camera, with testing performed throughout the process, Task 4) perform laboratory and ground-based validation tests of the camera performance, and Task 5) complete the software to demonstrate a working version of the flight simulator on a McDonnell Douglas system.

2.4.3 Progress

The 1997 PMMW camera project completed all five planned tasks.

Task 1. Final MMIC Chip Fabrication.

In 1997 the final set of MMIC receiver chips for the FPA was fabricated, and this was soon followed by the completion of the second half of the FPA. Altogether, 20 lots of 6 wafers each were started, of which 12 were production lots (the rest were either engineering development lots or were process development lots). The last lot that gave the program enough chips of adequate performance to finish the fabrication of the full FPA was completed in early March 1997.

Task 2. Final Subsystem Fabrication and Assembly.

Once enough chips were in hand, the assembly of the remaining 1x4 Modules (for the second half of the array, about 130 modules) was begun. This process continued through early May 1997, the bulk of the time spent reworking poor performing modules by replacing MMIC chips. As the modules were completed, work was started assembling the remaining 1x40 Cards (for the second half of the array, 13 cards). The last card was completed May 9, 1997, signaling the completion of the fabrication and assembly of the last subsystem.

Task 3. Demonstration Camera Integration.

The delivery of the second half of the FPA cards allowed the assembly of the full FPA. This was accomplished and the FPA integrated into the Demonstration Camera on May 16, 1997. The completed camera is shown in Figure 10. Once the full array was installed, a series of tests were begun to determine the operating characteristics of the camera with the full FPA. In particular, the thermal behavior of the camera was significantly affected, necessitating modifications to accommodate the increased thermal load.

The increase in the number of receivers pointed out deficiencies in both the electronics and the data handling by the image processor. In addition, the control and data handling of the calibration signals was proving difficult. These problems were resolved over the course of 2-3 months.

Task 4. Validation Tests.

A series of laboratory and ground-based validation tests of the camera performance followed the completion of the camera integration, and the results will be reported in the Section 3.

Task 5. Flight Simulator.

McDonnell Douglas completed a working version of a real-time passive millimeter wave flight simulator in their fix based flight simulator with the MD-11 cockpit. This is based on a Silicon-Graphics Onyx system using a Coryphius database to generate the out-the-window scene.

3.0 Validation Test Results

The following sections present results of measurements performed to validate the Demonstration Camera performance. Thermal tests began February 1997 (with

half of the array) and continued through June 1997 with the full array. Calibration of the camera began March 1997 (with half of the array) and continued with the full array through June 1997.

The thermal tests were performed primarily to reveal potential limitations in the FPA cooling, the electronics cooling, and the operating range of the water chiller system. These tests showed that the FPA could be maintained at a constant temperature through the use of the water coolant flowing through the backplate of the array. This coolant was maintained typically at 25C at the chiller reservoir, although it was varied over a limited range (± 3 C) to monitor the array sensitivity to temperature. The electronics was found to be inadequately cooled, so temporary measures were taken to allow continued camera operation while a more permanent fix (addition of cooling lines in the electronics housing) was implemented.

Calibration involved setting hardware gain and offset values in the Hybrid circuitry for each pixel. This was determined by using hot (room temperature) and cold (77K) loads to illuminate the array and monitoring the receiver outputs as a function of the Hybrid gain and offset settings. The settings needed to avoid saturation of the ADC were then determined. Additional software calibration gain and offset values were determined to fine tune the array response, to assure a flat field performance. Once the camera was calibrated, performance measurements could begin. Only the most significant measurements are presented.

3.1 FPA Performance

The full FPA was assembled and powered up successfully. After performing the necessary calibration steps to obtain normalized readings on an absolute Kelvin scale, measurements were made of the minimum resolvable temperature of the camera. When viewing a hot load (room temperature absorber), the array gave an average value of 293.8K with a standard deviation of 5.2K, while with a cold load (absorber

immersed in liquid nitrogen) the array gave an average of 75.4K with a standard deviation of 4.3K. These measurements are indications of the uniformity of the array, and were made through the full set of optics.

3.2 Optics Performance

The performance of the optics was determined using the calibrated FPA. This was done using a compact range noise source to illuminate the entrance lens and measuring the resultant point spread function on the array. The performance was found to be within expectations.

3.3 Calibrator Performance

Calibration was performed using an external hot and cold load to determine the individual receiver responses and the necessary calibration numbers to obtain a flat field on the display. The final testing of the calibrator was deferred to Phase 2.

3.4 OSM Performance

The Oversampling Mirror (OSM) was tested using a HeNe laser reflecting off of a visible light mirror attached to the surface of the OSM. The amplitude of the OSM swing in both axes was adjusted to obtain the correct angular movement, as shown by the size of the resultant "box" drawn by the reflected HeNe beam on a target plane.

3.5 Camera Bandwidth

The overall camera bandwidth was measured using a variable frequency source (80 to 100GHz) and monitoring the array response. Although the shape of the response is peaked at around 93 GHz, the FWHM is roughly 10 GHz, centered at about 90 GHz.

3.6 Imaging

The Demo Camera was taken to the roof of building R1 and set up on an elevation-over-azimuth platform to allow easy aiming of the camera. The scene from the roof is of the parking lot north of the building, with moving automobiles and people. The focus of the camera was set for both infinity and for approximately 100 feet to observe the effect (the depth of field of the camera is quite large, with the exact location of the array relative to the lens not turning out to be very critical. The resulting video showed good imaging. The imaging demonstrated the improvement in identifying objects in the scene whenever movement was present. The accompanying video demonstration tape shows samples of these early images. Note that these are “raw” images, with no additional post image processing having been performed on them.

4.0 Conclusion

The Phase 1 PMMW Demo Camera was completed and successfully operated, generating the first true video image in the W-band range of frequencies.

5.0 Acknowledgments

The contributions of the many team members in developing this camera should be acknowledged here. Over the course of the program, since its inception in the Fall of 1994, many people have come and gone, leaving their imprint on the camera. The following list covers the key TRW players and managers:

Managers

Larry Yujiri, Sam Dow, Alan Eskovitz, Paul Lee, Merit Shoucri

System Engineering

Steve Fornaca, Bruce Hauss, Karen Luebke, Steve Chaiken, Barry Stark,
Marlowe White

Optics

Tom Samec, Marty Flannery, Jon Yun

Signal Processing

Hiroshi Agravante, Karen Jordan, Thomas Wagner, Chris Shelton, Richard Yee

Calibration

Karen Yokoyama, Giovanni DeAmici

Oversampling Mechanism

Bill Quon

Electronics

Ron Johnson, Arpad Pallai, Miguel Armenta, Mike Griffin, Dave Hoffmaster, Ashok Jain, George Nakamura, Kash Vatandar

Mechanical/Thermal

Jamie Dunham, Arlen Rowe, Jim Rupert, Dave Vanevenhoven, Karl Morris

FPA

Roger Kuroda, Dan Moriarty, Paul Yocom, Teresa Cazares, Nely Bautista, Mike Biedenbender, Steeve Tran, Joe Montich, Ali Marashi, Charles Bailey, Phil Trujillo, Lee Howell, Omar Miramontes, Tom Chung, Yong Guo, Sam Esparza, Steve S. Chan, Eric Lin, Dennis Lo

Key Management Support

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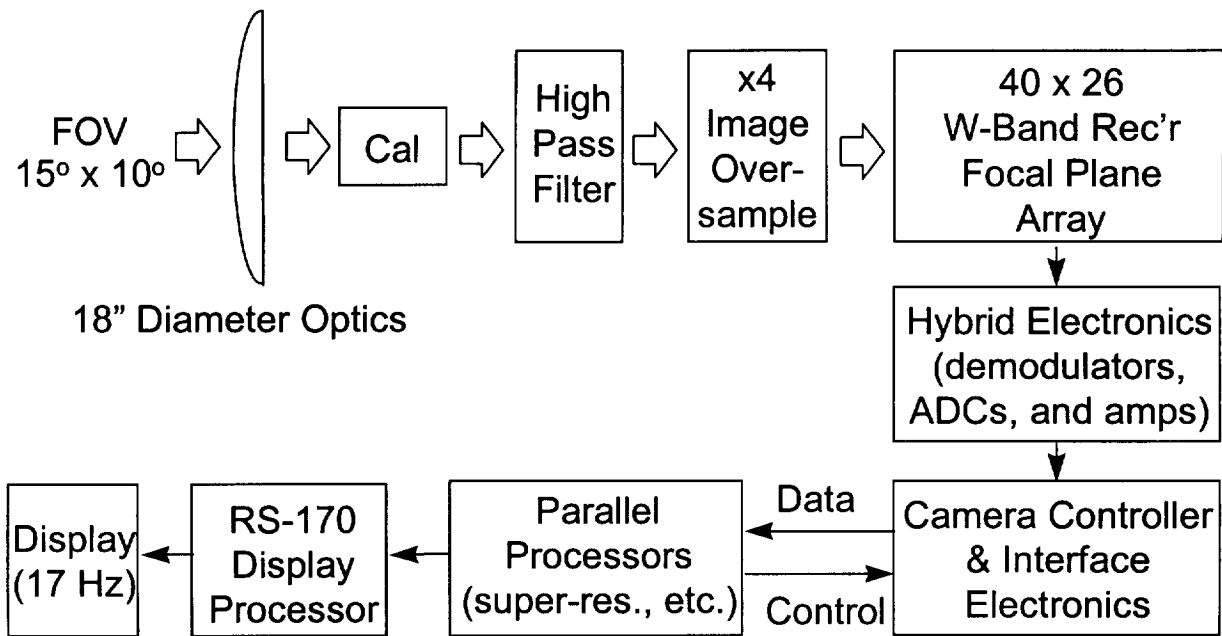


Figure 1 Demonstration Camera Block Diagram

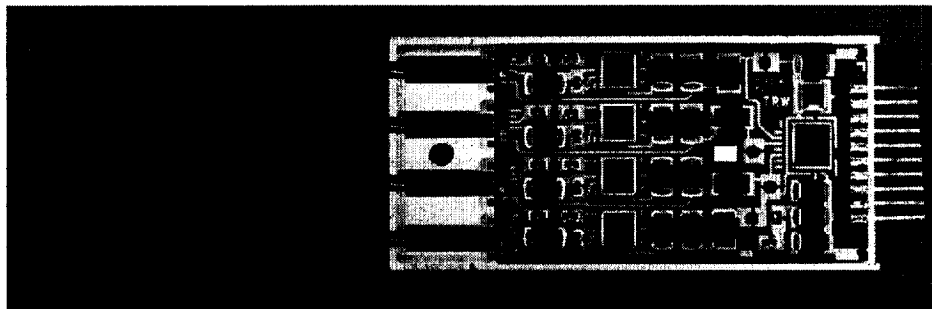


Figure 2 1x4 Module (without cover)

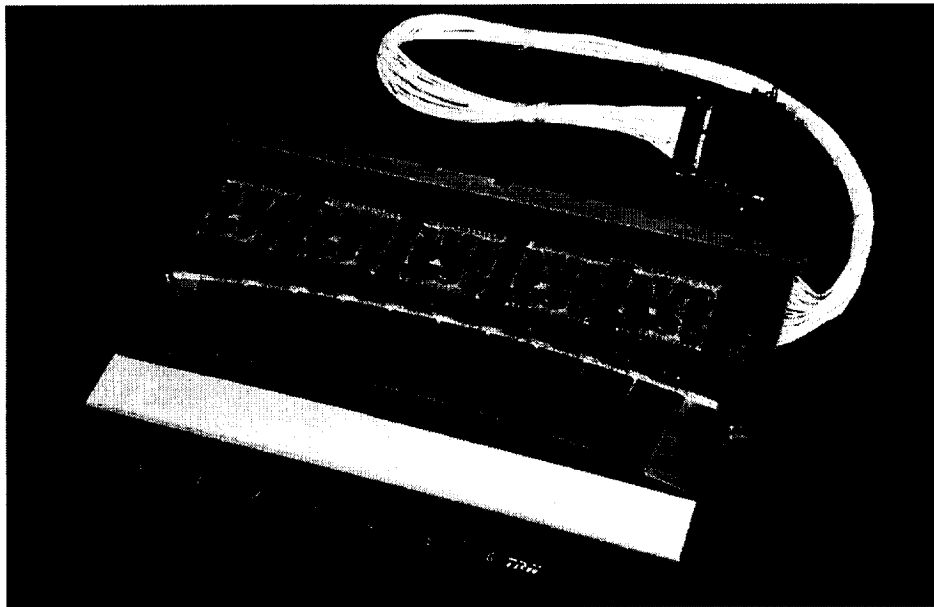


Figure 3 1x40 Card (proof of concept version)

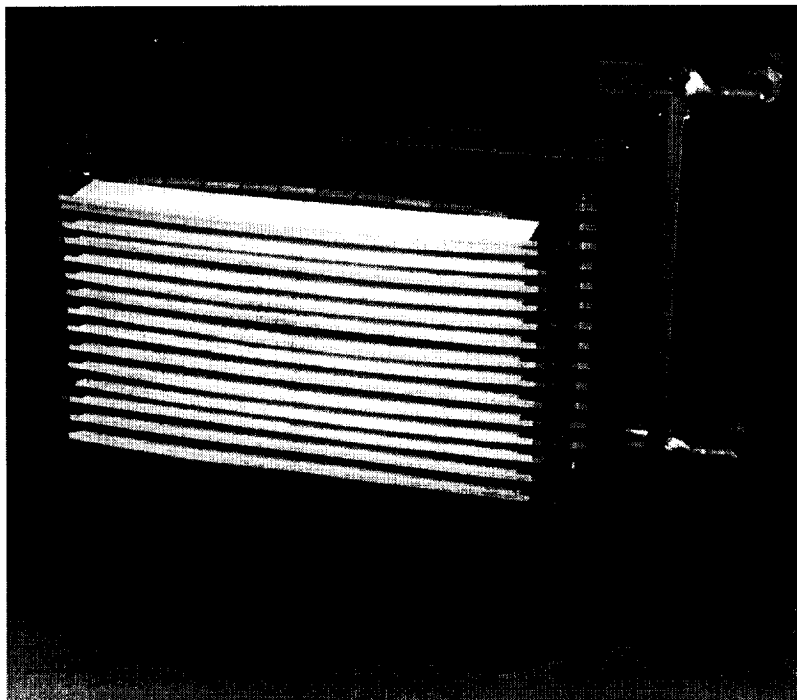
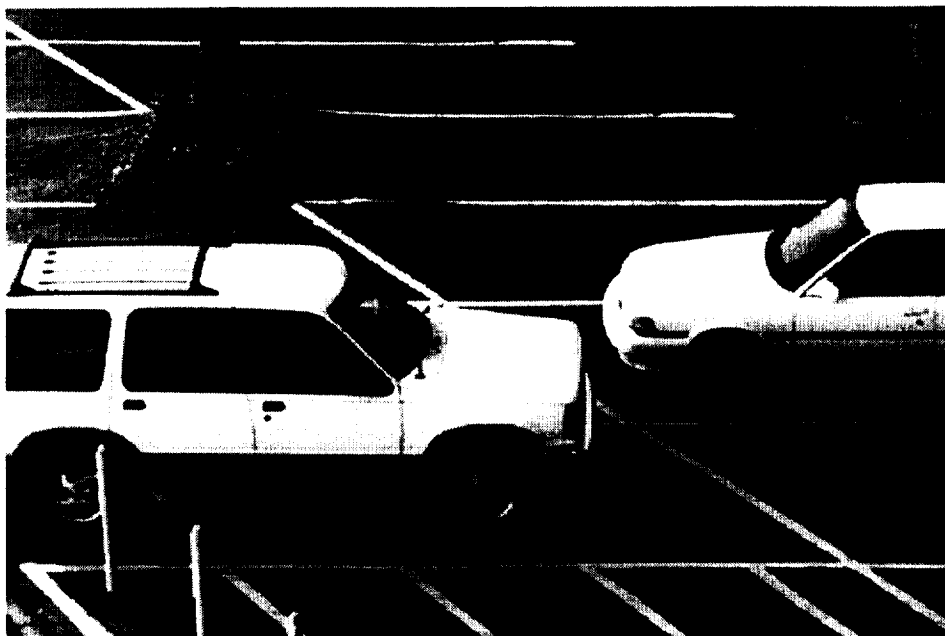


Figure 4 FPA Housing (with first 13 1x40 Cards + 2 edge cards)



(a) Visual Light Photograph



(b) PMMW Image

Figure 5 R1 North Parking Lot Image

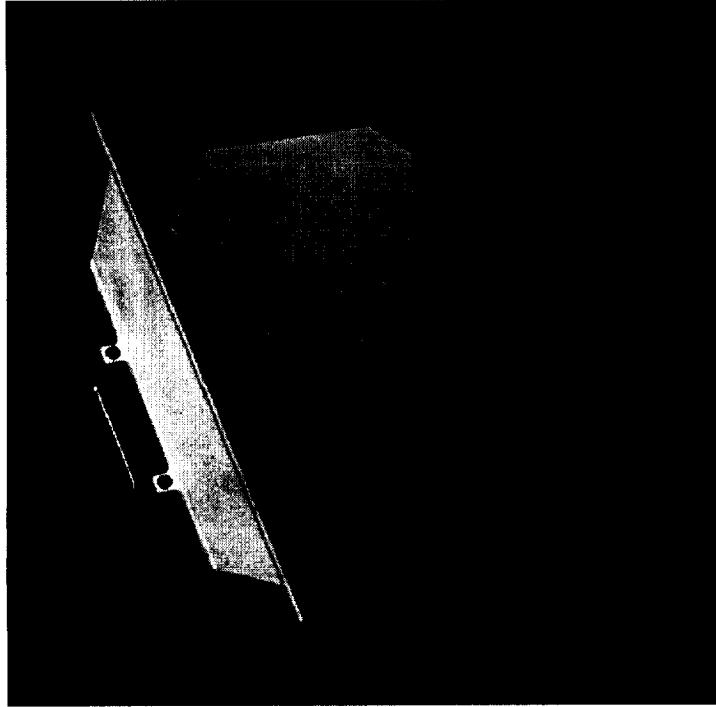


Figure 6 Oversampling Mechanism

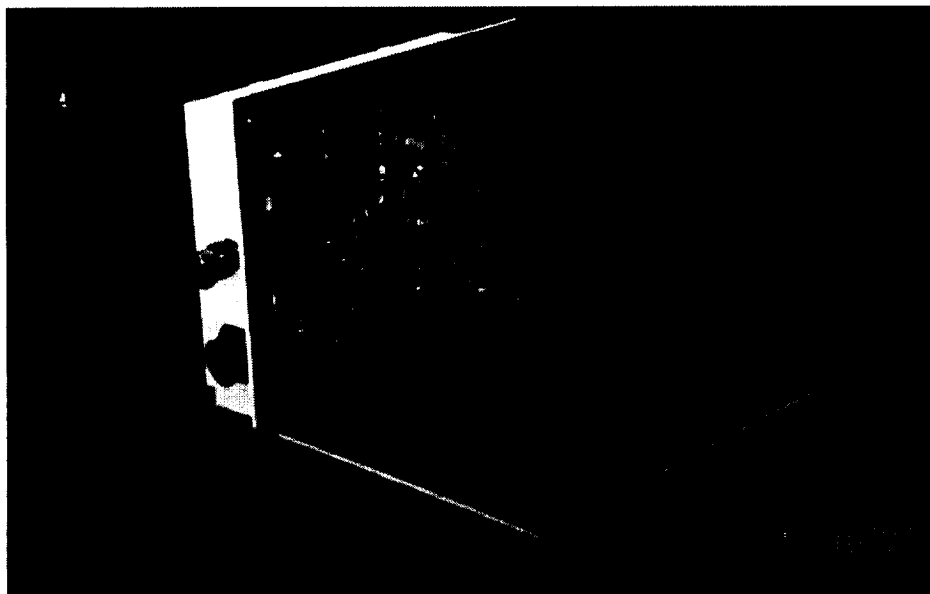


Figure 7 Calibrator

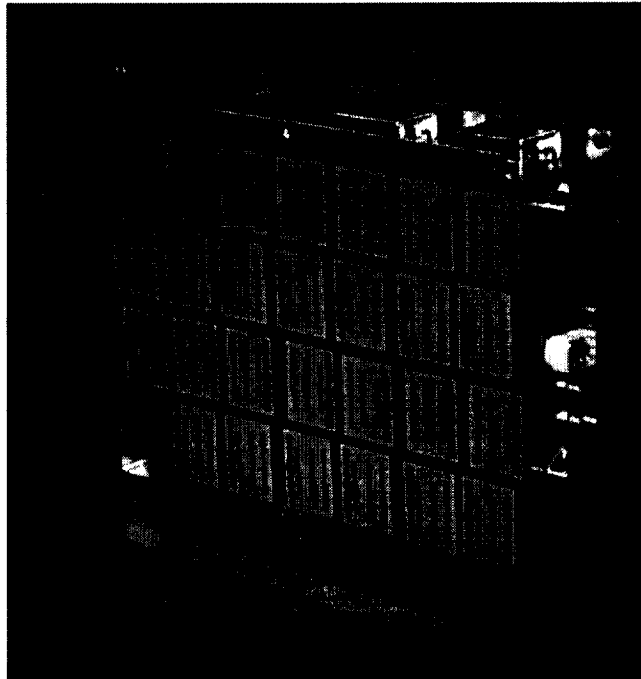


Figure 8 Electronics

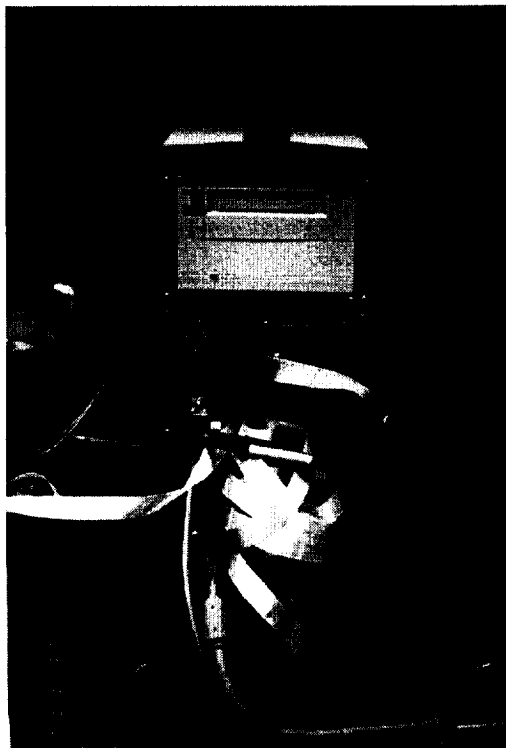


Figure 9 Image Processor

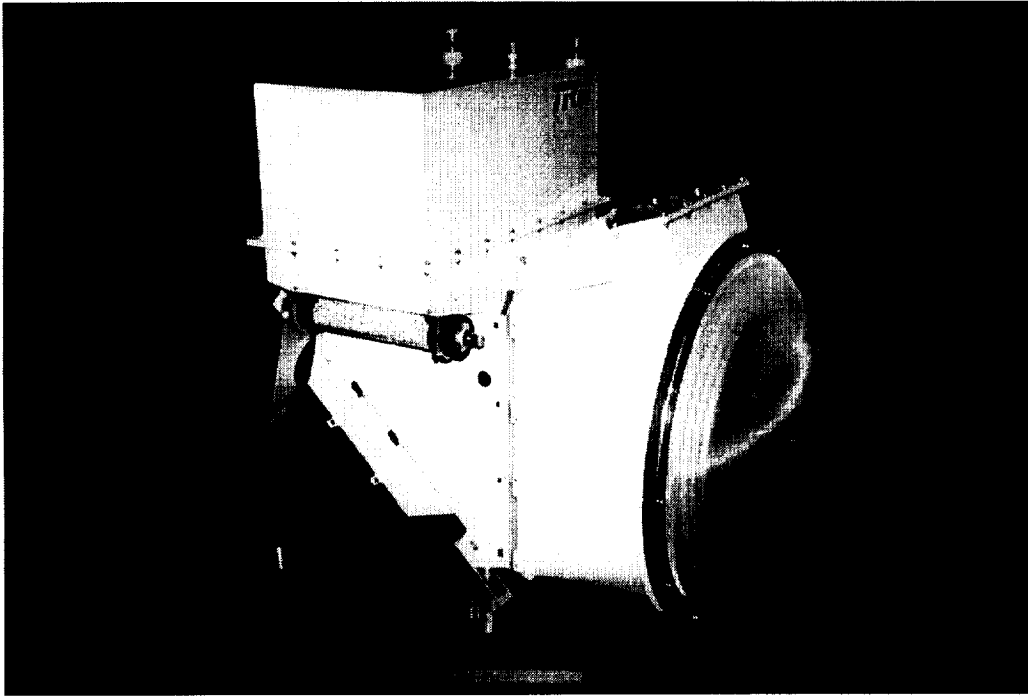


Figure 10 Assembled Camera