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Production Support Flight Control Computers: Research Capability for F/A-18 Aircraft at Dryden Flight Research Center

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ABSTRACT

NASA Dryden Flight Research Center (DFRC) is working with the United States Navy to complete ground testing and initiate flight testing of a modified set of F/A-18 flight control computers. The Production Support Flight Control Computers (PSFCC) can give any fleet F/A-18 airplane an in-flight, pilot-selectable research control law capability. NASA DFRC can efficiently flight test the PSFCC for the following four reasons: (1) Six F/A-18 chase aircraft are available which could be used with the PSFCC. (2) An F/A-18 processor-in-the-loop simulation exists for validation testing. (3) The expertise has been developed in programming the research processor in the PSFCC. (4) A well-defined process has been established for clearing flight control research projects for flight. This report presents a functional description of the PSFCC. Descriptions of the NASA DFRC facilities, PSFCC verification and validation process, and planned PSFCC projects are also provided.

NOMENCLATURE

A/D	analog-to-digital converter
AFSRB	Airworthiness and Flight Safety Review Board
BIT	built in test
BOM	Basic Operations Manual (NASA DFRC)
CCDL	cross-channel data link
CPU	central processing unit
D/A	digital-to-analog converter
DAF	dial-a-function
DDI	digital display indicator
DFRC	Dryden Flight Research Center, Edwards, California
DPRAM	dual port random access memory
EEPROM	electrically erasable programmable read only memory
FAST	Flight Control Automatic System Testing
FRR	Flight Readiness Review
HARV	High Angle of Attack Research Vehicle
INS	inertial navigation system
ISM	input signal management
LMCS	Lockheed Martin Control Systems, Binghamton, New York
MC	mission computer
MDA	McDonnell Douglas Aerospace, Seattle, Washington
NWS	nose wheel steering
PBIT	periodic built in test
PSFCC	Production Support Flight Control Computers
QIDS	quick instrumentation and data system
RAM	random access memory
RFCS	Research Flight Control System
SID	simulation interface device
SRA	Systems Research Aircraft
UFC	up-front controller
USN	United States Navy

UVPROM ultraviolet programmable read only
        memory
VMEM   variable memory

INTRODUCTION

Development of computer-controlled aircraft greatly expanded the possibilities for control system design engineers. Modern aircraft have handling qualities which can be dictated by the flight control system rather than the physical characteristics of the aircraft. Because computers translate pilot inputs and sensed feedbacks into surface positions, the choice of control law algorithms is unlimited.

However, control law software development on aircraft has historically been an extremely expensive and time-consuming proposition. The main reason for this situation is the large amounts of staff hours devoted to designing, implementing, and testing flight-critical software. Required testing facilities, such as processor-in-the-loop simulations, are also expensive and need long lead times to develop. Large amounts of hours are required because of the flight-critical nature of control law functions. Extremely thorough testing is required because a control law software malfunction can lead to the loss of an aircraft and of a pilot's life.

The large expense and extended development time have made in-flight experiments of different control laws not viable for the majority of aircraft programs. In general, once a control law architecture is agreed upon, it is not altered until an operational deficiency warrants change. Several organizations which do control law research have recognized this problem and developed aircraft that have research flight control computer systems which are designed for relatively fast control law modifications, while retaining safety of flight through the primary control system [1, 2]. Such systems can also be used to change airframe characteristics in-flight to simulate the characteristics of other airframes. These aircraft, such as the variable stability Learjet (Calspan Corporation, Buffalo, New York) and the F-16 Variable Stability In-Flight Simulator Test Aircraft (VISTA) (General Dynamics, Fort Worth, Texas), have been used primarily for handling qualities studies. However, some advanced control law architecture work has been done [2].

In the past, NASA Dryden Flight Research Center (DFRC), Edwards, California, engineers have also had aircraft designed for fast control law modification, such as the F/A-18 High Angle of Attack Research Vehicle (HARV) (McDonnell Douglas Aerospace (MDA), St. Louis, Missouri) [3]. The HARV, a modified F/A-18 airplane with thrust-vectoring paddles, was designed for flight test at high angles of attack. The HARV flight control computers were modified to include a pilot-selectable research control law processor. This system allowed the HARV to operate with conventional F/A-18 control laws for all phases of flight and with research control laws available at specified parts of the envelope. System reversion was accomplished either manually or automatically with system failure or envelope violation. The HARV design provided a flexible platform for control law algorithm research. The ability to restore aircraft control to a baseline flight control system with good handling qualities throughout a broad flight envelope addressed many of the safety-of-flight issues associated with experimental control law architectures. Because of HARV specific modifications, these flight control computers were confined to the HARV and would not work on other F/A-18 aircraft.

The United States Navy (USN) desires to develop a flight control system research capability for the F/A-18 aircraft. The USN flight control engineers want to duplicate F/A-18 flight control failures in-flight for accident investigations and in-flight demonstrations. This desire led the USN to finance the early design of the Production Support Flight Control Computers (PSFCC). These PSFCC are derived from the HARV flight control computer design, with one important difference: PSFCC are intended to function on any fleet F/A-18 airplane without modifications.

An interest in continuing control law research on an F/A-18 aircraft led NASA DFRC to convert one of the HARV flight control computer shipsets to a PSFCC. Two duplicate PSFCC shipsets now exist: one owned by the USN and one owned by NASA DFRC. To accomplish the mutual goal with the USN of using the PSFCC for in-flight research, the NASA DFRC is in the process of completing the processor-in-the-loop testing of the PSFCC in preparation for flight test. These organizations will work cooperatively to test the PSFCC at the NASA DFRC and at the Naval Air Warfare Center, Patuxent

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River, Maryland. Upon satisfactory completion of hardware-in-the-loop testing, the PSFCC will be flown on a NASA aircraft, initially by NASA and USN pilots.

There are five major benefits to testing the PSFCC at NASA DFRC. Dryden Flight Research Center has

- Six F/A-18 aircraft available for this type of research

- Chase aircraft equipped with instrumentation and telemetering systems for data transmission

- Processor-in-the-loop simulation for verification and validation testing

- Personnel familiar with programming of the research processor

- Safety-of-flight processes established which address the concerns for an aircraft research control system in a timely manner

Because of the resources already in place, NASA DFRC control law research using the PSFCC should be relatively easy and inexpensive.

This paper provides a functional description of the PSFCC. A discussion of the resources available for this type of research and of the excellent verification and validation options that researchers find at NASA DFRC is presented. In addition, potential activities or uses of the PSFCC are described. Note that use of trade names or names of manufacturers in this document does not constitute an official endorsement of such products or manufacturers, either expressed or implied, by the NASA.

FUNCTIONAL DESCRIPTION

The PSFCC design uses a Research Flight Control System (RFCS) processor in addition to the basic F/A-18 quadraplex flight control computers. The RFCS can be engaged by the pilot to exercise full-authority control of the aircraft with research flight control laws. The basic F/A-18 flight control system is used for flight phases when the RFCS is not engaged, such as takeoff and landing. This basic flight control system also serves as the reversion mode when the RFCS control laws are disengaged. The basic F/A-18 control laws and the RFCS control laws are computed continuously during flight.

Figure 1 shows how the PSFCC are integrated into the F/A-18 flight control system. The F/A-18 aircraft is controlled by a quadredundant flight control computer system. This system accepts quadredundant signals for rate gyroscopes, accelerometers, and pilot inputs. Dual input signals are used for airdata, angle of attack, and nose wheel steering (NWS). The system outputs quadredundant signals for stabilators and trailing-edge flaps. In addition, dual signals are outputted for leading-edge flaps, ailerons, and rudders. The baseline system also receives Military Specification 1553 multiplex bus data from the inertial navigation system (INS), airdata computer, and mission computers (MC).

Figure 2 shows the elements the pilot uses to interface with the PSFCC. Figure 2(a) shows the F/A-18 displays featuring the digital display indicators (DDI) and up-front controller (UFC). Figure 2(b) shows the DDI display with programmable buttons and "arm" discrete displayed. Lastly, figure 2(c) shows the pilot stick with the NWS and the paddle switch.

The pilot can specify a control mode using buttons on either of the cockpit DDI. Each DDI button is programmed to send the PSFCC research software two numbers: a table number and a row number. These numbers specify which research control mode is requested. The UFC is used to program the DDI buttons with the table and row numbers.

Currently, the PSFCC research software has three flight control modes: a replication mode of the basic F/A-18 flight control system, a variable dutch roll response mode, and a mode which locks the right stabilator. The variable dutch roll response mode has three levels of lateral–directional damping: overdamped, underdamped, and unstable. A unique table and row number exists for each of these selections, providing for five research control law choices. This portion of the PSFCC can be reprogrammed to meet future research needs.

The research software has been preprogrammed with two sets of requirements: arm requirements and engage–disengage requirements. Current aircraft parameters are evaluated against the requirements for differential stabilator, normal acceleration, yaw rate, bank angle, altitude, and Mach number. These parameters must meet the requirements to allow the system to be armed (enabled) and then engaged (activated). The PSFCC are programmed with a
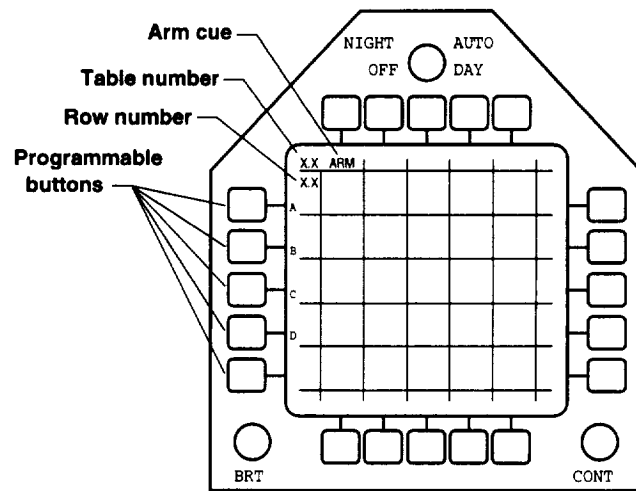
3
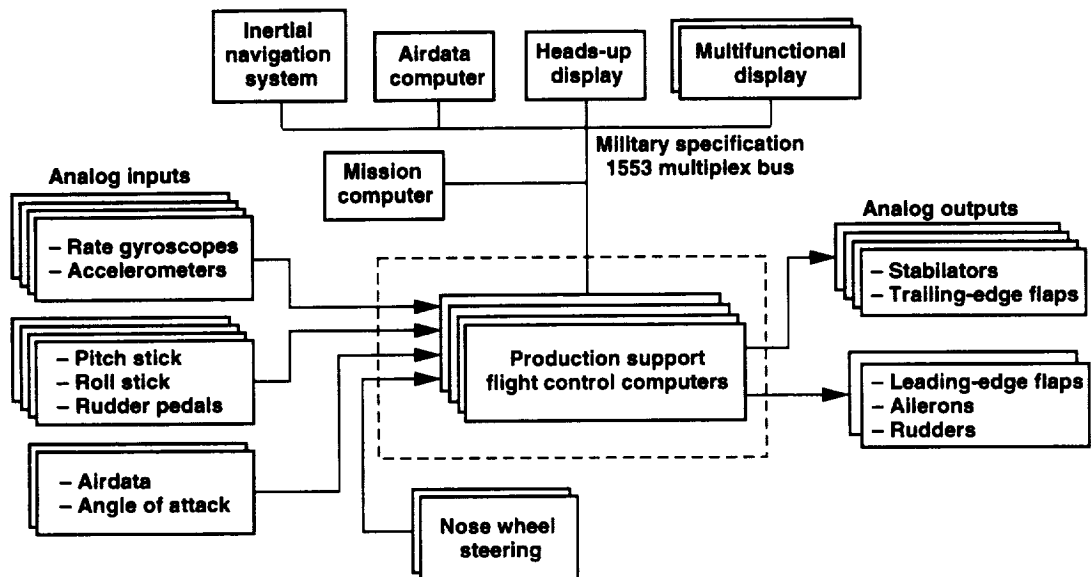
Figure 1. The F/A-18 control system components.
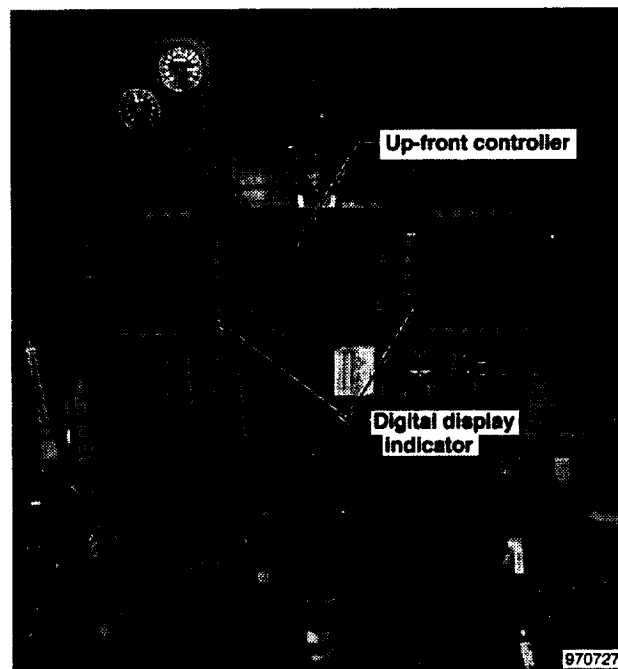
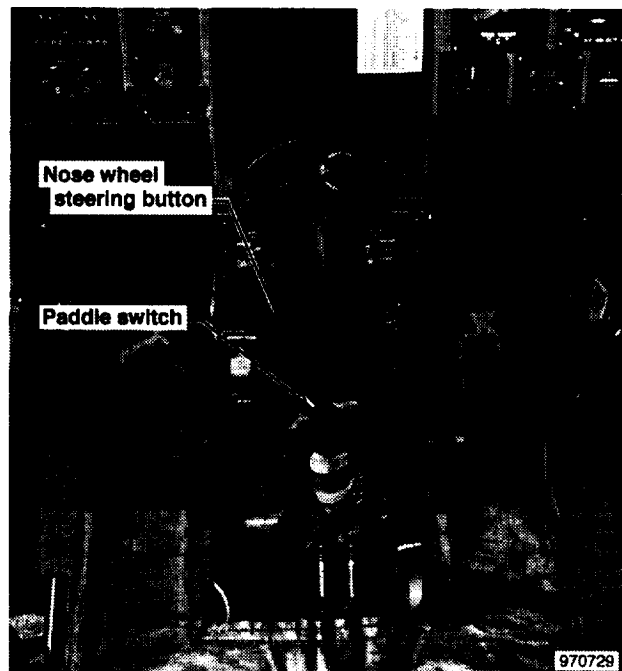(a) Digital display indicators and up-front controller.

Figure 2. The F/A-18 cockpit displays and pilot stick.

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Source: McDonnell Douglas Aerospace,
Seattle, Washington

970728

(b) Digital display indicator with program buttons.

(c) Pilot stick with nose wheel steering button and paddle switch.

Figure 2. Concluded.

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default set of limits for each research mode. The software contains tables of alternate limits which can be selected. These alternate limits may be selected using additional table and row numbers (by pressing another programmed button). Table and row number combinations exist which correspond to different sets of alternate limits. For example, one upper differential stabilator arm limit could be modified, or a complete set of altitude upper and lower arm and engage–disengage limits could be modified using one table and row number combination. Table 1 lists the value of the default limits for the current PSFCC modes. Alternate limits are presented in table 2.

Once the research mode is requested by selecting a DDI button, the arming requirements are checked. If these requirements are met, the PSFCC will give an armed indication on the DDI. The pilot can attempt to engage the mode by pressing the NWS button at the bottom of the control stick. If engagement requirements are satisfied, then the PSFCC will engage. The pilot can disengage the system by pressing the paddle switch at the bottom of the control stick. Automatic disengagements occur when any engagement–disengagement requirements are violated.

Integration with the F/A-18 Aircraft

Figure 3 shows the PSFCC modification to the basic flight control computer. The RFCS PACE 1750A

processor (Performance Semiconductor Corporation, Sunnyvale, California) is embedded in the same avionics box as the basic 701E flight control processors (Lockheed Martin Control Systems (LMCS), Binghamton, New York). The RFCS control laws are programmed in Ada and are independent of the basic control laws. Information to and from the RFCS is handled by the basic flight control system through dual port random access memory (DPRAM) to minimize communication delays and to isolate the basic system from RFCS failures. The 701E processor operates with 160-Hz subframes. It is synchronized with the RFCS using software flags. The RFCS will not start processing a frame until it receives a positive flag from the 701E processor indicating that the required data have been sent. The four F/A-18 processors are synchronized using a 10-Hz hardware pulse. The RFCS processors are synchronized with the basic F/A-18 processors using a 160-Hz hardware pulse.

All input–output and failure monitoring is done within the basic 701E flight control processor system. Sensor inputs, pilot inputs, and airdata parameters are transmitted to the basic flight control system through analog-to-digital (A/D) converters. These signals are then compared in the input signal management, and a selected signal is sent to the basic control laws and to the RFCS. Surface position commands from the basic F/A-18 control law and from the RFCS are sent to the output signal selection

Table 1. Default engage and disengage limits for the Production Support Flight Control Computers research modes.

| Parameter	Basic F/A-18 replication mode		Variable stability dutch roll mode, locked surface mode	
	Armed	Engage–disengage	Armed	Engage–disengage
Differential stabilator, deg	±5.0	±5.0	±5.0	±5.0
Normal acceleration, g	4.0 to –1.5	7.5 to –1.5	4.0 to –1.0	4.0 to –1.0
Yaw rate, deg/sec	±12.0	±25.0	±12.0	±12.0
Roll rate, deg/sec	±120.0	±120.0	±120.0	±120.0
Bank angle, deg	±150.0	±150.0	±75.0	±75.0
Altitude, kft	40 to 19	45 to 15	21 to 19	25 to 15
Mach number	0.90 to 0.40	0.95 to 0.25	0.8 to 0.6	0.8 to 0.6

Table 2. Alternate engage and disengage limits for Production Support Flight Control Computers research modes.

Parameter	Upper arm limit	Lower arm limit	Engage and disengage limit, upper	Engage and disengage limit, lower
Differential stabilator, deg	0.5	−0.5	2.0	−2.0
	1.0	−1.0	4.0	−4.0
	2.0	−2.0	6.0	−6.0
	3.0	−3.0	8.0	−8.0
	4.0	−4.0	9.0	−9.0
Normal acceleration, g	2.0	0.5	2.0	0.0
	4.0	0.0	4.0	−0.5
	5.5	−0.2	5.5	−2.0
	6.5	−0.6	6.5	−2.5
	7.0	−1.0	7.0	−3.0
Yaw rate, deg/sec	1.0	−1.0	5.0	−5.0
	3.0	−3.0	10.0	−10.0
	5.0	−5.0	15.0	−15.0
	7.0	−7.0	20.0	−20.0
	9.0	−9.0	30.0	−30.0
Roll rate, deg/sec	10.0	−10.0	25.0	−25.0
	30.0	−30.0	50.0	−50.0
	50.0	−50.0	100.0	−100.0
	70.0	−70.0	150.0	−150.0
	90.0	−90.0	200.0	−200.0
Bank angle, deg	10.0	−10.0	30.0	−30.0
	30.0	−30.0	45.0	−45.0
	45.0	−45.0	60.0	−60.0
	60.0	−60.0	90.0	−90.0
	90.0	−90.0	135.0	−135.0
Altitude, ft	22,500	17,500	22,500	17,500
	25,000	10,000	25,000	10,000
	30,000	7,500	30,000	7,500
	35,000	5,000	35,000	5,000
	45,000	2,000	40,000	2,000
Mach number	0.8	0.6	0.8	0.6
	0.9	0.5	0.9	0.5
	1.0	0.4	1.0	0.4
	1.2	0.3	1.2	0.3
	1.4	0.2	1.4	0.1

and fader logic, which selects the signal to be used by the actuator signal management. These surface positions are converted to analog signals through a digital-to-analog (D/A) converter.

To retain the integrity of the basic F/A-18 system, the functionality of the basic control laws was left unchanged except when incorporating RFCS input–output was required. The basic system not only provides the pilot and sensor inputs to the RFCS but also supplies internal basic F/A-18 control law results which can be used by the RFCS control law if desired. Built-in-test (BIT) functions reside in the basic system. The ability to monitor parameters
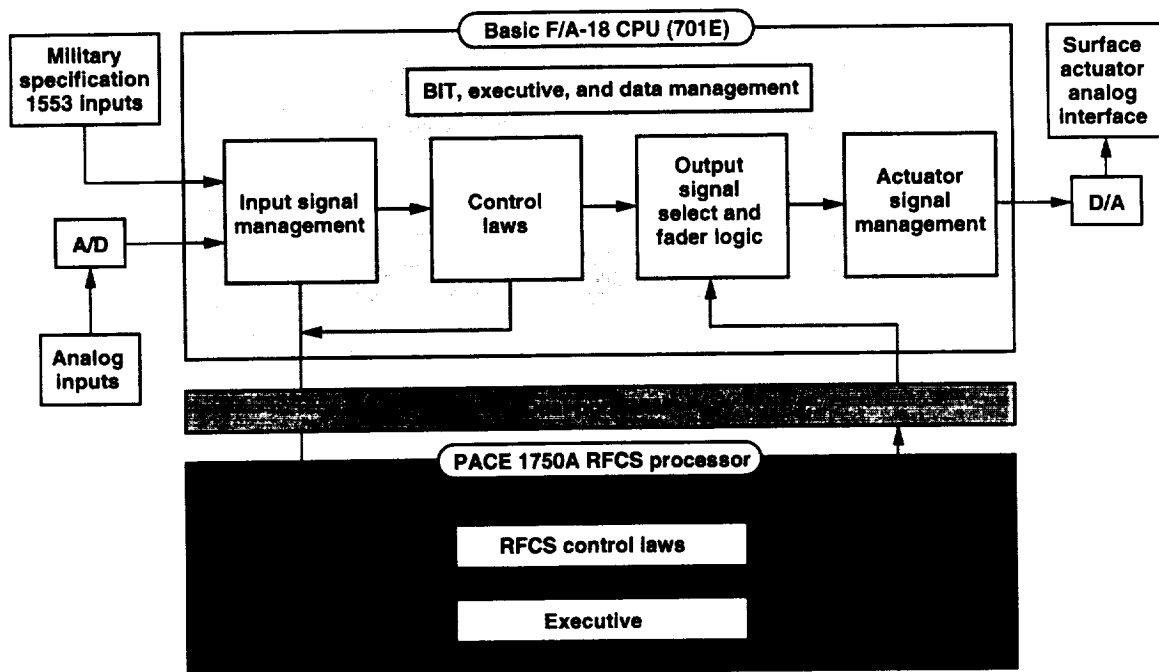
Figure 3. Integration of research processor and baseline F/A-18 systems [3].

within the basic RFCS control law computers was added for flight test information and evaluation. Sixty-four programmable words of data can be put on the aircraft Military Specification 1553 bus and recorded for subsequent analysis.

Because the basic F/A-18 and the RFCS flight control systems work concurrently, a desire to minimize the aircraft transient during RFCS and basic F/A-18 mode transitions exists. The PSFCC have a provision for aligning the pitch stabilator positions between the basic F/A-18 and the RFCS control laws. Symmetric stabilator commands from the basic F/A-18 and the RFCS control laws are available in the DPRAM. The unengaged flight control system (either the RFCS or the basic 701E processor control laws) computes a symmetric stabilator position equal to the engaged flight control system by aligning the pitch forward loop integrator state.

Hardware Description

The 1750A PACE processor has 58 kilowords of memory and uses a 40-MHz clock. This memory is divided in the following way:

Memory	Kilowords
DPRAM	2
Scratchpad random access memory (RAM)	8
Electrically erasable programmable read only memory (EEPROM)	32
Ultraviolet programmable read only memory (UVPROM)	16

Figure 4 shows memory map of the 1750A PACE processor. The experimental control laws are contained in the 32 kilobytes of EEPROM. The DPRAM has 1024 words for basic F/A-18 control law to RFCS communication (with approximately 750 spare words). There are also 1024 words for RFCS to basic F/A-18 control law communication (with approximately 800 spare words). There are 62 words reserved for RFCS status data to be placed on the Military Specification 1553 bus. A cross-channel data link (CCDL) capability allows 24 words to be broadcast to the other three processors, with 72 words (24 from each of the other processors) available for data comparison between channels. Data passed through the DPRAM include selected feedback signals, airdata and discrete data,
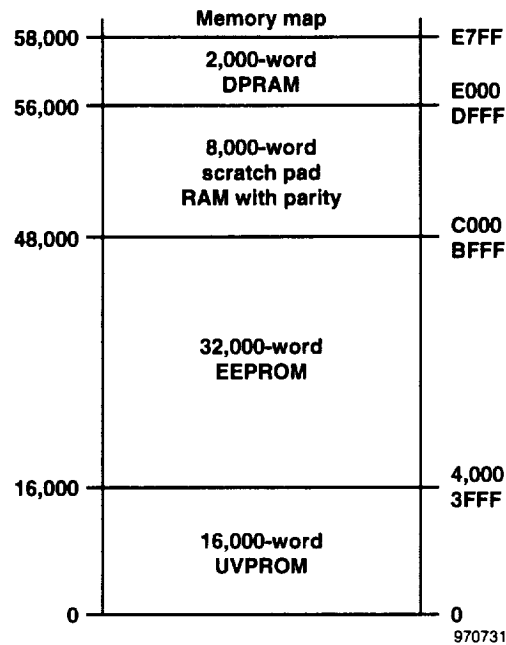
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Figure 4. Memory map of the PACE 1750A processor.

701E actuator servocommands, actuator positions, and CCDL from the other processors.

System Timing

Figure 5 shows the system timing between the basic F/A-18 processor and the RFCS processor for one 160-Hz frame. The basic F/A-18 processor performs an executive routine, a preprocessing routine for RFCS data, and the input signal management (ISM). (See segment A on the diagram.) A hardware timing discrete is then sent to the RFCS processor, which begins its executive routine. Concurrently, the basic F/A-18 processor and the RFCS processor begin executing control laws. When the basic F/A-18 processor is finished with its control law execution, it sends a data ready indicator to the RFCS processor. (See the end of segment B on the diagram.) At this point, updated basic F/A-18 control law calculated data, such as surface positions, have been placed in the DPRAM. The RFCS sends a data ready indicator when finished. (See the end of segment C on the diagram.) The basic F/A-18 processor expects segments B and C to be activated within 2.2 msec. If the RFCS data ready discrete signal is not received within 2.2 msec, the basic F/A-18 processor declares a failure and disengages the RFCS. The remainder of the 160-Hz subframe is used for the remaining RFCS and basic F/A-18 control law processing and background tasks.

NASA DFRC RESOURCES

A facility such as the PSFCC can only be used effectively for flight controls and handling qualities research if all the supporting elements are present. This section describes the PSFCC support elements available at NASA DFRC.

F/A-18 Aircraft

Six F/A-18 aircraft are probably the most valuable resource that NASA DFRC has in support of the PSFCC. Currently, five F/A-18 chase aircraft could be used as testbeds for the PSFCC. In addition, an F/A-18 dedicated research testbed called the Systems Research Aircraft (SRA) is available. Because none of these F/A-18 aircraft would be solely dedicated to PSFCC flight test, no separate funds are needed to maintain the aircraft testbed. This approach also allows experiments to be designed and tested on the PSFCC with no requirement to schedule flight until it is certain that the experiment will be ready. Note that the PSFCC require an MC software load which can
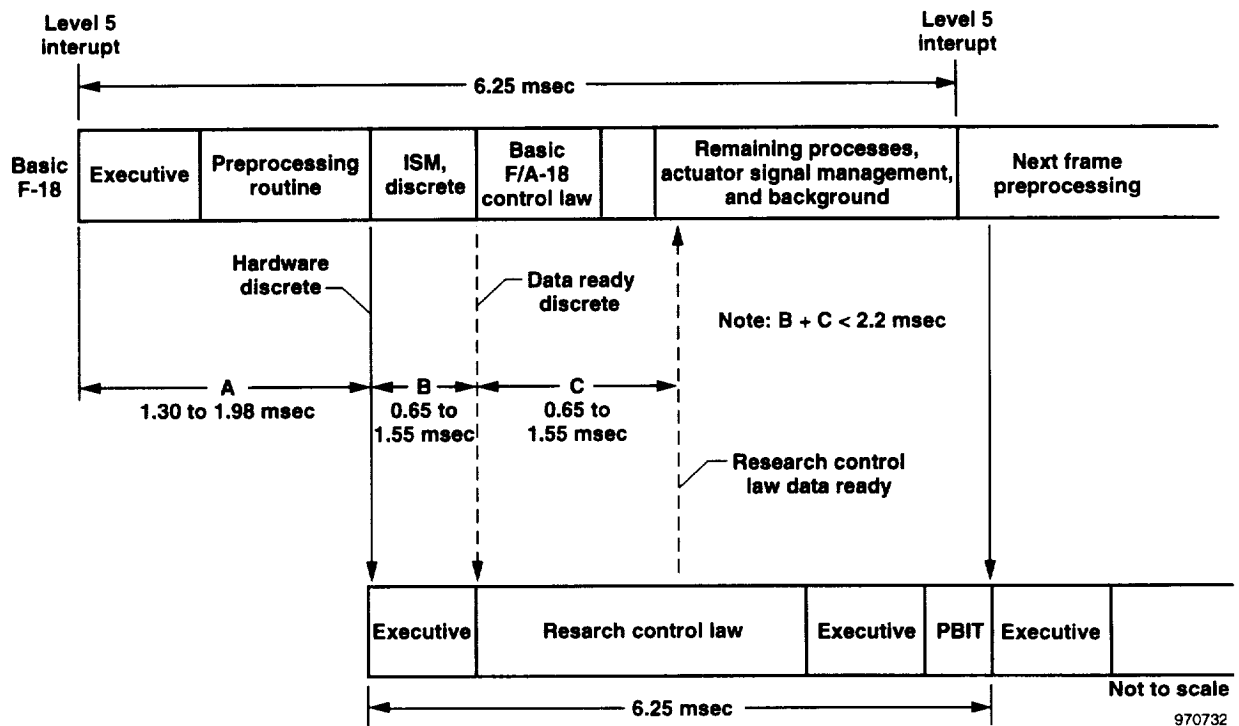
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Figure 5. Timing diagram of production support flight control computer.

display the programmable buttons. This capability is available in the majority of the MC software.

These F/A-18 chase aircraft are equipped with a USN telemetering device called a Quick Instrumentation Data System (QIDS). The QIDS installs easily on any F/A-18 aircraft and will telemeter any data which is on the Military Specification 1553 bus. The QIDS is currently configured to telemeter 64 words at 20 Hz. This configuration can gather handling qualities data and PSFCC status words. The SRA is already equipped with a NASA research instrumentation system which can telemeter any required parameters.

Hardware-in-the-Loop Simulation

One essential resource to have when flight testing new aircraft systems is a hardware-in-the-loop, or in this case, a processor-in-the-loop simulation. Such simulation allows for realistic validation and failure mode testing. This simulation must be at the same location as the flight testing, so rapid examination of flight anomalies can take place.

Figure 6 shows the processor-in-the-loop simulation configuration for the F/A-18 test bench. This simulation uses aircraft hardware for the PSFCC, MC's, cockpit displays, and UFC. The PSFCC are interfaced with the flight control computer console. This console exchanges information with a simulator interface device (SID) and a cockpit signal-conditioning unit. The SID provides analog and digital signals used by the simulation computers. The cockpit signal-conditioning unit provides an interface with the piloted cockpit. These simulation computers contain a full six-degree-of-freedom simulation which can simulate pilot inputs and provide full data recording. A Military Specification 1553 data bus is used to interface the MC's and PSFCC and to drive the cockpit DDI. Stripchart recorder capability is available for real-time data observation. The simulation can be driven with automated scripts, and data can be logged for posttest processing.

Experienced Personnel

During the HARV program, Ada programming and validation testing of new control laws using the
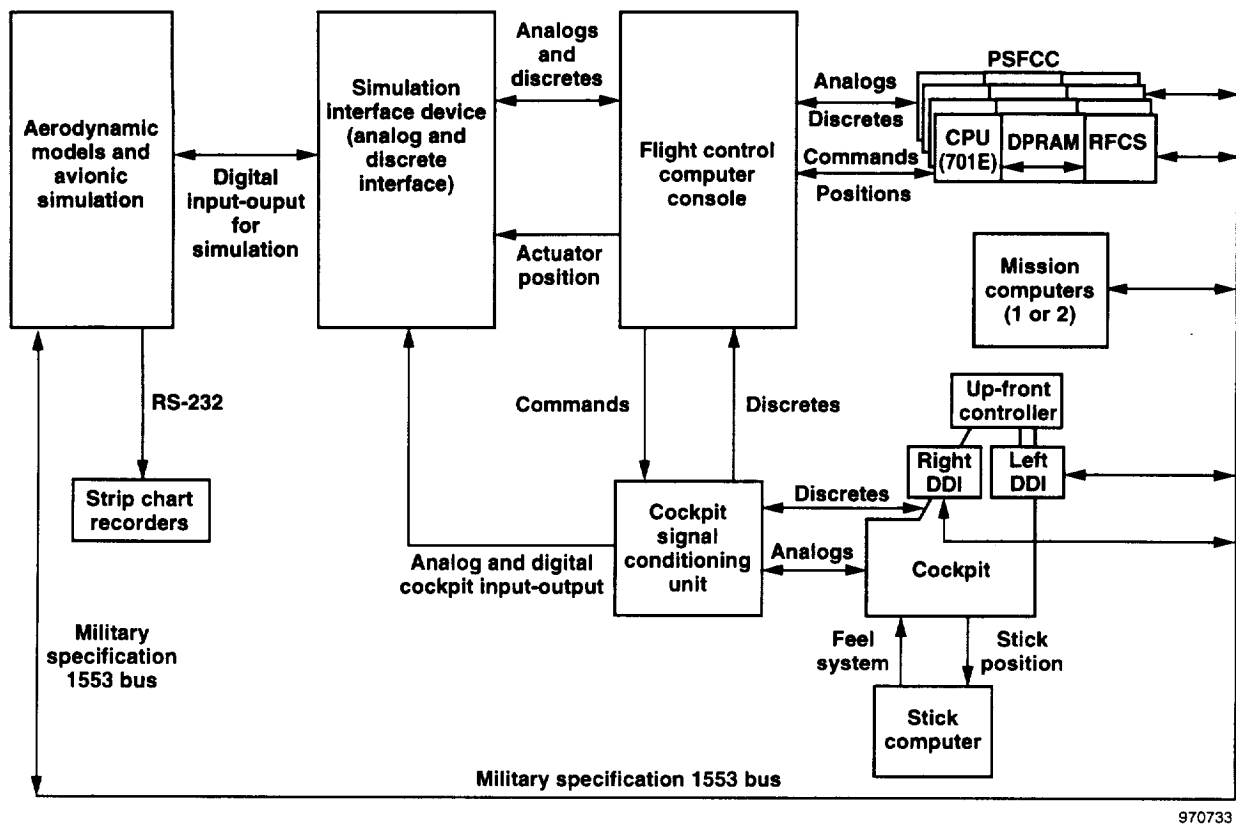
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Figure 6. Hardware-in-the-loop configuration [4].

PSFCC processor were performed. Many lessons were learned about practical issues concerning the programming of the RFCS processors. These lessons include

• Portability—Ada software on the HARV program was transferred to three platforms with only system specific changes.

• Documentability—Ada is self-documenting on the code level; however, added documentation on the system level operation of Ada is necessary for coding.

• Modifiability—Ada is easy to modify.

• Testability—Testing requirements for the Ada software were no different than those of any other high-order language.

Reference 4 provides additional detail on these and other related issues.

Safety-of-Flight Administrative Processes

To verify that issues addressing safe flight test have been properly resolved, a process consisting of a Flight Readiness Review (FRR) and an Airworthiness and Flight Safety Review Board (AFSRB) evaluation is conducted. An FRR consists of a panel of working level personnel assigned to evaluate whether a project is safe for flight test. The project presents analysis on the safety of the proposed flight program to the FRR panel. Then, the panel determines whether the project has fulfilled the requirements for safe flight. Next, the FRR panel presents its recommendation to the AFSRB. Lastly, the AFSRB makes the final decision on flight test for a given project. Without the proper experience, the FRR panel and the AFSRB could not accurately determine if a project should go forward to flight test. Over the past 50 years, experience in this process has been acquired and refined for a broad range of aircraft and other flight vehicles. This established,

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proven process provides an extremely safe and relatively fast flight approval process.

VERIFICATION AND VALIDATION TESTING

When clearing flight control computers for flight test, verification and validation testing are necessary. Verification testing ensures that the system was fabricated correctly, and it fulfills the design requirements. Validation testing determines if the design is suitable for the task. Validation testing uses the system under realistic conditions to determine if operational problems exist and to assess dangerous failure modes. The verification and validation testing for the initial flight test thoroughly evaluates the baseline F/A-18 flight controller and the research flight control system. In succeeding experiments, only the research flight control system will require verification and validation, thereby saving time, effort, and money for the next experiments.

Four organizations participated in testing of the PSFCC: LMCS, MDA, NASA DFRC, and USN. Note that LMCS and MDA perform the standard test suite that they normally use to clear a new flight control computer set. Tests that apply to operation in the baseline F/A-18 and in the research control laws, such as failure tests, are performed with the baseline F/A-18 control system and with the research F/A-18 replication mode.

Table 3 shows the testing which was conducted in each category and lists responsible organization. Note that the MDA, NASA DFRC, and USN conducted the same categories of validation testing. This overlap occurred because the NASA DFRC and USN have additional requirements which exceed the original MDA effort. In addition, the NASA DFRC and USN gathered valuable experiences during these validation tests. These experiences serve as initial training for flight test activities.

Module Level Testing

Low-level software testing was performed on the basic F/A-18 control law software by LMCS. This testing included software subroutine level testing of the 701E processor executive, BIT software, input—output signal management, and control laws.

Open-Loop Failure Testing

The MDA performed broken wire testing in which the processor-in-the-loop bench is used to disconnect various feedbacks and to determine if the computers react properly. The term *open loop* refers to the fact that the flight control processor is not linked to any aircraft simulation so that simulated aircraft reaction to each failure cannot be observed. Failures are individually inserted into dual redundant and quadredundant sensor and discrete signals to determine if the system reacts properly to each failure. Other failure tests include individual surface command feedback, position feedback, hydraulic system, and airdata failures.

Open-Loop Validation Testing

The MDA performed automated validation testing using a system called Flight Control Automated System Testing (FAST) on the processor-in-the-loop test setup. By inserting signal-generating software into the input plane of the baseline F/A-18 flight control computers, this automated testing validates each individual path in the control laws for functionality. The FAST is performed on the baseline F/A-18 flight control system and on the research F/A-18 replication mode.

The basic F/A-18 processors provide a great deal of flexibility in the FAST. A software routine which is patched into the basic F/A-18 processor software makes it possible to vary any software variable and to record a time history of any path in the software. As a result, thorough tests are completed. These tests use every flight control system input to every surface output and vary flight conditions for the entire envelope. Tests are conducted in the up-and-away, powered approach flight, and outer loop (automatic pilot) modes.

For the research software, FAST was performed through the DPRAM locations. Because this approach restricts the availability of internal variables to be changed, such as gains, five flight conditions were chosen. These conditions spanned the dynamic pressure envelope for the research software. The FAST is done from every flight control input to every flight control output. These tests consist of steps, ramps, and frequency sweeps. Software routines automatically perform the testing,

Table 3. Testing matrix for the Production Support Flight Control Computers.

Verification Tests	LMCS	MDA	DFRC	USN
Module level	X			
Open-loop failure				
Executive logic	X	X		
Channel identification	X	X		
Power on reset	X			
Initial BIT	X			
Military Specification1553 bus checks	X			
Quadsensor		X		
Airdata and angle-of-attack failures		X		
Quaddiscrete failures		X		
Surface command failures		X		
Surface position failures		X		
Hydraulic failures		X		
Dual discrete failures		X		
Validation Tests				
Open-loop tests	X			
Closed-loop tests	X	X	X	
Closed-loop failure	X	X	X	
Quadsensor failures	X	X	X	
Airdata and angle-of-attack failures	X	X	X	
Quaddiscrete failures	X	X	X	
Surface command failures	X	X	X	
Surface position failures	X	X	X	
Hydraulic system failures	X	X	X	
Dual discrete failures	X	X	X	
Mode transition	X	X	X	
Automatic pilot modes	X	X	X	
Spin mode				
Piloted tests	X	X	X	
Basic familiarity	X	X	X	
Mode transition tests	X	X	X	
Sensor failures	X	X	X	
Surface position failures	X	X	X	
Hydraulic system failures	X	X	X	
Combination surface failures	X	X	X	

Note: In the Validation Tests section, the columns for Closed-loop tests and below contain X marks under LMCS, MDA, and USN (the three rightmost data columns).

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record the time history results, and compare these results to time histories of software truth models.

Closed-Loop Validation Testing

The MDA, NASA DFRC, and USN will divide the tasks for the closed-loop validation testing. The PSFCC are interfaced with a six-degree-of-freedom simulation. The configuration of which is consistent among these organizations. Closed-loop time histories of the PSFCC testing are recorded and compared with software models of the baseline F/A-18 control laws and RFCS modes. This testing validates the performance of the baseline F/A-18 airplane and of the PSFCC control modes. Tests include automated pilot inputs of steps, doublets, and frequency sweeps.

The baseline F/A-18 control law tests are performed at 12 up-and-away flight conditions and 5 powered approach flight conditions. The PSFCC F/A-18 replication mode tests are performed at up-and-away flight conditions above 15,000 ft (the low altitude limit for the research modes). The variable stability and locked surface modes are performed at five flight conditions within their operating envelope.

Closed-Loop Failure Tests

In closed-loop failure tests performed by the MDA, NASA DFRC, and USN, pilot inputs are placed into the processor-in-the-loop test setup linked with a six-degree-of-freedom simulation. The same failures induced during the open-loop failure tests are induced here. Time history data are examined to see if excessive transients occur for the baseline F/A-18 flight control system and for the research flight control system.

Mode Transitions, Automatic Pilot Modes, and Spin Modes

In mode transition, automatic pilot, and spin mode tests, the auxiliary modes are tested for basic functionality. Automatic pilot modes tested include heading hold, barometric altitude hold, radar altitude hold, velocity hold, automatic carrier landing system, and instrument landing system. Flap transitions tested consist of up-and-away, half-flap, and full-flap operations. The spin mode is also tested.

Piloted Tests

Pilots fly the processor-in-the-loop simulation to gain basic familiarity with the system. Transients resulting from envelope and maneuvering requirement violations are evaluated to determine if excessive aircraft motion is encountered. Such system failures as sensor failures, surface command failures, and hydraulic failures are induced during simulated flight to determine if undesirable transients occur.

PRODUCTION SUPPORT FLIGHT CONTROL COMPUTERS POTENTIAL ACTIVITIES

The PSFCC provides a flexible control law and handling qualities research tool. Because the necessary facilities and personnel reside at the NASA DFRC, programs can easily be completed on a part-time or time available basis. This section describes potential activities for the PSFCC. Items described include experimental control law architectures, handling qualities experiments, and aircraft excitation systems.

Experimental Control Law Architectures

The primary goal of developing the PSFCC is for flight testing of experimental control law algorithms. Limiting the flight envelope with appropriate operational engagement and disengagement limits provides relatively fast prototyping and flight test of experimental control law designs.

Because the research processors in the PSFCC are quadredundant, operational issues concerned with redundancy management must be solved before flight test occurs. Many new algorithms contain neural network software which might learn differently across four channels, resulting in one or more computers being voted out. The CCDL capability of the PSFCC allows each research computer to use variable values from each of the other three computers. Perhaps, this knowledge can be used to implement advanced or neural network architectures.

The F/A-18 aircraft have surfaces which can be used for roll and yaw motions. Differential stabilator, ailerons, and rudder can be allocated in several

combinations to produce the same aerodynamic moment. If the surface combination can be optimized for the minimum overall surface deflection, aircraft drag and hydraulic system requirements can be reduced. A number of organizations, such as the Honeywell Technology Center, Minneapolis, Minnesota, and the Virginia Polytechnic Institute and State University, Blacksburg, Virginia, have studied this problem [5]. The PSFCC provides an opportunity to flight test differing philosophies concerning surface allocation.

A design effort has already been started to address the possibilities of using differential thrust on an F/A-18 airplane to dampen lateral–directional flight control modes. Thrust modulation has been used for backup control of aircraft, including an F-15 landing which was performed using thrust [6]. The PSFCC accommodates the addition of engines into the F/A-18 control law with numerous safety trips caused by unwanted flight dynamics.

Handling Qualities Experiments

Handling qualities experiments can be performed using the PSFCC. Many control laws, such as model-following techniques, are designed such that frequency and damping are specified for the airframe. The first phase of handling qualities research involves using such a control law to validate the frequency and damping of the airframe. Next, the results are compared to the requested frequency and damping. This approach would lay the groundwork for validation of experiments which equate aircraft frequency and damping to handling qualities rating, such as Cooper-Harper ratings [7].

Other experiments may include flight test with different pilot control sticks to assess changes caused by the different mechanical affects on a level 1 handling aircraft. By installing different sticks in the rear cockpit of a two-seat F/A-18 airplane, pilot evaluation could be obtained safely. The ability to revert to the baseline F/A-18 system would be retained.

Aircraft Excitation Systems

The PSFCC research control modes could be used for programmed excitations to surfaces, such as steps, doublets, and frequency sweeps. These excitations could provide parameter identification, in-flight gain,

and phase margin calculations. Singular value calculations, flutter evaluation, or aeroservoelasticity research could also be conducted.

As this paper is being written, the LMCS and MDA tests are finished, and the NASA DFRC and USN phases of the bench testing have recently begun. The USN and NASA DFRC are learning the specific aircraft requirements for using the PSFCC, such as correct mission computer loads. This testing and the NASA DFRC FRR process are expected to require approximately 3 months to complete. A first flight is planned for late summer 1997.

SUMMARY

The Production Support Flight Control Computers (PSFCC) can give any fleet F/A-18 airplane an in-flight, pilot-selectable, research control law capability. The PSFCC design uses a Research Flight Control System (RFCS) processor in addition to the basic F/A-18 quadraplex flight control computers. The RFCS can be engaged by the pilot to exercise full-authority control of the aircraft with research flight control laws. The basic F/A-18 flight control system is used for all flight phases when the RFCS is not engaged, such as takeoff and landing. It is also used as the reversion mode when the RFCS control laws are disengaged. Because the research processor in the PSFCC can be engaged or disengaged by the pilot or automatically disengaged due to system, flight envelope, or maneuvering limits, the mechanization addresses flight safety concerns. All of the redundancy management and safety systems of the F/A-18 remain unchanged. The PSFCC configuration reduces the amount of effort required for the design and test of experimental flight control software.

There are five major benefits of using the PSFCC at NASA DFRC. Dryden Flight Research Center has

- Six F/A-18 aircraft available for this type of research
- Chase aircraft which have been equipped with instrumentation and telemetering systems for data transmission
- Processor-in-the-loop simulation for verification and validation testing
- Personnel familiar with programming of the research processor

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• Safety-of-flight processes established which address the concerns for an aircraft research control system in a timely manner

Once the initial flight test of the PSFCC has been completed successfully, the PSFCC facility will be useful for a variety of flight control and handling quality research experiments. Because experiments can be designed and executed within a limited flight envelope, less work, such as analysis and testing, will be required to bring advanced concepts to flight. Advanced algorithms will be flight tested to find potential problems or payoffs associated with actual flight applications. Flight control systems which specify airframe frequency and damping can be flight verified and used to determine handling quality ratings as a function of airframe dynamics. Alternate control sticks can be used to determine their affects on aircraft handling qualities. In-flight excitation systems can be used for parameter identification, phase and gain or singular value calculations, and flutter or aeorsevoelasticity research.

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13. ABSTRACT (Maximum 200 words)

NASA Dryden Flight Research Center (DFRC) is working with the United States Navy to complete ground testing and initiate flight testing of a modified set of F/A-18 flight control computers. The Production Support Flight Control Computers (PSFCC) can give any fleet F/A-18 airplane an in-flight, pilot-selectable research control law capability. NASA DFRC can efficiently flight test the PSFCC for the following four reasons: (1) Six F/A-18 chase aircraft are available which could be used with the PSFCC. (2) An F/A-18 processor-in-the-loop simulation exists for validation testing. (3) The expertise has been developed in programming the research processor in the PSFCC. (4) A well-defined process has been established for clearing flight control research projects for flight. This report presents a functional description of the PSFCC. Descriptions of the NASA DFRC facilities, PSFCC verification and validation process, and planned PSFCC projects are also provided.

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