FABRICATION AND QUALIFICATION OF COATED CHIP-ON-BOARD TECHNOLOGY FOR MINIATURIZED SPACE SYSTEMS

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ABSTRACT

Chip-on-Board (COB) packaging technology is important in the miniaturization of space system electronics. We report the results of an extensive study to fabricate and qualify this technology for high reliability space applications. Rigorous environmental stresses including vibration, temperature cycling and temperature-humidity-bias testing have been carried out on candidate coating combinations used to protect bare die. Both robustness in space application and environmental protection on the ground-complete reliability without hermeticity were desired. Epoxy/parylene combinations proved to be superior.

1. INTRODUCTION

The major impetus for flight qualifying Chip-on-Board (COB) packaging technology is the shift in emphasis for space missions to smaller, better, and cheaper spacecraft and satellites resulting from the NASA New Millennium initiative and similar requirements in DoD-sponsored programs. The most important benefit that can potentially be derived from miniaturizing spacecraft and satellites is the significant cost savings realizable if a smaller launch vehicle may be employed. Besides the program cost saving, there are several other advantages to building COB-based space hardware. First, once a well controlled process is established, COB can be low cost compared to standard multi-chip module (MCM) technology. This cost competitiveness is regarded as a result of the generally greater availability and lower cost of known good die (KGD). Coupled with the elimination of the first level of packaging (chip package), compact, high density circuits can be realized with printed wiring boards (PWB) that can now be made with ever-decreasing feature size in line width and via hole. A second technical improvement is the reduced length of signal paths among devices resulting from use of unpackaged die which will enhance circuit performance by minimizing noise and signal coupling permitting operation at higher speed. A third advantage of COB is the reduction in thermal path from the die to the substrate which improves heat sinking, spreading and dissipation.

Since the COB packaging technique in this study is based mainly on populating bare dice on a suitable multi-layer laminate substrate which is not hermetically sealed, die coating for protection against the environment is required. In recent years, significant improvements have been made in die coating materials which further enhances the appeal of COB. Hysol epoxies, silicone, parylene and silicon nitride are desirable because of their compatible thermal coefficient expansion (TCE) and good moisture resistance capability.

2. DIE COATING MATERIALS

All bare dice have a thin layer of passivation of SiO_2 or Si_3N_4 that covers the circuit to provide protection from the environment, with the exception of the bond pads. This passivation is done by the IC foundry at the wafer stage. It requires high temperature and accurate application thickness. Since the bond pads are made of aluminum material, oxidization of the bond pads can easily occur if they are not protected. Therefore, coating materials are extremely important in COB technology. Selection of coating material requires a thorough understanding of the material behaviors. Five major factors are included in the material selection:

1. Thermal coefficient of expansion (TCE) should be close to that of the wire material (Gold wire has TCE = 14.2 ppm/°C),
2. High glass transition temperature (Tg),
3. Low cure shrinkage,
4. Void-free fill over wires, and chips
5. Low ionic contamination content (<20 ppm Na^+, K^+, Cl^-).

Silicones and epoxies are the two major groups of glob-top materials meeting the selection characteristics. Both of these materials are used in commercial electronic products. Silicone (HIPEC Q1-4939) is a gel-like material

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offering low alpha particle emission, high purity and low modulus of elasticity. Silicone also has very low ionic content and a low water saturation level. On the negative side, silicone's inherently high TCE can cause excessive thermal stresses on wire bonds. Epoxy (FP-4450, FP-4402) is an opaque glue-like material having low ionic content, a high glass transition temperature, and a high elasticity modulus. It also has a low TCE that is comparable to that of gold wirebonds and provides excellent mechanical compatibility.

Parylene C is a high melting-point, white, crystalline solid material used to provide a uniform conformal coating for electronic assemblies. It is a dimer with the chemical name of Dichloro-di-p-xylene. Parylene is a chemically and mechanically stable material insoluble in all organic solvents up to 150°C and resists permeation by all solvents with the exception of aromatic hydrocarbons. Typical applications of parylene coating have a thickness of about 25.4 microns. The application process is a vapor deposited process that applies a uniform coating material in a free molecular mode under vacuum.

Silicon nitride coating at room temperature is a proprietary process developed by Ionic Systems. It is a plasma enhanced chemical vapor deposition (PECVD) that has existed for many years in the electronic industry. Unlike the conventional silicon nitride deposition in wafer manufacturing that requires high temperature, this process deposits a uniform inorganic coating to silicon dice in COB assemblies at room temperature. Because of its extremely low moisture permeability, silicon nitride is a superior water block. A thin layer of 0.5 μm of the silicon nitride was used in the Polar satellite design and has successfully met all flight environmental requirements.

3. TEST VEHICLES

There were three different test vehicles used in this study– the FAD board, the DRAM boards, and the triple track chips.

Filter Analog to Digital (FAD) Board [Ref. 1]

A magnetometer that was flown on the Freja spacecraft was selected for the miniaturization experiment. The magnetometer is composed of three separate subsystems – the front-end sensor electronics, the FAD, and the processor board. To effectively demonstrate the manufacturability/viability of the COB packaging technology, a FAD circuit board was fabricated using COB packaging technology. The FAD board was chosen because of its relative circuit complexity compared with the other two boards. The FAD circuit design incorporates analog, digital and mixed signal circuitries and integrated circuit complexity ranging from discrete to VLSI technologies utilizing different power supply rails. It also employs a representative spectrum of electronic parts that may be used on typical subsystems in space hardware. The principal function of the FAD board is to condition an input signal from the sensor that detects magnetic field strength, and systematically digitize it for the processor board. A volume reduction of a factor of 7 was achieved with COB fabrication (see Figure 1).

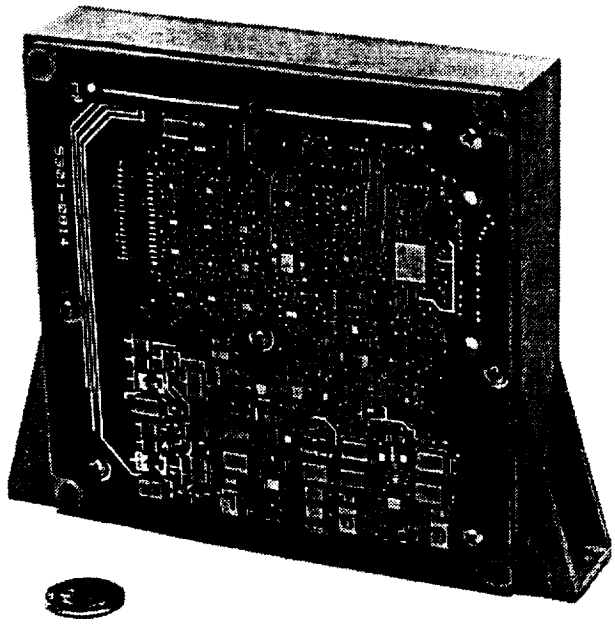


Figure 1
Photograph of the FAD Board with COB Design

DRAM Board [Ref. 2]

The second test vehicle is a DRAM board (Figure 2). The basic function of this circuit is to continuously and

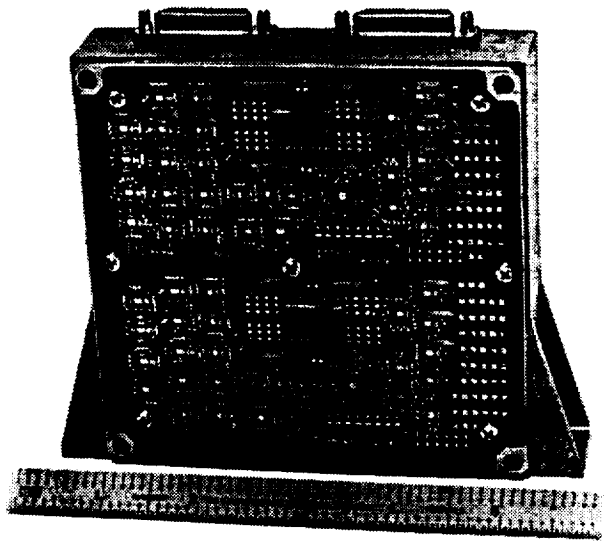


Figure 2
Photograph of the DRAM Board with 3-D Stacked DRAMs

completely exercise the 3-D stacked DRAM module with a memory capacity of 80 Mbits. The module consists of six DRAM die layers stacked on top of one another to form a 3-D rectangular cube. Only five die layers are used with the sixth one being a spare. The DRAM module is 4 million locations by 4 bits per location. Upon power-up, the circuit will be fully functional with an externally applied system clock and 8 digital pattern lines. The pattern bits are shifted at each system clock rising edge to provide a different data pattern to each memory location, upon which four distinct operations – refresh, write, refresh, and read are performed. Each address location in the DRAM module is accessed every 4,194,304 clock cycles.

Triple Track Device [Ref. 3]

The triple track device used to study coating integrity is the Assembly Test Chip, version 01 (ATC01) from Sandia National Laboratories. It is designed for use in monitoring integrated circuit damage due to corrosion of aluminum conductors. This test die contains several triple track and ladder test structures. The triple track test structures are basically very closely spaced, parallel aluminum tracks in triplets that run in a serpentine pattern. The track width and spacing are as small as 1.25 μm. The resistance of each track can be measured and monitored for detecting corrosion. The leakage current between the tracks can also be measured to detect the presence of any conducting path formed by ionic contaminants, dendritic growths or other corrosion agents. To characterize corrosion-induced failures quantitatively, ladder structures are available. A ladder consists of a number of aluminum conductor tracks connected in parallel between two wide metal bus bars. As open paths are created due to corrosion effects, the overall ladder resistance increases in stepwise fashion. An encapsulated sample is shown in Figure 3.

4. TEST PLAN, ENVIRONMENTS AND ACCELERATION FACTORS

The objective of the study was to qualify the coated COB technology for space application and also to determine which coating offered the most environmental protection. To space qualify the technology we used an environmental stress sequence of vibration followed by temperature cycle; to evaluate contamination and moisture protection we use the conventional 85°C/85% relative humidity temperature-humidity-bias (THB) test. Electrical functionality tests were performed before, at intervals during and after environmental stress on the Sentry-15 automatic tester.

The dynamic loads envelope used is representative of a spectrum of launch vehicle environments for various past space programs at APL. An electrical functional verification test at 0, 25, and 85°C was performed on the Sentry tester after vibration in each of the three axes. Sine

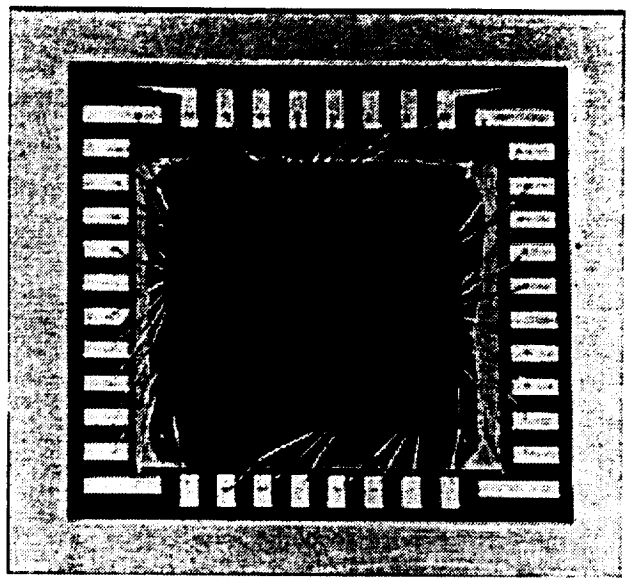


Figure 3
Photograph of a Triple Track Die Covered with Epoxy Encapsulant

burst (50g's at 35Hz, 10 cycles), random vibration (20-2000 Hz) and shock (100-10,000 Hz) tests were employed.

Thermal cycling was carried out in an environmental chamber for 1000 cycles. The temperature controller of the oven was set such that the test boards achieved a cooling and heating rate of between 10 to 12°C per minute with a dwell time of 10 minutes at -55°C and 15 minutes at 125°C. Electrical functionality was verified on the Sentry tester at intervals of 100, 250, 500, 750, and 1000 cycles.

The 85/85 THB stress test was conducted in a temperature-humidity chamber for 1000 hours. Test boards were mounted on a flat aluminum plate with the wirebond side exposed to the environment. A power supply external to the chamber provided bias voltage to the boards through cables. The interior chamber temperature, the power supply voltage and current of each board were periodically monitored by a data logger. At intervals of 100, 250, 500, 750, and 1000 hours, the specimens were removed from the humidity chamber. After a moisture bake-out inside another chamber, the boards underwent electrical functionality tests at 0, 25 and 85°C on the Sentry tester.

A total of eleven DRAM boards were fabricated and covered with a combination of die coating materials with or without a final conformal coating. The combinations of the coating materials are listed below:

1. Parylene/FP4402
2. Parylene/FP4450
3. Parylene/Si_3N_4

4. Parylene/Silicone/Si_3N_4
5. FP4402/Si_3N_4
6. FP4450/Si_3N_4
7. Silicone/Si_3N_4
8. Parylene/Silicone
9. No Coating

Six of the eleven boards were subjected to the vibration plus temperative cycling test sequence; the remaining five were exposed in the THB environment.

Table 1 shows the triple track die coating test matrix. The sample triple track dice, some originating from wafers with P-glassivation and others from unpassivated wafers, were assembled into standard microelectronics packages by the JHU/APL microelectronics assembly section. A standard 40 pin dual-in-line package for which electrical test sockets are readily available was selected. The die to package electrical interconnects are made with 25 μm diameter gold wire using a thermosonic ball bonder following normal wirebonding practices. All samples were then subjected to non-destructive bond pull test, visual inspection, and initial electrical test.

To minimize recontamination with moisture the encapsulant was applied within 2 hours after removal from a vacuum bake oven. The encapsulant material was manually applied in a class 10,000 clean room environment. All devices were then electrically retested. Note that Si_3N_4 was not included in the triple track test matrix while, in contrast, parylene by itself was not included in the DRAM test.

We conclude this section with a note on acceleration factors and environmental simulation. Since there is no moisture in space, the THB environment has no direct analog unless hardware were to sit on the ground for a prolonged period prior to launch. Acceleration factors can be calculated for the humidity and temperature but that is not the point of this discussion. The vibration test is designed to conservatively bound possible launch conditions so we need to consider the subsequent temperature cycling environment in the qualification sequence. An acceleration factor (AF) of

$$AF = (\Delta T_1/\Delta T_2)^q \qquad \text{(Eq 1)}$$

has been determined by Dunn and McPherson [Ref. 4] for failure modes such as fractured intermetallic bonds, chip-out bonds, shear stress induced failures and stress induced matching and voiding failures. The first three failure modes give uniform acceleration factors but the fourth does not. The number of temperature cycles to failure for several temperature ranges was compared for each of the four failure modes in Reference 4.

Table 1
Triple Track Die Coating Test Matrix

Test Sample	First Coating	Second Coating	Test	Note
Un-passivated die	FP-4450	None	85°C/85% RH THB	
Un-passivated die	FP-4450	Parylene	85°C/85% RH THB	
Un-passivated die	FP-4402	None	85°C/85% RH THB	
Un-passivated die	FP-4402	Parylene	85°C/85% RH THB	
Un-passivated die	Hipec Q1-4939	None	85°C/85% RH THB	Silicone filled
Un-passivated die	Hipec Q1-4939	Parylene	85°C/85% RH THB	
Un-passivated die	Parylene	None	85°C/85% RH THB	
Un-passivated die	None	None	85°C/85% RH THB	Control sample
Die with 7000 Å glassivation	FP-4450	Parylene	85°C/85% RH THB	
Die with 7000 Å glassivation	FP-4402	Parylene	85°C/85% RH THB	
Die with 7000 Å glassivation	Hipec Q1-4939	Parylene	85°C/85% RH THB	
Die with 7000 Å glassivation	Parylene	None	85°C/85% RH THB	
Die with 7000 Å glassivation	None	None	85°C/85% RH THB	Control sample
Die with 7000 Å glassivation	FP-4402	Parylene	-55°C to +125°C	
Die with 7000 Å glassivation	FP-4450	Parylene	-55°C to +125°C	
Die with 7000 Å glassivation	Hipec Q1-4939	Parylene	-55°C to +125°C	

These failure modes are designated as low cycle (<10,000) fatigue failures due to repeated stresses of thermal origin. Low cycle fatigue data is described by the Coffin-Manson law relating the plastic strain range of metals to the number of cycles to failure. The plastic strain range is proportional to the temperature range raised to some power (References 5 and 6).

For the first two bond failure modes mentioned above the exponent q is in the range between 4 and 7. Schultz and Gottesfeld (Ref. 7) state that although their investigations show that q can vary, a value of q = 4 is most applicable to bond wire fatigue failure. ΔT_1 is the range of the temperature in the cycling test; ΔT_2 is the range of base plate temperature for the spacecraft application.

$$\text{For } \Delta T_1 = 125 - (-55) = 180°C$$

$$\text{and } \Delta T_2 = 55 - (-30) = 85°C$$

typically we find using Eq. 1 that

$$AF = (180/85)^4 = 20$$

Thus, the 1000 cycle temperature cycling test simulates 20,000 cycles in space, e.g., for 90-110 minute low Earth orbits, this test represents 3.5-4.2 years. The mission time simulated is even greater for deep space missions during which there is a minimum of planetary shadowing and angles to the Sun are controlled.

5. TEST RESULTS

The FAD board was basically a manufacturability demonstration vehicle. Limited THB testing produced problems related to cleanliness issues during fabrication and handling.

For the COB DRAM boards, all but one coating combination passed the vibration test. The lone failure, parylene/silicone was functionally intermittent. The same boards that underwent vibration testing were temperature cycled. The two samples of the parylene/silicone/Si_3N_4 combination were completely non-functional after just 80 and 100 cycles. At 280 cycles, the parylene/silicone failed all electrical functionality tests. After the midpoint of 500 cycles, one parylene/FP4402 circuit failed at room and high temperature while still exhibiting some functionality in several die layers at cold temperature. The same circuit would subsequently fail complete electrical functionality after 780 cycles. Five of the 10 samples completely passed electrical tests after 1000 cycles. The successful combinations were FP4450/Si_3N_4, parylene/FP4450, and the second parylene/FP4402 sample.

A total of nine coating combination samples were used in the 85/85 test. The control sample with no coating was completely non-functional after 150 hours, as was the parylene/Si_3N_4 combination. All die layers failed electrical functionality for the circuits covered with Si_3N_4 only and silicone/Si_3N_4 die coating materials. The parylene/silicone had a bad die layer at 150 hours but otherwise remained mostly functional at 1000 hours. The only coating combinations that successfully completed the 85/85 test are parylene/FP4402, parylene/FP4450, and FP4402/Si_3N_4. There was exactly one coating combination for which all test samples passed all environmental tests – parylene/FP4450.

In summary, the DRAM board testing found (1) that the parylene over epoxy combination was preferred; (2) that combinations with silicone could not survive extensive temperature cycling due to the high TCE of silicone and (3) that the thin, inorganic silicon nitride coating was not uniform enough to offer adequate environmental protection under adverse circumstances.

Since the silicon nitride coating failed to perform well in THB, it was not included in the triple track chip test matrix (Table 1). Both parylene/epoxy combinations successfully passed the 1000 temperature cycle test; all silicone coated combinations failed in a confirmation of the DRAM board test result. Open circuits on silicone coated triple track die began to occur after 250 cycles. The number of wire bond failures increased as the test progressed reaching 86% after 1000 cycles. Broken wire bonds were observed and photographed (Figure 4).

The THB test results are divided into two groups: one with conventionally passivated (7000 Å glassivation) and a second with unpassivated die designed to evaluate just the applied coating(s). For the passivated dice the uncoated control samples failed after 250 hours exposure while all



Figure 4
Photograph of a Broken Wire Bond on a Silicone Coated Die

samples coated with epoxy (parylene/FP4402, parylene/FP4450), silicone (parylene/Q1-4939) and parylene by itself readily survived 1000 hours.

For the unpassivated die, the uncoated control sample failed immediately and only one coating combination, parylene/FP4402, survived without any failure for the complete 1000 hours. A scanning electron microscopy inspection revealed widespread corrosion on die surfaces and bond pads producing open and lifted wire bonds.

6. CONCLUSION

Parylene/epoxy coating combinations have proved to be qualifiable candidates for reliability without hermeticity in COB technology. The parylene/FP4450 combination was superior in temperature cycling since one parylene/FP4402 DRAM board failed (a second replicate sample passed). Failure analysis is in progress for the first parylene/FP4402 DRAM sample since it did survive 250-500 temperature cycles and we are unsure of the cause of failure. The parylene/FP4402 combination was superior in THB since it completely protected even unpassivated triple track die.

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