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Chip-On-Board Technology 1996 Year-End Report

(Design, Manufacturing, and Reliability Study)

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EXECUTIVE SUMMARY

The current increased industry emphasis on smaller, faster, and cheaper space missions has initiated an internal effort at The Johns Hopkins University Applied Physics Laboratory (JHU/APL) to develop a process for flight electronic hardware miniaturization. The miniaturization design effort began in 1994 and continues through 1996 with the objective of establishing a well-defined process to support miniaturized flight electronics. Figure 1 summarizes the progress of this study.

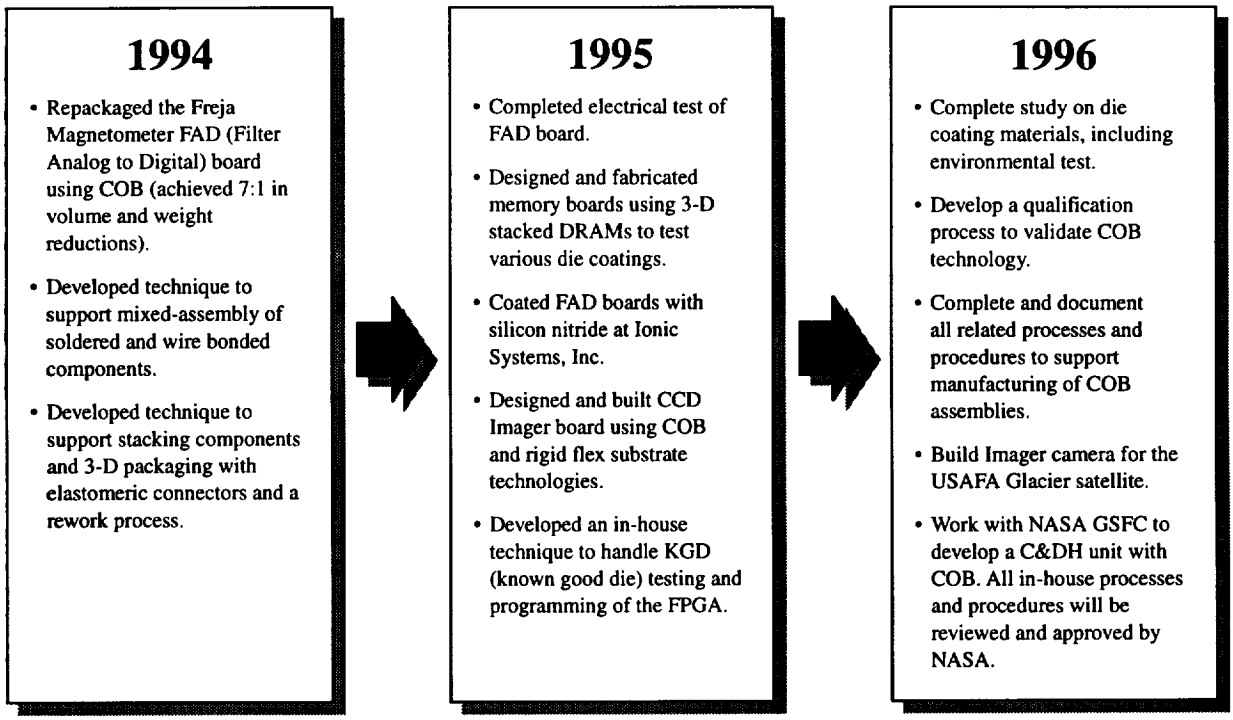


Figure 1
Chip-on Board (COB) Progress Summary

1994 Study

During the first year, the research study focused on completing one filter analog to digital (FAD) board assembly of the Magnetometer Signal Processor. This board was selected because it was the most complex board design that included both digital and analog devices. The objective of the study was to demonstrate that even without an optimized electronic circuit re-design, the new packaging approach would provide significant weight and volume reduction by at least a factor of four. Also, minimizing cost meant that the design must be re-workable and should permit circuit modifications during design iterations.

With the advent of known good die (KGD) technology and availability of KGD parts, the project objectives were achieved using the chip-on-board (COB) technology. The COB technology significantly reduced the weight and volume of electronic subsystems with the elimination of device packages. The FAD has been re-designed and has demonstrated that significant improvement in size and weight (by almost an order of magnitude) can be realized.

The only changes in this re-design were the use of COB technology and the three-dimensional modular packaging technique employing elastomeric connectors. Table 1 summarizes the results of the study and Figure 2 provides a comparison of the new packaging design versus the current design in the Freja Magnetometer.

Table 1
FAD Weight and Volume Summary

Component	Volume (cm^3)	Weight (kg)
FAD old design	1,360	1.01
FAD new design with COB	297	0.22
Signal Processor (old design)	4,500	3.06
Signal Processor (COB design - Estimate)	661	0.68

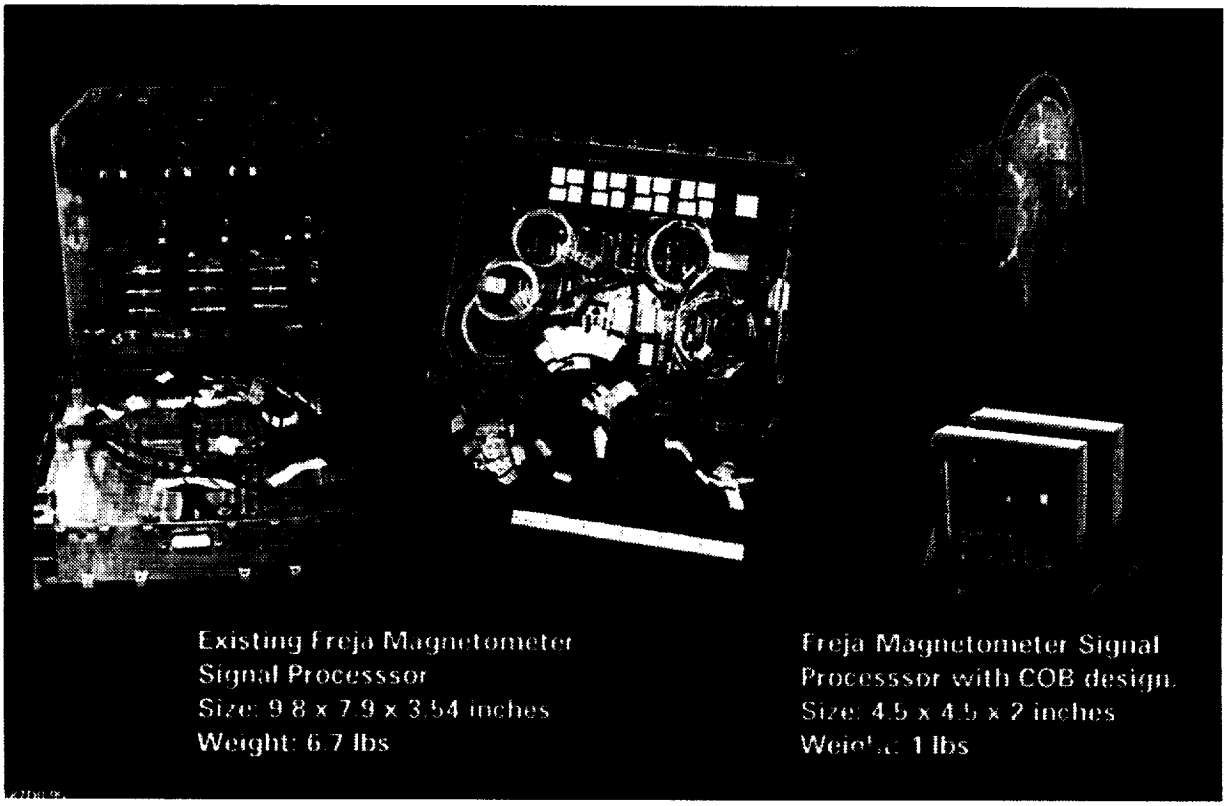


Figure 2
Photograph of the Freja Magnetometer Signal Processor

1995 Study

In the second year of the COB project, die coating material evaluation was the main focus for the research study. Die coating material is an extremely important aspect for the COB technology. It provides protection for bare dice during manufacturing, handling and throughout all flight environments. The optimum coating must also be re-workable to ensure the viability of low-cost satellite electronic designs. Several candidate materials were selected as a result of

years of extensive research in the automotive, military, communication, computer and space industries.

A test DRAM board with a 3-D stacked DRAM module from Irvine Sensors as shown in Figure 3 was used to support this study. Using stacked bare dice further miniaturizes electronic hardware, since it would only occupy the otherwise wasted area in the vertical direction. During the same year, another IR&D project was initiated to design a low-power, miniaturized CCD camera using an application specific integrated circuit (ASIC) that is easy to customize for specific science mission objectives. To support this design, COB technology was used and a technique to test bare dice was developed as shown in Figure 4.

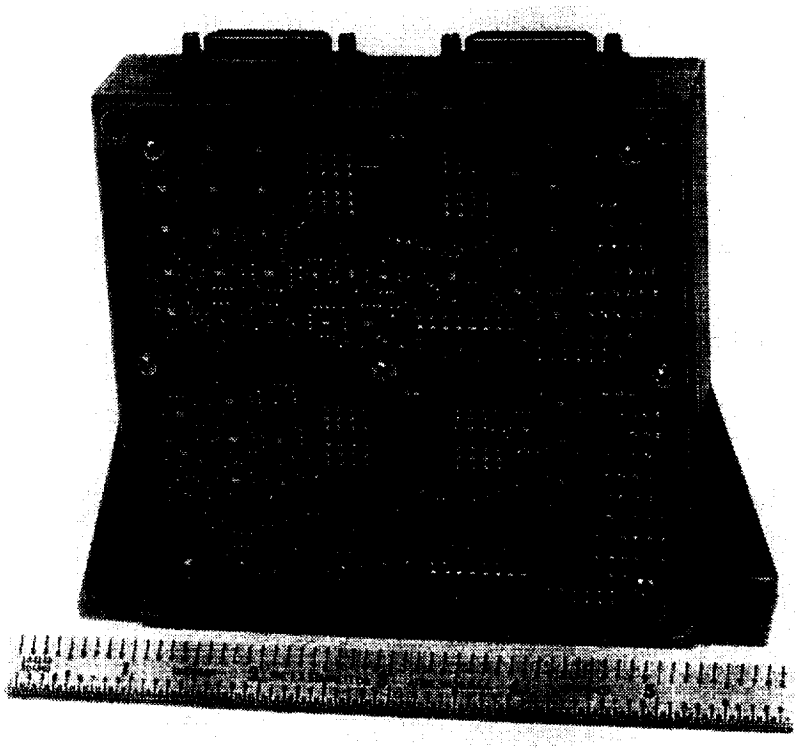


Figure 3
Photograph of the Memory Board with Stack DRAMs

1996 Study

In 1996, environmental testing consisting of dynamic loads test, a temperature cycling test, and an 85°C/85%RH temperature humidity bias (THB) test were performed to evaluate the reliability of COB for long-term satellite applications. This study was supported by a JHU/APL IR&D fund and a grant from NASA GSFC. Other activities related to COB technology included the development of a scientific miniaturized CCD camera to be flown on the Glacier USAFA satellite in 1997 (Figure 5), and the *"C&DH in your palm"* funded by NASA GSFC.

This report presents the lessons learned and environmental test results of an ongoing study to qualify COB technology for flight. Specifically, a COB version of the FAD board, test boards containing 3-D stacked DRAM memories and other bare dice covered by various combinations of die coatings, and triple track chips were the test vehicles employed. Test results

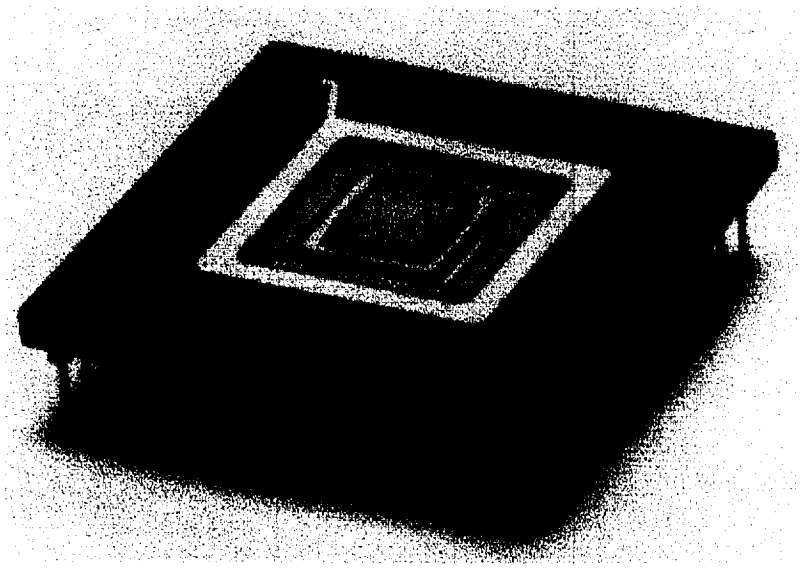


Figure 4
Photograph of Low Cost Bare Die Testing Developed at JHU/APL

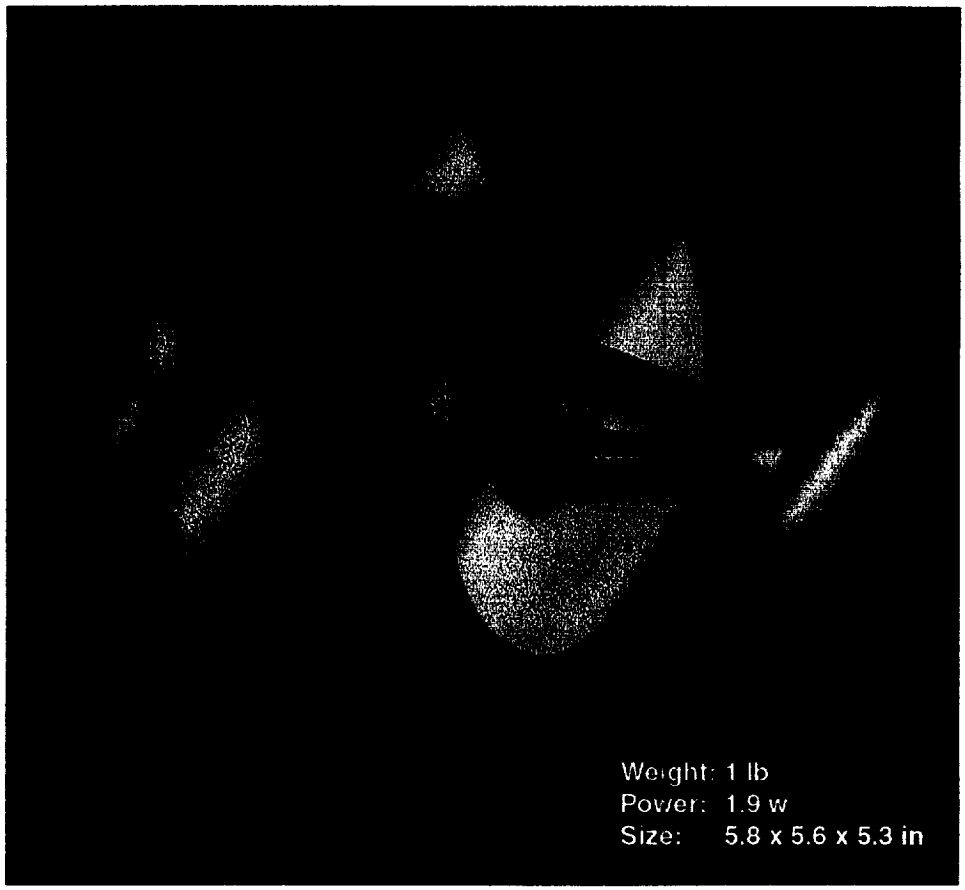


Figure 5
Conceptual Design of the Glacier Imager

obtained so far have shown that physical miniaturization is possible in light of the FAD board developed using COB technology which achieved a reduction in volume and weight by a factor of at least seven. The board was debugged and electrically tested and exhibited an electrical performance comparable to that of the original discrete, packaged-device design. Having proven the manufacturability of COB hardware, the test DRAM boards were designed and built to flight qualify the technology and to determine the best die coating material in terms of its effectiveness as a moisture barrier. Out of five candidate coating material combinations selected for this study based on their reputation and usage heritage, only one – parylene/FP4450, survived all stresses due to vibration, temperature cycling, and 85°C/85% RH temperature humidity bias (THB) accelerated environments. The triple track chips, which are designed for a supplementary corrosion study, are showing similar temperature cycling results.

Implementing COB technology requires some minor changes to the current process with packaged parts. This new packaging technology requires a controlled environment to avoid problems resulting from handling (the failure of the FAD board in the 85°C/85% RH test is a direct consequence of the handling problem) that may cause damage to the bare dice and the wirebonds interconnecting them. Controlled environments include many standard items that are being used at the JHU/APL for actual flight hardware such as protective covers for the COB assemblies, controlled ambient conditions for die storage with purged nitrogen, protective clothing for personnel, electrostatic discharge ESD protection, and laminar flow work benches. The COB technology with wire bonding technique uses existing hybrid technology that is being supported by numerous vendors and is fully supported by the existing facilities at JHU/APL.

The main attractive features of COB over other miniaturized technologies are the low cost and the re-workability. COB provides an improvement in size many times better than the existing technologies with packaged parts. Also, the shorter signal paths associated with miniaturized COB hardware enhance circuit performance. Elimination of packaged parts improves the reliability since it reduces the number of interfaces (component pins) between the parts. Finally, smaller and better electronic hardware will provide additional space for more instruments aboard a satellite thereby broadening mission objectives, and require potentially smaller launch vehicles resulting in a lower overall mission cost.

A summary of significant test results from this COB study is as follows:

(1) All COB assemblies with various coating combinations successfully passed the dynamic loads environment shown in Table 16.
(2) Silicone, either by itself or in combination with another type of coating such as parylene or silicon nitride, consistently failed temperature cycling as evidenced by the poor performance of the silicone-covered DRAM boards and the triple track dice.
(3) Ionic Systems' silicon nitride coating process is not compatible with the internal JHU/APL manufacturing process. Delamination and peeling of the coating were observed on silicon nitride covered DRAM boards.
(4) Only one coating combination, parylene/Hysol FP4450 successfully completed dynamic loads, temperature cycling and 85°C/85% RH tests (see the section on DRAM Boards for detailed information on the environmental conditions). The other coating material combinations either passed the temperature cycling or the 85°C/85% RH test but not both (this report provides details).

1.0 INTRODUCTION

The major impetus for flight qualifying COB packaging technology is the shift in emphasis for space missions to smaller, better, and cheaper spacecraft and satellites resulting from the NASA New Millennium initiative and similar requirements in DoD-sponsored programs. The most important benefit that can potentially be derived from miniaturizing spacecraft and satellites is the significant cost saving realizable if a smaller launch vehicle may be employed. Besides the program cost saving, there are several other advantages to building COB-based space hardware. First, once a well-controlled process is established, COB can be low cost compared to standard multi-chip module (MCM) technology. This cost competitiveness is regarded as a result of the generally greater availability and lower cost of known good die (KGD). Coupled with the elimination of the first level of packaging (chip package), compact, high-density circuit boards can be realized with printed wiring boards (PWB) that can now be made with ever-decreasing feature size in line width and via hole. Since the COB packaging technique in this study is based mainly on populating bare dice on a suitable multi-layer laminate substrate which is not hermetically sealed, die coating for protection from the environment is required. In recent years, significant improvements have been made in die coating materials which further enhance the appeal of COB. Hysol epoxies, silicone, parylene and silicon nitride are desirable because of their compatible thermal coefficient of expansion (TCE) and good moisture resistant capability. These die coating materials have all been used in the space and other industries with varying degrees of success. COB technology, specifically siliconnitride coated hardware, has been flown by Lockheed on the Polar satellite. In addition, DARPA has invested a substantial amount of resources on MCM and COB-related activities recently. With COB on the verge of becoming a dominant player in DoD programs, DARPA is increasing its support of the availability of KGDs which will help decrease their cost.

Aside from the various major developments and trends in the space and defense industries that are favorable to the acceptance and widespread use of COB packaging technology, implementing COB can be appealing in other aspects. Since the interconnection interface is usually the weak link in a system, the overall circuit or system reliability may actually be improved because of the elimination of a level of interconnect/packaging at the chip. With COB, mixing packaging technologies is possible. Because some devices are only available in commercial plastic packages, populating a multi-layer laminate substrate with both bare dice and plastic-package parts is inevitable. Another attractive feature of COB is that re-workability is possible if die coating is applied only on the die top. This method allows local replacement of individual dice that were found to be defective instead of replacing an entire board. In terms of thermal management, unpackaged devices offer a shorter thermal resistance path than their packaged counterparts thereby improving thermal sinking and heat removal from the parts.

2.0 COB TECHNOLOGY

COB technology utilizes the interconnections of bare dice on a substrate without the need for the component's package. Eliminating the component package reduces the required substrate area and assembly weight. Information from Table 2 indicates that the area occupied by a bare die is much less than that required by a packaged part. The area saving can be as much as 90% in some cases. With the conventional high density printed wiring board and standard wire bonding technology, COB technology can yield a factor of at least ten in weight and

Table 2
Area of Bare Chip in Standard Ceramic Single Chip Packages

Package Type	Pin Count (Pitch in 10^{-3} in)	Outside Package Dimension (in)	Max. Cavity for Bare Chip (in)	Bare Chip Area in Package (%)
PGA	68 (100)	1.10 x 1.10	0.55 x 0.55	25
	84 (100)	1.10 x 1.10	0.47 x 0.47	18
	100 (100)	1.32 x 1.32	0.50 x 0.50	14
	132 (100)	1.40 x 1.40	0.45 x 0.45	10
	208 (100)	1.77 x 1.77	0.45 x 0.45	6
LCC	24 (50)	0.40 x 0.40	0.27 x 0.27	46
	32 (50)	0.55 x 0.55	0.39 x 0.39	46
	68 (50)	0.95 x 0.95	0.63 x 0.63	44
	84 (50)	1.15 x 1.15	0.70 x 0.70	37
	100 (50)	1.35 x 1.35	0.39 x 0.39	8
QFP	24 (50)	0.40 x 0.40	0.28 x 0.28	49
	32 (50)	0.40 x 0.40	0.26 x 0.26	44
	68 (50)	0.95 x 0.95	0.50 x 0.50	28
	84 (50)	1.15 x 1.15	0.47 x 0.47	17
	132 (50)	0.95 x 0.95	0.40 x 0.40	18
SOJ	28 (50)	0.72 x 0.43	0.60 x 0.35	60
	32 (50)	0.83 x 0.42	0.65 x 0.27	50
DIP	24 (100)	1.20 x 0.61	0.65 x 0.43	38
	32 (100)	1.60 x 0.31	0.56 x 0.22	25
	48 (100)	2.40 x 0.61	0.49 x 0.40	13
	64 (100)	3.20 x 0.91	0.55 x 0.43	8

volume saving. Using bare dice, rather than a packaged device, can accommodate more components on a given board area, thus reducing the inductance created by the next level of interconnection between components. It also reduces the thermal resistance and the number of interfaces between the active die and the substrate (i.e., the package pins). This can potentially improve the speed of the circuit and the reliability of the design.

In theory, there is no distinct difference between MCM and COB technologies. In practice, MCM is often related to a smaller substrate with fewer active dice as compared with COB design. MCM technology is being supported by many companies. Major industrial consortiums have been formed under the auspices of DARPA in search of low-cost, quick turn-around substrates for MCM technology. Three major substrate technologies for MCM are: MCM-D, MCM-C and MCM-L. MCM-D provides the highest density in substrate design since it uses thin film processes to deposit metals and dielectric layers on a variety of rigid bases. MCM-C provides moderate density in substrate design. It uses thick film technology to form conductive patterns on ceramic or glass ceramic materials. MCM-L uses laminate structures and employs printed wiring board (PWB) technology to form conductive patterns over reinforced dielectric laminates. Conventional PWB technology with the etching process can provide a 0.005 in. feature size. To date, with the development of the additive process in the PWB technology, laminated substrates can have very fine line widths and spacing features as small as 0.004 in. These characteristics along with low cost make MCM-L technology very popular and attractive process. Figures 6, 7 and Table 3 provide a comparison for various MCM technologies.

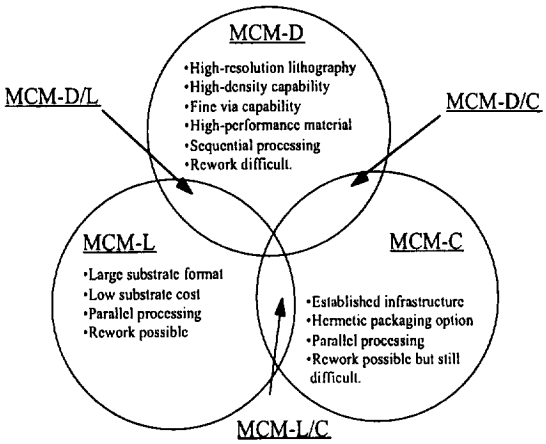


Figure 6
MCM Technologies Summary

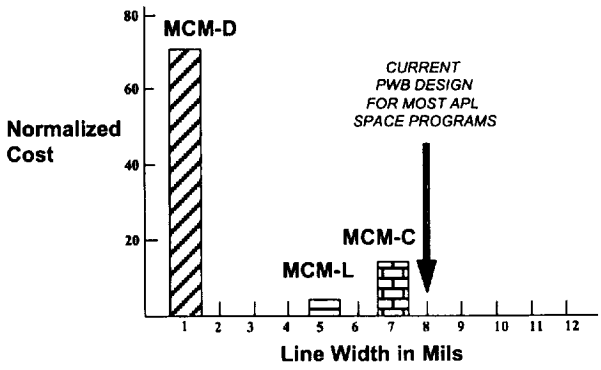


Figure 7
Density and Cost for Various Technologies

Table 3
MCM Substrate Technologies

Conductor Width (10^{-3} in)	Connectivity Level (# of conductors/in^2/level)	Technology
10	50	Normal thick film hybrid
5	100	Best thick film hybrid
4	50-70	Best printed wiring board
4	60-80	Multiwire
2.5	160	Microwire
2	250	Thin film polyimide

COB technology is very much similar to MCM-L technology. It supports the use of both conventional soldered components and bare dice on a laminate dielectric substrate. COB offers more weight and volume saving than MCM-L since it eliminates the intermediate substrate and pins of a MCM-L device. It supports re-work and rapid prototyping without the need to complete intermediate MCM devices. These are the major characteristics and potential advantages of COB over MCM technology. Figure 8 provides a schematic comparison between the COB, MCM and single-chip package technologies.

Implementing COB technology does not require dramatic changes in the manufacturing process. In fact, at JHU/APL, existing hybrid technology is already in place and has produced a substantial amount of reliable flight hardware in the past. Supporting laminated "soft" substrates in the COB design only requires minor modifications in setting up the wire bonding parameters. Current standard SMT technology at JHU/APL can also be extended to support the mixed technology with both COB and SMT components. These reasons serve as a basis for the Space Department to commit IR&D funds for investigating the miniaturization of flight electronics using COB technology. The following sections provide detailed discussions of KGD, substrate materials, die attachment and processes that ultimately effect the reliability of the COB technology.

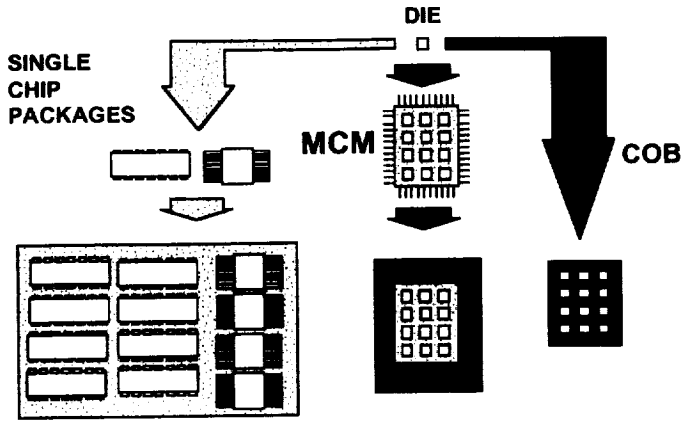


Figure 8
Comparison of Various Packaging Technologies

2.1 KNOWN GOOD DIE (KGD)

Success in design and manufacture of COBs and MCMs, whether for telecommunication, space, or military applications, starts with fully tested die or KGD. The COB or MCM yield depends on the chip yield and the number of chips in the design. In theory, the statistical yield of a COB assembly Y_m versus the chip yield Y_c and the number of chips Nc is given by the equation:

$$Y_m(\%) = 100\ (Y_c)^{Nc}$$

Figure 9 illustrates the significant impact of KGD on COB technology. This figure, however, only represents the theoretical statistic of the COB assembly without considering the maturity of the die technology and the re-work variables. Recent studies from the industry reveal that the yield for common components such as SRAMs, DRAMs and glue logics can exceed the 99.5% level. In addition, re-workability of COB technology would increase the potential yield of the final assembly to an acceptable level to meet the low cost and high reliability requirements for space electronics.

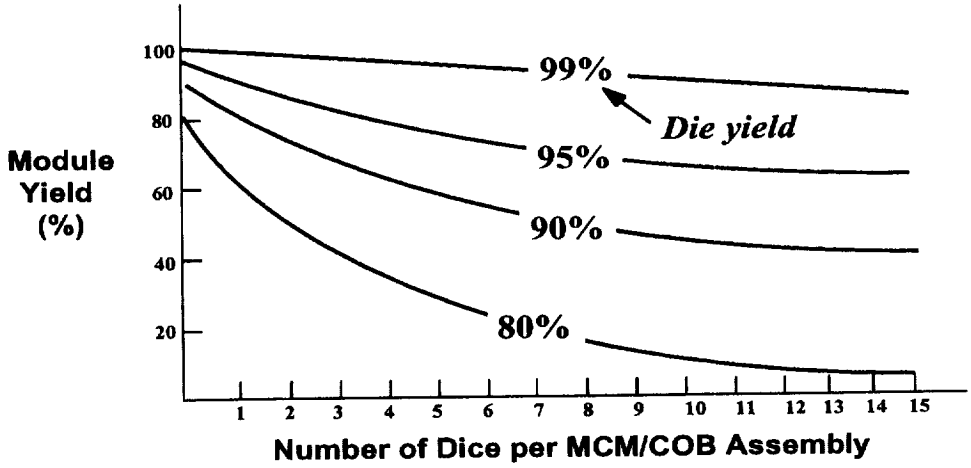


Figure 9
KGD Versus COB Module Yield

Since the early 90s, many commercial companies and government agencies have been seriously and actively searching for ways to maximize COB and MCM yield (Table 4). To date, KGDs can be purchased from various semiconductor companies. Other companies also provide services and tools for testing KGDs. Three main test technology categories currently available to support the KGD process are described in the following sections.

Table 4
List of KGD Suppliers

Company	Functional and DC Parametric Test	At Speed and At Temperature Test	Full KGD with Burn In
Advanced Micro Devices	x	x	
Allegro Microsystems	x		
American Microsystems	x	x	
Analog Devices	x	x	
Calogic	x		
Chip Express	x		
Chip Supply	x	x	x
Cypress Semiconductor	x		
Device Engineering	x	x	
Elmo Semiconductor	x	x	x
Eltek Semiconductor	x		
Harris Semiconductor			x
IBM Microelectronics	x		x
Integrated Device Technology	x		x
Intel		x	x
LSI Logic	x		
Micron Semiconductor	x	x	x
Minco Technology Labs	x		
Motorola	x	x	x
National Semiconductor	x	x	x
Rood Test House	x	x	x
Semi Dice	x		
SGS Thomson	x	x	
TI	x	x	x
Vitesse Semiconductor	x	x	
VLSI Technology	x	x	

2.1.1 Minimal Package Method

In this technique, the die is temporarily assembled in a sacrificial carrier. After the completion of all tests, the die will then be removed for the next assembly process. This technique is similar to the soft connection method described below. The main difference is that when the die is removed from the test carrier, only one end of the die wire bonds or ribbons will be cut. The die and its wire bonds or ribbons will then be single-point attached to bond pads in the final substrate. Table 5 describes several approaches for this method.

Table 5
Minimal Package Method[1]

Company	Description
Chip Supply	Traditional TAB chip on tape is available.
Hughes Aircraft	Testable Ribbon Bonding (TRB): Dies are ribbon bonded into low-cost carriers for burn-in and test. After the test, the ribbons are cut leaving a TAB-like die which can be single-point bonded into its final application.
Micro SMT	Wafer level die packaging technology. Silicon posts are formed in wafer scribe lines.
Northern Telecom	Dies are wire bonded into low-cost carriers for burn-in and test. After the test, the wires are cut leaving the die with stub wires bonded to each pad, which can be single point bonded to its final application.
Tessera	Flex circuit is used to route center or peripheral die bond pads to an array of nickel/gold bumps. An elastomeric layer provides compliance. The die array is temporarily attached to a PGA style carrier for burn-in and test and then removed. The die may then be flip chip array bonded into its final application.

2.1.2 Temporary Contact Method

Micro connectors in a compliant medium provide interconnection under pressure between the die and the pin-out of a re-usable carrier to support die testing. Once the electrical testing is completed, the die will be removed for the next assembly operation. This method requires a high degree of accuracy within the fixture to align with the die bonding pads. It is most useful in cases (e.g., production environment) where there is a large quantity of the same die to be tested. Table 6 provides details of this technique.

2.1.3 Soft Connection Method

In this technique, the die is temporarily assembled in a sacrificial carrier. After the completion of all tests, the die will then be removed for the next assembly process. This method is simple and can be used to support low volume production with a large variation in die types. Table 7 and Figure 10 provide details of this technique. This technique is used in the Glacier camera to test the ASIC bare die. In the "C&DH in your palm" project, a similar technique with *Snap-Strate* design will be used for testing bare FPGA dice.

2.2 PWB TECHNOLOGY

There are many different types of materials that can support COB technology. Typical PWB materials are FR4 epoxy glass, polyimide glass, bis-maleimide triazines (BT), cyanide ester, polyimide Kevlar or material with metal core. Among the various types of materials, FR4 is by far the most commonly used resin material in the electronic industry. However, due to its low glass transition temperature (Tg), polyimide resin material is more preferable for high reliability applications. Tg is the temperature at which the phase of the material changes to a gel-like substance. During this phase change process, the coefficient of expansion can increase by an order of magnitude which may impose excessive thermal stresses on dice and other on-board components. Other important factors to consider in selecting a suitable PWB technology include the compatibility with the thermal expansion and the water absorption of the board material. Polyimide Kevlar material, while offering a compatible TCE of 8-10 ppm/°C versus 2-3 ppm/ °C of the silicon die, has a high water absorption characteristic. This undesirable

Table 6
Temporary Contact Method[1]

Company	Description
Acsist Assoc.	Contact to die is made with a micro particle interconnect.
Aehr Test System	Nitto Denko's ASMAT polyimide film provides electrical contact between the die and uniquely designed carrier. Die are mechanically aligned.
California Contact	Electrical contact is made with a traditional scrubbing action by microbeams, which are individually cantilevered. Dies are placed directly into sockets on burn-in boards without the use of a carrier.
Fresh Quest	A scrubbing technology on a thin film membrane is used to make contact between the die and the carrier. This technology is limited to peripheral bond pads.
IBM	Palladium dendritic structures are used to make contact to C4 solder bump chips.
MCC	Reusable TAB tape with inner-leads bent upward and embedded in silicone elastomer provide normal force, compliance, and scrubbing under z-axis deflection. Usable with JEDEC standard TAB slide carriers and sockets for burn-in.
Micron Semi KGD plus	A family of reusable, socket-able, universal carriers is used to provide known good die. Specific information is limited.
Packard Hughes	Bumped flex carrier with gold dot microprobes is used with an elastomer backing, a spring clamp, and a support plate/heat spreader.
Plastronics	The carrier consists of a plastic base with a cavity for the die, a ceramic alignment plate with precision laser drilled holes for aligning wire probes to the die bond pads, and a contactor assembly which contains the probes. The compliant probes provide scrubbing contacts and the ability to accommodate non-planar surface.
Qualhi	Gold bumps are formed on thick film carriers by bonding gold ball bonds to the carrier; the wires are broken off and the remaining balls are planarized. Dice are placed in contact with the carriers using a flip chip bonder which provides enough scrubbing action to break through the oxide without forming an actual bond.
Sandia	Wafers are processed to reposition the normal peripheral bond pads of each die to an area array of much larger pads on top of the die to allow easy mechanical alignment to a pad array in a universal carrier. The die to carrier interface can be z-axis elastomers or diamond particle membranes.
TI/MMS	Pressure contact carrier uses copper/polyimide interconnect and proprietary non wiping contacts. Die self aligns to carrier.
Tribotech	Either face-up or face-down versions of this carrier are available. A proprietary, non scrubbing, fine point piercing method is used to contact the die and make contact to the thin film interconnect.
Yamaichi	Nitto Denko's ASMAT polyimide film material provides electrical contact between the die and a carrier.

feature will make cleaning of the board more difficult. Cyanide ester resin seems to be the most desirable material with excellent characteristics in water absorption, in TCE, and in dimensional stability. However, it is the most expensive PWB material and there are very few vendors who can support this technology. These are the rationales for the selection of the polyimide PWB material for the COB study. Table 8 provides detailed information on various PWB materials.

Table 7
Soft Connection Method[1]

Company	Description
Chip Supply	Soft Tab Process: TAB tape frame is fabricated and lightly attached to gold bumped bond pads on the die. After burn-in and test using TAB equipment, the tape frame is removed.
Elmo Semiconductor	Wafers are coated with barrier material, bond pads are reformed for larger bond area. The dies are packaged with thermoplastic die attach and wire bonded into a temporary reusable carrier. Following burn-in and test, the wire bonds are cut and the dies are removed.
GE	Die are coated with a protective polymer and via holes are laser drilled to the bond pads. Temporary bond pads are formed on the overcoat and are used to wire bond die into a standard package. After burn-in and test, dies are removed from the package and temporary bond pads are etched away.
IBM	Reduced Radius Removal (R3): Solder bumped dies are reflow attached to reduced radius pads on a reusable ceramic substrate. Dies are removed from carrier with a shearing process after burn-in and test.
Micron Soft Tool	Temporary die attached and "soft" wire bonds are used to place the die into a standard package. After burn-in and test, the "soft" wire bonds are pulled away from the bond pads and the die is removed from the package.
MCNC	Solder bumped dies are attached to a reusable multi-layer ceramic carrier using a sacrificial metallurgical connection. A special process is used to weaken the temporary wire bond and to allow removal of the die after burn-in and test.
n-CHIP	Die-level technology for at-speed burn-in and test employs a temporary package and temporary wire bonds. (This technology gas been identified only recently and no assessment is available.)
Samsung	Conventional wire bond from chip to PC board is made in a multichip carrier. Gold wire is cut from bond pad with proprietary tool. (This technology has been identified only recently and no assessment is available.)

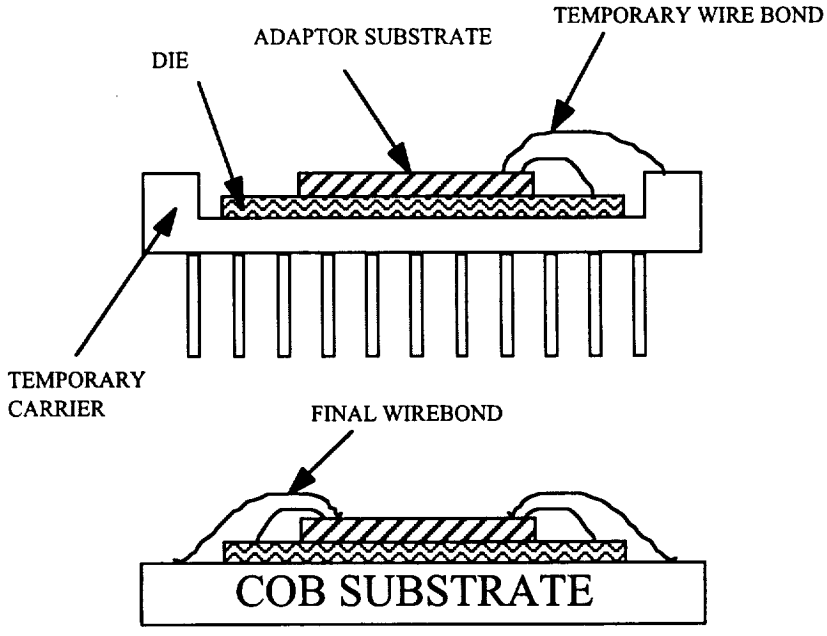


Figure 10
Low Cost Bare Die Testing Technique

Table 8
PWB Material Characteristics[6]

	Tg (°C)	X-Y CTE (ppm/°C)	Z CTE (ppm/°C)	Dielectric Constant (@1MHz)	Dim. Stability (%)	Water Absorption (%)	PWB Cost (vs. FR-4)
FR-4 E-Glass Fabric/Epoxy	170	15-18	60	4.5	0.04	0.2	1X
E-Glass Fabric/ Polyimide	250	13-16	45	4.3	0.04	0.35	1.25X
S-Glass Fabric/ Cyanite Ester	230	10-12	40	3.5	0.03	0.05	2X
Kelvar® Aramid Fabric/Epoxy	170	8-10	130	3.9	0.06	1.0	1.0
Thermount® Aramid Nonwoven Polyimide	250	8-10	110	3.9	0.03	1.0	1.5X

2.3 DIE ATTACH TECHNOLOGY

The choice of die-attach technology is an important consideration when examining the option of using dice in a design. There are many techniques for die attachment as listed in Figure 11, but the two most common techniques are wire-bonding and flip-chip, which is also known as controlled-collapse chip connection (C4). Flip-chip die bonding requires that the die has solder bumps placed on its bond pads. The IC vendor or a third party who specializes in this process can add this feature onto the die. In the flip chip process, the die is placed on the PWB with the circuitry of the IC facing the board. The solder bumps are then reflowed, providing both mechanical and electrical connection to the PWB. During the solder reflow process, surface tension of the solder material provides self alignment of the die with respect to the PWB in case there is an alignment mismatch during assembly. This process was invented by IBM in the 1960s. The advantage of this process is that it can significantly increase the number of pin-outs from the die without increasing the die area. After the completion of all tests, a low stress epoxy underfill material is injected underneath the die. This material further strengthens the attachment of the die to the board. It also provides a seal which protects the die from the environment, serving in the same capacity as a package. Re-workability, inspection, die availability, and manufacturing difficulties are still barriers for this die attachment process. Thus, only a few companies currently support this process.

In the case of wire bonding, the die is attached directly to the PWB on its back side and the electrical connection is made using bond wires (Figure 11). The bond wires can be made of aluminum or gold. The process was developed by Bell Laboratories in 1957. It is very similar to that used when placing die in standard chip packages, hybrids or multichip modules. As a result, many companies have standard production lines in place which can support wire bonding assemblies. The wire bonding process does not impose additional thermal stresses on the bond wires. The wires are self supported at both ends. This process supports visual inspection, non-destructive pull test, and re-work. Another advantage is that most dice are available in a form that supports a wire-bond process. Table 9 summarizes various parameters in the wire bonding process.

- WIRE BONDING

- DEVELOPED BY BELL LABS IN 1957
- WELL-KNOWN TECHNOLOGY
- REWORK POSSIBLE
- SUPPORT SMALL-VOLUME PRODUCTION
- DIE READILY AVAILABLE
- DOES NOT SUPPORT VERY HIGH I/O

- FLIP-CHIP
- CONTROLLED COLLAPSE CHIP CONNECTION (C4)
- CONTROLLED COLLAPSE BONDING (CCB)

- DEVELOPED BY IBM IN 1960s
- SHORT SIGNAL PATH
- VERY HIGH I/O
- REWORK, CLEANING, AND INSPECTION ARE DIFFICULT
- SUBSTRATE CTE MUST MATCH DIE CTE
- DIE AVAILABILITY ISSUE

- TAPE-AUTOMATED BONDING (TAB)

- DEVELOPED BY GE IN 1960s
- MOST SUITABLE FOR LARGE VOLUME
- SUPPORT BARE DIE TEST AT IC FACILITY
- MATERIAL AND EQUIPMENT ARE COSTLY AND NOT FLEXIBLE
- DIE AVAILABILITY ISSUE

Figure 11
Die Attach Technologies

Table 9
Wire Bonding Characteristics[7]

Parameter	Thermocompression (Gold Wire)	Automatic Thermosonic (Gold and Aluminum Wire)*	Ultrasonic (Gold and Aluminum Wire)
Develop and Control	Excessive capillary heat may cause annealing of wire and affect the ball formation	Easiest to control	Must control acoustical energy and force
Speed	~20 wires/minutes	~600 wires/minutes	~240 wires/minutes
Current capacity (0.001 in)	~0.55 Amps	~0.55 Amps	<0.40 Amps
Heat required	300-400°C	150°C	None
Acoustic energy required	None	Controllable	Controllable
Force required	Most force required	Less than ultrasonic and Thermocompression	Less than Thermocompression
Direction	Omni (360°)	Omni (360°)	7.5° off true line
Looping	Some control-operator dependent	Best control (machine controllable)	Good control (machine controllable)
Pad size (0.001 in wire)	Ball size dependent wedge size = 1.5X to 5X wire diameter in length and 1.5X to 3X wire diameter in width	Ball size dependent wedge size = 1.5X to 5X wire diameter in length and 1.5X to 3X wire diameter in width	Wedge size dependent width = 1.2X to 2.5X wire diameter length = 1.5X to 5X wire diameter
Bond head clearance	Largest head size maximum clearance required	Smallest head size min clearance required	Largest head size deep access available
Sensitive to contamination	Most sensitive	Less sensitive	Least sensitive
Purple plague	Most prominent	Increases with reduced hermeticity and increased temperature	Increases with reduced hermeticity and increased temperature

*Thermosonic wire bonding using aluminum wire is difficult and not supported by industry.

2.4 DIE COATING

All bare dice have a thin layer of passivation of SiO_2, Si_3N_4 or polyimide material that covers the circuit to provide protection from the environment, with the exception of the bond pads. This passivation is done by the IC foundry at the wafer stage. It requires high temperature and accurate application thickness. Since the bond pads are made of aluminum material, oxidization of the bond pads can easily occur if they are not protected. Therefore, coating materials are extremely important in COB technology. Selection of coating material requires a thorough understanding of the material behaviors. The material of choice must be compatible with the soldering assembly process, since COB technology is often mixed with surface mounted technology (SMT). It should have a TCE similar to that of the bond wire material and a glass transition temperature beyond the expected operating environment to avoid high thermal stresses. The material also must adhere well to the die surface with minimum void and have low ionic content to minimize the possibility of corrosion. Ionic contamination becomes corrosive in the presence of moisture and causes damage to the die structure. Ions can also move around under high electric fields which can cause problems in dense memory chips. In general, five major criteria in the material selection are:

1. TCE should be close to that of the wire material (Gold wire has TCE=14.2 x 10^{-6} in/in/°C),
2. High glass transition temperature (Tg),
3. Low cure shrinkage,
4. Void-free fill over wires and chip,
5. Low ionic contamination content (< 20 ppm Na^+, K^+, Cl^-).

2.4.1 Silicone

Silicones and epoxies are the two major groups of glob-top materials. Both of these materials are used in commercial electronic products. Silicone is a gel-like material. It offers low alpha particle emission, high purity and low modulus of elasticity. Silicone also has very low ionic content and a low water saturation level. On the negative side, silicone's inherently high TCE can cause excessive thermal stresses on wire bonds during temperature cycling.

2.4.2 Epoxy

Epoxy is an opaque glue-like material. It has low ionic content, high glass transition temperature, and high elasticity modulus. It also has a low TCE that is comparable to that of gold wire bonds and provides excellent mechanical protection. Table 10 summarizes the mechanical characteristics of the silicone and epoxy materials selected for this study.

2.4.3 Silicon Nitride

Silicon nitride coating at room temperature is a proprietary process developed by Ionic Systems. It is a plasma enhanced chemical vapor deposition (PECVD) that has existed for many years in the electronic industry. Unlike the conventional silicon nitride deposition in the wafer manufacturing that requires high temperature, this process deposits a uniform inorganic coating to silicon dice in COB assemblies at room temperature. It provides excellent protection against moisture owing to its extremely low moisture permeability. A thin layer of 0.50 μm of

Table 10
Mechanical Properties of Silicone and Epoxies

Material	TCE (in/in/°C)	Tg (°C)	Na+, K+, Cl- (ppm)	Young Modulus (psi)
Hysol FP4450	19E-6	157	2,3,5	
Hysol FP4402	22E-6	155	<20,20,20	
HIPEC Q1-4939 (Silicone)	105E-6/262E-6		2,2	321
Gold	14.2E-6	–	–	

the silicon nitride was used in the Polar satellite design and has successfully met all flight environment requirements. Table 11 provides the permeability comparison between silicon nitride and other die coating materials.

Table 11
Permeability of Various Die Coating Materials

Material	Moisture Permeability g/m²/24 Hr.
Parylene N	23.25
Parylene C, D	3.26-3.88
Epoxides	27.75-36.89
Silicones	68.2-122.45
Urethanes	37.2-134.85
Silicone Nitride	<0.00465

2.4.4 Parylene

There are many different types of parylene material. In this study, parylene C is used. It is a high melting-point, white, crystalline solid material used to provide a uniform conformal coating for electronic assemblies. It is a dimer with the chemical name of Dichloro-di-p-xylene. Parylene is a chemically and mechanically stable material. It is insoluble in all organic solvents up to 150°C and resists permeation by all solvents with the exception of aromatic hydrocarbons. Typical applications of parylene coating have a thickness of about 0.001 inch. The application process is a vapor deposited process that applies a uniform coating material in a free molecular mode under vacuum. Table 12 summarizes the properties of parylene and various materials.

3.0 COB DESIGN AND MANUFACTURE

3.1 DESIGN

COB design is very different from the conventional design. It requires careful planning that must be done early in the process to take into account testability, re-workability, handling protection, material compatibility, and KGD considerations. Unlike the conventional packaged

Table 12
Properties of Various Parylene Materials

Permeability	Method	Parylene N	Parylene C	Parylene D	Mylar	Teflon	Polystyrene
N2	Measured in Dow permeability cell at 25°C in cc (STP) 100 in²/24 hrs., atm.	7.7	1.0	4.5	1.0	75	50
O2	Same	3.9	7.2	32	1.8	150	300
CO2	Same	214	7.7	13	25	400	1,500
H2	Same	250	110	–	90	10,000	3,350
Moisture	Measured at 37°C in g. mil/100 in²/24 hrs. atm. 90% RH	1.6	0.5	0.25	1.7	3	7

parts that already have existing standards for size and pin-out arrangements, there is no such standard available for bare dice. Pin-out assignment and die size can vary among IC vendors. Sometimes, bare dice of the same die type can be different even if they come from the same company. As IC foundries continue to shrink dice to increase the die yield per wafer, different physical die sizes for the same die type may be simultaneously available depending on which lot the manufacturer ships to the customer. In the standard technology design with packaged parts, this die size change has no impact since dice of different sizes fit into the same package. In the COB design, it may require a complete re-design of the substrate. The back side interconnection of the bare die is also another important feature. It depends on the technology used by the IC foundry that may either require the back side to be connected to V_{cc}, ground or left floating. Therefore a close working relationship must be established with the die supplier to avoid such potential problems.

Re-work must be considered from the substrate design to the selection of die attachment, die coating, and substrate materials. In the substrate design, large bond pads are needed to accommodate multiple wire bonding applications. For a typical 0.001 in. wire bond, an area of four times the wire diameter is needed for a single wire bonding step. Thus a bond pad with the size of 0.005 in. by 0.040 in. can easily support ten wire bonds. In the selection of substrate material, one should use the material with a high Tg to avoid high thermal stresses due to repeated heating of the substrate to 150°C during re-work. Removal of die coating material, an essential step in the re-work process, is a difficult task for epoxies. Even though epoxy can be removed with the application of heat, this technique may leave epoxy residues on the bond pads which are a potential problem for wire bonding. In this study, we are evaluating the effect of protecting the dice by coating only the top surface of the die and not the area that surrounds the die. This approach permits replacement of the die without damaging the bond pads on the substrate. Figure 12 illustrates this technique.

3.2 MANUFACTURE

COB manufacturing starts with die purchase, shipping and storage. Many important steps are being implemented by the Space Department Reliability and Quality Assurance Group (SOR) to resolve the KGD issue and to avoid problems related to handling and die shrink. Details of this process are not included in this report. Since the COB assemblies include SMT

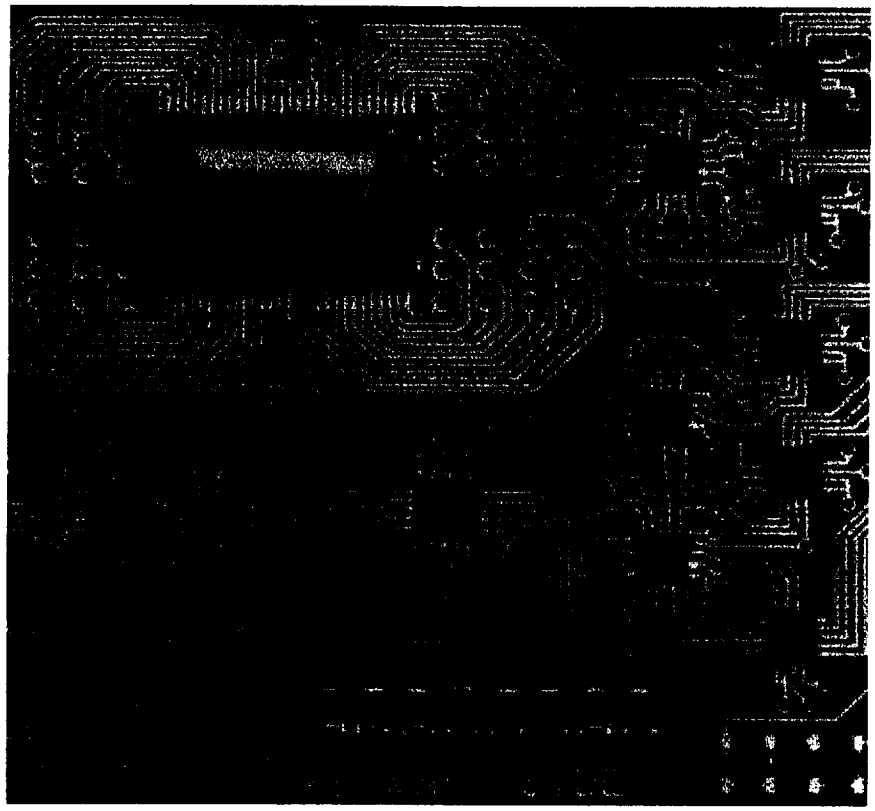


Figure 12
Photograph of Die with Epoxy Coat Only on Top Surface

components as well as bare dice, the assembly of COB has two distinctive steps as shown in Figure 13. In this assembly work flow, the most important step is to complete all soldered components prior to mounting bare dice. This approach will allow thorough cleaning of the solder fluxes – a very important requirement in providing a reliable COB assembly – prior to the wire bonding step. As indicated in the test results section, cleaning of solder fluxes must be done carefully to avoid corrosion and contamination problems.

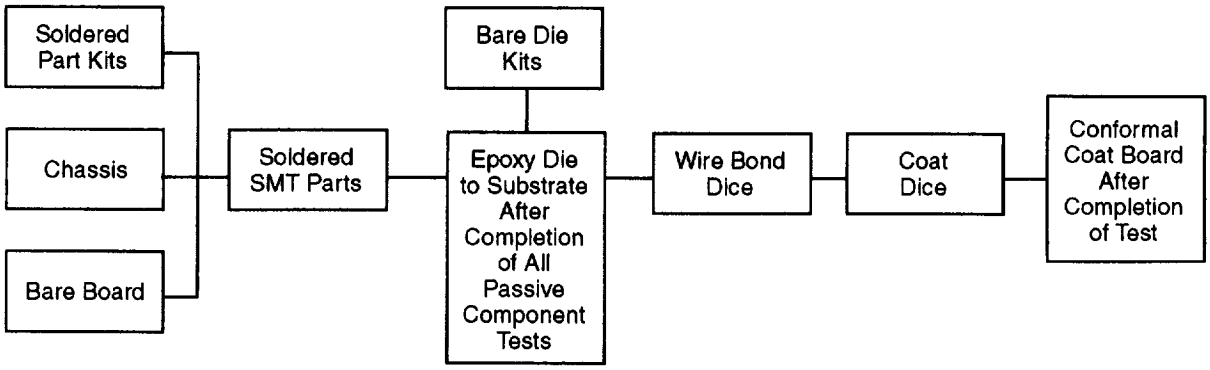


Figure 13
Simplified Assembly Flow of COB Assembly

4.0 TEST VEHICLES

There were three different test vehicles used in this study – the FAD board, the DRAM boards, and the triple track chips.

4.1 FILTER ANALOG-TO-DIGITAL (FAD) BOARD

A magnetometer that was flown on the Freja spacecraft was selected for the miniaturization experiment. The magnetometer is composed of three separate subsystems – the front-end sensor electronics, the FAD, and the processor board. To effectively demonstrate the manufacturability/viability of the COB packaging technology, a FAD circuit board was fabricated using COB packaging technology. The FAD board was chosen because of its relative circuit complexity compared with the other two boards. The FAD circuit design incorporates analog, digital and mixed signal circuitries and integrated circuit complexity ranging from discrete to VLSI technologies utilizing several different power supply rails. It also employs a representative spectrum of electronic parts that may be used on typical subsystems in space hardware. The principal function of the FAD board is to condition an input signal from the sensor that detects magnetic field strength, and systematically digitize it for the processor board. The input signal to the FAD board is passed through three parallel analog filters that decompose the signal into x, y, and z axis signals. The component signals are then amplified before being fed into a multiplexer controlled by a logic state machine with 2 kbits of RAM memory. The output of the multiplexer is subsequently sampled by a sample-and-hold amplifier whose output is digitized into 16-bit information. A FIFO then stores the data which are sequentially retrieved by an off-board processor.

The substrate design consists of two eight layer boards mounted in a magnesium housing with a elastomeric connector providing interconnection between the two boards. The board design used 125 μm lines and spacings to provide high density routing. The conductors on the outer layers have electrolytic nickel and gold plating as shown in Figure 14 to support the thermosonic wire bonding of the dice. The nickel layer serves as a diffusion barrier between the gold and the copper layers to prevent the formation of the inter-metallic (Au-Cu) compounds that often causes bond wire failure. The thermosonic process uses heat along with ultrasonic energy to create the bond. The material selection of the substrate is particularly important in this design, since it has to be compatible with both the soldering and the wire bonding processes. The most suitable material for this application is polyimide. This material is highly stable and is commonly used in the printed wiring board industry.

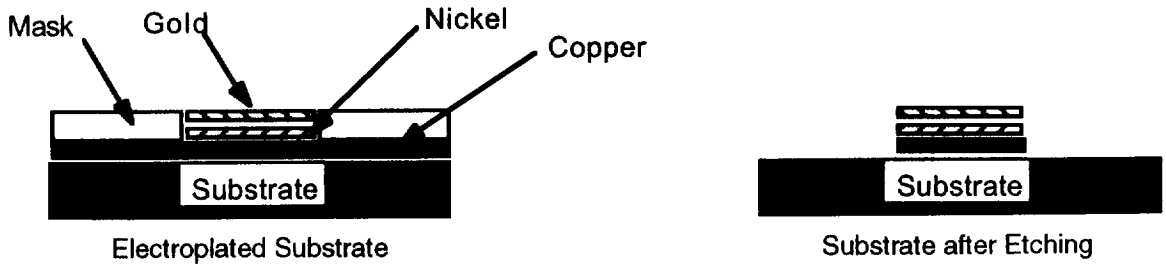


Figure 14
Plating and Etching Processes for COB Substrate

In the FAD design, integrated circuits and components of several package styles were used – unpackaged dice, ceramic-package IC's and plastic encapsulated microcircuits. On-board vias were available for probing. Packaged components were all surface mounted, and bare dice were attached to the board with Ablebond silver epoxy. An elastomeric connector makes 3-D packaging possible and interconnects the FAD board with the other two subsystems of the magnetometer, namely, the sensor and the processor boards. The connector consists of a thin flexible polyimide film, with individual parallel lines of soft gold plated copper conductors, wrapped around a soft, non-conducting silicone rubber core. The pattern of plated conductors consists of 75 mm wide lines on 175 mm centerlines which when compressed, will provide interconnection between the circuit pads on both boards. This approach provides extremely high density interconnection and eliminates the necessity of mating and de-mating conventional connectors that require a large amount of force, which is sometimes a problem in flight hardware. Figure 15 illustrates the application of the elastomeric connector in the FAD board design.

The COB FAD design was successfully developed resulting in a size and weight reduction of at least a factor of seven. Electrical performance of the FAD was verified with existing test equipment after the debugging and repair process was completed.

While in the temperature-humidity chamber, the FAD assembly, which is comprised of the FAD board, a companion capacitor board, and an adapter board for cabling with the elastomeric connector, was biased with ±7, ±14, and +5V power supplies to keep the analog and digital circuits powered. A clock signal was provided by a clock generator circuit board outside the chamber to maintain an active mode in some digital devices.

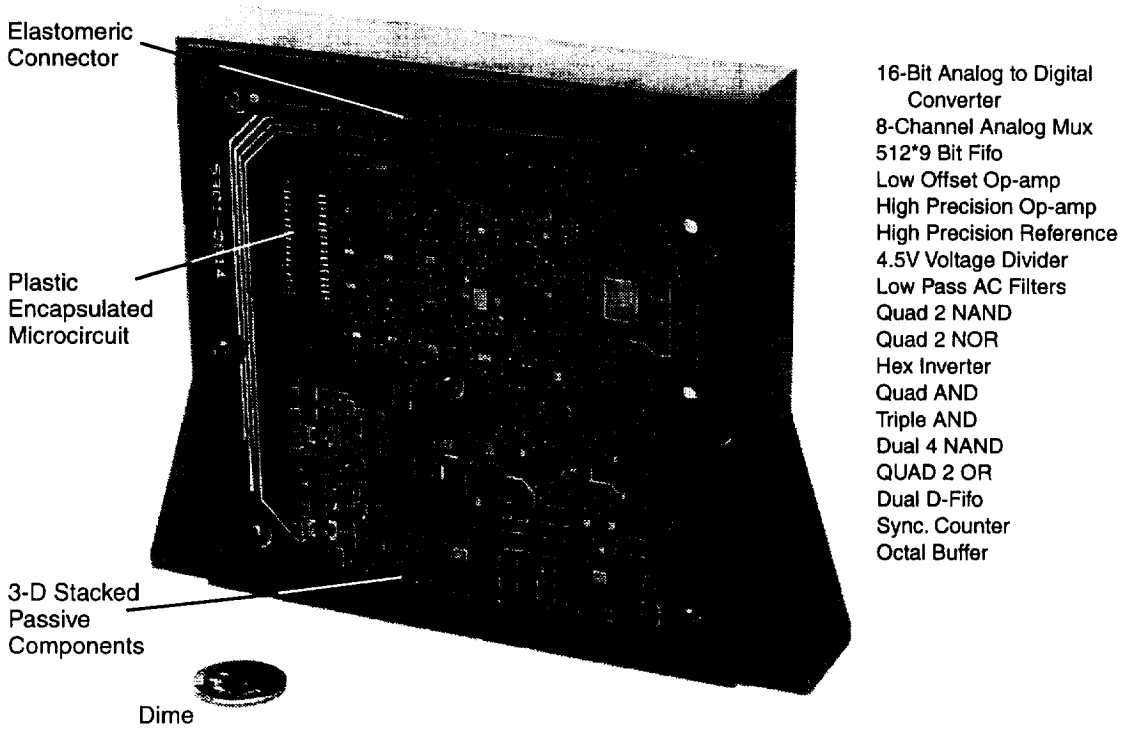


Figure 15
Photograph of the FAD Board with Elastomeric Connector

4.2 DRAM BOARD

The second test vehicle is a DRAM board (Figure 16). The basic function of this circuit is to continuously and completely exercise the 3-D stacked DRAM module with a memory capacity of 80 Mbits. The module consists of six DRAM die layers stacked on top of one another to form a 3-D rectangular cube. Only five die layers are used with the sixth one being a spare. The DRAM module is 4 million locations by 4 bits per location. Upon power-up, the circuit will be fully functional with an externally applied system clock and eight pattern lines. The pattern bits are shifted at each system clock rising edge to provide a different data pattern to each memory location, upon which four distinct operations – refresh, write, refresh, and read are performed. Each address location in the DRAM module is accessed every 4,194,304 clock cycles.

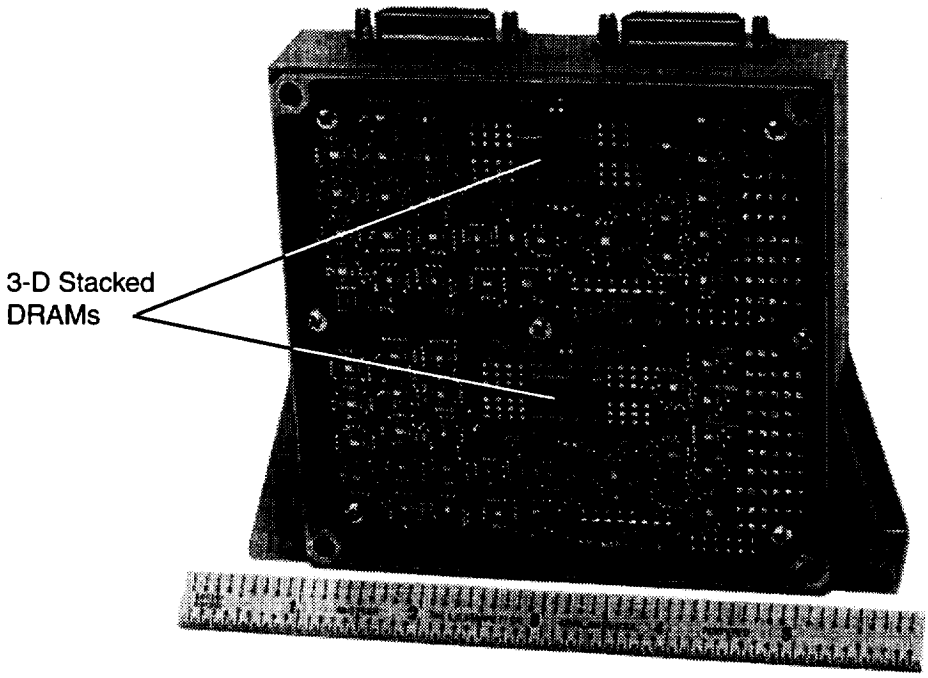


Figure 16
Photograph of the DRAM Board with 3-D Stacked DRAMs

The functional verification performed on the Schlumberger Sentry-15 automatic tester consists of four main steps:

(1) Circuit Resetting – Initialization
(2) Pattern Input – Bit pattern selection to be written into the part
(3) Clocking – Sequencing through Refresh-Write-Refresh
(4) Output Verification – Reading address locations

The functional tests were performed at two frequencies: 2 MHz and 8 MHz. First, each of the five memory layers was tested separately. Due to the memory limitation of the test head pins, the memory locations were sample tested. The functional test for a single layer was comprised of a simple verification of only the first 16 memory locations, and the individual layers were tested separately in sequence. Then, all layers were tested together in parallel. The first 8,192 memory locations on all layers were verified during parallel functional tests. A total

of twelve functional tests were performed, six at 2 MHz and six at 8 MHz. Table 13 shows the functional test sequence.

Table 13
DRAM Board Functional Test Sequences

Functional Number	Layer Number Being Tested	Test Frequency	Number of Memory Location Tested
1	1	2 MHz	16
2	2	2 MHz	16
3	3	2 MHz	16
4	4	2 MHz	16
5	5	2 MHz	16
6	1, 2, 3, 4, 5	2 MHz	8,192
7	1	8 MHz	16
8	2	8 MHz	16
9	3	8 MHz	16
10	4	8 MHz	16
11	5	8 MHz	16
12	1, 2, 3, 4, 5	8 MHz	8,192

A total of eleven boards were fabricated with two identical circuits on the two halves of the substrate. Construction of the DRAM boards is similar to that of the FAD described above. Each circuit is covered with a combination of die coating materials with or without a final conformal coating (see Table 14 for test matrix). Six boards were subjected to vibration and temperature cycling while the remainder were used in the THB test. Electrical functionality was checked using the Sentry-15 automatic tester periodically during environmental testing.

4.3 TRIPLE TRACK

The triple track is a special device designed to detect corrosion. Version 01 test chips provided by Sandia National Laboratories were used to complement this COB coating study. These test chips contain several triple track and ladder test structures. The triple track test structures are basically very closely spaced, parallel aluminum tracks in triplets that run in a serpentine pattern. The resistance of each track can be measured and monitored for detecting corrosion. The leakage current between the tracks can also be measured to monitor any conducting path formed by ionic contaminants, dendritic growths or other corrosion agents. To characterize corrosion-induced failures quantitatively, ladder structures are available. A ladder consists of a number of aluminum conductor tracks connected in parallel between two wide metal bus bars. As corrosion creates an open path in the individual conductors, the overall ladder resistance increases in a stepwise fashion. An experimental cumulative failure distribution can then be developed to test or fit failure models. The substrate of a triple track die is made of oxide coated silicon. Some dice are passivated with a 7000 Å silicon nitride capping layer while others are un-passivated. Fifteen samples of passivated and an additional fifteen un-passivated samples – coated with various combinations of parylene/FP4402, FP4402, parylene/FP4450, FP4450, parylene/silicone, silicone, and parylene die coating materials – were packaged in 40-pin DIP lead frames (see Figure 17 for details and Table 15 for test matrix). Additional samples without any coating are also included in this test to serve as the baseline samples. For the temperature cycling storage test, the parts are unbiased while inside the environmental oven. However, for

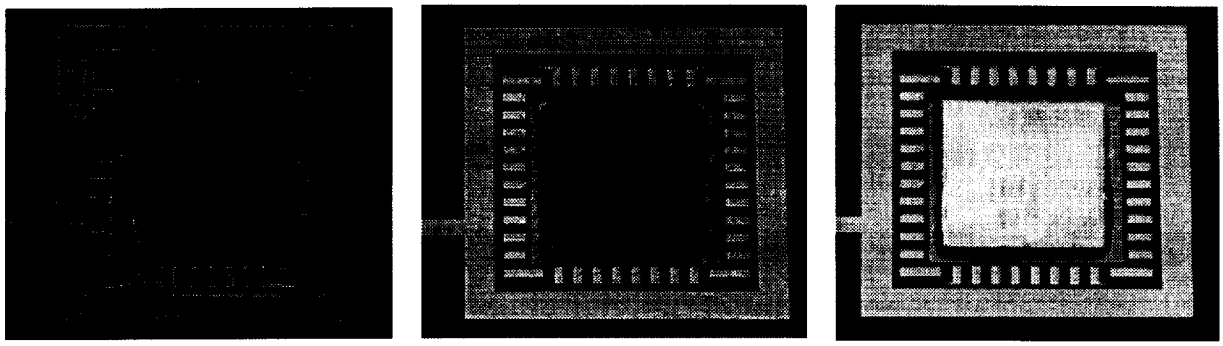
Table 14
DRAM Boards Coating and Test Matrix

S/N	85°C/85% RH Temperature/Humidity/Bias	Vibration Thermal Cycling
SN004 Side A SN004 Side B	Parylene/FP4402 Parylene/FP4450	
SN005 SideA	No Coating	
SN006 Side A SN006 Side B	FP4402/Si_3N_4 FP4450/Si_3N_4	
SN007 Side A SN007 Side B	Si_3N_4 Silicone/Si_3N_4	
SN012 Side A SN012 Side B	Parylene/Si_3N_4 Parylene/Silicone	
SN001 Side A SN001 Side B		FP4402/Si_3N_4 FP4450/Si_3N_4
SN002 Side A SN002 Side B		Parylene/Si_3N_4 Parylene/Silicone
SN003 Side A SN003 Side B		Parylene/Si_3N_4 Parylene/Silicone/Si_3N_4
SN008 Side A SN008 Side B		Parylene/Si_3N_4 Parylene/Silicone/Si_3N_4
SN009 Side A SN009 Side B		Parylene/FP4450 Parylene/FP4402
SN010 Side A SN010 Side B		Parylene/FP4402 Parylene/Silicone

the 85°C/85% RH THB test, the test devices will be powered to accelerate corrosion. The triple track structures will be biased at 5 V from the exterior track to the middle track and at -5 V from the interior track to the middle track. One ladder on each test chip will be biased at 5 V across the pads while the other one will be at -5 V. Electrical performance of the test chips will be verified using the Sentry-15 automatic tester at intervals of 100, 250, 500, 750, and 1000 hours of the 85°C/85% RH THB test, and at 100, 250, 500, 750 and 1000 cycles of temperature cycling.

5.0 TEST ENVIRONMENTS[11]

A survey was made of the literature on COB technology, plastic encapsulated microelectronics (PEM) and reliability without hermeticity, all of which have a similar goal with respect to the environmental qualification. The test levels used in this study exceed the requirements for typical space flight environments. They are designed to select the best coating material to qualify the technology and the process for a given program or mission. The test environments include the dynamic envelope loads covering all existing launch vehicles, the temperature cycling from -55°C to +125°C, and the 85°C/85% RH THB test. The THB test usually does not apply to the hermetically sealed technology. This test is equivalent to 22 years at 32°C and 63% RH, according to an Air Force Reliability Analysis Center study.



Triple Track Die Without Coating | Triple Track Die With Epoxy | Triple Track Die With Silicone

Figure 17
Photograph of the Triple Track Device Inside a 40 Pin DIP

Table 15
The Triple Track Coating and Environmental Test Matrix

Die Coating From IC Foundry	Glob Top, Coating		Test	Note
	1st Ctg	2nd Ctg		
No Passivation	FP4450		85°C/85% RH	
No Passivation	FP4450		85°C/85% RH	
No Passivation	FP4450	Parylene	85°C/85% RH	
No Passivation	FP4450	Parylene	85°C/85% RH	
No Passivation	FP4450		85°C/85% RH	
No Passivation	FP4402		85°C/85% RH	
No Passivation	FP4402	Parylene	85°C/85% RH	
No Passivation	FP4402	Parylene	85°C/85% RH	
No Passivation	Silicone	Parylene	85°C/85% RH	Top coat only
No Passivation	Silicone	Parylene	85°C/85% RH	Top coat only
No Passivation	Silicone		85°C/85% RH	Top coat only
No Passivation	Silicone		85°C/85% RH	Fill cavity
No Passivation	Parylene		85°C/85% RH	
No Passivation	Parylene		85°C/85% RH	
No Passivation	No ctg	No ctg	85°C/85% RH	
7KA SiN	FP4450	Parylene	85°C/85% RH	
7KA SiN	FP4450	Parylene	85°C/85% RH	
7KA SiN	FP4402	Parylene	85°C/85% RH	
7KA SiN	FP4402	Parylene	85°C/85% RH	
7KA SiN	Silicone	Parylene	85°C/85% RH	Top coat only
7KA SiN	Silicone	Parylene	85°C/85% RH	Top coat only
7KA SiN	Parylene	No ctg	85°C/85% RH	
7KA SiN	No ctg	No ctg	85°C/85% RH	
7KA SiN	FP4450	Parylene	Temp Cycling	
7KA SiN	FP4450	Parylene	Temp Cycling	
7KA SiN	FP4402	Parylene	Temp Cycling	
7KA SiN	FP4402	Parylene	Temp Cycling	
7KA SiN	Silicone	Parylene	Temp Cycling	Fill cavity
7KA SiN	Silicone	Parylene	Temp Cycling	Top coat only
7KA SiN	Silicone	Parylene	Temp Cycling	Top coat only

5.1 DYNAMIC LOADS

The dynamic loads environment envelops a spectrum of launch vehicle environments for various past space programs at JHU/APL. Table 16 shows detailed test levels. An electrical functional verification test at 0, 25, and 85°C was performed on the Sentry tester after each vibration test.

Table 16
Dynamic Load Levels

Pre and Post Sine Survey

Frequency (Hz)	Acceleration
5 - 2000	0.5 g Rate = 4 octaves/min

Sine Burst Test

50 g's @ 35 Hz.
10 Cycles

Random Vibration Test

Frequency (Hz)	PSD (G2/Hz)
20	0.048
20 - 50	+6 db/oct
50 - 800	0.3
800 - 2000	-6 db/oct
2000	0.048

Overall Level=19.3 Grms

Shock Test

Frequency (Hz)	Acceleration (g's)
100	10
1000	500
2200	1000
6000	2000
10,000	2000

Q = 10

5.2 TEMPERATURE CYCLING

Thermal cycling was carried out in an environmental chamber for 1000 cycles. The temperature controller of the oven was set such that the test boards achieved a cooling and heating rate of between 10 to 12°C per minute with a dwell time of 10 minutes at -55°C and 15

minutes at 125°C. Electrical functionality was verified on the Sentry tester at intervals of 100, 250, 500, 750, and 1000 cycles.

5.3 TEMPERATURE HUMIDITY BIAS

The 85°C/85% RH THB stress test was conducted in a temperature-humidity chamber for 1000 hours. Test boards were mounted on a flat aluminum plate with the wire bond side exposed to the environment. A power supply external to the chamber provided bias voltage of -5 V and +5 V applied to the boards through cables. The interior chamber temperature, the power supply voltage and current of each board were periodically monitored by a data logger. At intervals of 100, 250, 500, 750, and 1000 hours, the specimens were removed from the humidity chamber. After a moisture bake-out inside another chamber, the boards underwent an electrical functionality test at 0, 25 and 85°C on the Sentry tester.

6.0 TEST RESULTS AND ANALYSIS OF RESULTS

6.1 FAD BOARD TEST

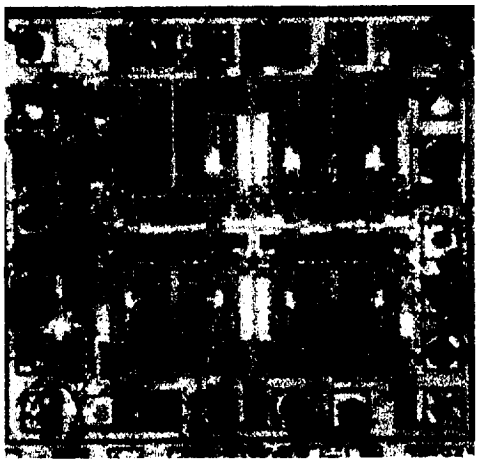
6.1.1 Corrosion Problem in the FAD Board

After successfully completing all electrical tests, the FAD board was subjected to an 85°C/85 % RH THB chamber to evaluate the effectiveness of the silicon nitride coating protection. The board completely failed to function when it reached 230-hours in the THB environment. Upon visual inspection, both the FAD board and an attached capacitor board along with the magnesium housing, which were coated with silicon nitride prior to the THB test, showed evidence of severe corrosion (Figure 18). Corrosion also showed up on the magnesium housing and on standard hardware (Figure 19). A more detailed inspection using a microscope revealed possible silver migration on the FAD board (Figure 20) and outgassing from solder fluxes, tin leads, etc. Other trouble signs included white residues found on de-laminated conductor strips on the elastomeric connector (Figure 21).

6.1.2 FAD Board Failure Analysis

To identify the cause for corrosion, a number of action items were initiated. A water sample obtained from the inlet to the boiler in the 85/85 chamber used to produce humidity was analyzed. The results showed negligible amounts (less than 0.9 ppm.) of a variety of ionic materials. A witness silicon wafer that was coated with silicon nitride in the same deposition run as the FAD board was analyzed[12]. A refractive index test revealed the presence of oxygen in the silicon nitride coating and a variation in the thickness of the silicon nitride of between 1700 to 2500 Å (the nominal thickness is 4000 Å). A micro-analysis conducted[8,9] using energy dispersive spectroscopy (EDS) found widespread ionic contamination on the board assembly that included chlorine, sodium, potassium and sulfur (Figure 20). However, no trace of nitride was found in the coating layer. Optical and scanning electron microscopy results indicated that the coating was uneven, exhibiting buckling and peeling on the board, its surfaces and on the die (Figures 22, 23). This was probably the main cause of the corrosion since unprotected bare dice may have been exposed to ionic contamination from handling.

It was not clear if the bare board was completely free of contamination prior to mounting parts on it. Questions also arose as to whether the FAD and the associated capacitor boards were thoroughly cleaned before the deposition of the silicon nitride layer. Material compatibility between the board assembly and the coating process was also an issue. It was found that the PECVD-deposited Si_3N_4 does not adhere well to a pure gold surface formed using the electrolytic process for deposition of nickel and gold over the copper traces. The ability of the silicon nitride to adhere to the PWB and on-board components also depends heavily on the level of cleanliness at the board level. This fact may explain why peeling of the silicon nitride material occurred on the FAD board.



Photograph of a Corroded Die

SEM Photomicrograph of a Corroded Die

Figure 18
Severe Corrosion Observed on the FAD Board

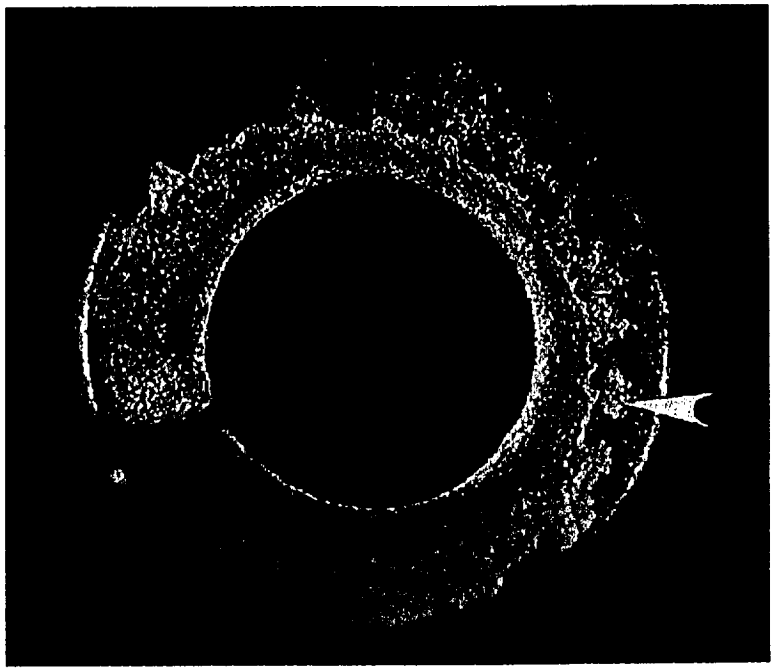
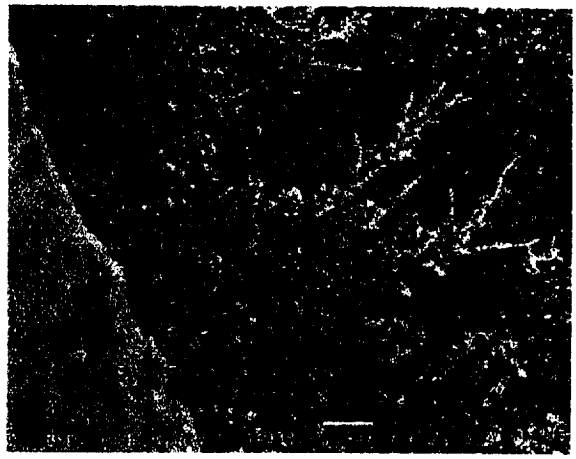
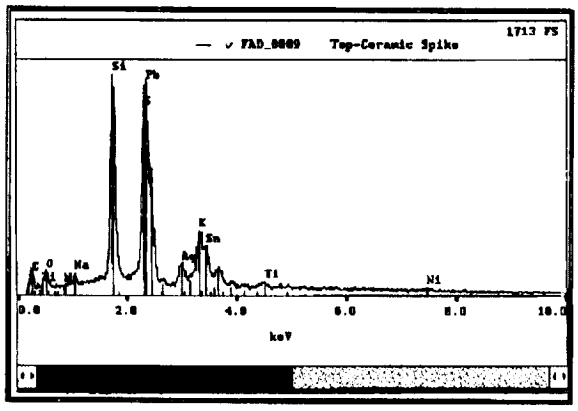


Figure 19
Corrosion Found on Washer of the FAD Assembly

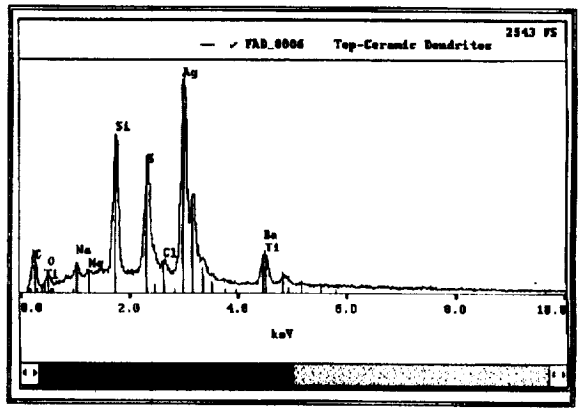
SEM photomicrograph of a capacitor on the FAD board. Notice the migration of material on the side wall.



SEM photomicrograph of dendrites on the side wall



EDS spectrum identifies potassium.



EDS spectrum identifies silver, and corrosives sulfur, chlorine, and sodium.

Figure 20
Photomicrograph and EDS Spectrum of a Capacitor on the FAD Board

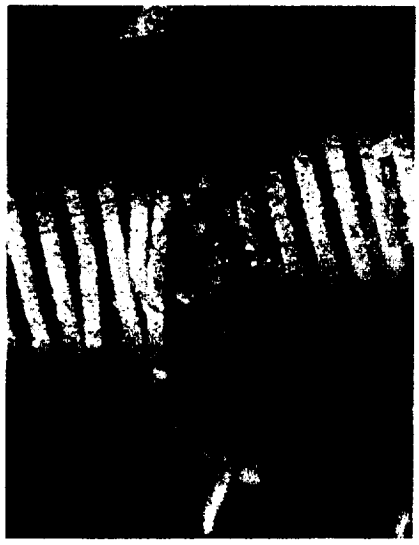


Figure 21
Corrosion and Delamination on Elastomeric Connector

Evidence of Silicon Nitride
Delamination Around the Plated Through Hole.

Evidence of Silicon Nitride
Delamination on Gold Plated Trace.

Figure 22
Delamination of Coating on the FAD Board Surface

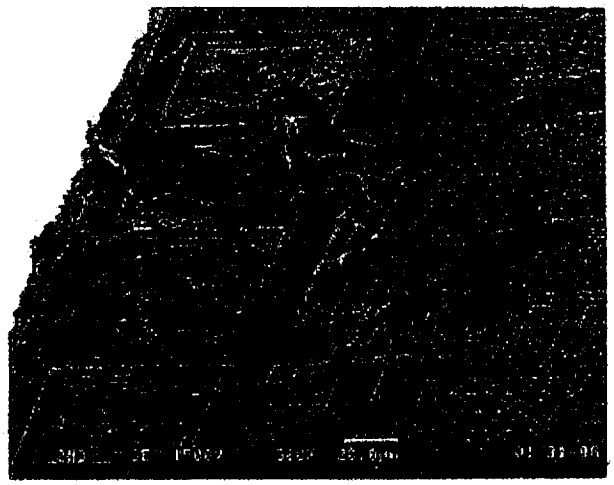
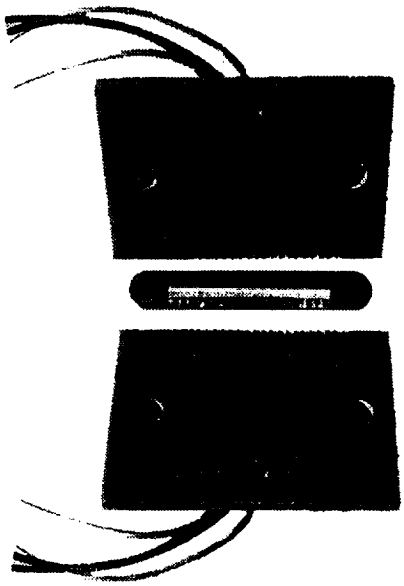


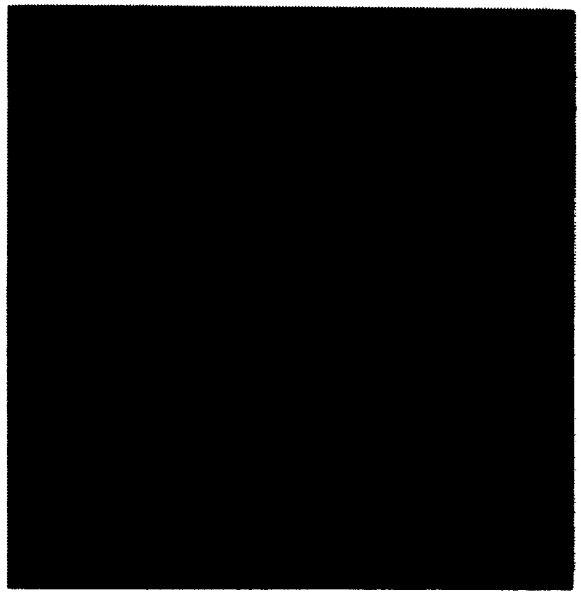
Figure 23
SEM Photomicrograph of an Eruption Site on a Die Surface

6.1.3 Material Compatibility Evaluation

As a result of the FAD board corrosion problem, a separate study to investigate different materials involving magnesium and aluminum lids and an elastomeric connector was carried out to simulate the FAD results. Specifically, the test samples consisted of one alodine-coated aluminum lid, one magnesium lid with intentionally deposited finger grease, one clean magnesium lid, one thoroughly cleaned aluminum lid that was kept in the clean-room, and an elastomeric connector (Figure 24). The connector was compressed between two bare PWBs with gold plated tracks (Figure 25). The conductor fingers that came into contact with the connector were deliberately tin plated, and the solder fluxes were not removed. Biases of ±15 V were applied to two selected pairs of adjacent conductor fingers on the PWB while inside the 85°C/85% RH THB chamber.



Test Board Assembly



Metal Lid Test Sample

Figure 24
Test Samples to Study the Effect of Humidity on Various Materials

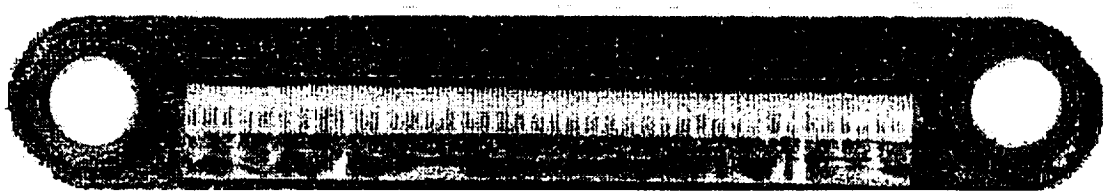


Figure 25
Elastomeric Connector

After 262 hours of 85°C/85% RH THB stress test, the specimens were removed from the chamber and examined. A number of observations were made upon visual inspection with a 60x microscope. The surfaces of both magnesium lids had darkened. The one with finger grease exhibited signs of severe corrosion similar to the appearance of the FAD chassis. Subsequent EDS spectrum surface elemental analysis revealed severe corrosion on the contaminated lid (Figure 26). There were also signs of ionic contamination on the cleaned magnesium lid (Figure 27). On the aluminum lids, it was noted that the alodine coating almost completely disappeared. However, these samples did not appear to be corroded (Figure 28). One of the two sets of screw and nut that held the two PWBs together with the elastomeric connector in between showed evidence of corrosion. The screw and nut that had corroded seemed to have traces of solder flux over them. As for the solder joints on the wiring, the solder flux had apparently migrated to other areas of the PWBs. Migration of copper and nickel between the biased traces was evident in the spacing between gold finger tracks where the solder joints were located (Figure 29). Despite the apparent corrosion found on the PWBs, there was no damage found on the elastomeric connector, and there were no signs of delamination of gold conductor strips on the connector.

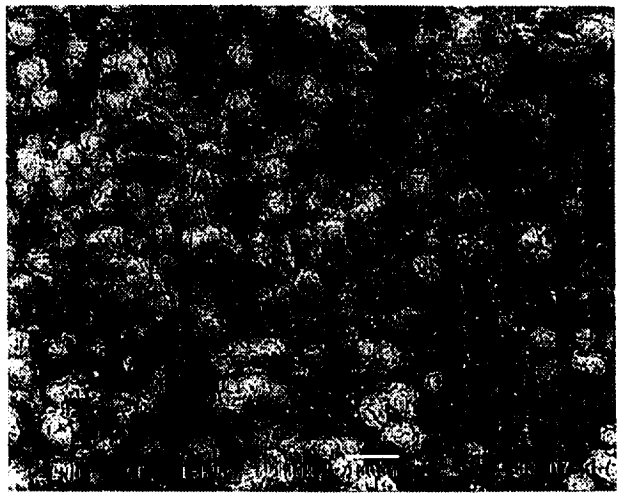


Figure 26
SEM Photomicrograph of the Contaminated Magnesium Lid
(Notice the pocked areas of charging material on top of a striated lid.)

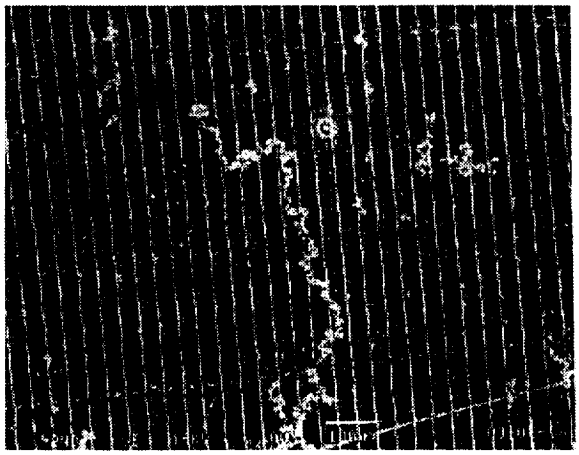


Figure 27
SEM Photomicrograph of the
Cleaned Magnesium Lid
(Notice the striated appearance that is significantly cleaner compared to Fig. 26)

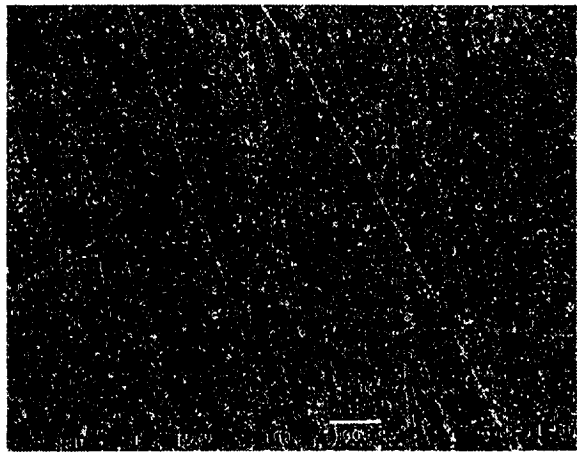


Figure 28
SEM Photomicrograph of the Aluminum Lid

6.2 DRAM BOARD TEST AND FAILURE ANALYSIS

For the test COB DRAM boards, all but one coating combination passed the vibration test. The lone failure, parylene/silicone was functionally intermittent. The same boards that underwent vibration testing were temperature cycled (see Table 14 or Table 17). The two samples of the parylene/silicone/Si_3N_4 combination were completely non-functional after just 80 and 100 cycles. At 280 cycles, the parylene/silicone circuit failed all electrical functionality tests. After the midpoint of 500 cycles, one of the parylene/FP4402 circuits failed at room and high temperature while still exhibiting some functionality in several die layers at cold temperature. The same circuit would subsequently fail complete electrical functionality after 780 cycles. Overall five of the 10 samples completely passed electrical tests after 1000 cycles. The successful combinations were FP4450/Si_3N_4, parylene/Si_3N_4, parylene/FP4450, and parylene/FP4402.

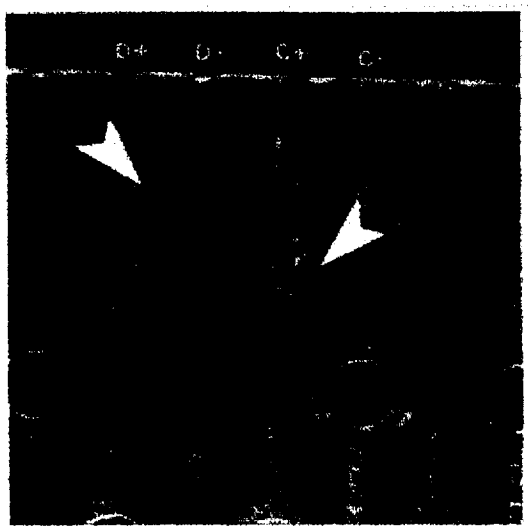


Figure 29
Migration of Copper and Nickel Between Biased Traces

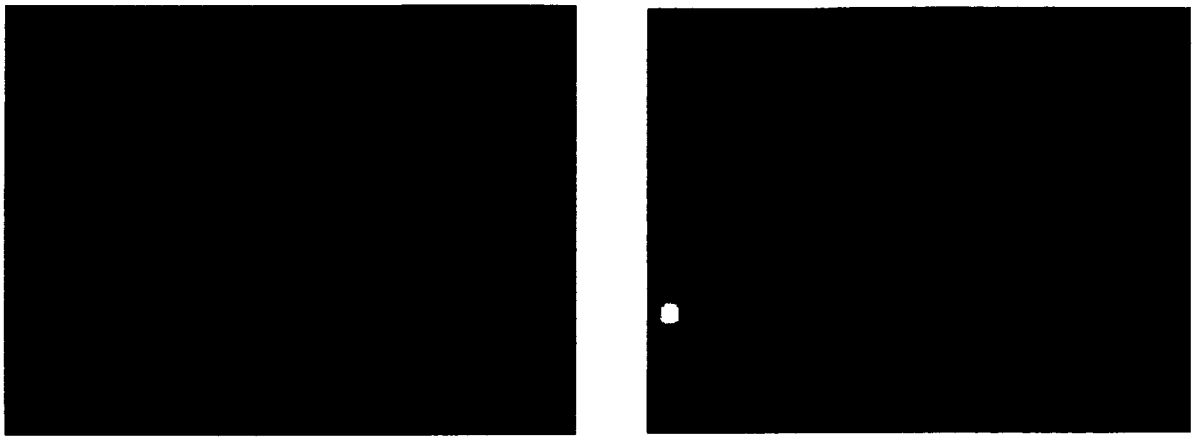
A total of nine coating combination samples were used in the 85°C/85% RH THB test. The control sample with no coating was completely non-functional after 150 hours, as was the parylene/Si_3N_4 combination. All die layers failed electrical functionality for the circuits covered with Si_3N_4 only and silicone/Si_3N_4 die coating materials. The parylene/silicone had a bad die layer at 150 hours but otherwise remained mostly functional at 1000 hours. The only coating combinations that successfully completed the 85°C/85% RH THB test were parylene/FP4402, parylene/FP4450, and FP4402/Si_3N_4. There was exactly one coating combination for which all test samples passed all environmental tests – parylene/FP4450. Table 17 summarizes the results of the tests.

It is difficult to determine the exact number of failed wire bonds out of a total of 500 wire bonds on the DRAM board. During the design of the DRAM board, test points were added

Table 17
COB DRAM Board Test Results

S/N	Coating	Dynamic Test	Temperature Cycle (-55°C to 125°C) Test	85°C/85% RH Bias Test
SN004 - Side A	Parylene/FP4402	NA	NA	PASSED
SN004 - Side B	Parylene/FP4450	NA	NA	PASSED
SN005 - Side A	No coating	NA	NA	Failed at 150 Hrs
SN005 - Side B	Not Required	NA	NA	NA
SN006 - Side A	FP4402/Si_3N_4	NA	NA	PASSED
SN006 - Side B	FP4450/Si_3N_4	NA	NA	Failed at 1000 Hrs
SN007 - Side A	Si_3N_4	NA	NA	Failed at 750 Hrs
SN007 - Side B	Silicone/Si_3N_4	NA	NA	Failed at 500 Hrs
SN012 - Side A	Parylene/Si_3N_4	NA	NA	Failed at 150 Hrs
SN012 - Side B	Parylene/Silicone	NA	NA	PASSED
SN001 - SideA	FP4402/Si_3N_4	NA	NA	NA
SN001 - Side B	FP4450/Si_3N_4	PASSED	PASSED	NA
SN002 - Side A	Parylene/Si_3N_4	PASSED	PASSED except one die in the DRAM stack	NA
SN002 - Side B	Parylene/Silicone	PASSED	Failed at 280 cycles	NA
SN003 - Side A	Parylene/Si_3N_4	NA	NA	NA
SN003 - Side B	Parylene/Silicone/Si_3N_4	PASSED	Failed at 100 cycles	NA
SN008 - Side A	Parylene/Si_3N_4	PASSED	PASSED	NA
SN008 - Side B	Parylene/Silicone/Si_3N_4	PASSED	Failed at 80 cycles	NA
SN009 - Side A	Parylene/FP4450	PASSED	PASSED	NA
SN009 - Side B	Parylene/FP4402	PASSED	Failed at 780 cycles	NA
SN010 - Side A	Parylene/FP4402	PASSED	PASSED	NA
SN011 - Side B	Parylene/Silicone	NA	NA	NA

for each device to facilitate probing of all components. However, probing on the board can only determine a bad die or a group of bad wire bonds on the same die. It does not provide information on the absolute number of failed wire bonds. This is the reason for the continued study of the die coating materials using the triple track devices. We are also investigating other non-invasive testing techniques such as infrared thermal imaging to map out the potential problem areas. Preliminary results of this technique are very encouraging. As shown in Figure 30, the bad die was highlighted with its high thermal signature. Additional work to further analyze the results of the DRAM boards will continue in 1997.



Thermal Imaging of a Working DRAM Board

Thermal Imaging of a Non-Working DRAM Board
(Note the high thermal signature of a bad die)

Figure 30
Failure Analysis of the DRAM Boards Using Infrared Thermal Imaging System

6.3 TRIPLE TRACK TEST

At present, seven triple-track samples (SNs 24 through 30) are undergoing temperature cycling. After 750 cycles, all three silicone samples failed either all or a majority of the resistance tests. One failed sample showed complete open circuits on all tracks and ladders. The other two chips still have connection on some of the wire bonds. It should be noted that silicone covered DRAM boards also failed temperature cycling. Figure 31 shows a severe crack on the silicone coating surface and a broken wire bond as a result of high thermally induced stress.The results of the DRAM samples are consistent with those of the silicone-covered triple track samples confirming the unsuitability of silicone with its high TCE for a COB coating. Table 18 summarizes the test results.

7.0 CONCLUSIONS AND RECOMMENDATIONS

The COB study over the past three years has shown that reliability without hermeticity is achievable for flight hardware. The FAD board was re-designed using advanced packaging technology of COB. Electrical test results indicated the board was completely compatible in functionality with the original wire-wrap version flown on the Freja satellite. This development represented a milestone of realizing miniaturization of space hardware. Reliability of COB technology is not assured, however, until a die/board coating material is flight qualified. The candidate coating material must successfully complete vibration, thermal cycling, and 85°C/

Figure 31
Severe Crack on Silicone Die Coating Surface and Broken Wire Bond
as a Result of High Thermal Stress

Table 18
Triple Track Temperature Cycling Test Results

S/N	Die Coating From IC Foundry	GLOB TOP, COATING		Test	Note	Temp Cycling Test			
		1st Ctg	2nd Ctg			100 Cycles	250 Cycles	500 Cycles	750 Cycles
24	7KA SiN	FP4450	Parylene	Temp Cycling		PASSED	PASSED	PASSED	PASSED
25	7KA SiN	FFP4450	Parylene	Temp Cycling		PASSED	PASSED	PASSED	PASSED
26	7KA SiN	FP4402	Parylene	Temp Cycling		PASSED	PASSED	PASSED	PASSED
27	7KA SiN	FP4402	Parylene	Temp Cycling		PASSED	PASSED	PASSED	PASSED
28	7KA SiN	Silicone	Parylene	Temp Cycling	Filled cavity	PASSED	8 wire bonds broken	16 wire bonds broken	17 wire bonds broken
29	7KA SiN	Silicone	Parylene	Temp Cycling	Top coated only	PASSED	2 wire bonds broken	11 wire bonds broken	15 wire bonds broken
30	7KA SiN	Silicone	Parylene	Temp Cycling	Top coated only	PASSED	PASSED	6 wire bonds broken	15 wire bonds broken

85% RH THB tests. Only one die/board coating combination – parylene/FP4450, has been found to pass all environmental tests. The finding is not surprising considering the track record of the glob top in the industry and its thermal coefficient of expansion (TCE). Hysol FP4450 and FP4402 epoxies have been widely used in the space community in recent years and have performed well. The major reason is that the TCEs for these epoxies are closely matched to that of gold wire bonds. The ability of the FP4450 to act as a water block and to withstand rigorous vibration launch conditions and simulated space thermal cycling environment makes it the top candidate for use in protecting bare dice and wire bonds in space electronics.

Physically shrinking space hardware complicates testability. Known-good-dice should be secured if possible. This eliminates one variable when debugging a COB board. There are two levels of testability – chip and board. At the chip level, for example, Actel designs should have Joint Test Action Group (JTAG) boundary scan capability. Another design-for-test feature is built-in two-node probing. Current 1020's and 1280's have a five-wire two-node internal logic probe setup that requires 5 I/O pins dedicated to this function. Test modes can also be designed into the Actel designs so that the circuits may be placed in a speed-up mode for low-frequency applications. Re-configuration of counters into smaller units would facilitate probing and debugging. There are at least four different methods to program Actel dice – DieMate™

fixture, cascade tape mount fixture, ceramic pad adapter, and on-board programming. Each has its own pros and cons with cost and flexibility the main issues. As for Actel die pad layout, all die pads may have a board pad or only die pads that are used may be connected to the board. Other parts considerations include selecting parts with boundary scan and/or JTAG capability and ordering parts with simulation models.

For board-level design-for-test, a number of guidelines should be observed. Test circuits should be designed within a board for testability to minimize probing during debug. Boundary scan and JTAG are standard ways of achieving this objective. In addition, multiplexing test and control signals to test connectors or an infrared link should be considered. Routing key circuit nodes to test points and connectors and partitioning circuits into smaller sub-circuits also improve testability. After a design is completed, simulation should be performed at the board level to minimize design errors and to help generate test vectors. Finally, there are three ways to test a board – board level tester, box-level tester, and automatic test equipment (ATE). The choice of any of these three test methods depends on the feasibility, practicality, and the cost-effectiveness of employing them.

8.0 ACKNOWLEDGMENTS

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ACRONYMS

ASIC	Application Specific Integrated Circuit
ATE	Automatic Test Equipment
BT	Bis-maleimide Triazines
C&DH	Command and Data Handling
CCD	Charged Coupled Device
COB	Chip on Board
DARPA	Defense Advanced Research Projects Agency
DIP	Dual Inline package
DOD	Department of Defense
DRAM	Dynamic Random Access Memory
EDS	Energy Dispersive Spectroscopy
ESD	Electrostatic Discharge
FAD	Filter Analog to Digital
FIFO	First In First Out
FPGA	Field Programmable Gate Array
GSFC	Goddard Space Flight Center
IC	Integrated Circuit
IR&D	Independent Research and Development
JEDEC	Joint Electron Device Engineering Council
JTAG	Joint Task Action Group
KGD	Known Good Die
LCC	Leadless Chip Carrier

MCM	Multichip Module
MCM-C	Multichip Module with Ceramic dielectric
MCM-D	Multichip Module with Deposited dielectric
MCM-L	Multichip Module with Laminated dielectric
NASA	National Aeronautics Space Administration
PECVD	Plasma Enhanced Chemical Vapor Deposition
PGA	Pin Grid Array
PWB	Printed Wiring Board
QFP	Quad Flat Package
RH	Relative Humidity
SEM	Scanning Electron Microscopy
SMT	Surface Mount Technology
SOJ	Small Outline J leaded
TAB	Tape-Automated Bonding
TCE	Thermal Coefficient of Expansion
THB	Temperature Humidity Bias
TRB	Testable Ribbon Bonding
USAFA	United State Air Force Academy
VLSI	Very Large Scale Integration