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On-Board Switching and Routing Advanced Technology Study

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On-Board Switching and Routing Advanced Technology Study

Final Report

COMSAT Laboratories SR000013

Space Systems/Loral TR01529

October, 1998

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1. Executive Summary

1.1. Introduction

Future satellite communications is expected to be fully integrated into National and Global Information Infrastructures (NII/GII). These infrastructures will carry multi gigabit-per-second data rates, with integral switching and routing of constituent data elements. The satellite portion of these infrastructures must, therefore, be more than pipes through the sky. The satellite portion will also be required to perform very high speed routing and switching of these data elements to enable efficient broad area coverage to many home and corporate users. The technology to achieve the on-board switching and routing must be selected and developed specifically for satellite application within the next few years. This report presents evaluation of potential technologies for on-board switching and routing applications.

The work effort that went into this study can be separated into three major components:

- Switching and routing technology review, which involved a comparison of optical switching and electronic switching technologies, analysis of trends in these technologies, and evaluation of the current state of radiation hardened technology;
- High level design for the next generation on-board packet switch, which included a review of on-board switching requirements and capabilities of proposed Ka-band satellite systems and high-end terrestrial switches, determining the size and throughput of the next generation on-board packet switch, and providing a high level design for the next generation on-board packet switch;
- Development of satellite system concepts that implement the proposed fast packet switch onboard.

Sections 2 through 4 of this executive summary provide the major findings of these studies.

1.2. Technology Review

The next generation on-board switch technology review covered electronic switching and optical switching technologies, a comparison of these technologies for their suitability in implementing the next generation on-board switch, and identification of commercial ATM switch fabric components. The technologies evaluated under electronic switching were CMOS, GaAs, and SiGe. These technologies were also compared in terms of radiation tolerance.

1.2.1. Electronic Switching

Table 1 summarizes the current state of technology and trends in three semiconductor technologies, i.e. CMOS, GaAs, and SiGe for fast packet switching applications. Based on this comparison and trends in semiconductor technology, the following projections were made for the next 3-6 years:

- CMOS is expected to be the dominant technology for implementing complex functions due to its reliability, low power consumption, high densities, and rich libraries.
- Level of integration in GaAs ICs is expected to grow faster than that of CMOS but is not expected to reach that of CMOS. Higher supply voltage requirements of CMOS may slow level of integration as external electric fields need to be reduced at higher densities.
- Commercial SiGe products will be available, however these are expected to be mainly RF products. In the longer term, SiGe can be the preferred technology due to simplicity in manufacturing, higher speeds and integration, and low power consumption.
- As switch port speeds exceed 1.6 Gbit/s, which seems to be the current maximum for CMOS, GaAs ICs are expected to be used at the switch front-end and output processors. 0.2μm CMOS technology is expected to be mainly applied to core switching and control functions which require high integration and low power dissipation.

- Further increases in switching speeds can be obtained by using wider buses and ping-pong memory arrangements and in the longer term by using GaAs Heterojunction Bipolar Transistor (HBT) for core functions at the expense of power, size, and cost.

	CMOS	GaAs	SiGe
Technology Review	VLSI technology development has been and will probably remain focused on Silicon CMOS. Very high densities allow highly complex functions to be implemented on a single chip. Very stable technology. Extensive libraries.	In use for more than 25 years, mainly applied to simple circuits such as solid-state lasers and RF amplifiers. GaAs IC construction is similar to CMOS, but somewhat simpler. Low yields compared to Silicon. Limited libraries. Lower degree of integration prevents complex functions to be implemented on a single chip.	IBM started SiGe research in 1982. SiGe combines integration and cost benefits of Si with the speed of GaAs. IBM is in the final process of qualifying SiGe technology for volume production (VCOs, LNAs, power amplifiers, mixers, digital delay lines). Future ICs may combine low-power high-density CMOS technology with high speed SiGe technology to perform many analog and digital functions on the same chip.
Component Density	~ 2.0×10^7 transistors/chip As miniaturization increases external voltages must be reduced. In CMOS shrinking supply voltages may slow speed.	~ 1.0×10^6 transistors/chip GaAs VLSI trails behind CMOS in feature sizes and component density. Technologies are converging in packing density. In GaAs, voltages can be dropped down to 1 V without impact on signal speed.	~ 1.0×10^4 transistors/chip The miniaturization/speed limit of CMOS can be exceeded by SiGe in the future.
Speed	150 ps gate delay	70 ps gate delay Higher performance than CMOS due to higher maximum frequency of operation	20 ps gate delay Up to 100 GHz operating frequency, will replace more expensive GaAs RF technology. 12 bit digital-to-analog converter that processes data at 1.0 G samples/s.

Table 1: CMOS, GaAs, and SiGe technology comparison for digital switching

	CMOS	GaAs	SiGe
Power	Typical gate power of 2-3 μW/MHz Gates use no power when idle. Reducing power supply voltages proportionally increases delay.	Typical gate power of 30-100μW All logic gates use up power regardless of the switching state. Power supply voltages can be reduced down to 1 V without degrading speed.	Lower power consumption than GaAs. Gates use no power when idle. Power consumption per switching event is about half of Si CMOS.
Radiation Hardness	Low tolerance to total radiation (~ 10^3 - 10^5 Rad-Si). Fairly good immunity to SEUs.	Inherently tolerant to total radiation dosage (> 10^7 Rad-Si) GaAs FET ICs are degraded by heavy ions (SEUs). Latch-up free. GaAs HBT ICs are more tolerant to heavy ions.	No data
Feature Size	0.25 - 0.35 μm	0.40 μm	No data
Switch Speed	Commercial: 1.6 (Gbit/s)/port 16x16 chip (IBM, 0.35μm) 400 (Mbit/s)/port 16x16 chip (IBM, 0.5 μm) Research/Development: 10 (Gbit/s)/port 32x32 multi chip (Tiny Tera, Stanford University)	Commercial: 1.3 (Gbit/s)/port 16x16 chip (TQS), 800 (Mbit/s)/port 32x32 chip (TQS), 1.25 (Gbit/s)/port 16x32 chip (Vitesse) 4x1 Mux (622 Mbit/s - 2.4 Mbit/s) (Vitesse) Research/Development: 2.6 (Gbit/s)/port 8x8 (0.5μm GaAs)	No data

Table 1 (Cont.): CMOS, GaAs, and SiGe technology comparison for digital switching

1.2.2. Optical Switching

The majority of the research into optical switching is aimed at terrestrial networks. This is driven by the continued rapid progress in the deployment of fiber optic communications. The goal of optical switching in terrestrial networks is the creation of totally optical, transparent terrestrial networks where transmission formats used by the end points can be chosen independently from the network. Mainstream research and development in the area of switching is still solidly based on electronics.

The near term technology of a photonic switching fabric is optical interconnect with electronic control. Fully optical switching, where both the controlling and the controlled signals are optical is a long term technology as optical memories and logic will be power inefficient and slow in comparison with electronic components in the foreseeable future. This is because there is no practical optical equivalent to the electronic transistor and therefore photons can be neither slowed down, localized, nor stored conveniently. Optical transistors have been proposed for use in optical computers. These photonic transistors rely on optical interference that occurs between two light sources passing through a thin hologram which are accurately synchronized to create the proper interference pattern. Although optical buffering can be done using fiber delay lines, this technology is not mature at present.

Current commercial applications for photonic switching using electronic control are primarily in the area of cross-connects and add-drop multiplexers where the control functions are slow or infrequent but where large bandwidths are switched. Simple photonic switch networks using Wavelength Division Multiplexing (WDM) also belong to this category, and are the near term vision of photonic switching

One of the important factors that make integrated optics different from integrated electronics is packaging. Packaging is much more complex for photonic ICs than for electronic ICs and it will take a long time before integrated optic components with a limited functionality can compete with micro-optic or fiber-optic alternatives.

With the abundance of new satellite ventures there has been a large research interest in the area of optical intersatellite links (ISL's) and some experimentation examining optical satellite feederlinks. Optical links have potential benefits for satellites including handling very high data rates, 2.5 to 10 Gbps which may be difficult to allocate at radio frequencies. Optical transmit and receive antenna equipment is small and lightweight compared to antenna subsystems used at radio frequencies. Furthermore, optical links are not as susceptible to mutual interference due to high antenna directivity. Therefore they can use the amplifier efficiently without interference. Disadvantages of optical links for satellites include high pointing accuracy requirement, maturity of radio transmission technology compared to optical, and in the case of feederlinks the performance is strongly affected by the weather condition, e.g. clouds and fog. Research into optical links for satellites has so far been concentrated on the transmit and receive portions of the link and not on switching.

Optical packet switching technology is in its infancy compared to electronic switch technology. Optical logic is not available and won't be for the foreseeable future. The level of integration in optical switches is orders of magnitude lower than electronic switches while the chip dimensions are orders of magnitude larger. Optical switching speeds are slower than electronic switches and optical switches dissipate more energy. Furthermore, several major obstacles in packaging of photonic IC's must be overcome in order for optical switches to reach a significant level of complexity. It is not expected that photonic IC's will become a significant part of the optical switching market in the next several years. Therefore, the conclusion of this study is that there seems to be very little advantage to be gained by using optical packet switching in satellites.

1.2.3. Radiation Tolerance

One of the most important factors that need to be considered when selecting the technology for the next generation on-board packet switch is radiation.

The effect of total radiation dose received over a long time period and the effect of transient but intense radiation on the semiconductor are different. While total radiation dose causes ionization, transient surges of radiation (solar flares and galactic cosmic rays) cause ionization, latch-up, and single event upset (SEU). A

semiconductor's radiation tolerance is specified in terms of its tolerance to total radiation (rad-Si), radiation intensity required to cause latch-ups, and radiation intensity required to cause SEUs. Radiation intensity can be measured in terms of radiation dose rate (rad/s) or in terms of an ion's Linear Energy Transfer (MeV/mg/cm^2). The total radiation dosage that satellite electronics parts will receive depends on the orbit angle and altitude, location, and shield thickness. This is illustrated in Figure 1. It can be seen that with a 2 mm Al shield, total radiation absorbed per year can range from 1 krad to 100 krad. The Linear Energy Transfer (LET) of most ions observed in the space environment is less than 40 MeV/mg/cm^2.

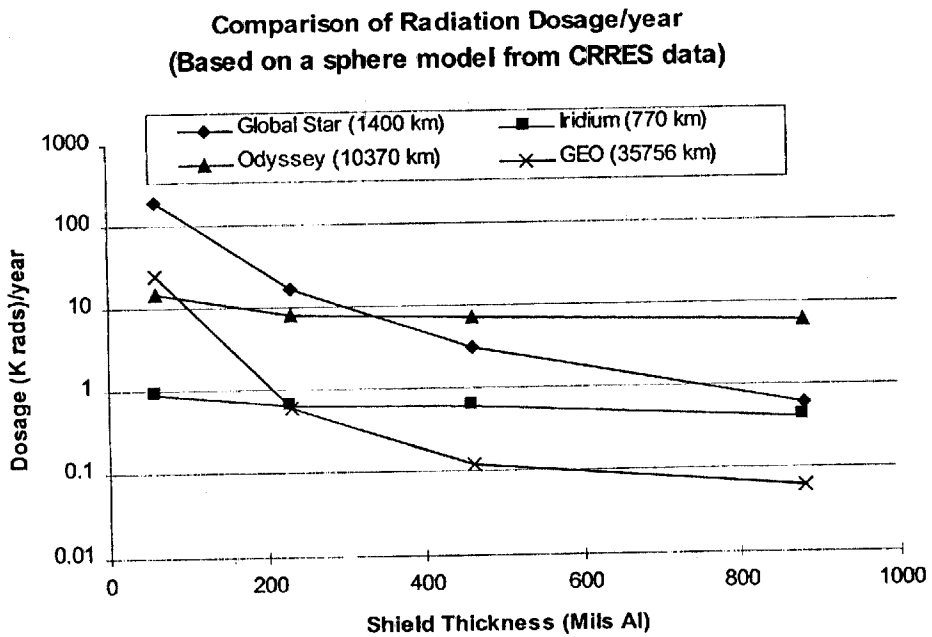


Figure 1: Dependence of total radiation dosage on orbital location

A comparison of radiation tolerance of different semiconductor technologies is given in Table 2. It can be seen that while CMOS technology is inherently tolerant to latchups and upsets it is prone to total dose radiation. Conversely, GaAs technology is inherently tolerant to total dose, however it suffers from upsets. Radiation hardened CMOS technology can provide the level of radiation tolerance that is required for space communications. GaAs ICs can be SEU hardened by low temperature grown GaAs, however manufacturability issues need to be resolved. SEU hardened GaAs ICs are not commercially available at the present.

	Total Dose (Rad-Si)	Latchup (Rad/s)	Upset (Rad/s)
Bulk CMOS	1.0×10^3 - 1.0×10^5	1.0×10^9	5.0×10^7
Rad hard CMOS	1.0×10^5 - 1.0×10^6	7.0×10^9	5.0×10^7 - 3.0×10^8
CMOS/SOS/SOI	3.0×10^3 - 7.0×10^4	1.0×10^{11}	1.0×10^9
Rad hard CMOS/SOS/SOI	1.0×10^5 - 1.0×10^6	high	1.0×10^{10}
BiMOS	1.0×10^4 - 8.0×10^7	3.0×10^9	1.0×10^8
GaAs (HBT)	1.0×10^6 - 3×10^7	2.0×10^{10}	1.0×10^8
GaAs (FET)	~ 1.0×10^6 - 3×10^7	~ 2.0×10^{10}	Poor (< 1.0 MeV/mg/cm^2)

Table 2: Radiation Tolerance of CMOS and GaAs ICs

1.2.4. Summary of Technology Review

The next generation on-board switch should be based on CMOS or a combination of CMOS and GaAs technologies where GaAs ICs are used at the front-end and output processors and CMOS is used in core switching and control functions which require high integration and low power dissipation. Radiation hardened CMOS ICs with access times as low as 15-20 ns are commercially available. Access times of 10 ns are expected to be reached in the next 3-6 years. GaAs FET technology is prone to SEUs and there are no commercially available rad-hard GaAs FET ICs at the present. GaAs HBT technology is more tolerant to SEUs, however they have very high power requirements. Shielding, rad-hardening, and fault tolerant architectures that can correct SEUs should be used concurrently to achieve required level of radiation tolerance for a given orbit.

1.3. Next Generation On-Board Switch

1.3.1 Current Satellite and Terrestrial Switch Capabilities

In order to define a system concept for the next generation on-board switch, the capabilities of proposed Ka-band system satellite switches and high end terrestrial switches were reviewed. The satellite systems considered were Astrolink, Celestri, and Teledesic. Table 3 provides a summary of these satellite systems' capabilities.

	Astrolink	Celestri	Teledesic
Coverage	Global (except oceans)	Global	Global
Frequency Band	Ka	Ka	Ka
No. of satellites	9	63	288
Constellation	5 Geo Orbital slots	LEO (1400 km), 7 planes with 9 satellites/plane	LEO (< 1400 km),12 planes with 24 satellites/plane
Satellite Capacity	7.0 Gbit/s	17.5 Gbit/s	13.3 Gbit/s
ISL	2 ISLs at 450Mbit/s at 60 GHz	6 optical links at 4.5 Gbit/s	1 Gbit/s at 60 GHz
Onboard Switching	Fast Packet Switch (ATM switch with modified cell header, VPI/VCI translation)	Fast Packet Switch (cell relay routing, individual cells are routed through ATM switches based on tag appended to the cells)	Fast Packet Switch (short, fixed length packets, destination-based packet addressing and a adaptive packet routing).
No. Transp.	58	Phased Array	64
Transponder BW	125 MHz	1 GHz divided into segments of 20, 32.8, 104, and 311 MHz	396 MHz
No. Of Beams	44 subscriber beams at up to 100 Mbit/s, 14 gateway beams at 113 Mbit/s	432 uplink, 260 downlink beams (both fixed)	576
Access Schemes	Uplink: TDMA/FDMA at 416/2048/10240 kbit/s Downlink: 100 Mbit/s TDM Gateway: 113 Mbit/s TDMA up, TDM down	Uplink: Demand-assigned FDMA/TDMA, 2.048/10.0/51.84/155.51 Mbit/s Downlink: FDM/TDM	Uplink: FDMA/TDMA at 224 kbit/s Downlink: TDMA at 324 Mbit/s High-speed links at 1.2 Gbit/s
Service Bit Rates	16 kbit/s to 10.24 Mbit/s (user), up to 113 Mbit/s (gateway)	64 kbit/s to 10 Mbit/s (user) and 155 Mbit/s (gateway)	16 kbit/s - 2.048 Mbit/s, 155 Mbit/s - 1.2 Gbit/s

Table 3: Astrolink, Celestri, and Teledesic System Overview

The on-board switching characteristics of these system can be summarized as follows: The Astrolink on-board switch provides connectivity among 58 beams and 2 ISLs with a total throughput of about 7 Gbit/s. The Celestri on-board switch provides connectivity among 432 up-link, 260 down-link beams, and 6 ISLs with about 17.5 Gbit/s of throughput. The Teledesic on-board switch provides connectivity among 576 beams with 13.3 Gbit/s of throughput. In all three systems, switching is based on fixed-length packets.

In terrestrial networks, switches with 25 Gbit/s to 100 Gbit/s throughput and 8x8 to 16x16 connectivity are commercially available. Switches with 100 Gbit/s to 1 Terabit/s throughput are being developed. The Thunder and Lightning switch developed at the University of California in Santa Barbara and the Tiny Tera switch developed at Stanford University are two examples. The Thunder and Lightning switch uses extensive multiplexing and demultiplexing and ATM cell-wide buses to achieve a throughput of 160 Gbit/s. This switch uses GaAs technology for implementing the input and output processors and CMOS technology for the switch core. The Tiny Tera is a 32x32 switch with 320 Gbit/s of throughput. This switch is implemented using CMOS technology exclusively.

Considering these capabilities in the currently proposed Ka band satellite switches and terrestrial switches, a switch throughput of 40-80 Gbit/s and a beam connectivity in the order of 500x500 was studied for the next generation on-board packet switch.

1.3.2. High Level Design for Next Generation On-Board Packet Switch

Despite recent advances in switch architectures, practical switch dimensions continue to be severely limited by technological and physical constraints of packaging. If a specific design is implemented in a VLSI chip, the input/output pin limitation restricts the switch size to approximately 100x100 with 64x64 or 32x32 as more practical values. The beam connectivity requirements of next generation packet switching satellites (100x100 - 500x500) can be met by using a growable switch architecture. A growable switch architecture employs hierarchical multiplexing of incoming signals to a higher speed for switching in the internal core fabric.

Considering the technology in currently available high-end terrestrial packet switches, two architectures were considered for the next generation on-board switch: shared memory switch with hierarchical multiplexing and crossbar switch with hierarchical multiplexing. Shared memory switch architectures were further divided into two as total memory sharing with RAM and total memory sharing with growable register array macros.

Total memory sharing with RAM requires wide data bus and fast RAM. One advantage of this architecture is that all buffering can be implemented within the switch fabric. Total memory sharing with growable register array has the advantage of delivering faster data access times than RAM. However the amount of internal buffering that can be performed by register arrays is limited, and this architecture requires external buffers. A crossbar switch can accommodate larger switch sizes in one chip compared to shared memory architectures. However, a crossbar switch requires input and output buffers, contention control hardware, external control to configure switch connectivity at each time slot, and higher clock speeds.

Of these three architectures, the one selected for the next generation on-board packet switch is the shared buffer architecture with growable register arrays. In this architecture switch speed is not limited by switch dimension, RAM speed, or the bus width unlike the other two architectures. In addition, commercial products available (the IBM Prizma switch) offer desirable features such as modularity, built in flow control, protocol independence, flexible multicast capability, and multiple priorities. The IBM Prizma switch is a 16x16 1.6 Gbit/s per port single chip element from which larger self routing switch fabrics can be constructed with Tera bit/s of throughput. Our recommendation is to use a single-chip switch component with similar functionality to construct the next generation on-board packet switch. The IBM Prizma switch chip is based on CMOS 0.35 μm technology and comprises about 5 million transistors. This is an achievable level of integration for space qualified ICs in the next 3 to 6 years.

Figure 2 illustrates the construction of a 32x32 switch with 40 Gbit/s of throughput from the 16x16 shared memory switch fabric. This design uses 6 switch chips. By using demultiplexing at the input processors link speeds of up to 2.4 Gbit/s can be supported.

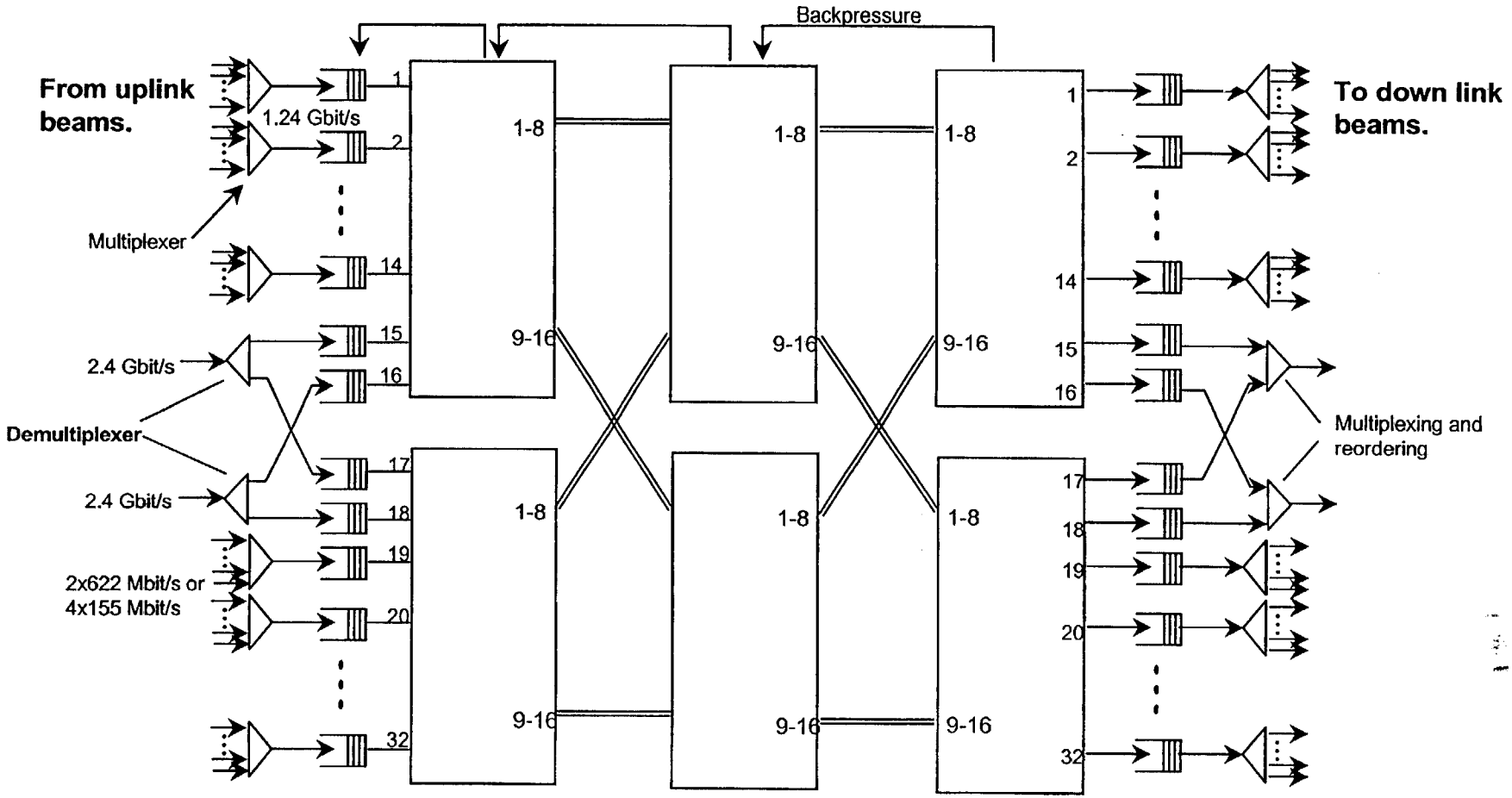


Figure 2: 32x32 switch with 40 Gbit/s throughput constructed from 16x16 shared memory switch fabric

1.4. Next Generation Satellite System

In this section a satellite system concept that uses the next generation fast packet switch is described. Subsequently, this system is compared with an alternative concept.

1.4.1. Proposed Satellite System

The proposed system is a hybrid of geosynchronous earth orbit (GEO) satellites and Stratospheric Telecommunications Service (STS) systems. The total constellation consists of four GEO satellites and 32 STS systems. The GEO satellites provide wideband data transport and multimedia communications services while the STS system is used to supplement the GEO capacity in highly populated geographic areas with high traffic demand. A typical coverage area of a single STS system is about 60 to 100 miles in diameter. Optical crosslinks are used for GEO-GEO, GEO-STS, and STS-STS links for global network interconnection. Figure 3 illustrates the hybrid GEO-STS communications system. The selected frequency band is the V-band where 3 GHz is available for GEO services and a 300 MHz portion is available for STS services (only 100 MHz per platform). In the proposed system, this frequency band is allocated between the GEO and STS systems as follows:

	Uplink	Downlink
STS	100 MHz in 47.9 - 48.2 GHz (3 STS can co-exist)	100 MHz in 47.2 - 47.5 GHz (3 STS can co-exist)
GEO	48.2 - 50.2 GHz	38.5 - 40.5 GHz

In this system we use an STS similar to the one proposed by Sky Station International. This system has about 700 user beams and 15 gateway beams. The uplink access is MFTDMA for the user link and MFTDM for the gateway links. The uplink bit rate is 5x2 Mbit/s in the user link and 8x34 Mbit/s in the gateway link. Downlink access is TDM in both the user link and the gateway link. Downlink bit rate is 10 Mbit/s in the user link and 8x34 Mbit/s in the gateway link. Total user link capacity is 7 Gbit/s and total gateway link capacity is 4 Gbit/s resulting in a total STS capacity of 11 Gbit/s.

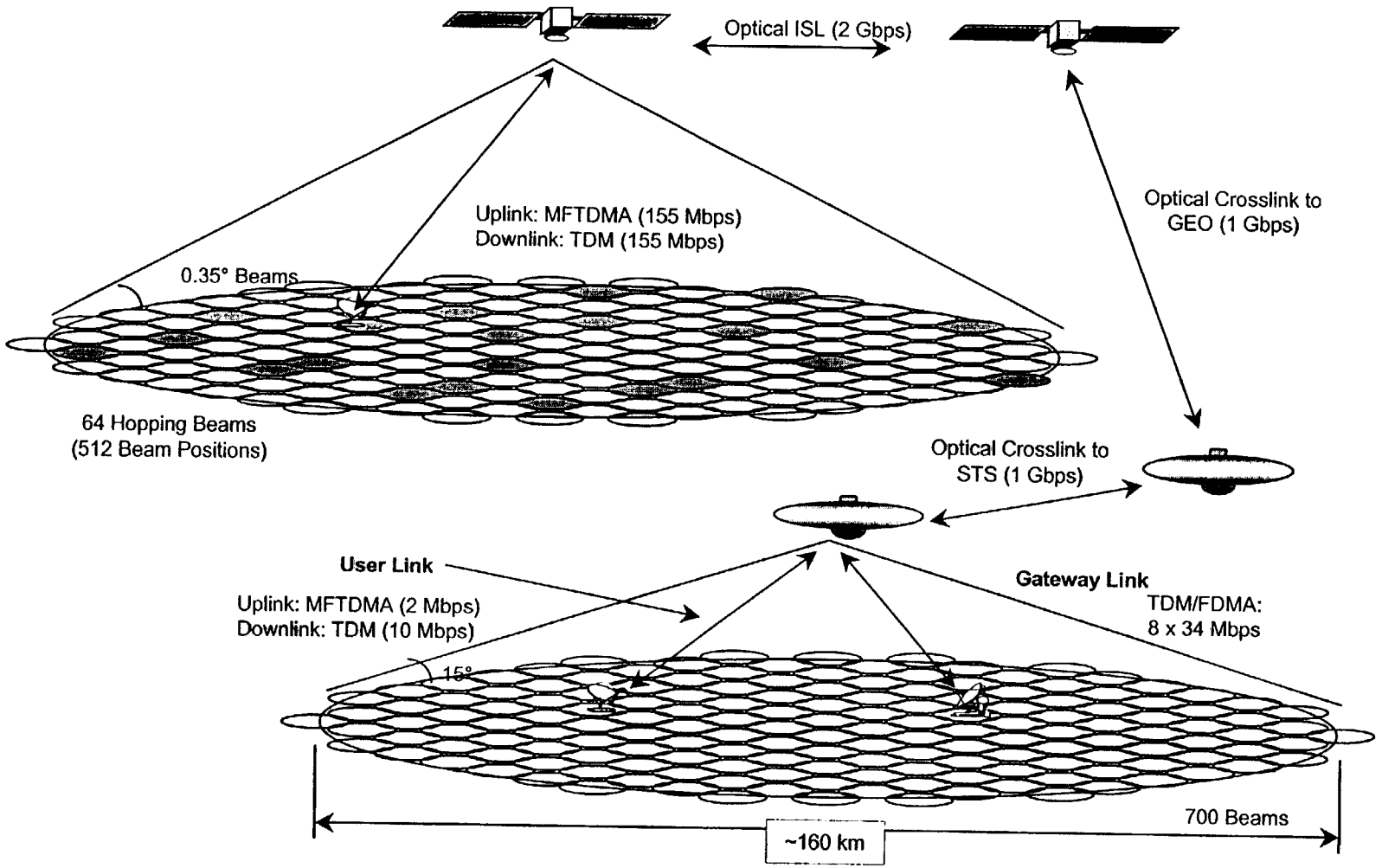


Figure 3: Proposed satellite system for using next generation on-board packet switch

The GEO system has 64 hopping beams in 512 beam positions. The modulation technique is QPSK both in the uplink and the downlink. Concatenated coding is used in both the uplink and the downlink. Both uplink and downlink access uses MFTDMA. Bit rate is 4x155 Mbit/s in the uplink and the downlink beams. Total user traffic capacity of the GEO system is 40 Gbit/s.

The on-board packet switch requirements for the GEO and the STS components of this system are summarized in Table 4. These requirements can be met by the switch design highlighted in Section 3. The STS on-board switch requires a throughput of only 14 Gbit/s. This switch can be implemented by using a 16x16, 1 Gbit/s per port single chip. User link and gateway link traffic are multiplexed at the switch input processors to 1 Gbit/s before they enter the core switch. The GEO satellite on-board switch can be implemented by using the three-stage architecture illustrated in Figure 2 by scaling up the core switch input port speeds from 1.2 Gbit/s to 1.625 Gbit/s.

	STS	GEO
System Capacity	11 Gbit/s	40 Gbit/s
Crosslink Capacity	1 Gbit/s	1 and 2 Gbit/s
Number of Crosslinks	3	8 and 2
Total Crosslink Capacity	3 Gbit/s	12 Gbit/s
Switch Capacity	14 Gbit/s	52 Gbit/s
Connectivity requirements	685 user beams 15 gateway beams 3 crosslinks (703x703 I/O ports at different speeds)	64 beams 10 crosslinks (74x74 I/O ports at different port speeds)

Table 4: On-board packet switch requirements for the hybrid STS-GEO system

1.4.2. Alternative Satellite System

This section describes an alternative satellite system using the fast packet switch concept developed earlier and compares it with the hybrid GEO-STS system described in the previous section. This satellite system is based on the V-band filing StarLynx.

The alternative satellite system is a hybrid GEO-MEO system. The total constellation consists of four GEO satellites at two GEO orbital positions and twenty MEO satellites. The MEO constellation consists of four planes with five satellites in each plane, inclined at 55 degrees with respect to the equator and in circular orbits at an altitude of 10,352 km. Optical GEO-GEO, GEO-MEO, and MEO-MEO crosslinks are used for global network interconnection.

MEO and GEO satellites use the same uplink and downlink frequency bands. The uplink frequency spectrum is a 1.1 GHz contiguous segment in the 45.5-46.7 GHz frequency band. The downlink frequency spectrum uses the the 37.5-38.6 GHz frequency band. The 1.1 GHz spectrum is divided into 4 segments of 270 MHz. Each beam uses two non-adjacent 270 MHz segments in opposite polarizations. Therefore, the effective bandwidth in each beam is 540 MHz in the uplink and in the downlink. The 270 MHz segment is further divided into three sub-segments of 90 MHz using FDMA. Each 90 MHz sub-segment supports six 8 Mbit/s CDMA carriers in the GEO system and eight 6 Mbit/s CDMA carriers in the MEO system. Each GEO satellite has 40 movable spot beams. Each MEO satellite has 32 spot beams.

The on-board packet switch requirements for the GEO and MEO components of this system are summarized in Table 5. These requirements can be met by the switch design illustrated in Figure 3 by running the core switch at 750 Mbit/s per port for the MEO system and at 550 Mbit/s per port for the GEO system. Appropriate multiplexers and demultiplexers are required at the input processors to match the traffic rate on the satellite beams and intersatellite links to these port speeds.

	MEO	GEO
System Capacity	9.2 Gbit/s	11.5 Gbit/s
Crosslink Capacity	3 Gbit/s	3 Gbit/s
Number of Crosslinks	5	2
Total Crosslink Capacity	15 Gbit/s	6 Gbit/s
Switch Capacity	24.2 Gbit/s	17.5 Gbit/s
Connectivity requirements	32 beams 5 crosslinks (37x37 I/O ports at different speeds)	40 beams 2 crosslinks (42x42 I/O ports at different port speeds)

Table 5: On-board packet switch requirements for the hybrid MEO-GEO system

When compared to the satellite system described above, the GEO-STS system has several advantages. The GEO-STS system does not require handover capability, simplifying terminal and communications payload design. The STS platforms are located at an altitude of about 21 km, significantly reducing propagation delay for user-STS communications. The STS platforms are relatively simpler to launch and the capability to bring them down to the ground for maintenance offers an additional advantage. The throughputs provided by the two systems are comparable.

1.5 Conclusions and Recommended Future Work

In this study, the currently available switching technologies and trends were analyzed, and a high level design for the next generation on-board fast packet switch was developed. Subsequently, a new satellite system concept that uses the proposed packet switch design was investigated. The time frame that was considered for implementing the proposed switch and satellite concept was the year 2002-2005 time frame.

As a continuation of this work effort, a follow-on study on the interworking issues between future terrestrial networks and the next generation satellite networks is recommended. In particular, the study may focus on signalling and transmission protocols and corresponding routing schemes that allow for, perhaps even capitalize on, the distinguishing attributes of the terrestrial and satellite systems. These attributes include time delay differences, point-to-multipoint and broadcast transmission capabilities, and channel quality differences. The dependence of these protocols and routing schemes on packet and data format, satellite system access method, and the onboard switch may be analyzed.

2. Switch Technology Review

- Electronic switching technology review, current technology and trends
- Optical switching technology review, current technology and trends
- Comparison of electronic and optical switching technologies
- Radiation issues for microelectronics in space systems
- Radiation tolerance of different semiconductors
- Conclusions of the technology review

2.1 Electronic Switching Technologies

Electronic Switching Technologies

- Super conductivity electronics
  - high bandwidth
  - low densities
  - high power
  - new technology
  - poor yields
  - special cooling requirements
- GaAs
  - high bandwidth
  - relatively high power

Electronic Switching Technologies

- SiGe
  - high bandwidth
  - low power
  - new technology
  - densities ~ 10 K
  - insufficient libraries for chip development
- CMOS
  - fairly high bandwidth
  - power proportional to bandwidth
  - very high densities
  - very stable technology

Technology Comparison

	CMOS	GaAs	SiGe
Technology Review	VLSI technology development has been and will probably remain focused on Silicon CMOS. Very high densities allow highly complex functions to be implemented on a single chip. Very stable technology. Extensive libraries.	In use for more than 25 years, mainly applied to simple circuits such as solid-state lasers and RF amplifiers. GaAs IC construction is similar to CMOS, but somewhat simpler. Low yields compared to Silicon. Limited libraries. Lower degree of integration prevents complex functions to be implemented on a single chip.	IBM started SiGe research in 1982. SiGe combines integration and cost benefits of Si with the speed of GaAs. IBM is in the final process of qualifying SiGe technology for volume production (VCOs, LNAs, power amplifiers, mixers, digital delay lines). Future ICs may combine low-power high-density CMOS technology with high speed SiGe technology to perform many analog and digital functions on the same chip.
Component Density	~ 2.0×10^7 transistors/chip As miniaturization increases external voltages must be reduced. In CMOS shrinking supply voltages may slow speed.	~ 1.0×10^6 transistors/chip GaAs VLSI trails behind CMOS in feature sizes and component density. Technologies are converging in packing density. In GaAs, voltages can be dropped down to 1 V without impact on signal speed.	~ 1.0×10^4 transistors/chip The miniaturization/speed limit of CMOS can be exceeded by SiGe in the future.
Speed	150 ps gate delay	70 ps gate delay Higher performance than CMOS due to higher maximum frequency of operation	20 ps gate delay Up to 100 GHz operating frequency, will replace more expensive GaAs RF technology. 12 bit digital-to-analog converter that processes data at 1.0 G samples/s.

Technology Comparison (Cont.)

	CMOS	GaAs	SiGe
Power	Typical gate power of 2-3 μW/MHz Gates use no power when idle. Reducing power supply voltages proportionally increases delay.	Typical gate power of 30-100μW All logic gates use up power regardless of the switching state. Power supply voltages can be reduced down to 1 V without degrading speed.	Lower power consumption than GaAs. Gates use no power when idle. Power consumption per switching event is about half of Si CMOS.
Radiation Hardness	Low tolerance to total radiation (~ 10^3 - 10^5 Rad-Si). Fairly good immunity to SEUs.	Inherently tolerant to total radiation dosage (> 10^7 Rad-Si) GaAs FET ICs are degraded by heavy ions (SEUs). Latch-up free. GaAs HBT ICs are more tolerant to heavy ions.	No data
Feature Size	0.25 - 0.35 μm	0.40 μm	No data
Switch Speed	Commercial: 1.6 (Gbit/s)/port 16x16 chip (IBM, 0.35μm) 400 (Mbit/s)/port 16x16 chip (IBM, 0.5 μm) Research/Development: 10 (Gbit/s)/port 32x32 multi chip (Tiny Tera, Stanford University)	Commercial: 1.3 (Gbit/s)/port 16x16 chip (TQS) , 800 (Mbit/s)/port 32x32 chip (TQS), 1.25 (Gbit/s)/port 16x32 chip (Vitesse) 4x1 Mux (622 Mbit/s - 2.4 Mbit/s) (Vitesse) Research/Development: 2.6 (Gbit/s)/port 8x8 (0.5μm GaAs)	No data

Trends, Projections, 3-6 years

	1998	2001	2004
Minimum Feature Size (μm)	0.25	0.18	0.13
Memory in bits/chip (Mbyte)	256	1000	4000
Memory Access Speed (ns)	10	8	6.5
Transistors per chip (Millions)	28	64	150
ASIC gates per chip (Millions)	14	26	50
Chip frequency (MHz) for a high performance on-chip clock	450	600	800
Switch on a Chip, throughput (Gbit/s)	25	~ 50	
Switch on a Chip, port speed (Gbit/s)	1.6	~ 3.2	
High-end ATM Switch Node, max. throughput (Gbit/s)	320	~ 600	
High-end ATM Switch Node, max. port speed (Gbit/s)	40	80	

- CMOS is expected to be the dominant technology for implementing complex functions due to its reliability, low power consumption, high densities, and rich libraries.
- Level of integration in GaAs ICs expected to grow faster than that of CMOS but not expected to reach CMOS. High voltage requirements of CMOS may slow level of integration.

Sources: *The National Technology Roadmap for Semiconductors, 1997, Semiconductor Industry Association*
S. E. Butner, et al., "On the limits of Electronic ATM Switching", IEEE Network, Nov./Dec. 1996,
T. Koinuma et al., ATM in B-ISDN Communication Systems and VLSI Realization, IEEE JSAC, April 1995
J. McCalpin, "Sustainable Memory Bandwidth in Current High Performance Computers", http://reality.sgi.com

Trends, Projections, 3-6 years (Cont.)

- Commercial SiGe products will be available, however these are expected to be mainly RF products. In the long term, SiGe can be the preferred technology due to simplicity in manufacturing, higher speeds and integration, and low power consumption.
- As port speeds exceed the 1.6 Gbit/s limit, which seems to be the current maximum for CMOS, Bipolar/GaAs ICs are expected to be used at the switch front-end and outputs. 0.2 μm CMOS technology is expected to be mainly applied to core switching and control functions which require high integration and low power dissipation.
- Further increases in switch speeds can be obtained by using wider buses (e.g. full ATM cell wide), ping-pong memory arrangements, and GaAs HBT based technology (in the long run) for core functions at the expense of power, size, and cost.

2.2 Optical Switching Technology

Technology Status

- Research is motivated by the goal of all-optical terrestrial networks
  - Eliminates the need for opto-electronic-opto conversions
  - Network transparency
  - Able to switch and route extremely high bandwidths
- Fully optical switch (Far in the future)
  - Photonic buffering, synchronization and control is either far too power consuming, and / or too slow relative to electronics

Technology Status (Cont.)

- Optical interconnect with electronic control (Commercially available)
  - Cross-connects and optical add-drop multiplexers
    - Used for disaster recovery, distribution, configuration and control
    - Avoids the issue of synchronization
    - Switching speed requirements are low
  - Optical switch networks
    - Research is concentrated in Wavelength Division Multiplexing (WDM) networks
    - Almost all WDM demonstrations to date have used a fixed mapping of wavelength to spatial port
    - Wavelength conversion is under intensive investigation but not yet practical

Commercial Products

WDM Systems

Alcatel Telecom
Artel Video Systems
Ciena Corp.
Fujitsu
IBM
Lucent Technologies
NEC
Nortel
Pirelli
Tellabs

WDM Devices

AG Electro-Optics
Alliance Fiber Optics
Amphenol Fiber Optics
Bosch Telecom
Canadian Instrumentation & Research Ltd.
Dicon Fiberoptics
Fibersense & Signals Inc.
GCA Fiberoptics Ltd.
Instruments S.A., Inc.
JDS Fitel
Lightwave Microsystems
Micron Optics, inc.
Nortel
Optical Corp. of America
Photonic Integration Research Inc.
Queensgate Instruments
Soltec Corp.
Alcatel Optronics
AMP
Aurora Associates
Broadband Communications Products
Corning, Inc.
E-Tek Dynamics, Inc.
GEC Marconi
Gould Fiber Optics Division
Integrated Optical Components, Ltd.
Kaifa Technology. Inc.
Lucent Technologies
MP Fiberoptics, Inc.
Oplink
Optilas
Photonic Technologies
Sifam

WDM Test Equipment

Anritsu Wiltron
Burleigh Instruments
Hewlett Packard
ILX Lightwave Corp.
Tektronics

Commercial Products (Cont.)

Manufacturer	Astarte	DiCon	JDS Fitel, Inc.	Optivision
Switch Size	8 x 8	1 x N and M x N (up to 100 channels)	1 x N (up to 100)	8 x 8
Technology	micro-optic device controlled electronically using piezoelectric elements	Optically passive device with motor control	Lens technology and motor control	Semiconductor with optical amplifiers
Switching Speed	150 msec	400 msec	15 msec	sub μsec
Insertion Loss	1.7 dB @1310 nm 1.9 dB @820 & 1550 nm	0.6 dB typ 1.2 dB max	0.7 dB	0 dB ±3 dB
Throughput	40 Gbps demonstrated			> 3 THz

Commercial Switches

Optical Components

- Fiber based: Made from fiber, such as couplers, polarizers and filters
- Integrated-Optic devices where light is guided in planar waveguides
  - Single-component devices such as lasers, semiconductor optical amplifiers, and phase modulators
  - photonic integrated circuits (PIC's) where a number of optical elements are monolithically integrated
  - Technologies
    - fiber-matched waveguides - lithiumniobate ($LiNbO_3$)
    - Semiconductor optical chips - indium phosphide (InP)
- Microoptic: Employs techniques where light is not guided but relies on diffractive/reflective elements such as lenses/mirrors.

Component Market

- There is more than a 20 year time difference in development between integrated electronics and integrated optics
- Component market is approximately $1.4 billion in North America
  - 85%: Active components such as lasers and photodiodes
  - 11%: Fiber based couplers
  - 1-2%: Integrated optic and microoptic products
- The market for complex optical functionalities is so small that it is not likely to be substantial until after the year 2005

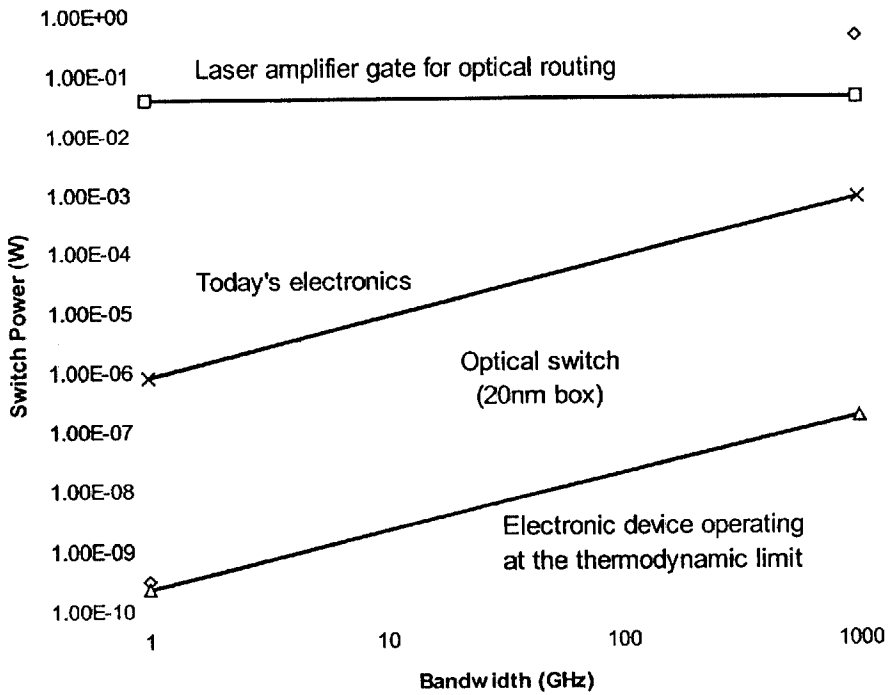
Comparison of Photonics and Electronics

- Packaging is much more complex for photonics than for electronics
  - fiber-chip coupling
  - reflections
  - temperature sensitivity
- Throughput
  - electronic switches - 1.2 Mbps/port
  - Photonic switches - >40 Gbps/port

Comparison of Photonics and Electronics

- Single Chip Size
  - Electronics: only a few microns.
  - Optical space-division switches are limited to less than 100 input and output ports
  - $LiNb0_3$:
    - Many millimeters to several centimeters
    - 16x16 switch has been demonstrated with an area of 69x2.5 mm
  - Optical semi-conductor
    - Smaller than $LiNb0_3$ technology, but the decrease is less than an order of magnitude
    - A 2x2 laser amplifier switch is 2 mm

Comparison of Photonics and Electronics



Theoretical comparison of switch power for an optical absorption switch compared to electronic switches

Comparison of Photonics and Electronics

- The optical switch power is scaled with the volume of the device and with the square of the frequency
- According to the theoretical comparison above, optical switches could compete with today's electronics up to about 50 GHz if they could be shrunk to a box size of 20nm
- It is expected that the electronics will progress toward the thermodynamic limit faster than the optical technology will progress toward smaller size.
- Conclusions
  - Optical switches consume more power than electronic switches
  - For the same power, optical switches will switch slower than electronic switches

Comparison of Photonics and Electronics: Conclusions

- Optical logic elements don't exist
- Optical switching lags behind electronic switching in terms of switching speed / power consumption, maturity of the technology, integration densities, and packaging cost.
- Research into optical links for satellites has so far been concentrated on the transmit and receive portions of the link and not on switching.
- Per packet switching will most likely be required and this is feasible only in the electronic domain
- The next generation of multimedia satellite may process up to 10 Gbits/s per port. GaAs ICs can handle this throughput.

2.3 Radiation Tolerance

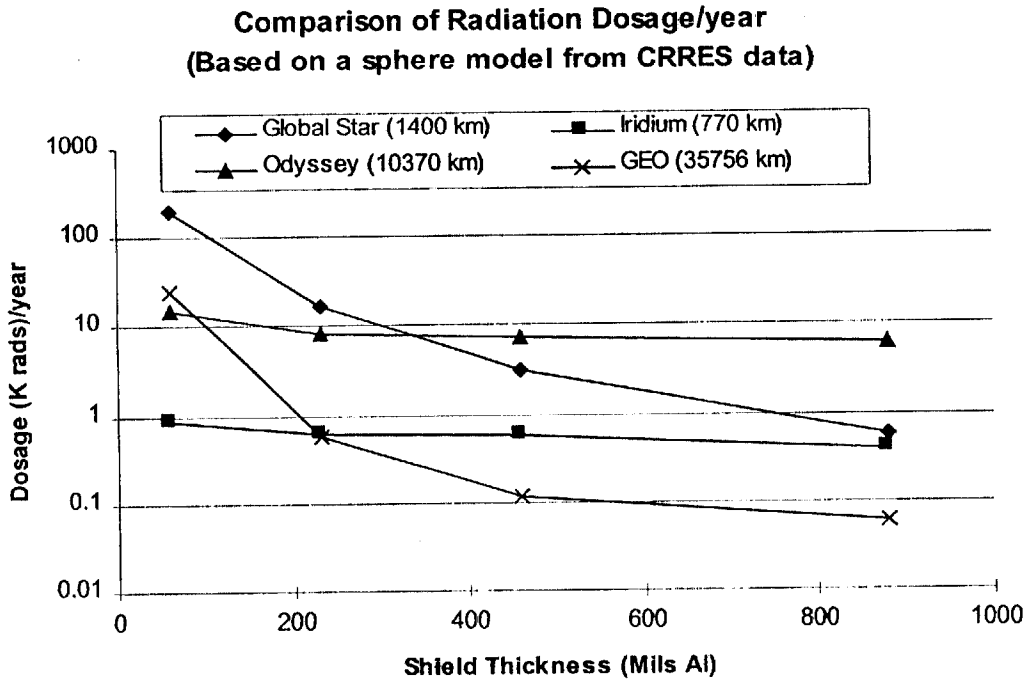
Space Radiation Environment

- Significant dependence on orbital location, angle of inclination, coordinates, and time.
- Three major sources of radiation:
  - Electrons and protons trapped by the Earth's magnetosphere (between altitudes of approximately 1000 km and 32,000 km).
    - Higher energy particles concentrated at lower altitudes
    - Significant exposure at LEO in South Atlantic
  - Solar flares (particularly protons)
    - At LEO proton fluxes are lower at solar flares !
  - Galactic cosmic rays (GCR)
    - Lower radiation observed at LEO
- In spite of the uncertainty in radiation levels due to solar flares, sophisticated models exist for calculating expected radiation levels for a particular mission (JPL Publication 96-25).

Shielding

- A nominal shield (< 100 Mils Al, 2-3 mm Al) can reduce the dose by several orders of magnitude. When this is not sufficient for certain circuits, spot shielding of the part is possible.
- Most effective in reducing the low to moderate energy component (electrons and protons). For very high energy radiation such as gamma rays and cosmic ray ions, shielding is not particularly effective.
- Typically, beyond a few tens of Mils of Al-equivalent shielding, the weight penalty outweighs the added benefit of radiation shielding.

Radiation Dosage Dependence on Orbit



Single Event Effects

- Single Event Effects (SEEs) include Single Event Upsets (SEUs) and latches
- CMOS/GaAs ICs are susceptible to SEEs (from both cosmic-ray heavy ions and protons trapped in the Earth's radiation belts.
- The Linear Energy Transfer (LET), measured in MeV/mg/cm^2 of an ion is a common measure of the ion's effectiveness in causing SEEs.
- The LET of most ions observed in the space environment are less than 40 MeV/mg/cm^2.
- Unhardened CMOS ICs typically have LET thresholds less than 3 MeV/mg/cm^2. Radiation hardened CMOS ICs that tolerate LETs of 80 Mev/gm/cm^2 are commercially available.

Single Event Effects (Cont.)

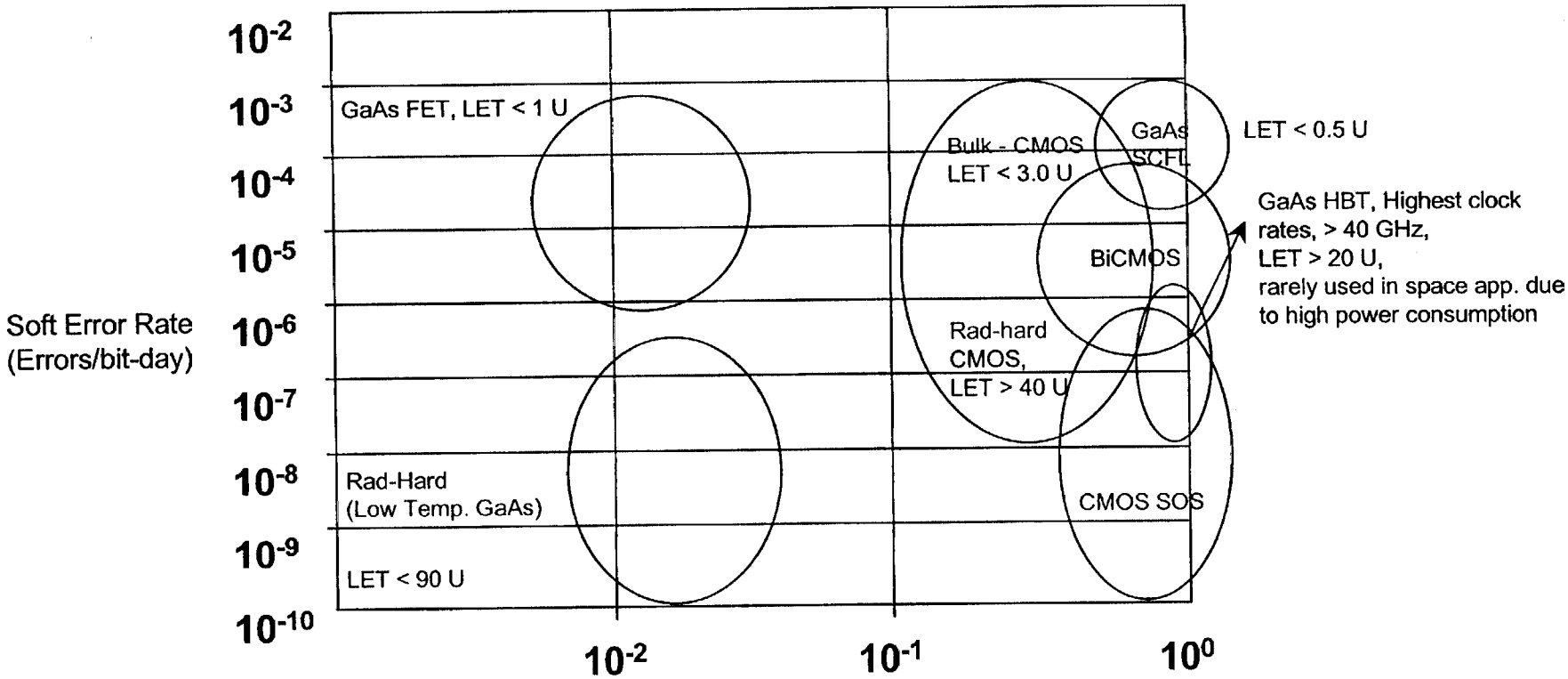
- Unhardened GaAs FET-based ICs have LET thresholds of less than 1 MeV/mg/cm^2 resulting in predicted SEU rates in the order of 10^{-4} - 10^{-3} in geosynchronous orbit.
- Shielding (0.25 mm Al) can eliminate the effect of trapped protons
- GaAs ICs can be SEU hardened by low temperature grown GaAs - manufacturability and reproducibility issues need to be resolved.
- SEU sensitivity increases as feature sizes decrease.
- Currently SEU hardened GaAs ICs are not commercially available.

Single Event Effect Dependence on Orbit

Orbit	Sources	Effects
Low orbit, low inclination	Trapped Protons	SEE in the South Atlantic
Polar orbit	Solar Protons Cosmic Rays Trapped Protons	SEE SEE (essentially at the poles) SEE
Elliptic Orbit, high inclination	Trapped Protons Solar Protons Cosmic Rays	SEE at perigee SEE at higher altitude SEE at higher altitude
GPS orbit	Solar Protons Cosmic Rays	SEE during solar events SEE in polar zones
GEO orbit	Solar Protons Cosmic Rays	SEE during solar events SEE

Measurement results on orbit and geographic location dependence of SEEs can be found in, "Review of Commercial Spacecraft Anomalies and Single Event Effect Occurrences C. Barillot et al., IEEE Trans. on Nuclear Science, April 1996, pp. 453 - 460.

Predicted SEU Rate for Geosynchronous Orbit



U: Unit for Linear Energy Transfer (LET), MeV/mg/cm^2

Source: D. McMorrow et al., "Single-Event Phenomena in GaAs Devices and Circuits", IEEE Trans. on Nuclear Science, April 1996, pp628-644

Radiation Tolerance of CMOS and GaAs ICs

	Total Dose (Rad-Si)	Latchup (Rad/s)	Upset (Rad/s)
Bulk CMOS	1.0×10^3 - 1.0×10^5	1.0×10^9	5.0×10^7
Rad hard CMOS	1.0×10^5 - 1.0×10^6	7.0×10^9	5.0×10^7 - 3.0×10^8
CMOS/SOS/SOI	3.0×10^3 - 7.0×10^4	1.0×10^{11}	1.0×10^9
Rad hard CMOS/SOS/SOI	1.0×10^5 - 1.0×10^6	high	1.0×10^{10}
BiMOS	1.0×10^4 - 8.0×10^7	3.0×10^9	1.0×10^8
GaAs (HBT)	1.0×10^6 - 3×10^7	2.0×10^{10}	1.0×10^8
GaAs (FET)	~ 1.0×10^6 - 3×10^7	~ 2.0×10^{10}	Poor (< 1.0 MeV/mg/cm^2)

Sources: *Harris Semiconductor Data Book*
Kato et al., IEEE JSAC, May 1987, pp. 685 - 699
JPL Publication 96-25, "GaAs MMIC Reliability Assurance Guidelines for Space Applications

Hardness Levels and Speed by Technology

Rad-Hard Technology	Total Dose (Rad-Si)	Dose Rate (Rad-Si/s)	RAM Cycle Time (ns)	RAM size (kbytes)	LET Threshold ($MeV/mg/cm^2$)
Hardened Gate	2.0×10^4	1.0×10^8	450	1	37
Gamma Guard Ring with Hardened Gate	1.0×10^5	1.0×10^8	250	4	36
Gamma Guard Ring with Hardened gate and Cross-Coupled Resistors	1.0×10^5	1.0×10^8	250	4	> 80
Hardened Field with Hardened Gate	2.0×10^5	1.0×10^9	90	16	20
Hardened Field with Hardened Gate and Cross-Coupled Resistors	2.0×10^5	1.0×10^9	90	16	41
Silicon-On-Insulator	1.0×10^6	1.0×10^{10}	50	64	40
Bulk CMOS on EPI	1.0×10^6	1.0×10^9	30	1000	120

- Source: Harris Semiconductor and Lockheed Martin (Bulk CMOS on EPI) product information
- Radiation hardened devices are still scarce and expensive due to difficult processing, low run rates, complex testing, and periodic radiation testing. This situation is changing as manufacturers develop a wider selection of radiation hardened common usage devices such as memories, microprocessors, and peripheral chips. However, radiation hardened ICs will probably remain primarily custom and ASIC semicustom devices for many years to come.

Technology Study Summary

- The next generation on-board switch should be based on CMOS or a combination of CMOS/GaAs technologies where GaAs ICs are used at the front-end and output processors and CMOS is used in core switching and control functions which require high integration and low power dissipation.
- Radiation hardened CMOS ICs with access times in the order of 30 ns are commercially available. GaAs FET technology is prone to SEEs and there are no commercially available rad-hard GaAs FET ICs. GaAs HBT technology is more tolerant to SEEs, however they have very high power requirements.
- Shielding, rad-hardening, and fault tolerant architectures that can correct SEEs should be used concurrently to achieve required level of radiation tolerance for a given orbit

3. Next Generation On-Board Switch Design

- Review of proposed Ka-band satellite systems on-board switching capabilities
- Review of current terrestrial fast packet switch capabilities
- Next generation on-board packet switch size and throughput
- Review of fast packet switch architectures
- High level design for next generation on-board packet switch

3.1 Proposed Ka-band Satellite Systems' On-Board Switching Capabilities

Astrolink, Celestri, and Teledesic - System Overview

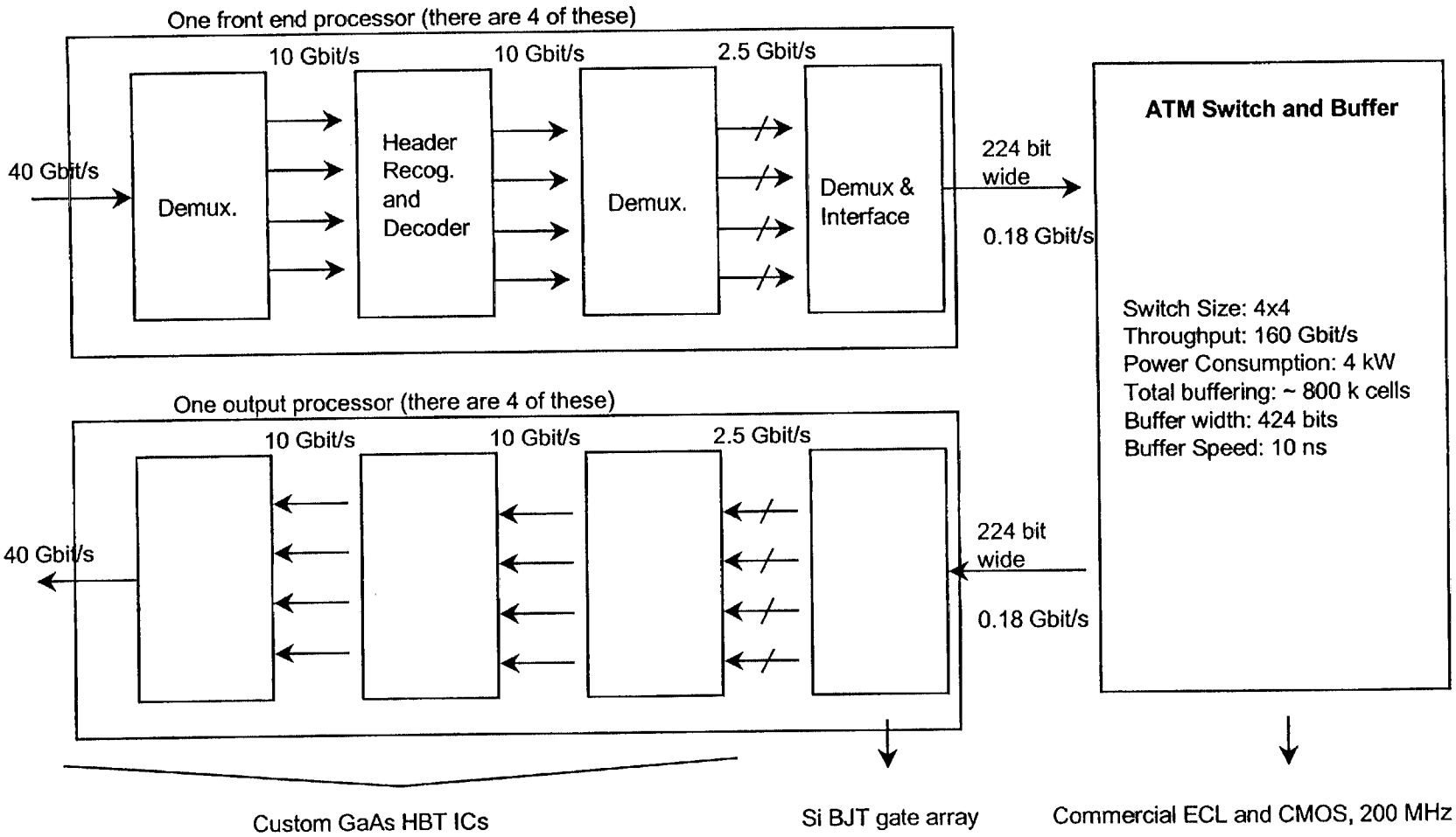
	Astrolink	Celestri	Teledesic
Coverage	Global (except oceans)	Global	Global
Frequency Band	Ka	Ka	Ka
No. of satellites	9	63	288
Constellation	5 Geo Orbital slots	LEO (1400 km), 7 planes with 9 satellites/plane	LEO (< 1400 km),12 planes with 24 satellites/plane
Satellite Capacity	7.0 Gbit/s	17.5 Gbit/s	13.3 Gbit/s
ISL	2 ISLs at 450Mbit/s at 60 GHz	6 optical links at 4.5 Gbit/s	1 Gbit/s at 60 GHz
Onboard Switching	Fast Packet Switch (ATM switch with modified cell header, VPI/VCI translation)	Fast Packet Switch (cell relay routing, individual cells are routed through ATM switches based on tag appended to the cells)	Fast Packet Switch (short, fixed length packets, destination-based packet addressing and a adaptive packet routing).
No. Transp.	58	Phased Array	64
Transponder BW	125 MHz	1 GHz divided into segments of 20, 32.8, 104, and 311 MHz	396 MHz
No. Of Beams	44 subscriber beams at up to 100 Mbit/s, 14 gateway beams at 113 Mbit/s	432 uplink, 260 downlink beams (both fixed)	576
Access Schemes	Uplink: TDMA/FDMA at 416/2048/10240 kbit/s Downlink: 100 Mbit/s TDM Gateway: 113 Mbit/s TDMA up, TDM down	Uplink: Demand-assigned FDMA/TDMA, 2.048/10.0/51.84/155.51 Mbit/s Downlink: FDM/TDM	Uplink: FDMA/TDMA at 224 kbit/s Downlink: TDMA at 324 Mbit/s High-speed links at 1.2 Gbit/s
Service Bit Rates	16 kbit/s to 10.24 Mbit/s (user), up to 113 Mbit/s (gateway)	64 kbit/s to 10 Mbit/s (user) and 155 Mbit/s (gateway)	16 kbit/s - 2.048 Mbit/s, 155 Mbit/s - 1.2 Gbit/s

Astrolink, Celestri, and Teledesic - On-Board Switch Capabilities

- Astrolink
  - 60x60 (44 inputs at 100 Mbit/s, 14 at 113 Mbit/s, 2 at 450 Mbit/s, ~ 7 Gbit/s throughput)
  - ATM cell switching with VPI/VCI translation, on-board traffic management
- Celestri
  - 432x260 (6 optical ISL at 4.5 Gbit/s, ~ 17.5 Gbit/s throughput)
  - Cell relaying based on tag appended to the cells
- Teledesic
  - 576x576 (1 ISL at 1 Gbit/s, ~ 13.3 Gbit/s throughput)
  - Short fixed length packets, destination tag and sequence number appended at the terminals, combination of destination based packet addressing and a distributed adaptive packet routing

3.2 Terrestrial Switch Capabilities

Thunder and Lightning Switch



Thunder and Lightning (Cont.)

- The system uses extensive multiplexing and demuxing with some portions of the switch implemented at full ATM cell width. The 100 MHz cell arrival rate is equal to the cycle time of the fastest commercial Silicon FIFO chips on the market (~ 10 ns).
- The current design may be sufficient to support a speed-up factor of two (running the ECL at 400 MHz) and 80 Gbit/s links can be supported. However a ping-pong arrangement would be required for the FIFOs since they are running at their full rate speed already. Improvement of the custom GaAs circuitry to 80 Gbit/s would require serious improvement.
- Moving the switch implementation to GaAs is not expected to help much as this approach would increase the system power, size, and cost. Buffering requirement is the main issue.

Tiny Tera

- 32x32, 10 Gbit/s per port, input queued, fixed-size packet switch, size of a soda can
- Totally implemented using off-the-shelf CMOS technology
- 4 traffic classes
- Switch architecture consists of port processors, a central crossbar switch, and a central scheduler
- Port processors are application dependent (e.g. ATM)
- At peak rate an ATM cell arrives every 42.4 ns, scheduling decision made in less than 40 ns
- There are 32 crossbar slices (one per port) operating on a bit by bit basis. Packets are switched on a 64 bit basis.
- The bottleneck is the memory bandwidth and scheduler speed

IBM Prizma

- 16x16 1.6 Gbit/s per port (or 400 Mbit/s per port) single chip switch element from which larger, self-routing single stage and multistage switch fabrics can be constructed
- CMOS 0.35 μm technology (0.5 μm for the 400 Mbit/s switch)
- Capable of switching any protocol (Frame Relay, ATM, Ethernet, Token Ring)
- Capable of switching variable size packets (14 to 256 bytes)
- Self-routing based on internal routing headers
- Dynamically shared output buffer space
- Flexible multicast capability without packet duplication in memory
- Four levels of priority per logical output queue

3.3 High Level Design For Next Generation On-Board Packet Switch

Next Generation On-Board Packet Switch Size and Throughput

- Terrestrial switches with 25 Gbit/s throughput and 8x8 or 16x16 connectivity are commercially available. Switches with 100 Gbit/s to 1 Terabit/s throughput are being developed.
- Proposed Ka-band satellite systems with on-board packet switches require a switch throughput of about 10 Gbit/s and a beam connectivity of 100x100 to 500x500.
- For the next generation on-board packet switch we propose a switch throughput of 40-80 Gbit/s and a beam connectivity of 100x100 to 500x500.

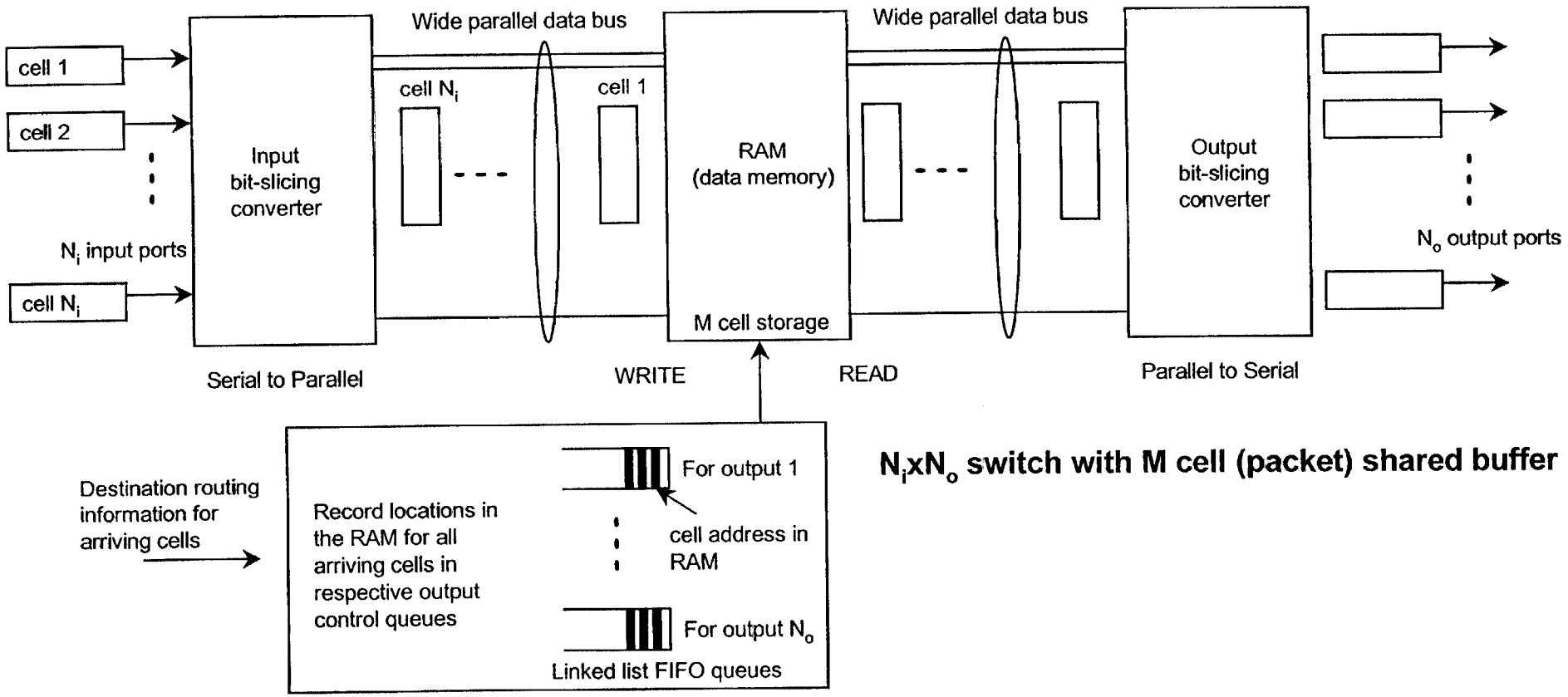
Growable Switch Architecture

- Despite recent advances in switch architectures, practical switch dimensions continue to be severely limited by technological and physical constraints of packaging.
- If a specific design is implemented in a VLSI chip, the input/output pin limitation restricts the switch size to approximately 100x100 with 64x64 or 32x32 as more practical values.
- The beam connectivity requirements of next generation packet switching satellites (100x100 - 500x500) can be met by using a growable switch architecture. A growable switch architecture employs hierarchical multiplexing of incoming signals to a higher speed for switching in the internal core fabric.

On-Board Switch Architectures

- Considering the technology in currently available high-end terrestrial packet switches, two architectures are being considered for the next generation on-board switch:
- Shared memory switch with hierarchical multiplexing
  - Lucent Globeview2000 (8x8, 20 Gbit/s throughput)
  - IBM-Prizma switch-on-a-chip (16x16, 25 Gbit/s total throughput)
- Crossbar switch with hierarchical multiplexing
  - Vitesse VSC850 (16x32, 20 Gbit/s total throughput)
  - Triquint TQ8016 (16x16, 20 Gbit/s total throughput)
  - Triquint TQ8032 (32x32, 25 Gbit/s total throughput)

Total Memory Sharing with Packet Wide Bus (Lucent - GlobeView 2000)



N_ixN_o switch with M cell (packet) shared buffer

Total Memory Sharing - Performance

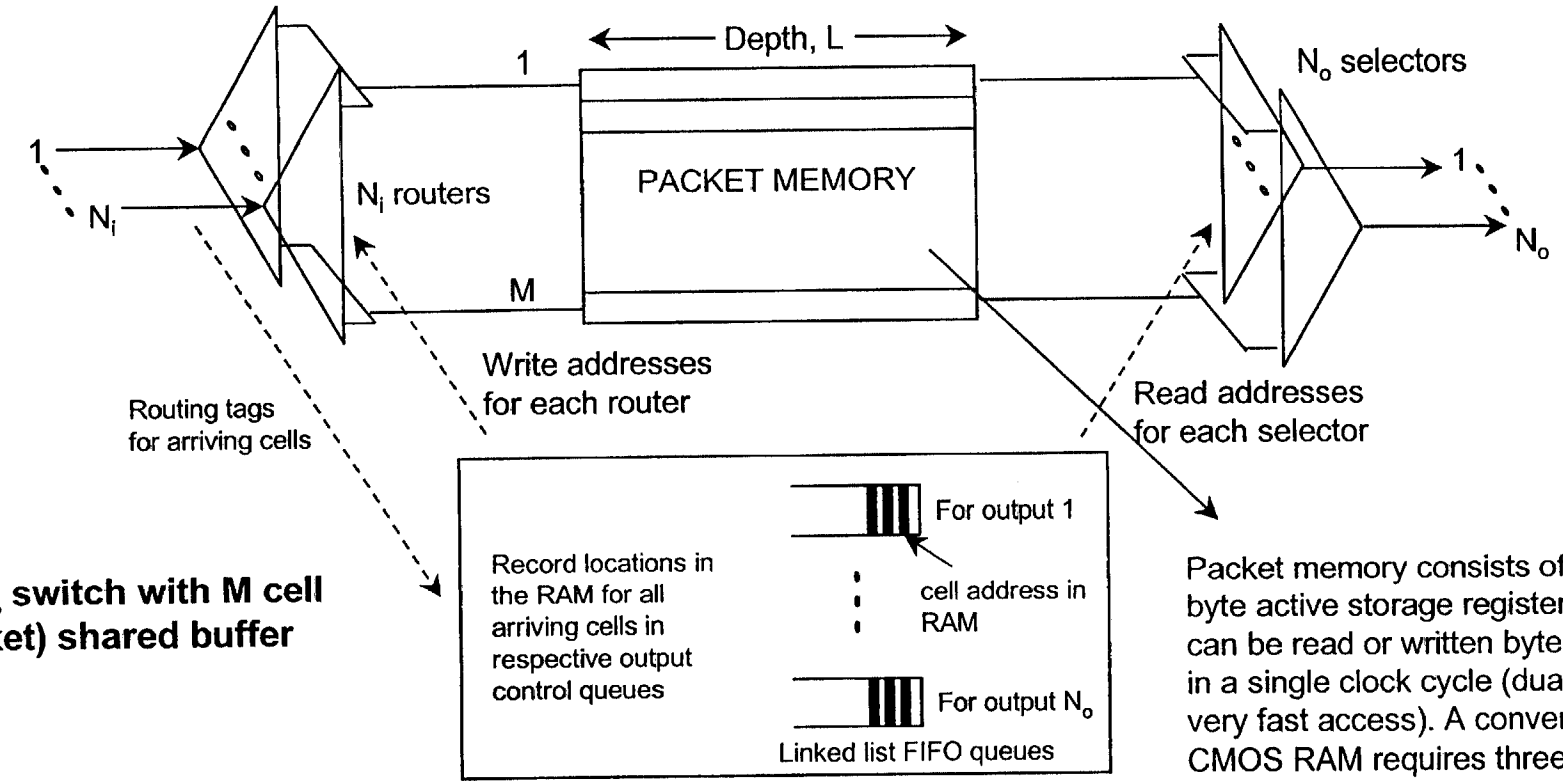
- P: Number of read/write ports to RAM (1 or 2)
- W: Bus width in bits
- L: Packet width in bits - assume an integral multiple of W
- T: RAM READ/WRITE cycle time
- V: Maximum port speed in bits/s

$$V = \frac{W}{(N_i + N_o)T} \quad if\ P = 1$$

$$V = \frac{W}{\max(N_i, N_o)T} \quad if\ P = 2$$

- Maximum port speed is limited by RAM speed and bus width
- e.g. Lucent GlobeView 2000: P=1, N_i=N_o=8, T=10 ns, W=424 bits, then V = 2.65 Gbit/s per port

Total Memory Sharing with Growable Register Array Macros (IBM-Prizma)



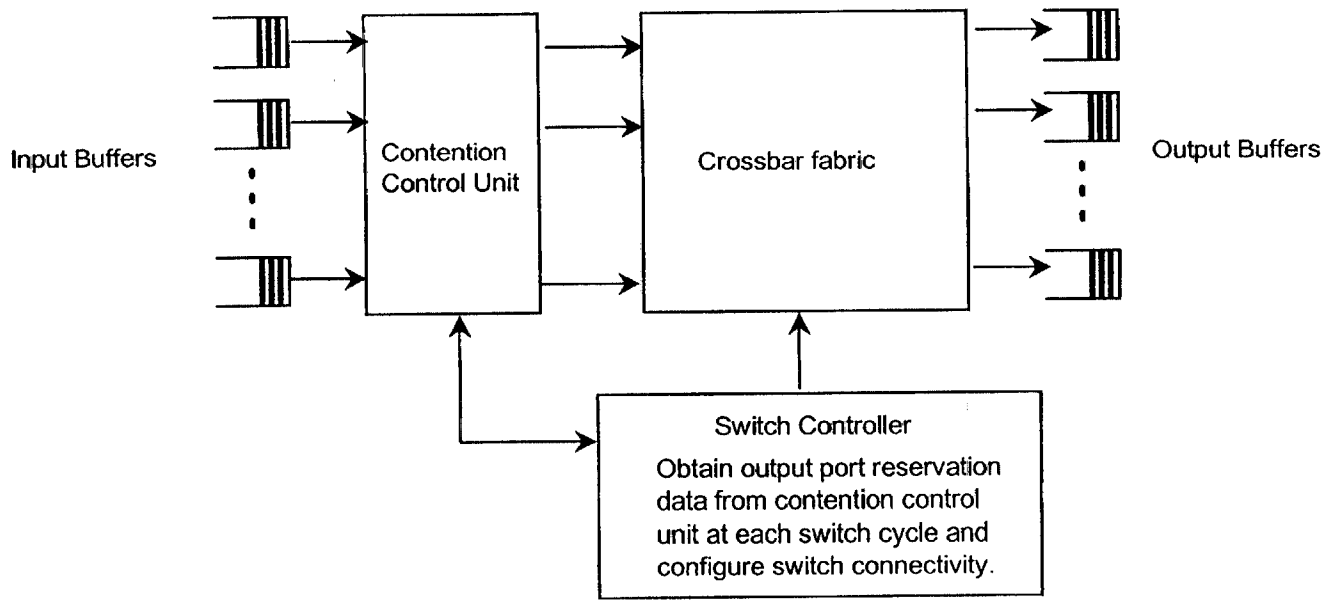
N_ixN_o switch with M cell (packet) shared buffer

Packet memory consists of M L-byte active storage registers which can be read or written byte at a time in a single clock cycle (dual port very fast access). A conventional CMOS RAM requires three clock cycles for read/write.
The packet buffer is accessed in parallel - it can be thought of as a memory of L M-byte words.

Total Memory Sharing with Growable Register Array Macros - Performance

- 1 byte of data is written to memory per input port and 1 byte of data is read from memory per output port during one clock cycle.
- Maximum port speed depends totally on the clock frequency, not on the number of ports unlike conventional memory sharing.
- Maximum clock frequency is limited by the register access time. Register access time must be smaller than one clock cycle.
- e.g. IBM Prizma P14160, register access time = 6 ns, therefore a clock frequency of 100 MHz can be used (10 ns cycle time), then Max port speed = 8/10 = 800 Mbit/s.

Crossbar Switch



Crossbar Switch - Performance

- In order to reduce Head of Line (HOL) blocking a contention control procedure must be used along with a faster switch speed. Main limitations to achievable throughput are:
- speed of contention control
  - required switch clock frequency
  - output module RAM speed
  - internal data bus width

Switch Parameters:
V: input link speed bit/s
C: switch speed per port bit/s
d: contention control depth (packets)
W: crossbar fabric internal data bus width (bits)
C_I: crossbar fabric clock frequency (Hz)

Performance:
$C >= dV$
$C = WC_I$
$=> C_I >= dV/W$
e.g. d = 4, W = 1, V = 622 Mbit/s
=> CI >= 2.4 GHz

Comparison of Three Switch Architectures

- Total memory sharing with RAM
  - Wide data bus (internal) and fast RAM required
  - All buffering can be implemented in switch fabric
- Total memory sharing with growable register array
  - Register array provides faster memory access speeds
  - Requires external buffers
- Crossbar switch
  - Larger switch sizes can be accommodated in one chip
  - Requires higher clock speeds
  - Requires input and output buffers
  - Requires contention control hardware
  - Requires external control to configure switch connectivity for each time slot

Selected Switch Architecture

- Common output buffer with growable register array
  - switch speed is not limited by switch dimension
  - switch speed is not limited by RAM speed
  - switch speed is not limited by bus width
  - hardware does not fix the packet size
  - commercial products available offer additional advantages

Switch Fabric (~ IBM Prizma)

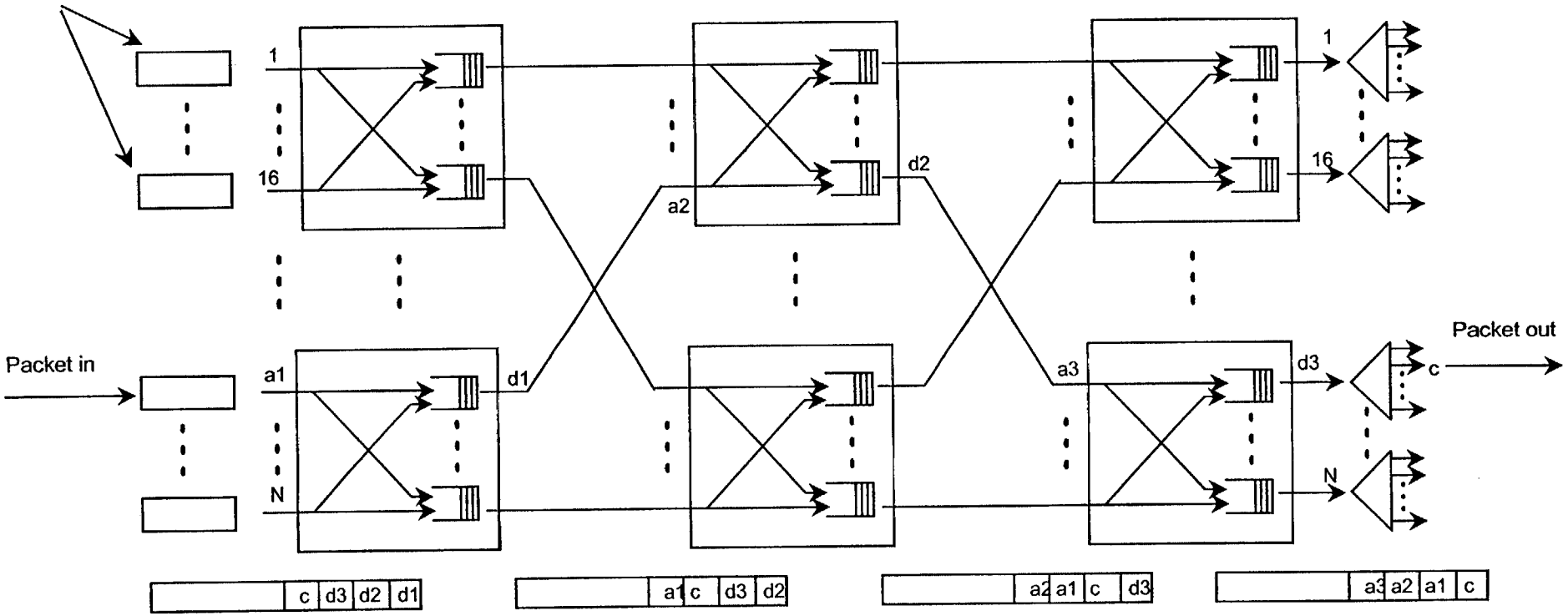
- 16x16 1.6 Gbit/s per port single chip switch element from which larger, self-routing switch fabrics can be constructed with Tbit/s of throughput
- Organized as a dual 800 Mbit/s per port sub-switch element - 8-bit parallel I/O data path between the switching chip and the I/O adapter is doubled to 16 bits (packets enter the switch at the 2-byte per clock rate)
- Shared output buffer (256 fixed size data packets of 64 to 80 bytes) - limited buffer space is dynamically shared among all outputs while maintaining logical separate queues - for queueing fairness space allocation to a specific output can be restricted - supports four levels of priority per output port
- Built in flow control by backpressure

Switch Fabric (Cont.)

- Self routing - the switch inspects the internal routing header
- Capable of switching any protocol (Frame Relay, ATM, Ethernet, Token Ring) - Protocol specific technology is located on the port adapters
- Flexible multicast capability without packet duplication in memory - Multicast connections are activated through the packet routing header and dynamically programmable internal or external table
- Companion Serializer/Deserializer chips to ease the interconnection of switch elements, interface chips for rate adaptation at the input and output ports
- CMOS 0.35 μm technology - 5 Million transistors - achievable level of integration for space qualification

Switch Fabric - Routing

Input adapter: Receives packet, uses address fields in the packet header to locate the correct entry in the routing table, retrieves the routing vector (1 byte per stage + 1 byte for output adapter) from the routing table and appends it to the packet.



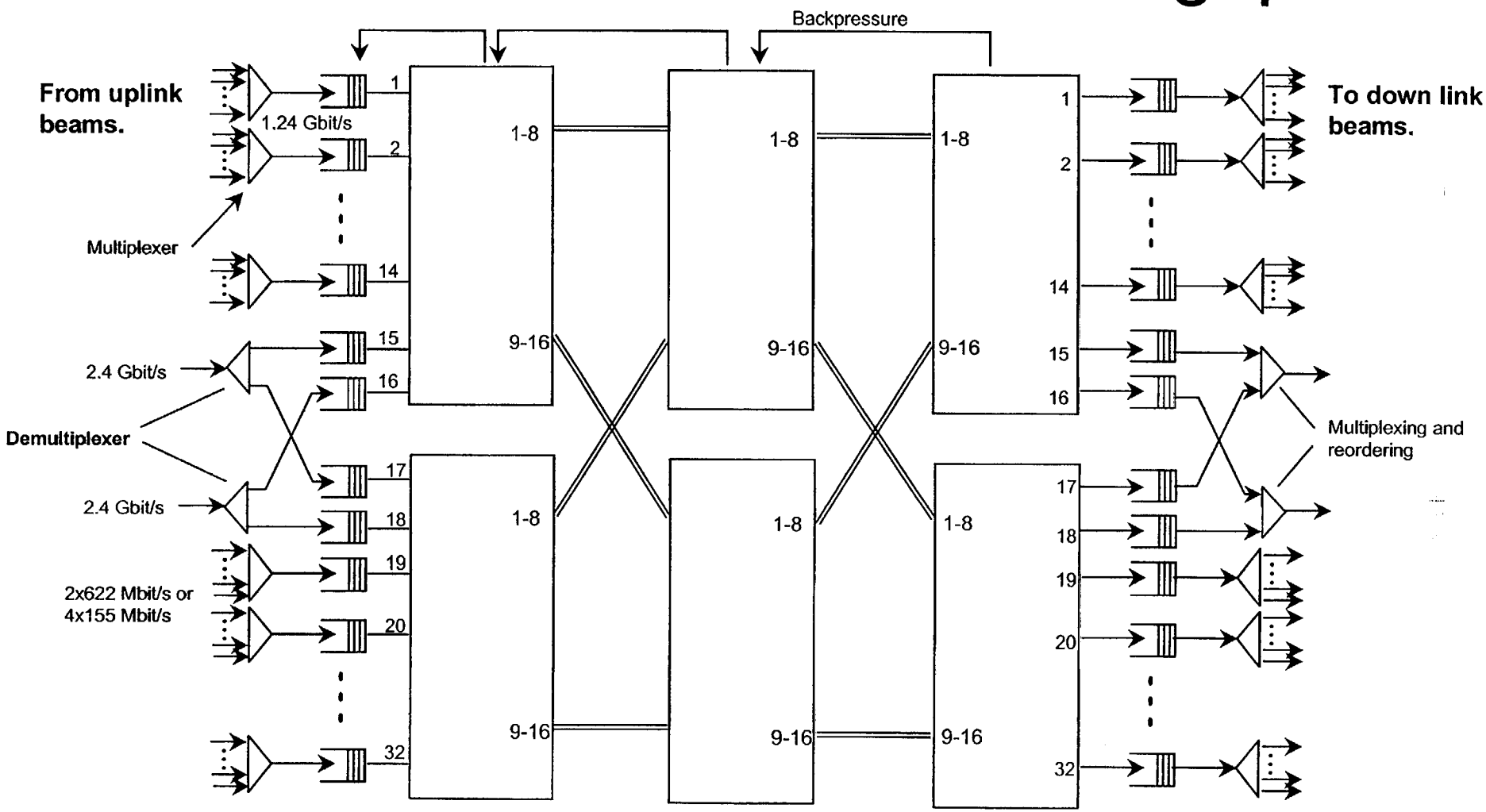
Packet entering the first switch at input port a1 with current destination d1.

Packet entering the second stage switch.

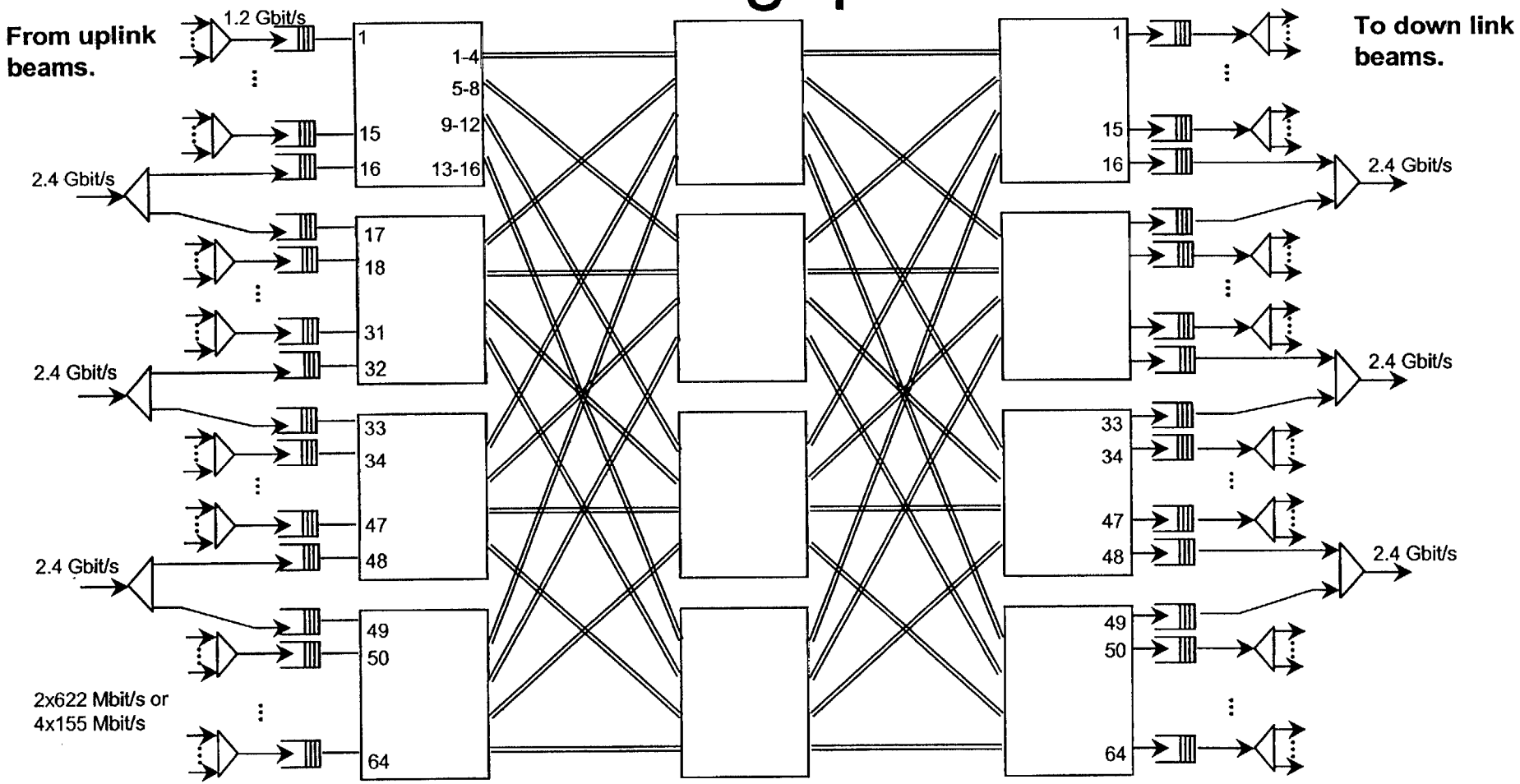
Packet entering the third stage switch.

Packet entering the output adapter.

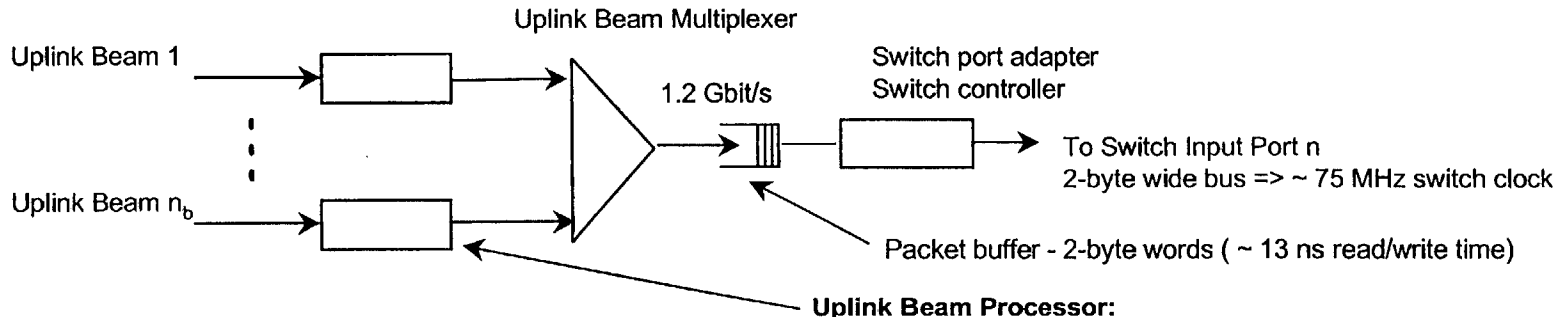
32x32 switch with 40 Gbit/s throughput



64x64 switch with 80 Gbit/s throughput



Input Processors



$C_1 + C_2 + .. + C_{nb} < 1.2$ Gbit/s

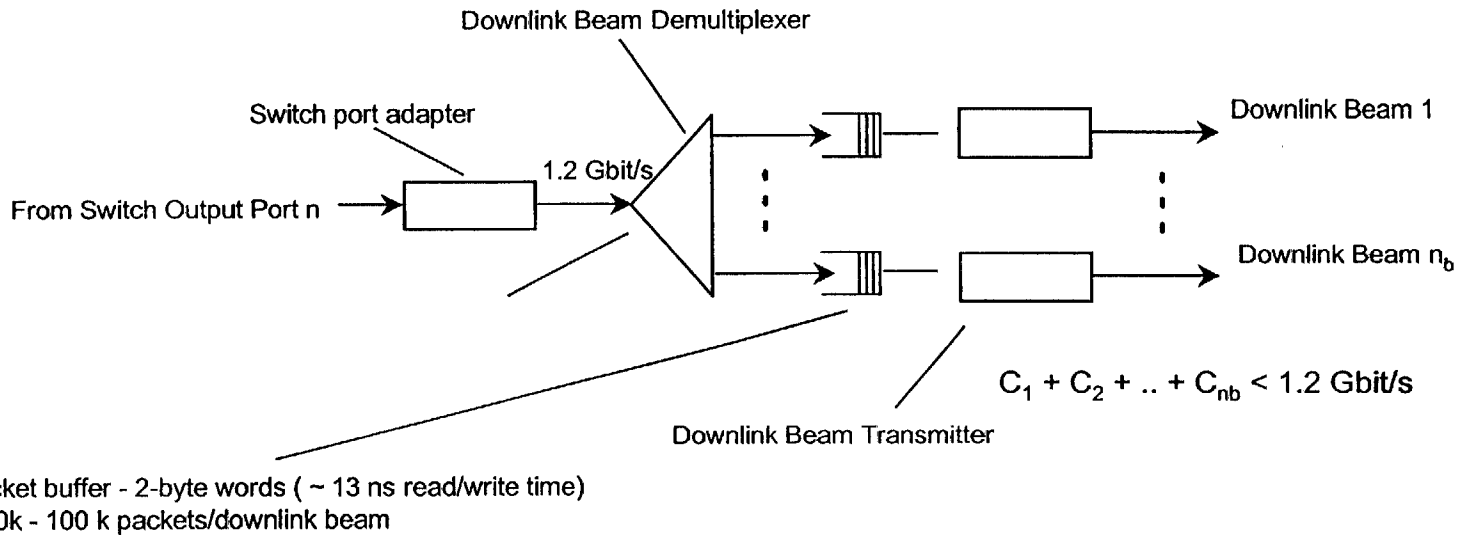
Uplink Beam Processor:
Uplink beam interface
Packet header FEC - decoding/coding
Packet routing and translation memory
Routing table look-up
Packet header translation
Packet segmentation
Routing tag appending

Input Packet Buffer Size: 1-10 K packets/port ~ 80-800 Kbytes, can be made smaller by running the switch at a higher rate
Number of Connections per Beam: 10-100 K
Number of Beams: 100-500
Packet size: 64-80 bytes
Routing Memory Access Time: For a 622 Mbit/s beam and a packet size of 80 bytes, the routing table entry must be located within 1 µs. For a 2.4 Gbit/s beam, this value should be less than 250 ns.
Routing Memory Size: 10-100 K entries X 10 bytes + overhead for efficient routing table look-up
Alternative Routing Memory Implementation: Append Dnlink Beam and the Internal Routing Tag to packets on the ground - makes multicasting more difficult

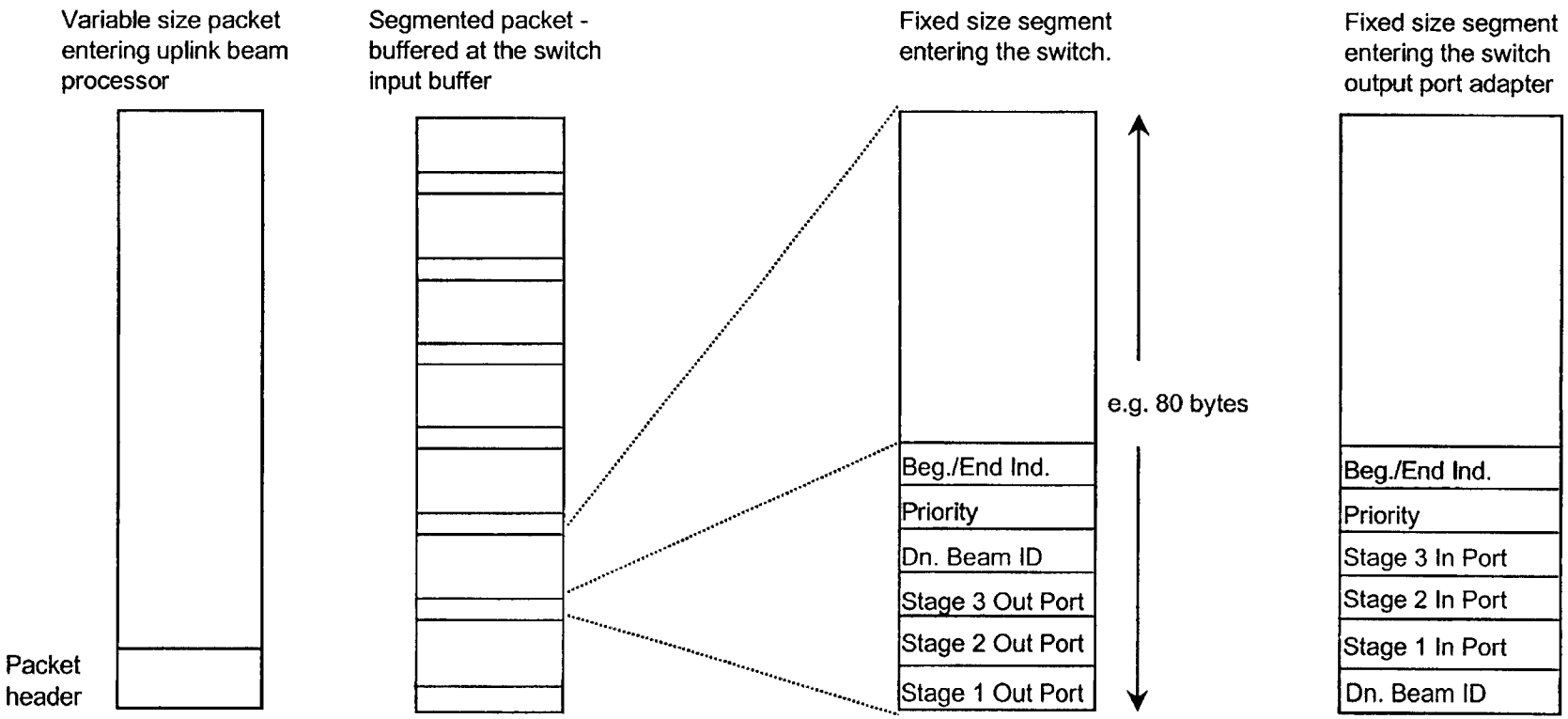
Index — Internal Routing Tag

Incoming Routing Field (e.g. ATM VPI/VCI)	Uplink Beam	Outgoing Routing Field (e.g. ATM VPI/VCI)	Dnlink Beam	Port 1	Port 1	Port 3
⋮						
~ 16-17 bits	7-9 bits	~ 16-17 bits	7-9 bits	8 bits	8 bits	8 bits

Output Processors



Packet Segmentation



The original packet is reconstructed at the down-link beam buffer. There is a separate logical buffer at the down-link beam buffer for each stage 1 input port (32 or 64) and each priority (4).
Since the uplink beam buffer passes only one packet at a time for a given priority to the switch input port and since the switch will maintain the order of the segments belonging to this packet, the original packet can be reconstructed at the down-link beam buffer. While a packet is in transit into the input switch port, if a higher priority packet arrives it can preempt the entry of the lower priority packet into the switch port.

Hardware Requirements

- Uplink Buffer
  - 1k - 10k segments per input port organized in 2-byte words
  - 13.3 ns read/write time
  - 2-20 Mbytes RAM for the 32x32 switch (4-40 Mbytes for 64x64) at 64 bytes/segment
- Routing Memory
  - 10k - 100k entries per beam
  - < 820 ns routing table look-up per packet (based on a 64-byte packet size) for a 622 Mbit/s beam (< 205 ns for a 2.4 Gbit/s beam)
  - ~ 10 - 20 bytes per entry, actual size depends on how routing table is implemented (tradeoff between memory size and look-up time)
  - ~ 12.8M - 256Mbytes for 32x32 switch (25.6M - 512 Mbytes for 64x64)

4. Next Generation Satellite System Concepts

- This section includes:
  - A hybrid Stratospheric Telecommunications Service (STS) and GEO satellite system
  - A hybrid GEO-MEO satellite system
  - A comparison of the two systems

4.1 Proposed System Concept: Hybrid STS-GEO Satellite System

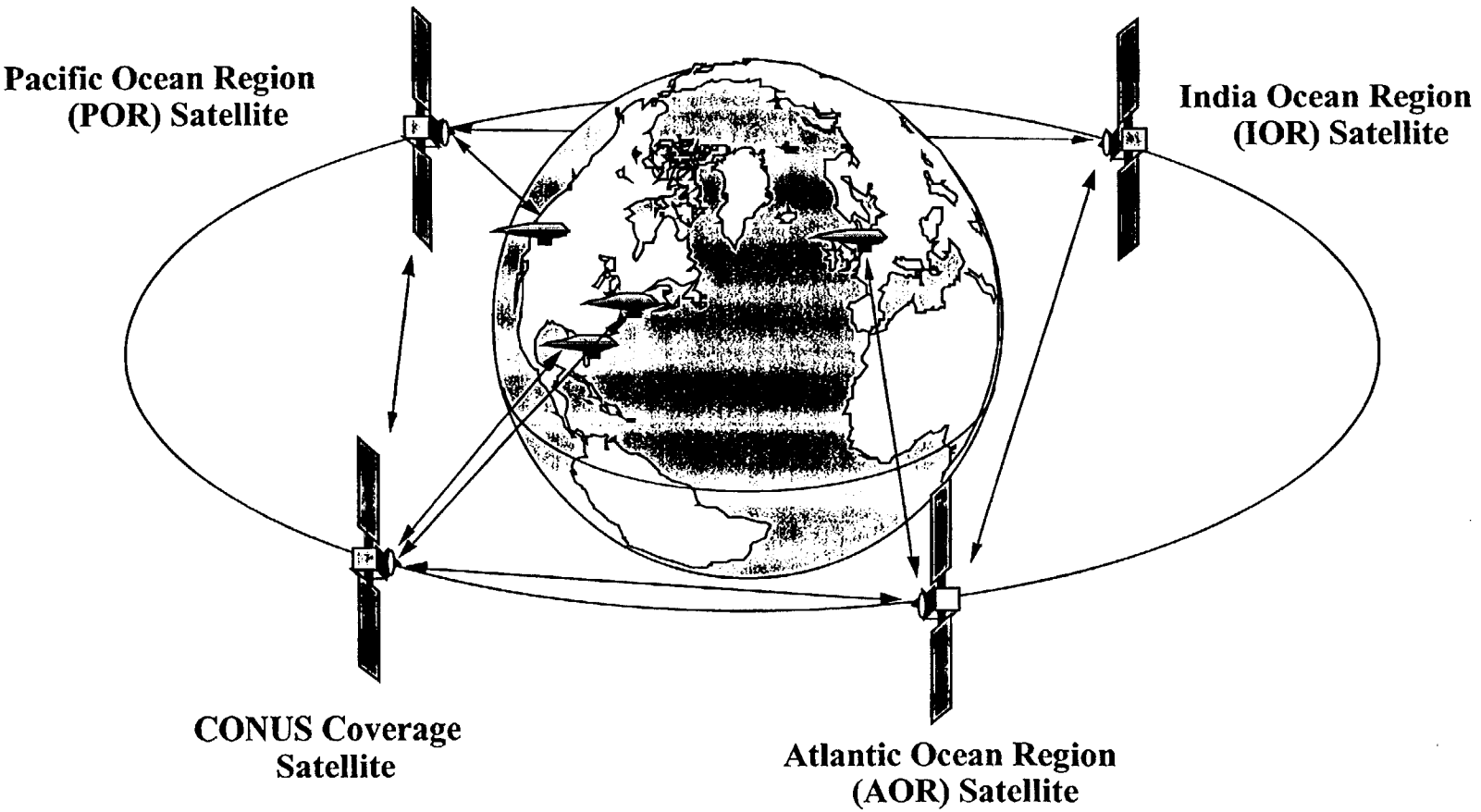
Design Considerations

- Maximum of 3 GHz is available for V-band GSO services
- Frequency reuse cluster of 5 yields 600 MHz available bandwidth
- Use of dual polarization results in about 1.2 Gbps of capacity per beam
- Stratospheric Telecommunications Service (STS) system yields about 11 Gbit/s of capacity for the same area coverage
- Thus, a hybrid system comprising GEO and STS system will provide a cost-effective solution for wideband telecommunications services

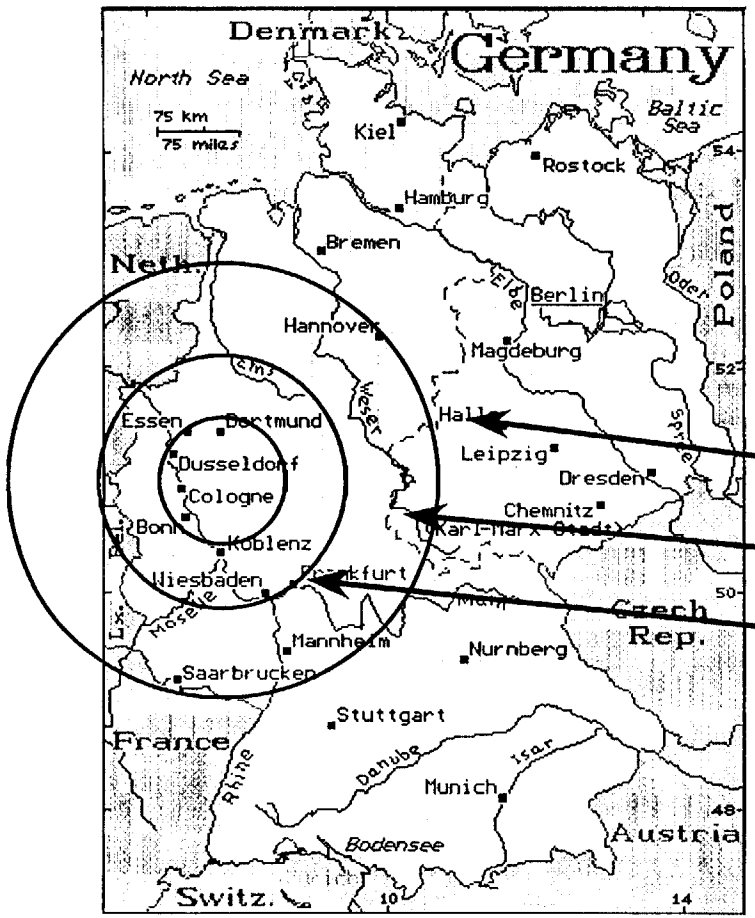
System Concept

- 4 GEO satellites combined with 32 STS system using air platforms.
- The GEO satellites provide wideband data transport and multimedia communications services.
- The STS is used to supplement the GEO capacity for geographic ares with high traffic demand. A typical coverage area of a single STS system is a 60 to 100 mile diameter.
- Optical crosslinks are used for GEO-GEO, GEO-STS, and STS-STS links for global network interconnection.
- Use of V-band (50/40 GHz) for GEO and STS to earth links, but STS system can also be used to support IMT-2000 mobile communications services using S-band.

Constellation



Typical STS System Coverage

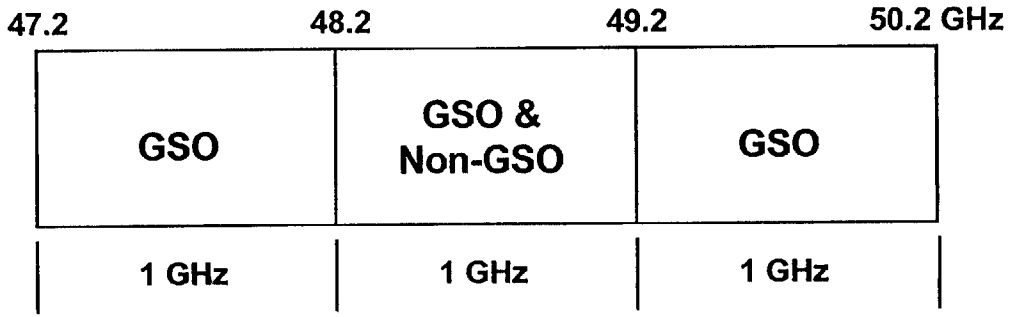


Altitude = 23 km

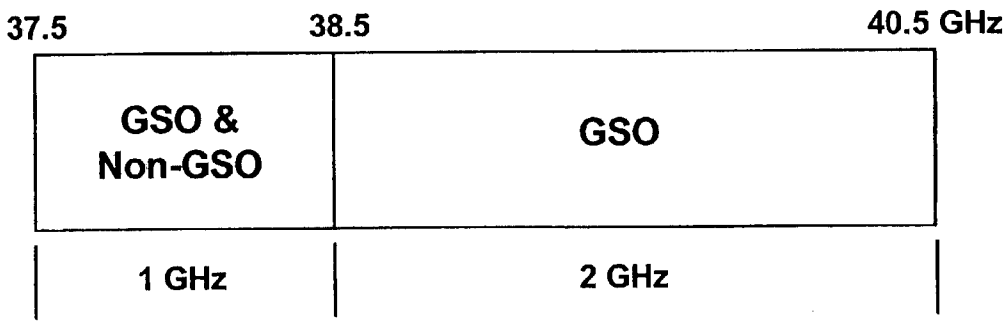
Elevation Angle	Diameter
5°	438 km
10°	246 km
20°	124 km

V-Band Frequency Allocation (FCC)

Uplink



Downlink



Q-Band	**33 - 50 GHz**
V-Band	**50 - 75 GHz**
U-Band	**40 - 60 GHz**
W-Band	**75 - 110 GHz**

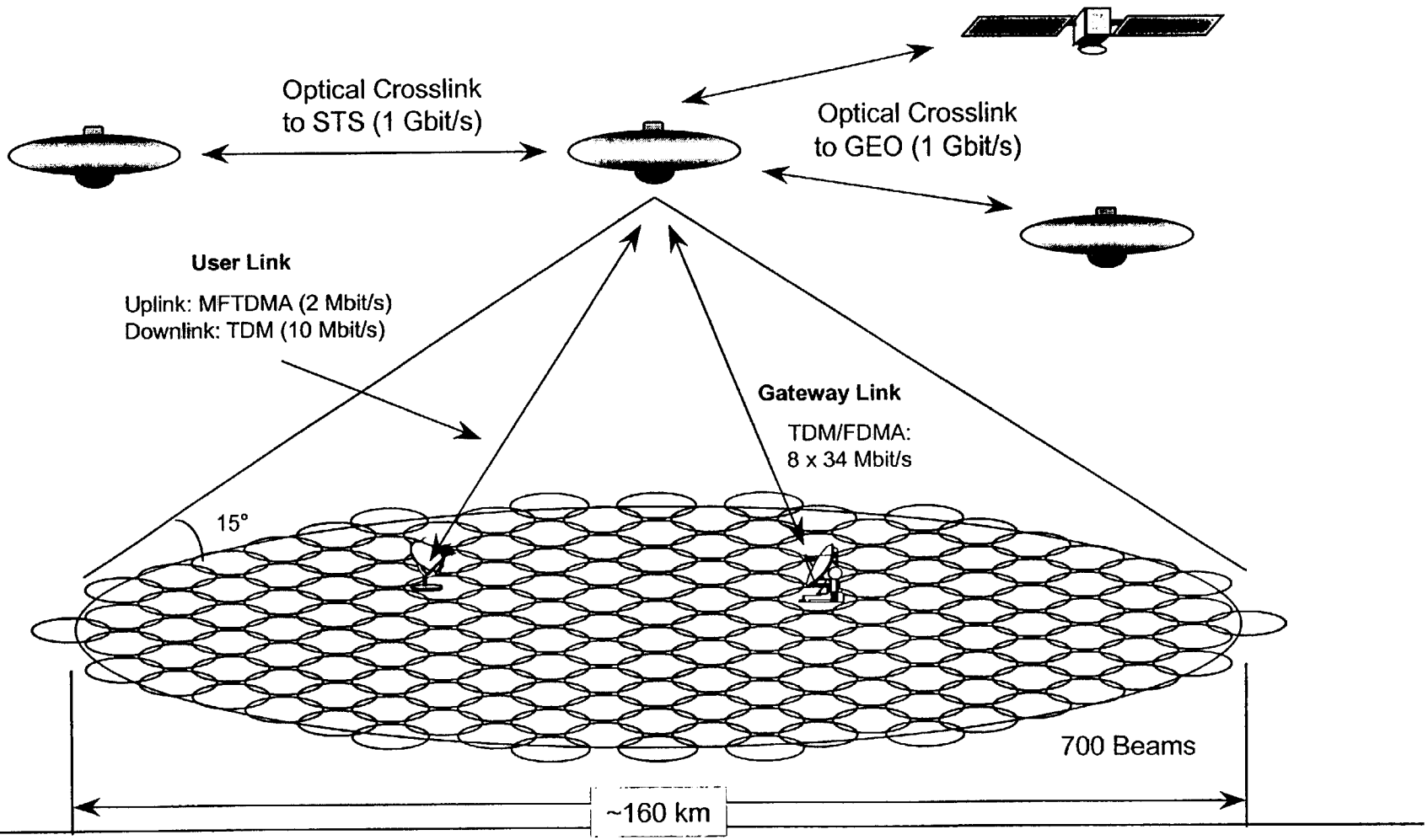
Conventional Usage:

V-Band: 40 - 50 GHz

Frequency Allocation for Sample Design

- STS System
  - Uplink: 100 MHz in 47.9 GHz - 48.2 GHz (3 STS can co-exist)
  - Downlink: 100 MHz in 47.2 GHz - 47.5 GHz (3 x 100 MHz)
- GEO
  - Uplink: 48.2 GHz - 50.2 GHz (2 GHz)
  - Downlink: 38.5 GHz - 40.5 GHz (2 GHz)

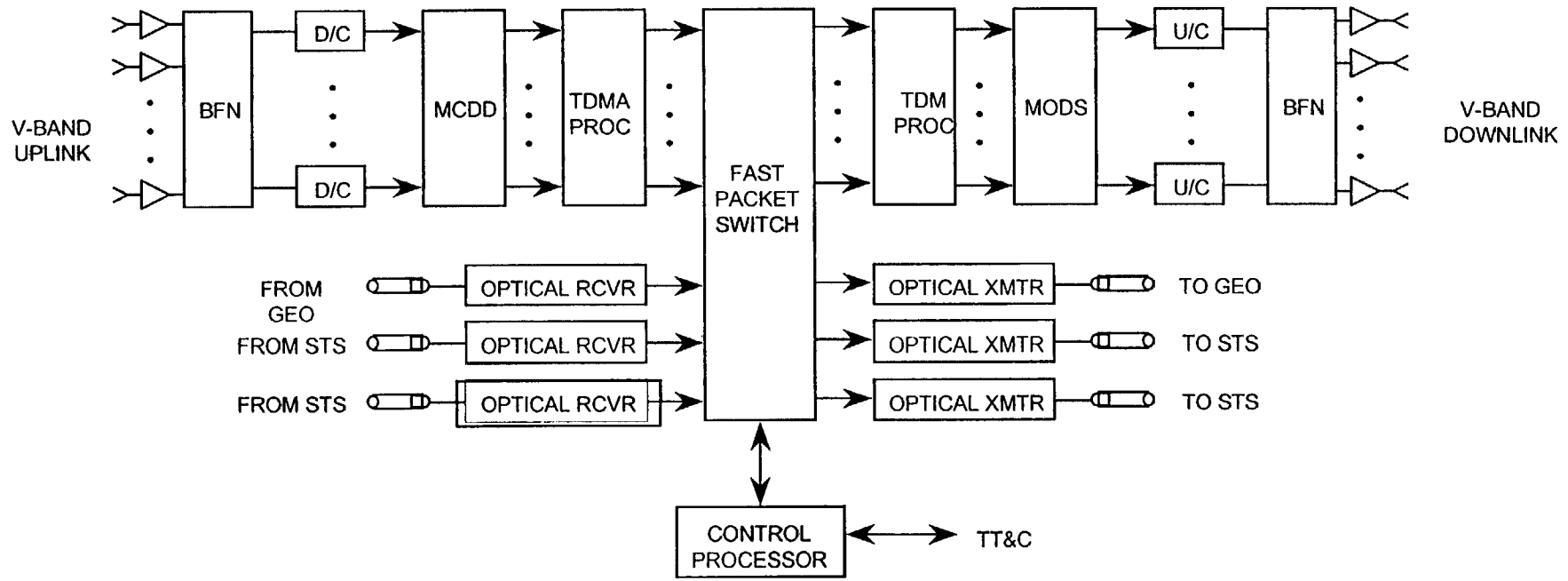
STS System


Optical Crosslink
to STS (1 Gbit/s)
Optical Crosslink
to GEO (1 Gbit/s)
User Link
Uplink: MFTDMA (2 Mbit/s)
Downlink: TDM (10 Mbit/s)
Gateway Link
TDM/FDMA:
8 x 34 Mbit/s
15°
700 Beams
~160 km

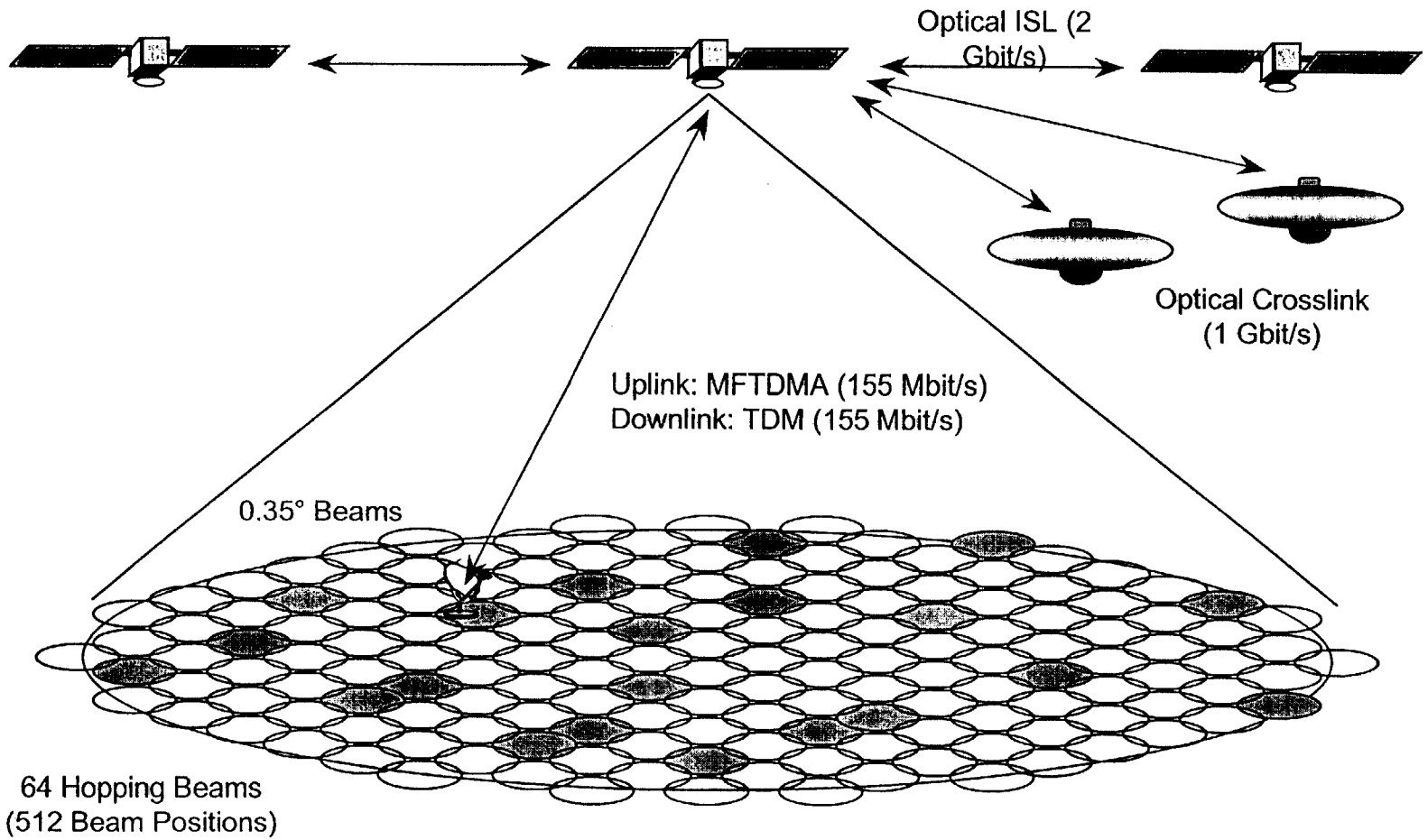
STS System Parameters

User Link	Gateway	Link
No. of Beams	70015 (out of 700)	
Modulation	QPSK	64 QAM
Coding	Concatenated	Concatenated
Uplink Access	MFTDMA	TDM/FDMA
Uplink Bit Rate	5 x 2 Mbit/s	8 x 34 Mbit/s
Downlink Access	TDM	TDM
Downlink Bit Rate	10 Mbit/s	8 x 34 Mbit/s
Total Capacity	7 Gbit/s	4 Gbit/s

STS System Payload Configuration



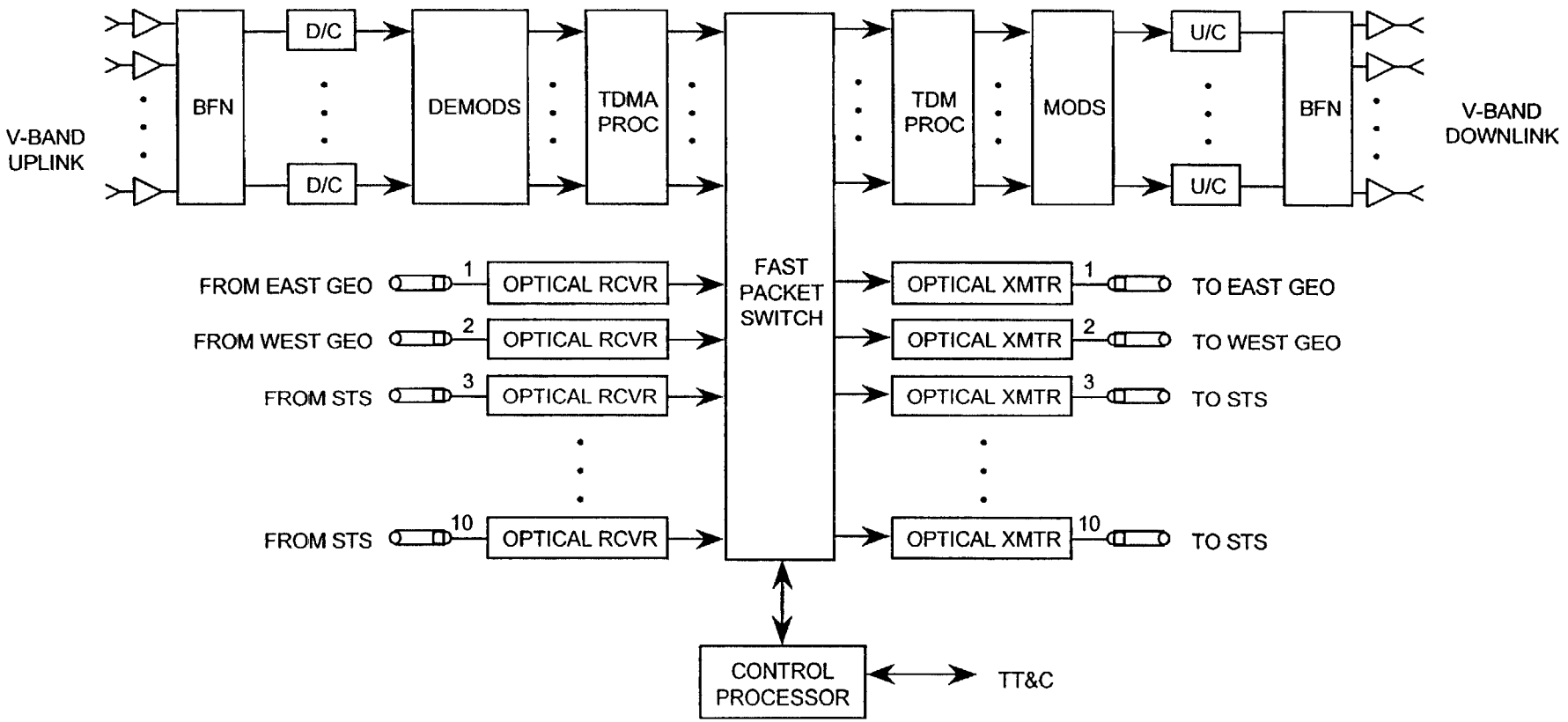
GEO System


Optical ISL (2 Gbit/s)
Optical Crosslink (1 Gbit/s)
Uplink: MFTDMA (155 Mbit/s)
Downlink: TDM (155 Mbit/s)
0.35° Beams
64 Hopping Beams
(512 Beam Positions)

GEO System Parameters

- No. of Beams — 64 (out of 512)
- Modulation — QPSK
- Coding — Concatenated
- Uplink Access — MFTDMA
- Uplink Bit Rate — 4 x 155 Mbit/s
- Downlink Access — MFTDMA
- Downlink Bit Rate — 4 x 155 Mbit/s
- Total Capacity — 40 Gbit/s

GEO Payload Configuration



Onboard FPS Requirements

	STS	GEO
System Capacity	11 Gbit/s	40 Gbit/s
Crosslink Capacity	1 Gbit/s	1 & 2 Gbit/s
No. of Crosslinks	3	8 & 2
Total Crosslink Capacity	3 Gbit/s	12 Gbit/s
Switch Capacity	14 Gbit/s	52 Gbit/s
Connectivity Requirements	685 user beams 15 gateway beams 3 crosslinks	64 beams 10 crosslinks

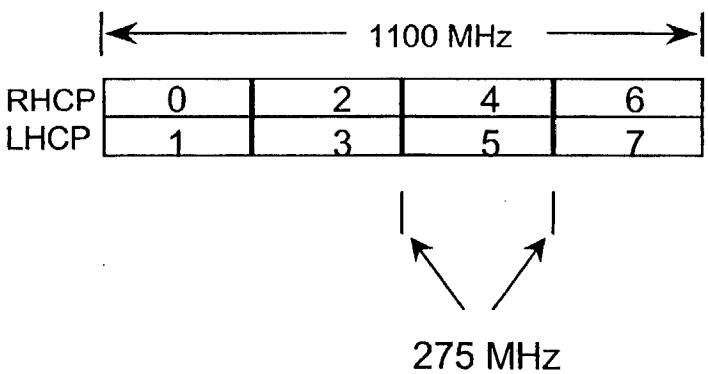
4.2 Alternative System Concept: Hybrid MEO-GEO Satellite System

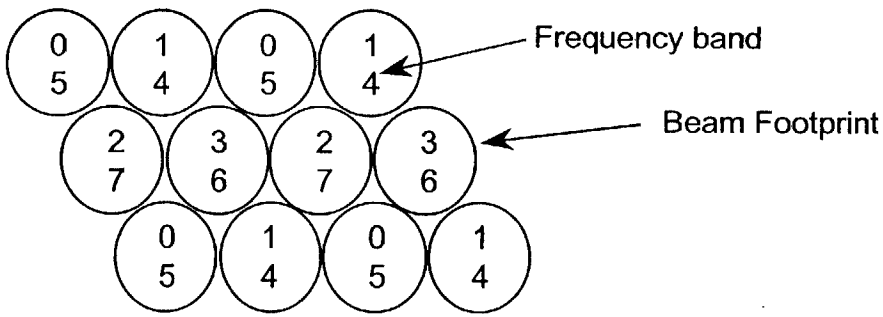
System Concept

- Similar to V-band filing StarLynx
- 4 GEO satellites at two orbital positions combined with 20 MEO satellites
- The MEO constellation will consist of four planes with five satellites in each plane, inclined at 55 degrees with respect to the equator and in circular orbits at an altitude of 10,352 km
- The system will provide multimedia services to mobile terminals for data rates up to 8 Mbit/s.

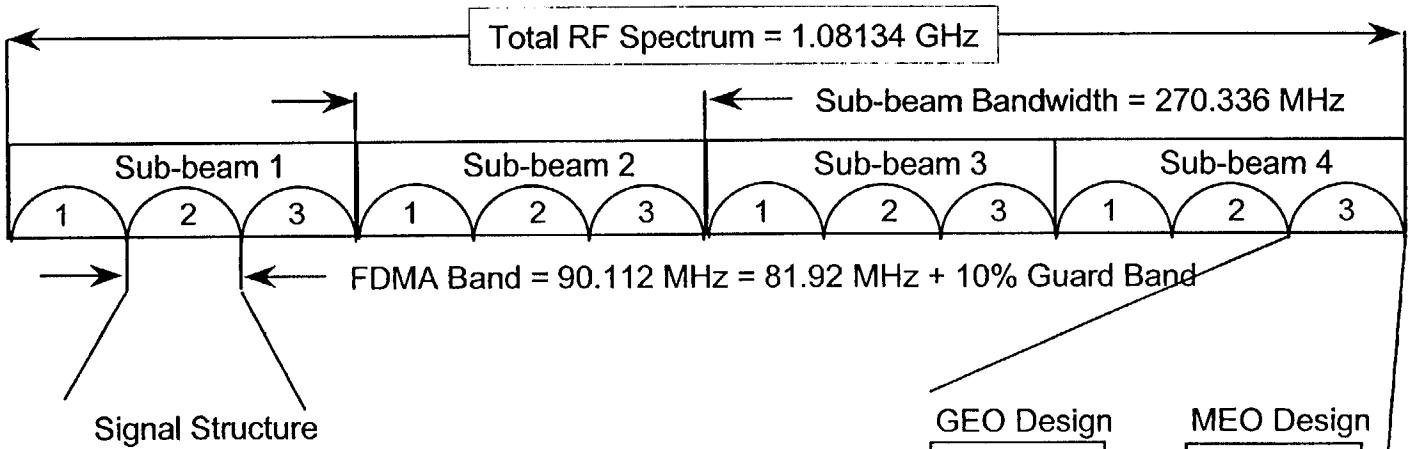
Frequency Plan and Beam Configuration

- MEO and GEO satellites use the same uplink and downlink frequency bands. The uplink frequency spectrum is contiguous 1.1 GHz from 45.5 to 46.7 GHz and the downlink frequency spectrum is from37.5 to 38.6 GHz.
- The system uses a frequency reuse cluster of four and dual polarization.





FDMA/CDMA Signal Design



Signal Structure

- CDMA with PN Chip Rate = 81.92 Mcps
- QPSK Modulation
- Convolutional-concatenated, Reed-Solomon, error-correction coding

GEO Design
CDMA 1
CDMA 2
CDMA 3
CDMA 4
CDMA 5
CDMA 6

MEO Design
CDMA 1
CDMA 2
CDMA 3
CDMA 4
CDMA 5
CDMA 6
CDMA 7
CDMA 8

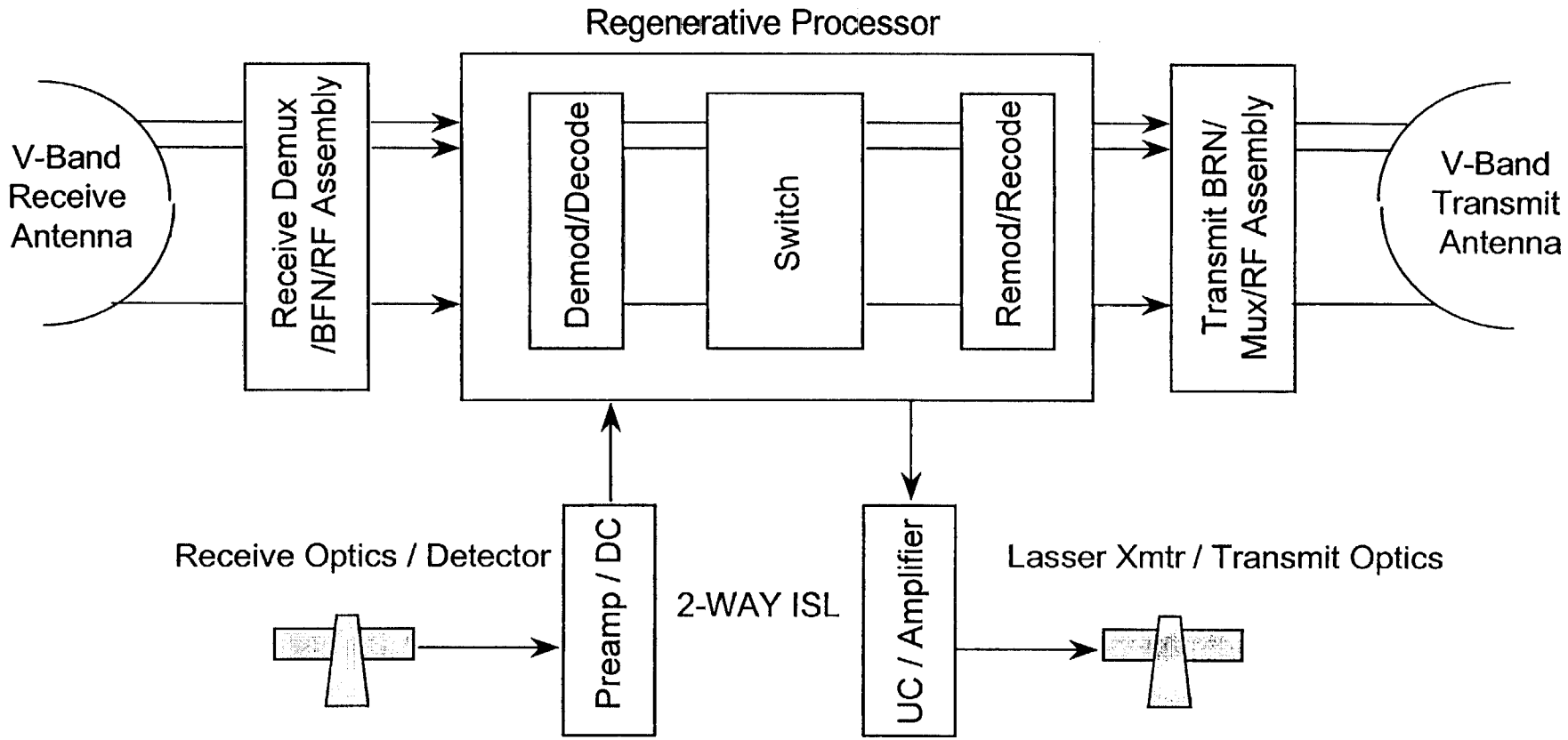
Terminal Types and Data Rates

Terminal Type	Mbit/s	Scanned-Beam GSO	Narrow-Beam MEO
Mobile User	8.192 Mbit/s	1.2 Mbit/s	6.011 Mbit/s
Portable User	2.048 Mbit/s	0.3 Mbit/s	1.544 Mbit/s
Mobile SAN	8.192 Mbit/s	1.2 Mbit/s	6.011 Mbit/s
Portable SAN	2.048 Mbit/s	0.3 Mbit/s	1.544 Mbit/s
SAN-Mobile	8.192 Mbit/s	1.2 Mbit/s	6.011 Mbit/s
SAN-Portable	2.048 Mbit/s	0.3 Mbit/s	1.544 Mbit/s

Satellite Antenna Characteristics

- GEO Satellite
  - Each satellite can select up to 40 movable spot beams out of a possible 204 in its field of view.
  - Each spot beam has a beamwidth of 0.15 degrees.
  - A spot beam scanning function can be utilized.
  - Each satellite has two optical ISLs operating at 3 Gbit/s: one ISL to a MEO satellite and the second to another GEO satellite.
- MEO Satellite
  - Each satellite has 32 spot beams.
  - Each spot beam has a beamwidth of 0.6 degrees.
  - There are five optical ISL links each operating at 3 Gbit/s: four to adjacent MEO satellites (two MEOs in the same plane and one MEO each in two adjacent planes) and one to a GEO satellite.

Communications Subsystem Block Diagram



Onboard FPS Requirements

	MEO	GEO
System Capacity	9.2 Gbit/s	11.5 Gbit/s
Crosslink Capacity	3 Gbit/s	3 Gbit/ss
No. of Crosslinks	5	2
Total Crosslink Capacity	15 Gbit/s	6 Gbit/ss
Switch Capacity	24.2 Gbit/s	17.5 Gbit/s
Connectivity Requirements	32 beams 5 crosslinks	40 beams 2 crosslinks

Comparison of Concept 1 and Concept 2

- The GEO-STS system does not require handover capability, simplifying terminal and payload design.
- The STS platforms are located at an altitude of about 21 km significantly reducing propagation delay for user-STS communications.
- The STS platforms are relatively simpler to launch and the capability to bring an STS platform back on the ground for maintenance offers an additional advantage.
- The throughputs provided by the two systems are comparable.

5. Conclusions and Recommended Future Work

Switch Technology

- CMOS is expected to be the dominant technology for implementing complex functions due to its reliability, low power consumption, high densities, and rich libraries.
- Level of integration in GaAs ICs is expected to grow faster than that of CMOS but is not expected to reach that of CMOS. Higher supply voltage requirements of CMOS may slow level of integration as external electric fields need to be reduces at higher densities.
- Commercial SiGe products will be available, however these are expected to be mainly RF products. In the longer term, SiGe can be the preferred technology due to simplicity in manufacturing, higher speeds and integration, and low power consumption.

Switch Technology (Cont.)

- As switch port speeds exceed 1.6 Gbit/s, which seems to be the current maximum for CMOS, GaAs ICs are expected to be used at the switch front-end and output processors. 0.2mm CMOS technology is expected to be mainly applied to core switching and control functions which require high integration and low power dissipation.
- The next generation on-board switch (2002-2005) should be based on CMOS or a combination of CMOS/GaAs technologies where GaAs ICs are used at the front-end and output processors which require high speed operation and CMOS is used to implement core switching and control functions which require high integration and low power dissipation.

Radiation Study

- It was concluded that shielding, radiation-hardening, and fault tolerant architectures that can correct SEEs should be used concurrently to achieve required level of radiation tolerance for a given orbit.
- Radiation hardened CMOS ICs with access times in the order of 30 ns are commercially available. GaAs FET technology is prone to SEEs and there are no commercially available rad-hard GaAs FET ICs. GaAs HBT technology is more tolerant to SEEs, however they have very high power requirements.
- While radiation hardened CMOS with desired total dose and SEE performance and speeds will become available, SEE hardened GaAs technology may not be available within the time frame of interest.

Next Generation On-Board Switch

- Based on the capabilities of high end terrestrial fast packet switches and of the on-board switches in the proposed Ka-band systems, recommended a throughput of 40-80 Gbit/s and a beam connectivity of 100x100-500x500 for the next generation on-board fast packet switch.
- Compared the performance requirements of various fast packet switch architectures and recommended a growable switch architecture based on a 16x16 common-buffer switch fabric for the next generation on-board fast packet switch.
- Provided high level designs for fast packet switches operating at 40 Gbit/s and 80 Gbit/s throughputs.

Satellite System Concepts

- Proposed a satellite system concept with 4 GEO satellites combined with 32 stratospheric telecommunications service (STS) systems using air platforms. The estimated switch capacity of the STS system switch is 14 Gbps while the estimated switch capacity of the GEO satellite is 52 Gbps.
- Proposed an alternative satellite system concept with 4 GEO satellites combined with 20 MEO satellites. The estimated switch capacity of the GEO satellite is 17.5 Gbit/s while the estimated switch capacity of the MEO satellite is 24.2 Gbit/s.
- Compared the two concepts in terms of complexity, performance, and throughput.

Recommended Future Work

- Interworking issues between future terrestrial networks and the next generation satellite networks
  - Satellite resource access
    - Out-of-band vs in-band access channels
    - Access channel type
    - Access channel multiple access method
    - Location of resource controller
    - Access channel signal modulation and signaling rate
    - Access channel information content and format
    - Channel protocol
    - Integration with terrestrial network signalling
  - Data routing and protocols

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13. ABSTRACT (*Maximum 200 words*)

Future satellite communications is expected to be fully integrated into National and Global Information Infrastructures (NII/GII). These infrastructures will carry multi gigabit-per-second data rates, with integral switching and routing of constituent data elements. The satellite portion of these infrastructures must, therefore, be more than pipes through the sky. The satellite portion will also be required to perform very high speed routing and switching of these data elements to enable efficient broad area coverage to many home and corporate users. The technology to achieve the on-board switching and routing must be selected and developed specifically for satellite application within the next few years. This report presents evaluation of potential technologies for on-board switching and routing applications.

14. SUBJECT TERMS

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