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Binning for IC Quality: Experimental Studies on the SEMATECH* Data

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Extended Summary

1 Introduction

Screening based on the locality of defects has long been informally practiced in the industry whereby die from wafers, or parts of the wafer, that display a high incidence of failures are discarded. More recently we have refined this approach such that tests results for neighboring die on the wafer are also considered in evaluating test results for a particular die [1]. It has been shown [2-4] that by exploiting information about defect clustering on the wafer, test cost can be optimized and low defects levels achieved for complex VLSI circuits. A particularly useful capability of this new approach is the ability to bin dice (or chips) following testing so as to separate out a high quality bin with defect levels (due to test escapes) up to an order of magnitude better than the average for the lot. Furthermore, such a strategy may also be able to screen for potential burn-in failures, thereby eliminating the need for expensive burn-in of bare dice. It is important to note that this proposed approach is orthogonal to other techniques for improving test effectiveness (e.g. increased fault coverage, addition of I_{DDQ} tests, etc.), and can probably screen for defect levels up to an order of magnitude better than can be otherwise achieved without exploiting defect clustering information.

Because of the difficulty of obtaining defect map data from semiconductor manufacturers, the effectiveness of this new approach was initially established in [1-4] through detailed analytical analysis. The mathematical models employed were based on widely accepted negative-binomial defect distributions first introduced by Stapper [5]. Recently we presented the first experimental study to practically demonstrate the viability of the proposed approach based on test results from a few wafers from an older IBM bipolar process [7]. *In this paper we present the first results on the effectiveness of die screening for a modern submicron CMOS process.* The data comes from the SEMATECH test methods experiments conducted by IBM on a production ASIC (144K gates) in 0.5μm process. The 18,466 CMOS die tested in this experiment provide an order of magnitude more data than the earlier bipolar study and for the first time allows validation of the analytical models in [2-4].

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* This data comes from the work of the test thrust at SEMATECH, Project S121. The analysis here is the work of this university, the conclusions are our own and do not necessarily represent the views of SEMATECH or its member companies.

The rest of this extended summary is organized as follows. Section 2 reviews the die screening approach based on defect clustering. In Section 3 we outline the experimental approach and provide details of the test data. Results are presented in Section 4. We conclude with Section 5. The complete paper will additionally include a more comprehensive comparison of the experimentally observed data with the theoretical predictions in [3,4].

2 Review of the Die Screening Approach

The basic idea here takes advantage of the fact that defect levels in tested components (test escapes) depend not only on the quality of the test applied, but also on the yield of the incoming components, i.e. how many of the manufactured components are good to begin with. Thus, if yield is very high, even a poor test will result in mostly good parts being shipped. On the other hand, if yield is very low, then a poor test will let through many faulty parts. For example, if yield is 90%, even a poor test that fails to detect faults in 10% of the bad components will only let through, on average, one bad part for every 90 good parts a defect level (DL) of 1.1%. However, if the manufacturing yield is 10%, then the same poor test will be applied to 90 bad parts out of every 100, and will let through 9 bad parts along with the ten good ones. In this latter case, using the same test, the defect level in the parts being shipped is 47%, almost 45 times higher than in the first case.

Because of the observed clustering of defects in semiconductor wafers, not all dice on a fabricated wafer have the same probability of being defective if test results for other dice in the neighborhood are known. A die next to another die that is known to be defective has a higher *a priori* probability of being defective, and a lower expected yield than a die with good neighbors. Now if dice that test good are binned based on these *a priori* yields, the different bins can be expected to display defect levels that reflect the incoming yield variations. Bins with high *a priori* yields will contain dice with low defect levels.

In the scheme described in [1] each die that tests good during the wafer-probe test is binned into one of nine separate bins based on how many of the die's adjacent neighbors (0-8) on the wafer tested faulty. Although only dies that test good are binned, each bin can be expected to contain some faulty dies as a result of test escapes (i.e. have higher defect levels). This is because, due to the clustering of defects, a larger fraction of dies with faulty neighbors are likely to be faulty to begin with when compared to dies with zero or only a few faulty neighbors. Assuming that the test is equally effective in detecting faulty dies from all neighborhood classes, a larger fraction of faulty dice in the tested sample will result in a larger fraction of fault escapes and therefore higher defect levels. Thus the nine bins containing the dies that tested good at wafer probe time can be expected to have significantly different defect levels depending on the extent of the defect clustering existing on the wafer. These different defect levels imply differing likelihood's of a random die being defective in each of the nine bins.

Analytical analysis in [3,4] based on negative binomial yield statistics has shown defect levels in the best bin up to an order of magnitude better than the average for the lot. In [7] we present the results from actual wafer test data collected at IBM for a bipolar process. Dice were binned based on the results of a basic DC functional test. Test escapes were then uncovered using a more comprehensive test which included delay testing. It was observed that while all the

bins taken together had an 8% escape rate, the best bin contained no test escapes at all. However, due to the limited amount of available data (approximately 1200 good dice from 23 wafers) binning only considered a die's North, South, East and West neighbors (5 bins); and even then the best bins were very sparsely populated.

3 The Experiments

Data for the experiments presented here comes from the SEMATECH "Test Methods Evaluation" [6] study. This was an experiment to determine the relative merits of several test methodologies often used by SEMATECH member companies and other IC manufacturers. The experiment was designed to determine the following: given X seconds of VLSI test time, how should that time be optimally allocated among the various test techniques currently employed by IC manufacturers. As previously mentioned, the experiment was conducted by IBM on approximately 18,500 die from 75 wafers of a production ASIC (144K gates) in 0.5μm process. Four major test methods were selected that are in common use within the member companies. These methods were:

- Functional test, e.g., design verification patterns
- Scan-based stuck-at fault tests
- Scan-based transition (delay) fault tests
- I_{DDQ} tests

Figure 1 shows a typical wafer map. The legend indicates the several different possible results from the various tests and the test results for each die site. Dots indicate missing dice or locations for which test results were not available.

Based on this wafer map data we constructed three experiments to study the effects of defect clustering on test escapes. In the first experiment we "assume" that only the functional test and I_{DDQ} tests were run at wafer probe. This means that all dice marked $$ (all pass), 1P (failed delay exclusive), 1T (failed stuck-at exclusive) and 2B (failed both delay and stuck-at tests) will be "passed" as good. We can now look upon the dice marked 1P, 1T and 2B as test escapes for the functional and I_{DDQ} tests and study how they are binned. All the die that passed the functional and I_{DDQ} tests were then binned based on the 8 neighbor test results. Bin 0 then contains those die which passed the functional and I_{DDQ} tests with no faulty dice among the die's eight adjacent neighbors; bin 1 dice have only 1 faulty neighbor; bin 2 dice have two faulty neighbors, etc. up to bin 8 in which the dice have all eight neighbors faulty.

Similarly, the second experiment assumes that only the stuck-at test and I_{DDQ} were run at wafer probe. This results in all dice marked $$, 1P, 1F (failed functional exclusive) and 2A (failed both delay and stuck-at tests) will be passed as good dice and therefore end up as test escapes in the subsequent binning.

Finally, in the third experiment we assume that the only test not available at wafer probe time is the I_{DDQ} test. In this case the I_{DDQ} only failures constitute the test escapes. Since there were a large number of these, they provide significantly more data. One thing to note here is that in the SEMATECH study a 5μA threshold was used to declare I_{DDQ} failures. This resulted in a substantial number of dice which otherwise passed all test but had an I_{DDQ} level above 5μA.

For our third binning experiment we raised the I_{DDQ} threshold to 100μA. Therefore, dice which had a test result of 1I (failed I_{DDQ} exclusive) and had an I_{DDQ} level above 100μA were taken to be failures while those dice which were 1I but had an I_{DDQ} level of 100μA or below were passed and resulted in test escapes.

After binning for each experiment based on the available wafer map data we investigate the different bins for the total number of test escapes out of the total number of dice in each bin to obtain defect levels.

4 Results

One of the decisions to be made before compiling the results is in the handling of dice for which some neighborhood test results are missing. All dice on the periphery of the wafer fall in this category, along with some internal dice as shown in Figure 1. For the purposes of our experiments we considered these missing dice to be failures. This is because dice on the periphery of the wafer typically have a high defect rate.

Table 1 shows the results when failures detected exclusively by the stuck-at and delay tests are considered escapes. Observe that the best bin, with all eight good neighbors, has only one test escape and a defect level of 0.17%. The fraction of test escapes (stuck-at and delay failures) generally increases as the number of faulty neighbors for a bin increase, although there is a reversal for some bins. This is most likely a statistical aberration because of the small sample size. The overall defect level is 102 defective dice out of 11,881 or 0.86%, which is 5 times that for the best bin.

Table 2 shows the results when failures detected exclusively by the functional and delay tests are considered escapes. Again observe that the best bin has only one test escape and a defect level of 0.17%. As seen in Table 1, the fraction of test escapes (functional and delay failures) generally increases as the number of faulty neighbors increase, although there is a reversal for some bins. In this case the overall defect level is 56 defective dice out of 11,881 or 0.47%, which is 2.75 times that for the best bin.

Similarly Table 3 shows the results when failures detected exclusively by only the IDDQ tests are considered escapes. For this case the best bin ended up with 43 test escapes and a defect level of 3.45%. The fraction of test escapes continues to increase through bin 7 with bin 8 having the only reversal. Again, this is probably a statistical aberration due to the small sample size in bin 8. The overall defect level is computed as 766 out of 12,649 or 6.06%, which is almost twice that of the best bin.

For comparison, we have included in Table 4 the results from the bipolar data presented in [7]. In this instance a DC functional test was applied at wafer sort and test escapes were those dice which failed more elaborate DC functional tests delay tests. These results show a similar trend to what we have seen in Tables 1 - 3. These results are less stable because of the smaller number of dice used in that study.

The earlier smaller bipolar study did not provide a high enough bin 0 population to directly observe test escapes and thereby estimate defect levels for the best bin. Results presented here indicate that the best bin can be reasonably expected to show a 2 - 5 factor improvement in defect levels over the average for the lot for moderate to high yields (the overall yield for these experiments was approximately 65%). The experiments also confirm the dependence of the best bin quality on test transparency. The defect level improvement is poorer for the case of I_{DDQ} escapes where the tests applied had a much higher escape rate. Overall experimental results are consistent with analytical projections for typical values of the clustering parameter in [9]. The final version of this paper will include extensive analysis to validate the analytical models based on this data.

5 Conclusion

The primary contribution of this paper is the analysis of actual submicron CMOS experimental test data to validate the potential of the defect cluster based die screening approach. Wafer defect maps for state of the art processes are very difficult to obtain for published studies; the availability of the SEMATECH experimental data has been invaluable.

The experimental study presented here has conclusively established the effectiveness of defect clustering based strategies in screening dice (and chips) with very low defect levels. Because this approach is orthogonal to all other techniques for improving test effectiveness, it can provide quality levels that cannot be achieved without exploiting defect clustering information. Defect level improvements of up to a factor of 5 can potentially be achieved for moderate to high yielding dice, and perhaps even more for large complex dice with low yields.

Observe that this screening approach is equally effective in screening out IDDQ failures as it is for DC functional failures and delay faults. This is because the underlying physical mechanism that our approach relies on is defect clustering. Defects, in general, can cause a range of faults with different manifestations. For this reason, binning can be expected to be equally effective in screening dice for other fault types, such as "faults" that are likely to result in burn-in failures. This is an important potential application for this die screening approach.

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Wafer Map Legend

$$ = Pass All Tests
IO = Shorts/Open Fail
SP = Softpower Fail
AF = All Fail
1T = Failed Stuck-at Exclusive
1F = Failed Functional Exclusive
1P = Failed Delay Exclusive
1I = Failed IDDQ Exclusive
3T = Failed All EXCEPT Stuck-at
3F = Failed All EXCEPT Functional
3P = Failed All EXCEPT Delay
3I = Failed All EXCEPT IDDQ
2A = Failed Functional Test and Delay test Only
2B = Failed Stuck-at Test and Delay test Only
2C = Failed Stuck-at Test and IDDQ test Only
2D = Failed Functional Test and IDDQ test Only
2E = Failed Functional Test and Stuck-at test Only
2F = Failed IDDQ Test and Delay test Only
XX = Test was not applied

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
0	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	.
1	..	..	..	..	..	..	..	..	$$	$$	AF	AF	$$	3F	..	..	..	..	..	..	..	.
2	..	..	..	..	..	..	3P	$$	AF	1I	1I	$$	$$	$$	$$	$$	AF	..	..	..	..	.
3	..	..	..	..	1I	$$	$$	AF	$$	$$	..	$$	AF	2E	$$	AF	AF	..	..	..	..	.
4	..	..	..	..	3F	$$	$$	$$	$$	$$	$$	$$	$$	..	3F	AF	1I	$$	AF	..	..	.
5	..	..	$$	$$	AF	$$	$$	AF	AF	3F	$$	$$	$$	$$	$$	$$	3F	$$	$$	AF	..	.
6	..	..	$$	$$	$$	$$	$$	$$	$$	$$	$$	$$	3F	$$	$$	$$	AF	$$	AF	AF	..	.
7	..	..	..	$$	$$	AF	$$	$$	$$	$$	AF	..	$$	AF	$$	3F	$$	$$	$$	$$	..	.
8	..	AF	AF	$$	AF	..	AF	$$	$$	$$	$$	..	$$	$$	$$	AF	$$	$$	$$	AF	3F	.
9	..	..	$$	$$	$$	$$	$$	$$	$$	..	3F	$$	$$	$$	$$	$$	$$	$$	$$	$$	AF	.
10	..	$$	$$	AF	$$	AF	$$	..	$$	AF	$$	3F	$$	$$	$$	AF	$$	$$	$$	$$	$$	.
11	..	..	2E	1I	3F	$$	3F	$$	$$	3F	$$	$$	..	$$	$$	$$	3F	$$	3F	AF	3F	.
12	..	..	3F	$$	AF	AF	..	$$	$$	$$	1I	$$	..	$$	AF	$$	$$	$$	..	$$	..	.
13	..	..	$$	AF	$$	3F	$$	AF	$$	$$	$$	AF	$$	AF	$$	$$	AF	$$	AF	..	..	.
14	..	..	..	..	$$	AF	$$	..	AF	..	AF	$$	AF	..	$$	$$	$$	$$	..	..	..	.
15	..	..	..	..	$$	AF	$$	$$	$$	3F	$$	AF	..	AF	AF	..	$$	..	..	..	..	.
16	..	..	..	..	..	$$	..	$$	$$	$$	..	3F	$$	AF	AF	..	AF	..	..	..	..	.
17	..	..	..	..	..	..	..	..	AF	..	..	..	..	AF	AF	..	..	..	..	..	..	.
18	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	.

Figure 1. Typical Wafer Map

Bin	No. Passing Functional & I_{DDQ}	Delay and Stuck-at Failures	% Fails after Functional and I_{DDQ}
0	600	1	0.17
1	1584	15	0.94
2	2378	19	0.79
3	2533	15	0.59
4	2109	23	1.08
5	1468	12	0.81
6	814	11	1.33
7	308	5	1.60
8	87	1	1.14
Lot Average	11881	56	0.86

Table 1: Binning results for Experiment #1

Bin	No. Passing Stuck-at & I_{DDQ}	Delay and Functional Failures	% Fails after Stuck-at and I_{DDQ}
0	590	1	0.17
1	1547	9	0.58
2	2379	3	0.13
3	2526	12	0.47
4	2110	11	0.52
5	1506	7	0.46
6	824	9	1.08
7	312	3	0.95
8	87	1	1.14
Lot Average	11881	56	0.47

Table 2: Binning results for Experiment #2

Bin	No. Passing Stuck-at & I_{DDQ}	Delay and Functional Failures	% Fails after Stuck-at and I_{DDQ}
0	1205	43	3.45
1	2322	117	4.80
2	2746	164	5.64
3	2491	149	5.64
4	1824	120	6.17
5	1203	98	7.53
6	611	48	7.28
7	198	24	10.81
8	49	3	5.77
Lot Average	12649	766	6.06

Table 3: Binning results for Experiment #3

Bin	No. Passing DC Tests	Failures after DC Tests	%Fails after DC Tests
0	1	0	0.00
1	9	1	11.11
2	39	0	0.00
3	108	9	8.33
4	224	14	6.25
5	297	21	7.07
6	324	41	12.70
7	194	31	16.0
8	91	19	20.9
Lot Average	1287	136	10.57

Table 4. Results from [7] with 9 Bins