



# Novel Three-Dimensional Vertical Interconnect Technology for Microwave and RF Applications

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# NOVEL THREE-DIMENSIONAL VERTICAL INTERCONNECT TECHNOLOGY FOR MICROWAVE AND RF APPLICATIONS

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**Abstract**—In this paper, novel 3D interconnects suitable for applications in microwave and RF integrated circuit technology have been presented. The interconnect fabrication process and design details are presented. In addition, measured and numerically modeled results of the performance of the interconnects have been shown. The results indicate that the proposed technology has tremendous potential applications in integrated circuit technology.

## I. INTRODUCTION

Recently, Microwave and RF integrated circuits (ICs) based on Silicon/Silicon germanium device technology have emerged as a viable alternative to ICs based on III-V semiconductor device technologies for wireless applications. These applications have experienced an exponential growth during the past few years. Current state-of-the-art digital ICs are also based on silicon technology and have the potential to be mono-lithically integrated with the above analogue ICs. Therefore, it is apparent that future generation of silicon analog circuits would have integrated digital control functions to enable them to make intelligent decisions. These advanced silicon mixed signal ICs would require efficient interconnects to allow combining different transmission media, such as, Coplanar Stripline (CPS) and Coplanar Waveguide (CPW) for maximum design flexibility. In addition, they are useful for enhancing packing density in the vertical direction as in small hand held communication devices. The interconnects have to be small in size for low parasitic coupling capacitances, and simple to fabricate for high yield and low manufacturing cost.

In this paper, we present several new design concepts for three-dimensional (3D) interconnects on a high resistivity (HR) silicon ( $\epsilon_{r2} = 11.7$ ) wafer. The 3D interconnects constitute very small sections of CPS at two levels connected by metallized vias and separated by a thin layer of spin-on-glass (SOG). CPS has the advantages of eliminating backside processing due to its uniplanar construction, and greatly simplifying vertical integration by the use of metallized vias. In addition, CPS being a slot type of transmission line allows easy integration of other transmission media, such as, slotline, CPW with finite width ground planes and micro-CPS [1] for greater design flexibility. The SOG has the advantage of low dielectric constant ( $\epsilon_{r1} = 3.1$ ) and hence low parasitic coupling capacitance. In addition, the SOG also planarizes the circuit and this

facilitates vertical integration [1]. The HR silicon wafer ( $\rho > 3000\Omega\text{-cm}$ ) has the advantage of lowering the signal attenuation in addition to improving the isolation between adjacent circuits.

In the following sections, first, the fabrication process of vertical interconnects is presented. Next, design considerations for the CPS vertical interconnects treated here are presented. The interconnects that are presented here are: CPS vertically interconnected overpass with a crossover, a CPS vertical interconnect with  $180^\circ$  phase shift and a CPW vertical interconnect with  $180^\circ$  phase shift. Last, in the section on results and discussion, first, the measured loss for CPS lines on HR Silicon is presented. Second, the computed results showing the performance of the CPS vertically interconnected overpass with a crossover is presented. The Finite Difference Time Domain (FDTD) [2] technique has been used to compute the performance of the CPS vertically interconnected overpass with a crossover. Finally, the measured phase characteristics of the CPS and CPW interconnects with  $180^\circ$  phase shift are presented. The experimental work for the purpose of demonstrating the low loss feature of the interconnects was performed using RT/duroid. The fabrication and characterization of interconnects with SOG-on-HR silicon are currently in progress. It is interesting to note that the measured and FDTD simulated results indicate that the interconnects presented here exhibit very good performance over a broad range of frequencies.

## II. INTERCONNECT FABRICATION

To begin the fabrication process, the lower strip conductor of thickness  $t_1 = 0.8 \mu\text{m}$  is fabricated on the HR Silicon substrate by a lift-off process [3]. Next, the dielectric spacer layer is built-up to the required thickness by multiple spin-coats. Accuglass 512 SOG [4] is used as the dielectric spacer layer. The thickness  $h_1$  of the Accuglass 512 SOG used here is  $2.0 \mu\text{m}$ . Lastly, the upper strip conductor of thickness  $t_2 = 2.0 \mu\text{m}$  is fabricated using the lift-off process once again. Gold metallization is used for the conductors.

## III. DESIGN CONSIDERATIONS

(a) CPS vertically interconnected overpass with crossover:

A CPS vertically interconnected overpass with a crossover on a HR silicon wafer of thickness  $h_2 = 400 \mu\text{m}$  is

shown in Figure 1. In this interconnect, the CPS strip width  $W_1 = W_2 = W$  and the separations  $S_1 = S_2 = S$  are chosen such that the characteristic impedance  $Z_{0(\text{CPS})}$  is  $50\Omega$ . The thickness of the SOG layer is  $h_1$ . The vertical interconnection between the first and the second level CPS conductors are provided by a pair of circular metallized vias. Each via in a pair is symmetrically located on the strip conductor and has a diameter  $d$ . A via pair is design as a small section of a vertical balanced transmission line with characteristic impedance  $Z_{0(\text{via})} = 50\Omega$ . The  $Z_{0(\text{via})}$  is related to the diameter  $d$ , separation between vias in a pair  $S_4$  and the dielectric constant of the medium surrounding the via  $\epsilon_{r1}$  through the expression,  $Z_{0(\text{via})} = (60/\sqrt{\epsilon_{r1}})\cosh^{-1}(N)$ , where  $N = 0.5[(2S_4/d)^2 - 2]$ . The probe pad at the input and output for the characterization with microwave wafer probes is typically about  $100\mu\text{m} \times 100\mu\text{m}$  in size.

(b) CPS Vertical Interconnect with  $180^\circ$  phase shift:

A CPS  $180^\circ$  phase shifter with vertically interconnected twisted overpass is shown in Figure 2. In this phase shifter, the CPS strip width  $W$  and separation  $S$  are chosen such that the characteristic impedance  $Z_{0(\text{CPS})}$  is  $50\Omega$ . The via diameter  $d$  is chosen to be the same as in Figure 1.

(c) CPW Vertical Interconnect with  $180^\circ$  phase shift:

A CPW  $180^\circ$  Phase shifter with vertically interconnected U-shaped overpass is shown in Figure 3. In this phase shifter, the CPW center strip conductor and slot widths  $S$  and  $W$  are chosen such that the characteristic impedance  $Z_{0(\text{CPW})}$  is  $50\Omega$ . The via diameter is chosen to be the same as in Figure 1.

#### IV. RESULTS AND DISCUSSION

(a) Measured Loss of CPS on HR Silicon:

In order to estimate the efficiency of the interconnects, the loss per unit length for  $50\Omega$  CPS is measured for a range of CPS test structures with  $W$  ranging from 26 to  $133\mu\text{m}$  and  $S$  ranging from 2 to  $10\mu\text{m}$ . This range presents typical dimensions encountered in practical circuits. In Figure 4, the measured loss is presented as a function of  $W$  and frequency. As an example, for a CPS with  $W = 54\mu\text{m}$  and  $S = 4\mu\text{m}$ , the measured loss is of the order of  $0.46\text{ dB/mm}$ . The CPS crossover in Figure 1 has a length of about  $328\mu\text{m}$  between the via pairs and hence the loss is estimated to be about  $0.15\text{ dB}$  at  $20\text{ GHz}$ . However, instead of choosing such small dimension, if  $S$  is chosen to be larger, say  $10\mu\text{m}$ , the corresponding loss for a  $50\Omega$  line reduces to about  $0.25\text{ dB/mm}$ , roughly reducing the total loss of the CPS crossover to about  $0.075\text{ dB}$  at  $20\text{ GHz}$ .

(b) CPS vertically interconnected overpass with crossover:

In order to study the performance of this interconnect, the scattering parameters (S-parameters) were computed using the FDTD scheme and they are shown in Figure 5.

The computed S-parameters for the overpass alone indicate that the insertion loss, ( $S_{21}$ ) is negligible and that the return loss ( $S_{11}$ ) is about  $-28\text{ dB}$ . The computed S-parameters for the overpass with a crossover shows that the insertion loss is still very small. However,  $S_{11}$  has increased from  $-28\text{ dB}$  to  $-12\text{ dB}$ . This increase in  $S_{11}$  can be offset by providing a step compensation as shown in Figure 1. Simulations with the step compensation are in progress. Computed  $S_{31}$  shows that the coupling between the overpass and the crossover is less than  $-40\text{ dB}$ .

(c) CPS and CPW vertical interconnects with  $180^\circ$  Phase Shift:

The measured phase characteristics for these circuits are shown in Figures 6 and 7. In these figures, the phase shift of the interconnect is compared with the phase of an equivalent length of through-line. From the figures, it is observed that the phase shift of the interconnect is close to  $180^\circ$  over a very broad range of frequencies. The excess loss of the interconnect is close to  $0.1\text{ dB}$ . FDTD simulations of the phase shifters are in progress.

#### V. CONCLUSION

A new 3D interconnect technology suitable for applications in microwave and RF integrated circuits has been proposed. Small sections of Coplanar Striplines connected by metallized vias and separated by a thin layer of spin-on-glass have been used to realize a variety of broadband high performance circuits. This technology yields small sized interconnects which are simple to fabricate. As examples, the CPS vertically interconnected overpass with a crossover, and  $180^\circ$  CPS and CPW phase shifters have been presented. The results obtained indicate the suitability of the proposed approach in facilitating 3D integration.

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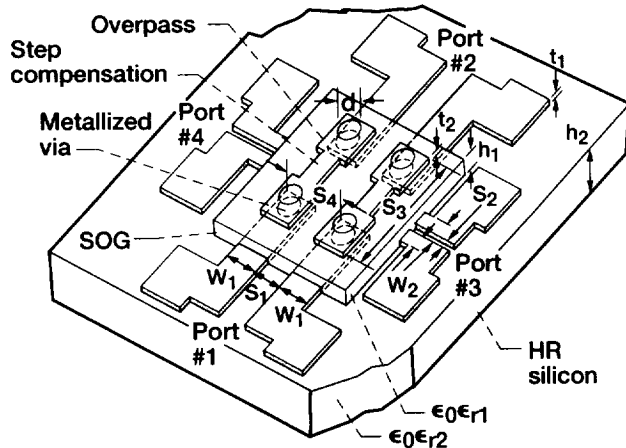


Figure 1.—Geometry of CPS overpass with crossover  
 $W_1 = W_2 = W = 54 \mu\text{m}$   $S_1 = S_2 = S = 4 \mu\text{m}$ ,  $d = 45 \mu\text{m}$ ,  
 $S_3 = 328 \mu\text{m}$ ,  $S_4 = 58 \mu\text{m}$ .

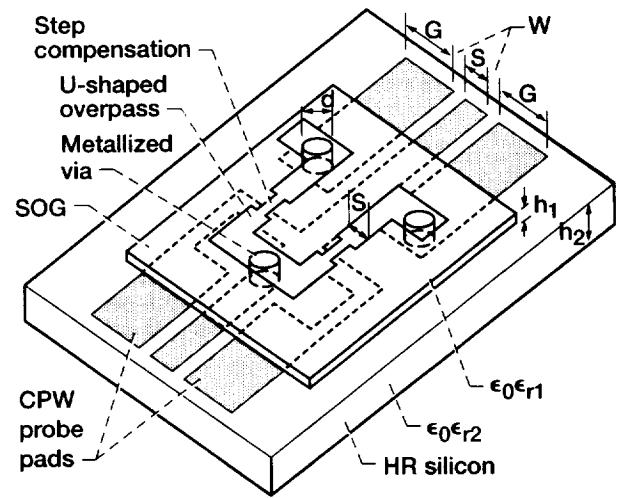


Figure 3.—CPW vertical interconnect with  $180^\circ$  phase shift  
 $S = 54 \mu\text{m}$ ,  $W = 34 \mu\text{m}$ ,  $G = 239 \mu\text{m}$ .

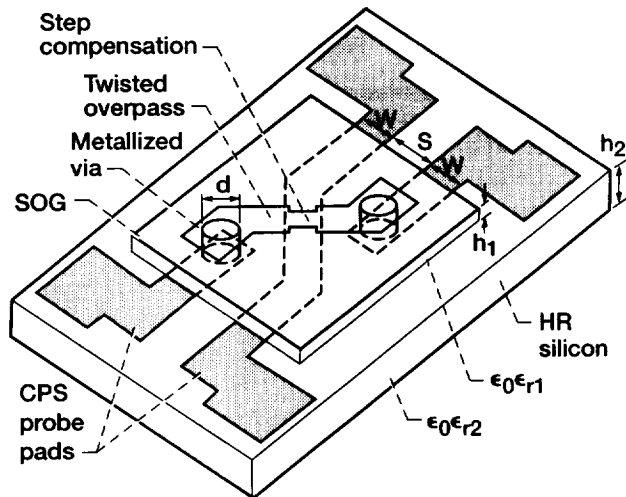


Figure 2.—CPS vertical interconnect with  $180^\circ$  phase shift  
 $W = 54 \mu\text{m}$ ,  $S = 4 \mu\text{m}$ .

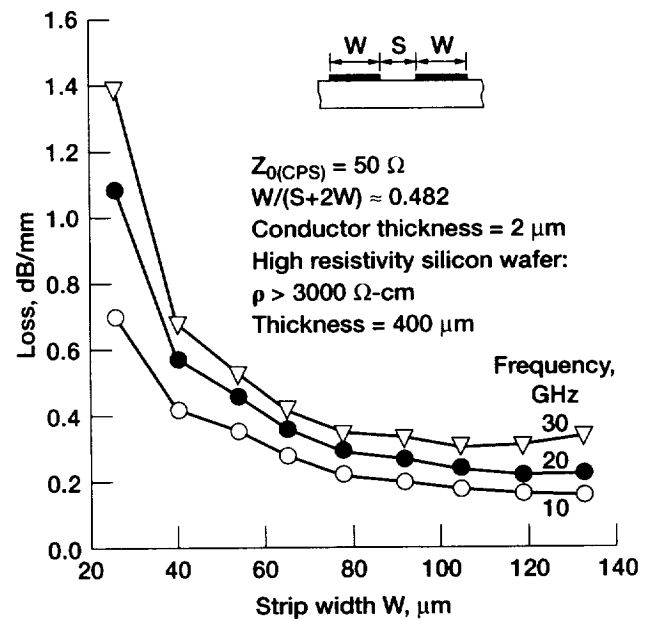


Figure 4.—Measured CPS loss versus strip width.

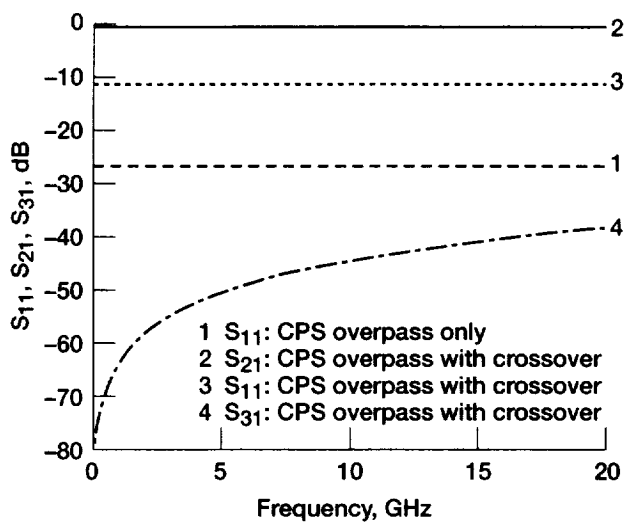


Figure 5.—Computed S-parameters for CPS vertically interconnected overpass with crossover.

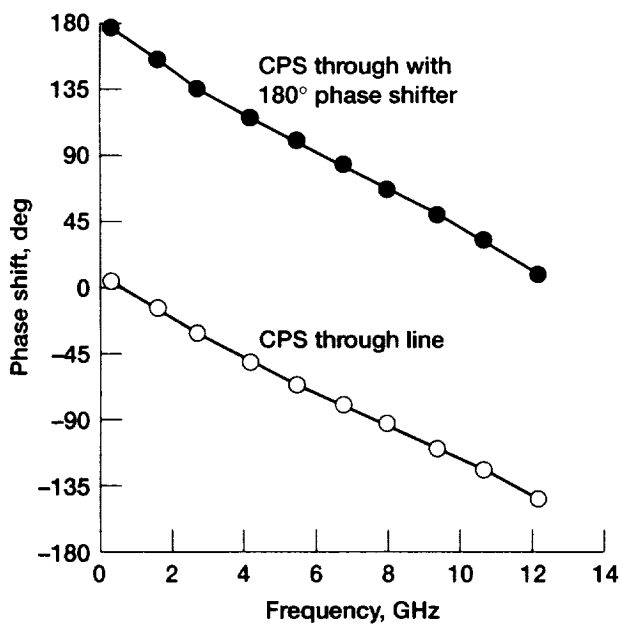


Figure 6.—Measured phase shift versus frequency  
 $h_2 = 254 \mu\text{m}$ ,  $\epsilon_{r2} = 10.5$ ,  $W = 254 \mu\text{m}$ ,  $S = 75 \mu\text{m}$ .

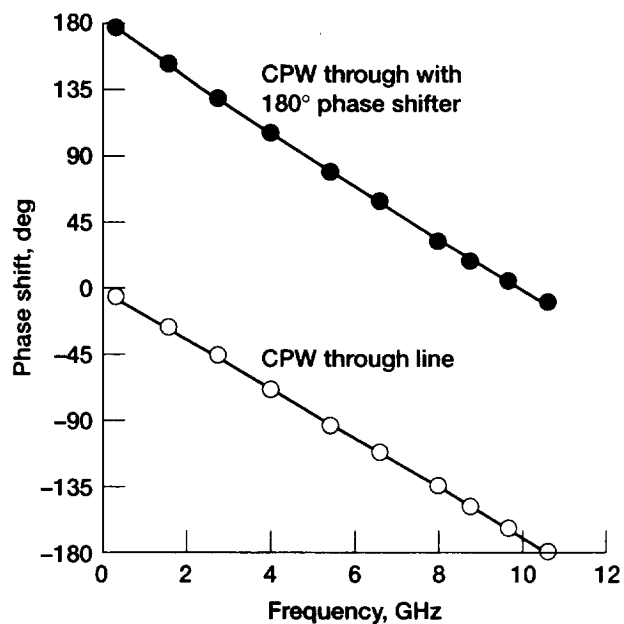


Figure 7.—Measured phase shift versus frequency  
 $h_2 = 254 \mu\text{m}$ ,  $\epsilon_{r2} = 10.5$ ,  $S = 165 \mu\text{m}$ ,  $W = 75 \mu\text{m}$   
 $G = 457 \mu\text{m}$ .



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