Report 11296
26 October 1998

Integrated Advanced Microwave Sounding Unit-A (AMSU-A) METSAT A2 Signal Processor Engineering Test Report (P/N: 1331120-2, S/N: F05) (Instr. S/N 109)

Contract No. NAS 5-32314
CDRL 207

Submitted to:

National Aeronautics and Space Administration
Goddard Space Flight Center
Greenbelt, Maryland 20771

Submitted by:

Aerojet
1100 West Hollyvale Street
Azusa, California 91702

TABLE OF CONTENTS

1.0 Introduction

This report presents a description of the tests performed, and the test data, for the A2 METSAT Signal Processor Assembly PN: 1331120-2, S/N F05. The assembly was tested in accordance with AE-26754, "METSAT Signal Processor Scan Drive Test and Integration Procedure".

The tests were conducted at room temperature in the AMSU-A test area of building 57. The tests fall into six categories: 1) Continuity, 2) Power Distribution, 3) Digital Processor, 4) Analog Processor, 5) Scan Drive, and 6) Supply Current.

2.0 Objective

The objective is to demonstrate functionality of the signal processor prior to instrument integration.

3.0 Test Data

All test data is presented on the enclosed copies of the test data sheets (TDSs) numbered TDS 11 through TDS 20 (Pages A-15 through A-25). TDS 11 (Pg. A15) was redlined to incorporate a design change defined in ECN CAMSU-1930. The redline was accomplished in accordance with program directive No. 91 and approved by Quality and the test engineer.

4.0 TESTS

4.1 Continuity

A complete continuity test of the backplane wiring is performed at the facility where the wirewrapping of the backplane is done. The continuity tests performed here involve 1) the I/O interface card slots, J301 and J324, and 2) chassis return connections. The tests are manual resistance measurements tests. Test data is presented on TDS 11.

4.2 Power Distribution

In these tests supply voltages are input to the signal processor from the Test Relay Unit (TRU) as in normal testing. No CCAs are installed in the signal processor for the tests. The test verifies that the four supply voltages are present on the proper pins of all backplane connectors. The test setup block diagram is shown in Figure 1, and test data is presented on TDS 12.

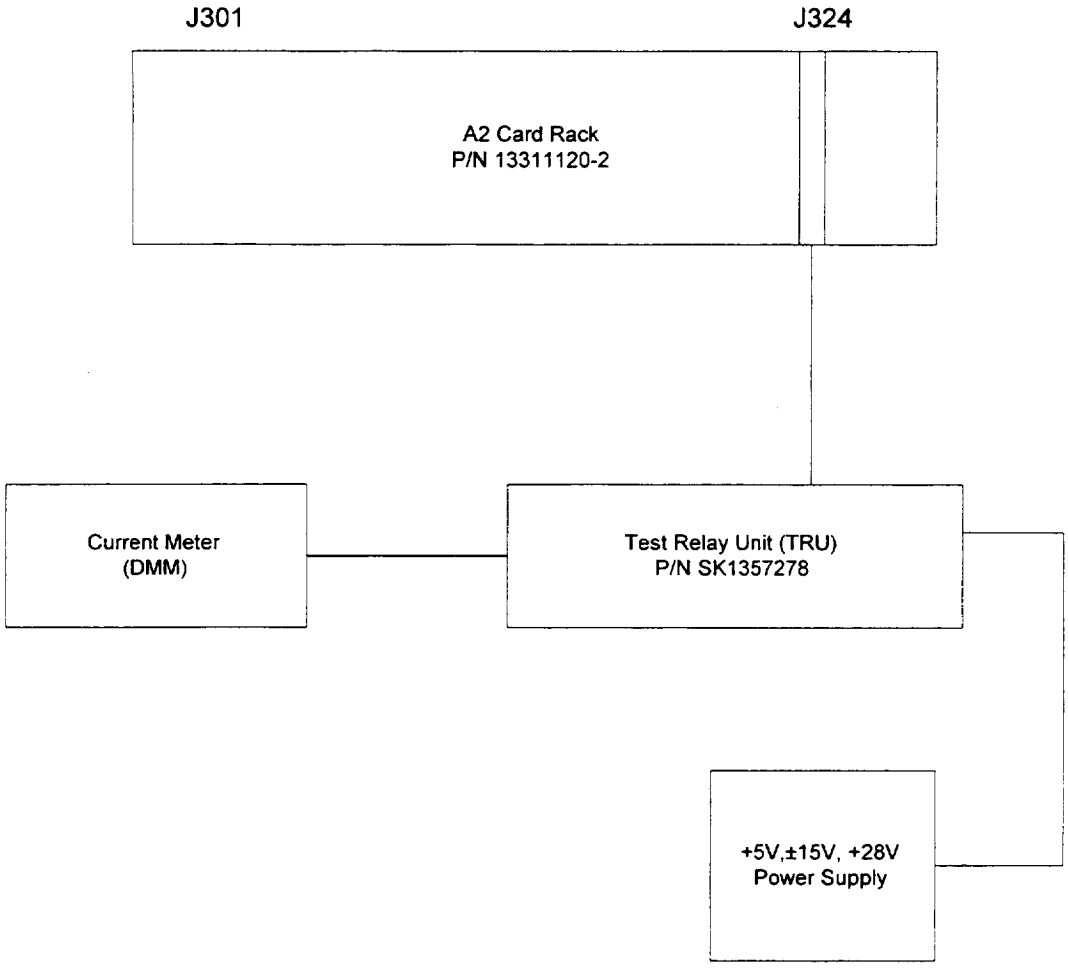


Figure 1. A2 Signal Processor Test Setup

4.3 Digital Processor

Beginning with this test, CCAs are installed into the card cage as required to perform the test, and then remain installed. At the conclusion of all tests, a complete set of CCAs has been installed. The complete test setup block diagram which is required for performing any of the tests is shown in Figure 2.

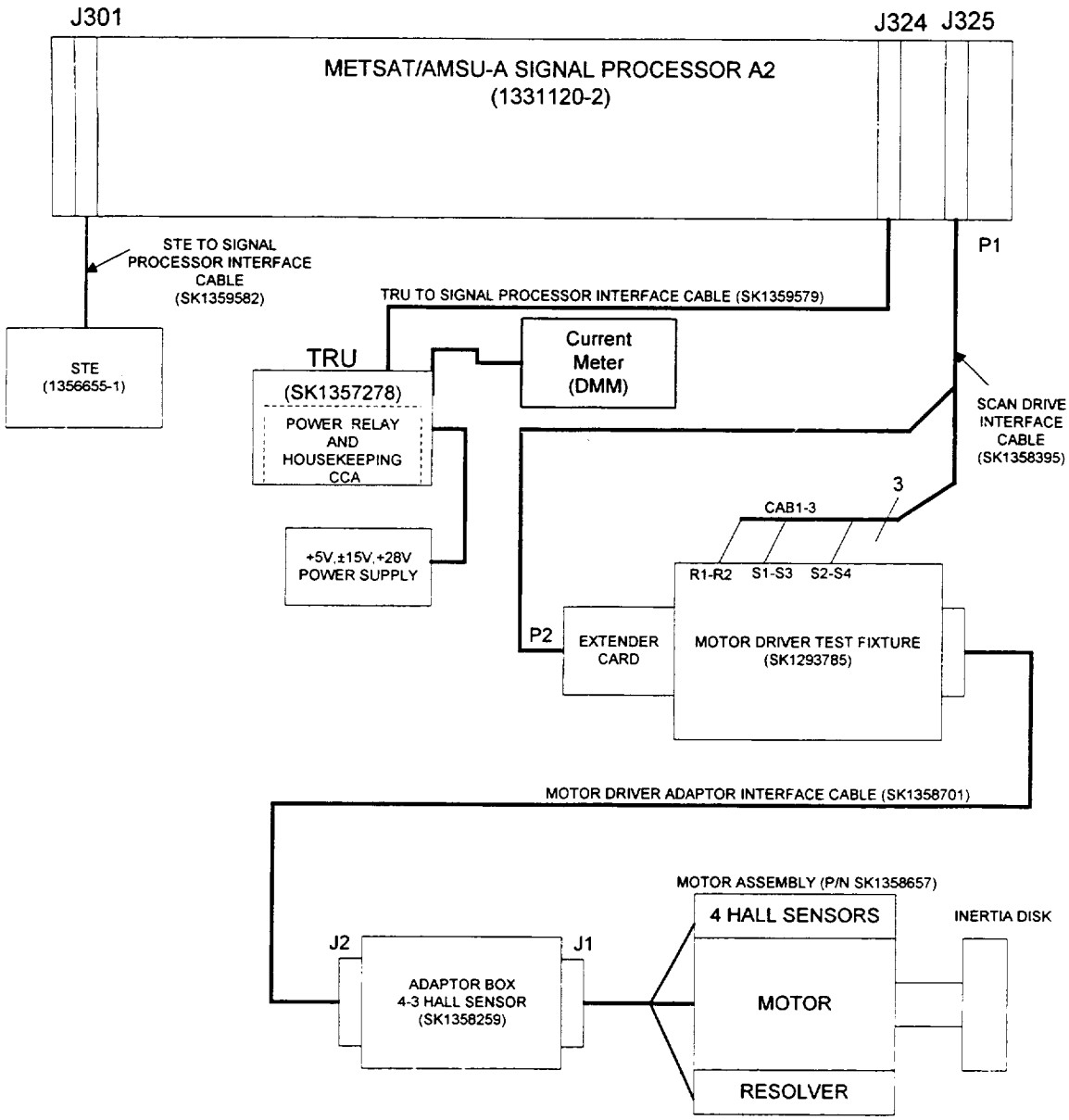


Figure 2. A2 Scan Drive Test Setup

4.3.1 Memory

In this test, the digital test set is used in place of the CPU CCA to read and verify data of the test PROMs on the "GOLD" Memory CCA. Test data is presented on TDS 13.

4.3.2 CPU

The CPU test requires that the CPU Auxiliary test CCA be installed in place of the Memory CCA. In this test, the RAM and various instructions performed by the CPU are tested. In addition, the waveform of the clock signal to the DC-DC converter is measured at the CLOCK jack on the TRU. Test data is presented on TDS 13.

4.3.3 Scan Control Interface

In this test, input and output ports 0 through 3 are tested. In addition, the disable feature of the input ports is checked out. Test data is presented on TDS 13.

4.3.4 Timing and Control

In this test, the proper time intervals of I/H, DUMP, INTCMPL,TSCMPL, STOP, and ANTENNA STROBE are verified. In addition to the above tests, the test set also checks the input ports 16 and 17, output port #13 (4 MSBs), output port 14, input port #15 (DAC BSY signal), and output port #13 (4 LSBs). Test data is presented on TDS 13.

4.3.5 Spacecraft Interface

In this test, the STE is turned on and initialized. The STE is tested with a series of self-tests to verify the readiness of the STE to test flight hardware. After successfully passing the self-tests, the STE is used to simulate the spacecraft command signals and retrieve limited test data for the remaining signal processor tests. STE test data is presented on TDS 14.

4.3.6 Relay Control

This test verifies the operation of the module power command and the survival heater command. The presence of the +10 volt Interface power is verified. The Scanner and Compensator relay drive and position indicators are also verified. Test data is presented on TDS 14.

4.4 Analog Processor

4.4.1 Independence of Measurements

This test is performed using the Analog CCA Test Fixture, the Integrate and Dump Filter and the Analog Mux and A/D Converter CCAs. The test gives a measurement of the sample-to-sample crosstalk within a channel, which is dependent on the completeness of the dump of the integration capacitor. Test data is presented on TDS 15.

4.4.2 Integrate/dump filter, radiometric data multiplexing, and digitization tests

In this test, a 2 volt dc signal is input to each integrate and dump filter, and the channel output code from the A/D converter is measured. The integrator output waveform is also displayed on an oscilloscope for verification of timing. Test data is presented on TDS 16.

4.4.3 Temperature monitoring circuits

In this test a resistor of value approximating the room temperature of the PRTs is connected at the input of each PRT readout circuit, and the output code from the A/D converter is measured. The reference voltage used in the PRT readout circuits is also measured.. Test data is presented on TDS 17.

4.4.4 Analog telemetry

In this test each of the analog telemetry signals is measured at the ANALOG HSKP jack on the TRU. Test data is presented on TDS 18.

4.5 Scan Drive

This test includes all CCAs involved in the scan drive function. The circuitry is programmed to provide one complete revolution of the drive motor as it steps through each of the thirty scene positions and the two calibration positions. The circuitry is programmed to park at the Warm Cal, Cold Cal, and the Nadir positions during the test sequence. The GSE test modes are also verified. To verify proper performance, the inertia disk on the motor shaft is visually observed through the one revolution and the various calibration positions. Test data is presented on TDS 19.

4.6 Supply Current

In this test, the total current drawn by the signal processor from each of the four supply voltages is measured with the signal processor fully populated with CCA's. Test data is presented on TDS 20.

5.0 TEST ANOMALIES

No test anomalies occurred during the Signal Processor engineering tests.

6.0 TEST RESULTS

The METSAT/AMSU A2 SIGNAL PROCESSOR TEST was successfully completed and all test data is within specified limits.

TEST DATA SHEET 11

A2 Continuity Tests (Paragraph 5.2.1)

Enter a Pass or Fail to indicate the result of the tests:

From	To	Signal Name	Pass/Fail
E1	J301-60	CHASSIS GND	P
E2	J301-90	CHASSIS GND	P
E4	J302-46	CHASSIS GND	P
E3	J324-76	CHASSIS GND	P
J324-73	J312-70	1.248 MHZ PS CLK	P
J324-74	J312-89	5V RTN(1) (1.248 MHZ PS CLK RTN)	P
~~J324-75~~	~~J312-91~~	~~5V RTN(1) (PS CLK SHIELD)~~	

Deleted per ECN CAMSU-1930
D Lund
9/17/98
QC 227

Assembly No. 1351120-2 Shop Order No. 548033

Serial No. F05 Pass ✓ Fail

Test Engineer D Lund 9/24/98 (Signature) (Date)

Quality Control 7A 268 SEP 24 '98 (Signature) (Date)

Customer Representative (Flight hardware only) (Signature) SEP 25 '98 (Date)

TEST DATA SHEET 12

A2 Power Distribution (Paragraphs 5.2.2 & 5.2.3)

Power Supply Voltages:

+5.7 ± 0.1V: 5.729V
+15.7 ± 0.1V: 15.694V
-15.7 ± 0.1V: -15.680V
+28.7 ± 0.1V: 28.699V

Test Set-up Verified: YES ✓ NO ____

Para. 5.2.3 Step No.	Connector No.	+5 ±0.5V	P/F	+15 ±0.3V	P/F	-15 ±0.3V	P/F	+28 ±0.56V	P/F	+9 ±1V*	P/F
7*	J301									9.42	P
2	J302			14.98	P	-14.99	P				
3	J303			14.98	P	-14.99	P				
4	J304			14.98	P	-14.99	P				
5	J305			14.98	P	-14.99	P				
6	J306	4.98	P	14.98	P	-14.99	P				
6	J307			14.98	P	-14.99	P				
6	J308	4.99	P							9.42	P
6	J309	4.99	P							9.42	P
6	J310	4.99	P								
6	J311	4.99	P								
6	J312	4.99	P								
6	J313	4.99	P								
6	J315	4.99	P								
6	J317	4.99	P	14.98	P	-14.99	P	27.96	P		
6	J318	4.99	P	14.98	P	-14.99	P				
6	J320	4.99	P								
6	J321	4.99	P	14.98	P	-14.99	P				
6	J322	4.99	P	14.98	P	-14.99	P	27.95	P		
6	J323	4.99	P	14.98	P	-14.99	P	27.94	P		
7	J325							27.96	P		

*measured at parragraph 5.2.5.2. test

Assembly No. 135-1120-2 Shop Order No. 548033

Serial No. F-05 Pass ✓ Fail ____

Test Engineer D Lund 9/24/98 Quality Control _____ SEP 24 '98
(Signature) (Date) (Signature) (Date)

Customer Representative (Flight hardware only) _____
(Signature) (Date)

TEST DATA SHEET 13 (Sheet 1 of 2)
A2 Digital Processor (Paragraph 5.2.4)

CPU CCA Serial No. (J312) F05
Scan Control Interface CCA Serial No. (J315) F17
Timing and Control CCA Serial No. (J311) F11

5.2.4.1 Memory tests:

5.2.4.1/10 Circle PASS or FAIL to indicate the result of the tests: (Pass) Fail

If "Fail", record the error code and error description.

Error Code: N/A
Error Description: N/A

5.2.4.2 CPU tests:

5.2.4.2/10		Measurements	Limits	Pass/Fail
	Vp-p	3.75 Vpp	3.30 - 4.94 V	P
	T	804 nS	761 - 841 ns	P

5.2.4.2/19 Circle PASS or FAIL to indicate if LEDs indicate CCA passed or failed: (Pass) Fail

5.2.4.3 Scan Control Interface Tests:

5.2.4.3/14	The input ports 0 and 1 tests	(Pass) Fail
5.2.4.3/21	Inhibit input port 0 and 1 tests	(Pass) Fail
5.2.4.3/29	The input ports 2 and 3 tests	(Pass) Fail
5.2.4.3/41	The output ports 0 and 1 tests	(Pass) Fail

If "Fail", record the error code and error description.

Error Code: N/A
Error Description: N/A

TEST DATA SHEET 13 (Sheet 2 of 2)
A2 Digital Processor (Paragraph 5.2.4)

5.2.4.4 Timing and Control Tests:

5.2.4.4/13	The Integrate and Hold pulse and the Dump pulse at the card rack slot J307.	(Pass)	Fail
5.2.4.4/25	The Integrate and Hold pulse and the Dump pulse at the card rack slot J301.	(Pass)	Fail
5.2.4.4/35	The Antenna Strobe pulse test.	(Pass)	Fail
5.2.4.4/47	The test of the interface to the Temp. Sensor Analog Mux card rack slot J303.	(Pass)	Fail
5.2.4.4/59	The test of the interface to the Analog Mux and Converter card rack slot J308.	(Pass)	Fail

If "Fail", record error code and error description:

Error Code: N/A

Error Description: N/A

Assembly No. 1351120-2 Shop Order No. 548033

Serial No. 105 Pass ✓ Fail ____

Test Engineer [signature] 9/24/98
(Signature) (Date)

Quality Control [signature] SEP 24 '98
(Signature) (Date)

Customer Representative (Flight hardware only) [signature] SEP 25 98
(Signature) (Date)

TEST DATA SHEET 14
A2 Relay Driver Tests (Paragraph 5.2.5.2)

Spacecraft Interface #2 CCA (J308) Ser. No. F20
Spacecraft Interface #1 CCA (J309) Ser. No. F16
Parallel to Serial Converter CCA (J310) Ser. No. F19
Relay Driver And Current Monitor CCA (J317) Ser. No. F03

Test Set-up Verified: Yes ✓ No ____ STE Self Test: Pass ✓ Fail ____

Step No.	Test Description	Pass/Fail
24	Module power connects	P
30	Survival heater power turns on	P
31	Survival heater power turns off	P
32	Module power disconnects	P
34	Scanner 2 power turns on	P
35	Compensator motor power turns on	P
36	Scanner 2 power turns off	P
36	Compensator motor power turns off	P
37	Module power disconnect	P

Assembly No. 1351120-2 Shop Order No. 548033
Serial No. F05 Pass ✓ Fail ____
Test Engineer [signature] 9/24/98 (Signature) (Date)
Quality Control [signature] SEP 24 '98 (Signature) (Date)
Customer Representative (Flight hardware only) [signature] SEP 25 '98 (Signature) (Date)

TEST DATA SHEET 15

A2 Independence Of Measurements (Paragraph 5.2.6.1)

Integrate and Dump CCA (J307): Serial No. F40

Analog Mux and A/D Converter CCA (J306): Serial No. F06

Test Set-up verified: YES ✓ NO _____

Supply (V)	Measured Value (V)	Limits (V)
+5	4.804V	+5 ± 0.25
+15	15.882V	+15 ± 1.0
-15	-15.427V	-15 ± 1.0

Channel No.	Average for SIGNAL switch in Hi position	Average for SIGNAL switch in LO position	Measurement Dependence ≤0.01%	Pass/ Fail
0	14043.4	14041.9	0.00229	P
1	14045.5	14043.1	0.00366	P
2	14035.7	14033.5	0.00336	P
3	14063.5	14061.6	0.0029	P

Assembly No. 1351120-2 Shop Order No. S48033

Serial No. F05 Pass ✓ Fail ____

Test Engineer D Lind 9/24/98 Quality Control _____ SEP 24 '98
(Signature) (Date) (Signature) (Date)

Customer Representative (Flight hardware only) _____ SEP 25 '98
(Signature) (Date)

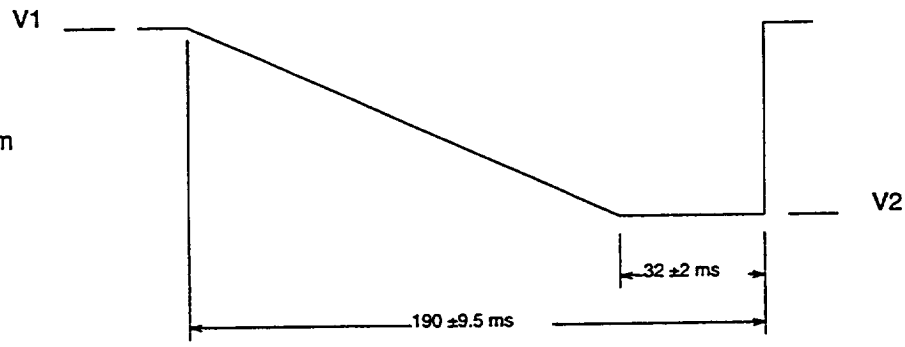
TEST DATA SHEET 16

A2 Integrator Signal Multiplexing, And Digitization (Paragraph 5.2.6.2)

Analog Mux and A/D Converter CCA(J306): Ser. No. F06

Integrate and Dump/Filter CCA (J307): Ser. No. F40

Output Waveform



Channel	Data	Data Limits	Data Pass/Fail	Integrator Waveform Pass/Fail
1	27703	26125 to 29757	P	P
2	27575	26125 to 29757	P	P

Signal Name	Pass/Fail
I/H	P
Dump	P
+5 Vdc GSE Interlock A	P
+5 Vdc GSE Interlock B	P

Assembly No. 1351120-2 Shop Order No. 548033

Serial No. F05 Pass ✓ Fail ____

Test Engineer D Lind 9/24/98 (Signature) (Date)

Quality Control (Signature) SEP 24 '98 (Date)

Customer Representative (Flight hardware only) (Signature) SEP 25 '98 (Date)

TEST DATA SHEET 17

A2 Temperature Monitoring Circuits (Paragraph 5.2.6.3)

Temperature Sensor Analog Mux CCA (J303) Serial No. F17

Temperature Sensor B CCA (J304) Serial No. F27

Temperature Sensor A CCA(J305) Serial No. F12

Dig. A Temp No.	Description	Data	Data Limits	Pass/Fail
1	Scan Motor	31132	28259 to 32513	P
2	Feedhorn	30941	28259 to 32513	P
3	RF MUX	31013	28259 to 32513	P
4	Mixer IF CH 1	30978	28259 to 32513	P
5	Mixer IF CH 2	30891	28259 to 32513	P
6	LO Channel 1	30972	28259 to 32513	P
7	LO Channel 2	31000	28259 to 32513	P
8	Comp Motor	31038	28259 to 32513	P
9	Subreflector	30778	28259 to 32513	P
10	Dc/Dc Converter	31104	28259 to 32513	P
11	RF Shelf	30956	28259 to 32513	P
12	Det/Preamp	31020	28259 to 32513	P
13	Warm Load Cntr	22540	20339 to 23401	P
14	Warm Load 1	22544	20339 to 23401	P
15	Warm Load 2	22265	20339 to 23401	P
16	Warm Load 3	22570	20339 to 23401	P
17	Warm Load 4	22222	20339 to 23401	P
18	Warm Load 5	22444	20339 to 23401	P
19	Warm Load 6	22360	20339 to 23401	P
20	Thermal Reference	25082	23340 to 26320	P

Assembly No. 135120-2 Shop Order No. 548033

Serial No. F05 Pass ✓ Fail ____

Test Engineer D Lind 9/24/98 Quality Control _____ SEP 24 '98

(Signature) (Date) (Signature) (Date)

Customer Representative (Flight hardware only) _____ SEP 25 '98

(Signature) (Date)

TEST DATA SHEET 18

A2 Analog Telemetry (Paragraph 5.2.6.4)

ANALOG HSKP Switch Position	DVM Reading (V)	Limits (V)	Pass/Fail
1	2.957	2.85 to 3.15	P
2	3.462	3.30 to 3.66	P
3	2.985	2.87 to 3.17	P
4	2.981	2.85 to 3.15	P
5	3.455	3.30 to 3.66	P
6	2.996	2.87 to 3.17	P
10	3.572	3.42 to 3.78	P
12	2.965	2.84 to 3.14	P
13	2.957	2.84 to 3.14	P
21	-0.01	-0.05 to 0.05	P
21	2.956	2.8 to 3.4	P
22	-0.012	-0.05 to 0.05	P
22	2.953	2.8 to 3.4	P

Assembly No. 1351120-2 Shop Order No. 548033

Serial No. F05 Pass ✓ Fail ____

Test Engineer D Lud 9/24/98 Quality Control SEP 24 '98
(Signature) (Date) (Signature) (Date)

SEP 25 98

Customer Representative (Flight hardware only) _____
(Signature) (Date)

TEST DATA SHEET 19

A2 Scan Drive/Compensator Drive/Signal Processor Tests (Paragraph 5.3.1)

A2 Scan Drive Subsystem CCAs:

Interface Converter CCA (J318) Ser. No. F24
Resolver Data Isolator CCA (J320) Ser. No. F24
R/D Converter/Oscillator CCA (J321) Ser. No. F12
Motor Drive 3-hall sensor CCA (J322) Ser. No. F07

Test Set-up Verified: Yes ✓ No ____

Para./Step No.	Mode	Pass/Fail
5.3.1.2.1/12	Motor in warm cal position	P
5.3.1.2.2/3	Motor in nadir position.	P
5.3.1.2.3/2	Motor in cold cal position 1	P
5.3.1.2.3/3	Motor in cold cal position 2	P
5.3.1.2.3/4	Motor in cold cal position 3	P
5.3.1.2.3/5	Motor in cold cal position 4	P
5.3.1.2.4/5	Motor in full scan mode	P
5.3.1.2.5/9	GSE mode 2	P
5.3.1.2.6/4	GSE mode 4	P
5.3.1.2.7/4	GSE mode 5	P
5.3.1.2.8/4	GSE mode 1	P
5.3.1.2.9/4	GSE mode 3	P
5.3.1.2.9/7	GSE mode 7	P
5.3.1.2.10/2	Scan power off	P

A2 Compensator Drive Subsystem CCAs:

Motor Driver 3-hall Sensor CCA (J323) Ser. No. F08

Test Set-up Verified: Yes ✓ No ____

Para./Step No.	Mode	Pass/Fail
5.3.2.2/4	Compensator motor operation	P
5.3.2.2/5	Power-off test of compensator motor	P

Assembly No. 1351120-2 Shop Order No. S48033

Serial No. F05 Pass ✓ Fail ____

Test Engineer [signature] 9/24/98 (Signature) (Date)

Quality Control [signature] SEP 24 '98 (Signature) (Date)

Customer Representative (Flight hardware only) [signature] SEP 25 '98 (Signature) (Date)

TEST DATA SHEET 20
A2 Supply Currents (Paragraph 5.4)

Voltages	Measured Current	Limits (in mA)	Pass/Fail
+28.7 V	7.68 mA	6 to 12	P
+5.7 V	444 mA	400 to 700	P
+15.7 V	129 mA	100 to 196	P
-15.7 V	-155 mA	-110 to -218	P

Assembly No. 135120-2 Shop Order No. 548033

Serial No. F05 Pass ✓ Fail ____

Test Engineer D Lund 9/24/98 (Signature) (Date)

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Customer Representative (Flight hardware only) ____ SEP 25 '98 (Signature) (Date)

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Report Documentation Page

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.
---	---	---

4. Title and Subtitle	5. Report Date
Integrated Advanced Microwave Sounding Unit-A (AMSU-A), Engineering Test Report	26 October 1998
	6. Performing Organization Code: ---
7. Author(s): D. Lund	8. Performing Organization Report No.: 11296
	10. Work Unit No.: ---
9. Performing Organization Name and Address: Aerojet, 1100 W. Hollyvale, Azusa, CA 91702	11. Contract or Grant No.: NAS 5-32314
	13. Type of Report and Period Covered: Final
12. Sponsoring Agency Name and Address: NASA, Goddard Space Flight Center, Greenbelt, Maryland 20771	14. Sponsoring Agency Code: ---

15. Supplementary Notes: ---

16. ABSTRACT (*Maximum 200 words*)

This is the Engineering Test Report, METSAT A2 Signal Processor (P/N 1331120-2, S/F F05), S/N 109, for the Integrated Advanced Microwave Sounding Unit-A (AMSU-A).

17. Key Words (Suggested by Author(s))	18. Distribution Statement
EOS Microwave System	Unclassified --- Unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of pages	22. Price
Unclassified	Unclassified		---

NASA FORM 1626 OCT 86

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Block 10. Work Unit No. Provide Research and Technology Objectives and Plants (RTOP) number.

Block 11. Contract or Grant No. Provide when applicable.

Block 12. Sponsoring Agency Name and Address. National Aeronautics and Space Administration, Washington, D.C. 20546-0001. If contractor report, add NASA installation or HQ program office.

Block 13. Type of Report and Period Covered. NASA formal report series; for Contractor Report also list type (interim, final) and period covered when applicable.

Block 14. Sponsoring Agency Code. Leave blank.

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Form Approved OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED

4. TITLE AND SUBTITLE
Integrated Advanced Microwave Sounding Unit-A (AMSU-A), Engineering Test Report

5. FUNDING NUMBERS
NAS 5-32314

6. AUTHOR(S)
D. Lund

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Aerojet
1100 W. Hollyvale
Azusa, CA 91702

8. PERFORMING ORGANIZATION REPORT NUMBER
11296
26 October 1998

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
NASA
Goddard Space Flight Center
Greenbelt, Maryland 20771

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
---

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE
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13. ABSTRACT (*Maximum 200 words*)

This is the Engineering Test Report, METSAT A2 Signal Processor (P/N 1331120-2, S/N F05), S/N 109, for the Integrated Advanced Microwave Sounding Unit-A (AMSU-A).

14. SUBJECT TERMS
EOS
Microwave System

15. NUMBER OF PAGES

16. PRICE CODE
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17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
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NSN 7540-01-280-5500

Standard Form 298 (Rev. 2-89)
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INPUT FROM: DATE D. Lund	CDRL: 207	SPECIFICATION ENGINEER: DATE N/A	
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REPORT DOCUMENTATION PAGE

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1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	October 1998	Contractor Report

4. TITLE AND SUBTITLE
Final Report: Integrated Advanced Microwave Sounding Unit-A (AMSU-A) Engineering Test Report METSAT A2 Signal Processor (P/N 1331120-2, S/N F05)

5. FUNDING NUMBERS
NAS5-32314

6. AUTHOR(S)
D. Lund

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS (ES)
Aerojet
1100 West Hollyvale St.
Azusa, CA 91702

8. PEFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS (ES)
National Aeronautics and Space Administration
Washington, DC 20546-0001

10. SPONSORING / MONITORING AGENCY REPORT NUMBER
CR—1998–208626

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT
Unclassified - Unlimited
Subject Category: 33
Report available from the NASA Center for AeroSpace Information,
Parkway Center/7121 Standard Drive, Hanover, Maryland 21076-1320

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13. ABSTRACT *(Maximum 200 words)*

This is the Engineering Test Report, METSAT A2 Signal Processor (P/N 1331120-2, S/N F05), S/N 109, for the Integrated Advanced Microwave Sounding Unit-A (AMSU-A).

14. SUBJECT TERMS
EOS, METSAT, engineering test report, microwave sounding

15. NUMBER OF PAGES
16

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
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