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The Effects of Architecture and Process on the Hardness of Programmable Technologies

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Abstract

Architecture and process, combined, significantly affect the hardness of programmable technologies. The effects of high energy ions, ferroelectric memory architectures, and shallow trench isolation are investigated. A detailed single event latchup (SEL) study has been performed.

I. Introduction

This paper will address the effects of architecture and process on the hardness of programmable microcircuits. Four issues will be explored in detail: (1) architectural effects on ferroelectric memories, (2) thin dielectric rupture and SEL energy dependence, (3) shallow trench isolation in 0.25 µm technology, and (4) the effects of scaling and process on SEL.

Non-volatile memories are important for spacecraft electronics. Traditionally, they have been used for program storage for microprocessors. With the introduction of SRAM-based FPGAs, the need for large, non-volatile memories will increase. An analysis of the architecture of ferroelectric memories (which is distinctly different from ferromagnetic memories) for SEE has been completed. Preliminary heavy ion and total dose testing has been completed using devices from several foundries.

Over the past several years much work has been focused on the dependence of SEUs on the impinging particle's energy [1,2]. The most common separation point low energy versus high energy is around 7-10 MeV/amu. The general result is that there may be a small variance in LET_{TH} for some devices where low energy regime gives a conservative result. In this work we focus on the particle energy dependence of SEL and antifuse dielectric rupture.

Modern FPGAs are now using leading edge fabrication processes. Moving from 0.35 µm to 0.25 µm technology, the isolation has changed from local oxidation of silicon (LOCOS) to shallow trench isolation. We have analyzed the effects of this with respect to radiation and present experimental SEL, SEU, and total dose results from several commercial foundries.

Finally, the A1020x series of FPGAs was used to conduct the latchup study. The 2.0 µm and 1.2 µm devices have been shown to be free of latchup, while the shrunk 1.0 µm device has latched repeatedly. Recent tests have shown a SEL_{TH} of ~ 20 MeV-cm^2/mg for Texas Instruments (TI) parts and between 27 and 37 MeV-cm^2/mg for Matsushita Electric Company (MEC) devices. The first part of the study investigated the cause of the A1020B 1.0 µm latchup. The second investigated, over a large sample size, the variability between parts and manufacturing lots and the effect of leaving the device latched for an extended period.

II. Ferroelectric Memories

The ferroelectric RAM (FRAM) provides non-volatile storage. Architecturally, it fits in a niche between DRAM, SRAM, and EEPROM. These architectural features each contribute to the SEU effects in this class of device.

The interface to the FRAM looks similar to a synchronous SRAM. This provides a short write cycle and eliminates the long write times associated with EEPROM technology and the need for polling. Also eliminated is the high voltage circuitry and the increased chance of rupture during the write cycle, which plagues EEPROMs. The synchronous interface, however, makes the latched address, for example, vulnerable to SEUs for a non-hardened device.

Like the EEPROM, the device has a limited number of write cycles; a difference is that the device will still be functional after the limit is exceeded but it will lose non-volatility. The FRAM is capable of a larger number of write operations, over 10^8, while EEPROM technology supports a significantly lower number. However, like a DRAM the read is destructive and must be restored with an internally generated write cycle. When the read/write cycle limited is exceeded, there is an increase, according to the commercial specification, of the soft error rate [3]. This suggests that an increase in the SEU rate may also be expected. The number of accesses for a device of this class must be managed, as the device can not be used like a battery-backed SRAM. Fortunately, for FPGA configuration storage applications, 10^8 cycles is far more than would be needed. For microprocessor boot code storage applications, this is more of a concern, as the microprocessor can not execute code stored in FRAM for an indefinite period of time. The read cycle, similar to that of the DRAM, uses pre-charged bit lines and sense amplifiers which latch, followed by a restore operation. The number of read operations is limited, which differs from EEPROM technology.

Figure 1 shows the basic mechanism for the non-volatile storage structure. Unlike the DRAM cell, which stores charge on a capacitor or an EEPROM cell which stores

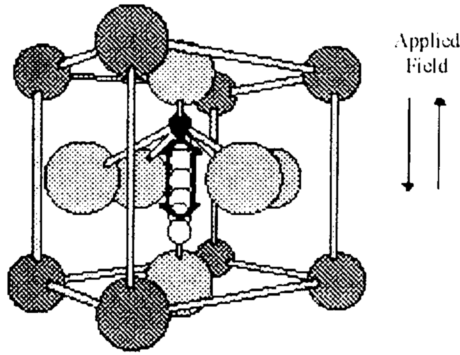

Figure 1. FRAM memory cell stores data within a crystalline structure and maintains two stable states, providing non-volatile storage. The ferroelectric film is deposited between electrode plates to form a capacitor [Figure from RAMTRON, Corp.].

charge on a gate structure, the FRAM cell stores data within a crystalline structure, called a Perovskite crystal. Figure 2, below, shows a "two transistor, two-capacitor" (2T2C) topology. The two cells in this differential architecture provide a local reference. High density devices will likely use a 1T1C topology with a global reference.

Based on the brief architectural analysis above, we would expect to see SEUs independent of the hardness of the storage cell for non-hardened, COTS technology. Latches, both for digital data and in the sense amplifier, along with the pre-charged bit lines, may be susceptible. Our initial test results on both research and pre-production devices showed upsets at modest LET's; i.e., ~20 MeV-cm^2/mg. These two sets of devices are produced at two different fabrication facilities. Other radiation effects precluded us from obtaining a large enough data set to produce a meaningful cross-section vs. LET curve.

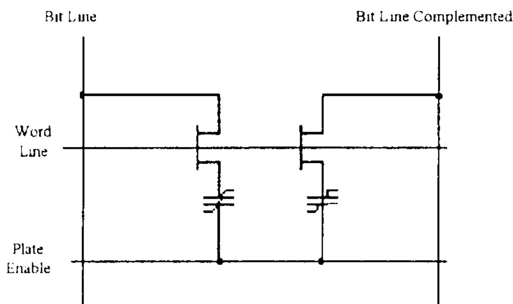

Figure 2. Two-transistor, two-capacitor (2T2C) FRAM memory cell. The differential architecture provides each bit with its own reference, eliminating capacitor variance over the die. High density memories, 1 megabit, will likely use a 1T1C cell and a global reference. Reads are destructive [Figure from RAMTRON, Corp.].

Two serial FRAM devices, the FM24C16 and the FM25160, are produced at a different fabrication facility (Rohm) than the FM1680. These devices did not latchup at an LET = 74 MeV-cm^2/mg when tested at V_{DD} = 5.5VDC. No functional testing was done on the serial devices. This initial screen was for SEL detection, only.

For the parallel FM1608 device, we observed what appeared to be latchup. For the research parts, the SEL currents ranged from 125 mA to over 800 mA, the limit programmed into the test equipment. For pre-production parts from the Fujitsu foundry, our three samples each latched at an LET of 18 MeV-cm^2/mg, the lowest LET used in our test. Latchup currents observed for these devices ranged from 200 to 700 mA. Because of the low SEL_{TH}, detailed SEU measurements were not performed nor were accurate SEL cross-sections determined. Fujitsu devices with improved latchup characteristics, according to the manufacturer, are currently being shipped to our lab and will be tested and reported in future works.

SEE testing showed an additional failure mode during heavy ion irradiation of the parallel FM1608 device. In this case, the current draw of the device dropped sharply to zero. The device became non-functional, then later recovered, with the ion beam still on. A typical example is shown in Figure 3. It is seen that the current dropped from its active, dynamic level of approximately 6.3 mA to near zero, coinciding with the lost of functionality. It then increased to approximately 0.5 mA before returning to its normal, dynamic level. The device operated normally during the remainder of the test. This effect was seen at least three times during our limited testing of this set of devices. This current signature is similar to that seen in our analysis of IEEE 1149.1 JTAG structures [4] and it is tempting to assume that the device entered a test mode. The manufacturer indicated that this was not a plausible explanation. This temporary loss of functionality remains an open area for investigation and will be pursued in more detail when more SEL-tolerant parts are produced. From a worst-case analysis viewpoint, it is assumed that a bit gets toggled during the heavy ion test. For an actual space-flight mission, it would not get a second SEU, if that is needed, to clear the fault, resulting in system failure. Again, if SEL-tolerant devices are produced, this will be pursued, and an experiment conducted to see if the beam is required to clear the fault.

Total dose "quick-look" experiments were run on two types of serial devices and the parallel FM1608 device. In situ static current measurement data is shown in Figure 4. This exposure showed that the samples produced at Rohm and at Ramtron's research fabrication facility could withstand moderate doses without significant leakage currents. Post irradiation testing of the FM1608 showed that all devices catastrophically failed, with all locations containing the same value. Room temperature and 100°C annealing steps did not recover functionality. In situ functional tests or the more

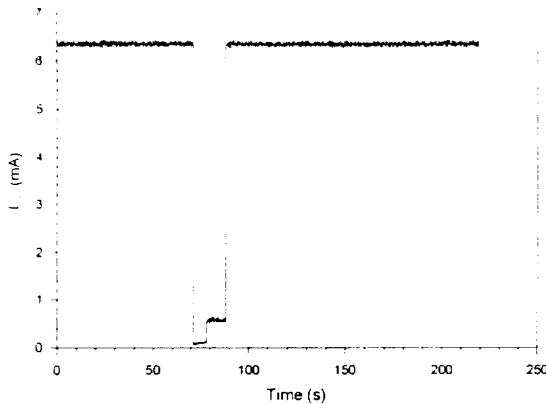

Figure 3. Strip chart of FM1608 (research fab) current during heavy ion irradiation. The device lost functionality during the test while the current decreased from it's normal dynamic levels of approximately 6.3 mA to it's quiescent value, near zero. The device recovered functionally and operated normally throughout the latter part of the test. This effect was seen at least three times during the limited testing of this device.

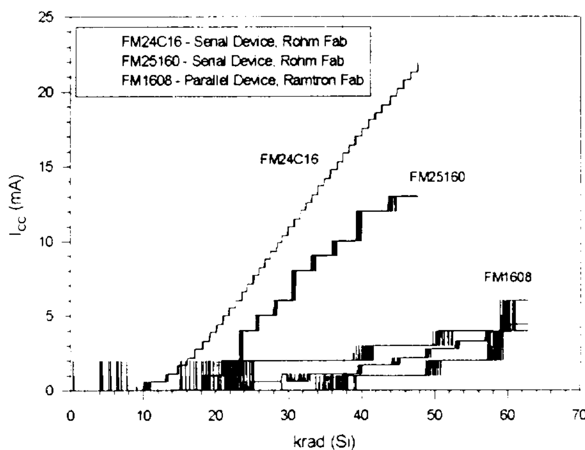

Figure 4. In situ static current measurements of two serial and one parallel FRAM device types. This initial study showed that Rohm (serial) and Ramtron research fab (parallel) devices could withstand moderate doses without significant leakage currents. Post irradiation testing of the FM1608 showed that all devices catastrophically failed. Annealing did not help. In situ functional tests or a step irradiation method are needed for determination of the functional limit. The base CMOS process is not the limiting factor for the FM1608. Only I_{CC} was measured on the serial devices.

labor intensive step irradiation method is needed for determination of the functional limit. The base CMOS process does not the appear to be the limiting factor for the FM1608. It is suspected that circuits specific to the sensing or writing of the FRAM circuit element are sensitive to the total dose exposure.

III. Energy Dependence of Heavy-Ion Induced Single Event Latchup and Dielectric Rupture

A. Introduction

Over the past several years much work has been focused on the dependence of single event upsets measurements on the impinging particle's energy [1,2]. The most common separation point between low energy and high energy is around 7-10 MeV/amu. The general result is that there may be a small variance in the threshold LET for SEU for some devices where low energy regime gives a conservative result. These data show that for most modern devices there is little or no variation in SEU cross section and threshold LET over the available ground test particle energies. In this work we focus on the particle energy dependence of single event latchup (SEL) and single event dielectric rupture (SEDR) in the Actel FPGA. The irradiations were carried out at Tandem van de Graaff at Brookhaven National Laboratory (BNL) and at the National Superconducting Cyclotron Laboratory (NSCL) at Michigan State University.

B. Using the Appropriate Ground Based Radiation Environment

The space environment seen by most microelectronics has particles with energies that range over orders of magnitude [5]. For example: behind 100 mils of aluminum the iron spectrum ranges from 1×10^{-1} to 1×10^{3} MeV/amu with less than an order of magnitude variation in the flux. The LET for this environment ranges from 0.2 to >30 MeV-cm^2/mg. Figure 5 gives two LET spectra behind 100 mils of aluminum at geostationary orbit. The closed circles are for all heavy particles with atom number between 1 and 92. The open circles show the curve for iron (Z=26) ions. The solid line is the ratio of the iron to all other ions. It is interesting to note that the environment is comprised of >50% iron for LETs > 1 MeV-cm^2/mg. Also note that for LETs > 20 MeV-cm^2/mg the space environment is >65% iron. The energy per unit mass for iron ions with this LET must be < 10 MeV/amu. If one suspects that the single event phenomena being studied is particle energy dependent, it is not sufficient to perform testing within one energy regime.

C. SEDR Experimental Setup and Results

Past experimental testing [4 and references therein] has shown that biased, unprogrammed Oxide-Nitride-Oxide (ONO) antifuses are susceptible to single particle induced

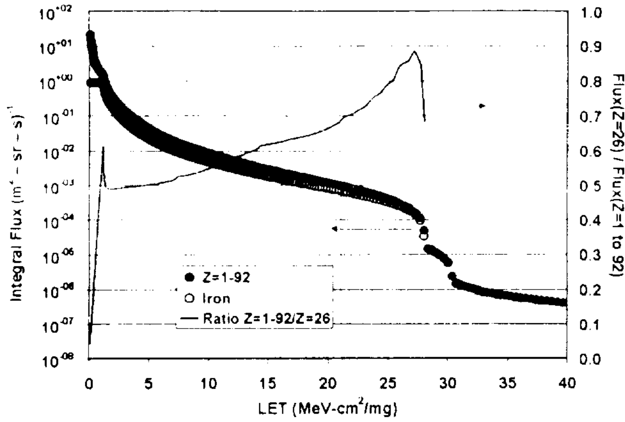

Figure 5. Comparison of galactic cosmic ray spectrum between all elements and iron at geostationary orbit behind 100 mils of spherical aluminum shielding. Note that for LETs > 20 MeV-cm²/mg the space environment is >65% iron. The energy per unit mass for iron ions with this LET is < 10 MeV/amu. This shows the importance of performing radiation testing at low and high energy for phenomena exhibiting an energy dependence.

rupture. In [4] we reported the minimum required bias to rupture the dielectric for the A1280A when measured at Brookhaven National Laboratory (BNL) (<4 MeV/amu). In this study we performed irradiations on the Actel A1280A at the National Superconducting Cyclotron Laboratory (NSCL).

At NSCL 7740 MeV (60 MeV/amu) Xe ions were used. Aluminum energy degraders were used to increase the normal incidence LET. At an LET of 37 MeV-cm²/mg the energy is decreased to 26 MeV/amu. At 45 MeV-cm²/mg it is decreased to 17 MeV/amu. The residual energy after passing though the degraders was > 2191 MeV for all case.

Figure 6 shows the data collected on the A1280A at BNL and the same for data on the A1280A at NSCL. There is no difference in the critical bias for rupture at the two energies. At NSCL (> 17 MeV/amu) and at BNL (<4 MeV/amu) the critical bias when the LET was 37 MeV-cm²/mg the critical bias was ~6V, and at 45 MeV-cm²/mg the critical bias was ~5.5V.

The areal geometry of the antifuse in the device study is on the order of a square micrometer. Predictions of radial track distributions are typically less than a micrometer, with a majority of the charge being located in a region < 0.1 micrometers from the center of the track. These devices are ideal structures to experimentally measure effects of track structure in dielectrics. They have a well-defined structure both in thickness and lateral dimensions. Had significant charge been deposited in the region outside 1 micrometer area of the antifuse the there would have been a significant

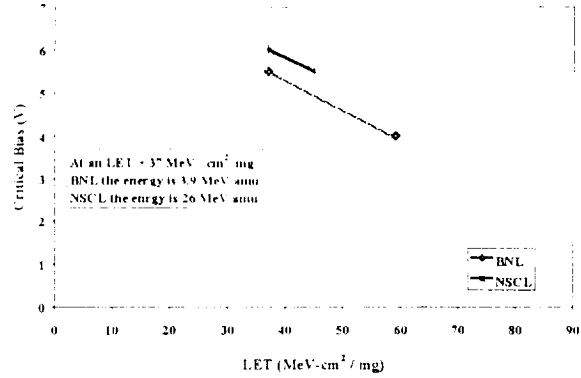

Figure 6. Comparison of critical bias measurements for antifuse rupture at BNL and NSCL. No significant dependence on energy is found and the lower energy BNL ions were the worst-case.

difference in the critical bias. We did not observe an energy dependence on the critical bias for these devices.

D. SEL Experimental Results and Discussion

SEL testing was preformed on the Actel A1020B at BNL and at NSCL. Texas Instruments fabricated the devices. The same devices where used at both facilities (serial numbers TIC42 and TIC43). Testing was done at V_{CC} = 5.5V and at room temperature.

At BNL 250 MeV (5.3 MeV/amu) Ti ions, LET = 19 MeV-cm²/mg, and 220-MeV (6.4 MeV/amu) Cl ions, LET = 11 MeV-cm²/mg were used. Angles were used to increase the effective LET.

At NSCL 5040 MeV (60 MeV/amu) Kr ions were used. Aluminum energy degraders were used to increase the normal incidence LET. At an LET of 23 MeV-cm²/mg the energy is decreased to 18 MeV/amu. At 26 MeV-cm²/mg it is decreased to 14 MeV/amu and at 30 MeV-cm²/mg the energy per unit mass drops to 10 MeV/amu. The residual energy after passing though the degraders was > 800 MeV for all case.

Figure 7 compares the results obtained at each facility for TIC43. The solid filled symbols connected by the solid line are the total number of latchup events divided by the total integral fluence for all exposures. There are between 5 and 7 events for each data point or a fluence of at least 1×10^7 p/cm² was achieved. The triangles data collected at NSCL at normal incidence. The squares are data collected at BNL at normal incidence (Ti, Ni, Br). The circles are data collected at BNL at some angle of incidence (Cl, Ti).

At first glance, this data appears to show that for high energy data the SEL cross section is an order of magnitude lower and has a higher threshold LET. This may be a valid analysis of the data. However, having only 5 to 7 events as a

measure of cross section would result in a 3 sigma of the data that overlaps, an order of magnitude accuracy is all that is expected for these types of measurements. Given the statistics of the data we cannot clearly state that we have observed and energy dependence in error cross section.

Also at first glance, the data in Figure 7 appears to show a difference in threshold LET for high (NSCL) and low (BNL) energy measurements. For the NSCL data the estimated the threshold LET one somewhere between 23 and 26 MeV-cm^2/mg. For the BNL data collected at some angle of incidence the threshold LET is found to less than 19 MeV-cm^2/mg. For the BNL normal incidence data the threshold is found to be between 19 and 26 MeV-cm^2/mg. Comparison of the data collected at BNL normal (squares) incidence versus some angle of incidence (circles) at an LET of 18 MeV-cm^2 / mg shows that difference can also be by an angular dependence. Threshold LET for the ActelA1020B FPGA with serial number TIC42 was determined to be between 21 and 26 MeV-cm^2/mg at both NSCL and BNL measured at normal incidence.

The data shows that when there are inconsistencies in high energy and low energy data that they are small and that the low energy data is conservative. Looking at this in context with the high percentage of low energy iron particles that exist in the space environment one must consider that, at least for these devices (and perhaps others), low energy data is required to evaluate this technology for space flight applications.

Table 1. Ion species used at each facility

Facility	Ion	LET (MeV-cm^2/mg)	Energy/mass (MeV/amu)
NSCL	Xe	37	26
NSCL	Xe	45	17
NSCL	Kr	23	18
NSCL	Kr	26	14
NSCL	Kr	30	10
BNL	Cl	11	6.4
BNL	Ti	19	5.3
BNL	Ni	26	4.8
BNL	Br	37	3.9

IV. SHALLOW TRENCH ISOLATION

It has been a concern that modern commercial processes will limit the use of devices to radiation soft applications. Additionally, with the move to 0.25 µm technology, local oxidation of silicon (LOCOS) has been replaced with shallow trench isolation (STI). A discussion of the LOCOS and STI technologies, and their performance in radiation circuits, can be found in [6]. It is discussed that

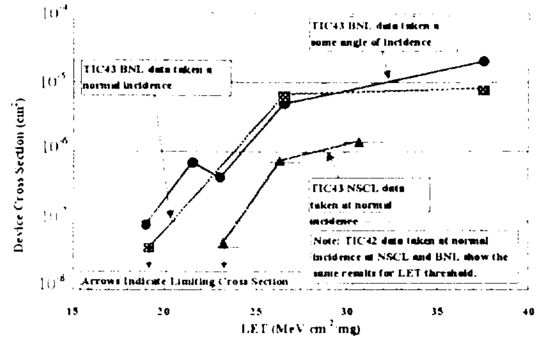

Figure 7. Heavy-ion cross section data taken at BNL and at NSCL on TIC43. Note that BNL data taken at some angle of incidence shows a different LET threshold than that at normal incidence. The NSCL data is normal incidence. The energy dependence of LET threshold is small with lower energy being more conservative. Low number of events limits the analysis of difference in SEL cross section.

most LOCOS commercial circuits would have low radiation-hardness (< 10 krad (SiO_2) because of leakage currents; STI was expected to do no better or perhaps worse.

Recently, processes have moved from 0.6 µm to 0.35 µm and then to 0.25 µm. Correspondingly, supply voltages have changed from 5.0 V to 3.3 V and then 2.5 V as typical field oxide thickness decreased from 7000 Å to 3500 Å then to 3000 Å. The thinner field oxide reduces the hole generation and trapping. Thin gate oxides, < 100 A, removes most of the total dose affects from the gate oxide.

A series of tests were run on two very early prototype FPGAs, each of radically different architectures, having little

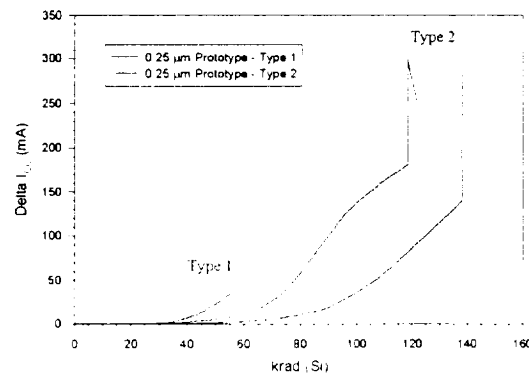

Figure 8. Leakage current of STI as a function of total dose exposure. Two device types (both early prototypes) of completely different architectures were tested. Each was built on a 0.25 µm, 2.5 volt STI process. Results are similar to 0.35 µm, 3.3 volt LOCOS process.

in common. One device type is an SRAM-based FPGA; the other is antifuse-based. In addition to the configuration memory technology, one device employs lookup tables (LUTs) for the implementation of logic; the other contains multiplexors and flip-flops.

Figure 8 shows the leakage current of these 0.25 µm, 2.5 volt STI devices as a function of total dose exposure. It is noted that the results fall into the "radiation-tolerant" range and are similar to 0.35 µm, 3.3 volt LOCOS process [4].

V. LATCHUP ISSUES

Previous work has shown that the A1020B 1.0 µm device was susceptible to single event latchup (SEL) while its larger cousins, the 2.0 µm A1020 and the 1.2 µm A1020A showed no sign of SEL. The 1.0 µm A1280A, a second-generation architecture, with a better design for SEL prevention, also demonstrated no evidence of SEL. Destructive physical analysis (DPA) did not identify the cause of the A1020B SEL, with correct processing factors such as epi-layer thickness verified. Circuit layout was considered a factor, with the smaller spacing of the A1020B believed to be the cause in this scaled device. To aid in our understanding of the causes of this latchup, we used experimental devices (A1020Z) fabricated on the 1.0 µm processing line but using the 1.2 µm mask set. The resulting A1020Z test samples did not exhibit latchup up to a LET of 120 MeV-cm^2/mg, showing that the scaling of the circuit design caused the SEL sensitivity, not the change in process at MEC.

For the large sample size A1020B SEL test, devices were taken from several lots. Only MEC dies are reported here, with the TI-produced dies less often used in space-flight electronics. The resulting summary of SEL data is listed in Table 2. The effective LET of the ions used in the test ranged from 18 to 74 MeV-cm^2/mg. The test samples were dynamically operated during exposure and the operating current of the device under test (DUT) was sampled and during the irradiation. The supply current was initially limited to 800 mA; later it was raised to a 2 A limit to test for destructive SEL. The saturated latchup cross section is defined as the "mean +2 sigma" of all cross sections at an LET of 75 MeV-cm^2/mg that exhibited latchup and whose beam time was greater than 10 seconds.

The SEL LET_{TH} for the test samples ranged from 37 to >75 MeV-cm^2/mg with no significant grouping dependent on lot. The latchup cross section ranged from 10^{-6} to 10^{-5} cm^2/device with a discernable dependence on lot: mean+2σ is 4×10^{-6} cm^2/device for lot U1P054 and 10^{-5} cm^2/device for lot U1P126. None of the test samples exhibited spontaneous destruction from the latched condition; however, four test samples were damaged when the latched condition was allowed to remain. We are making no conclusion on the length of time required for damage to occur from a SEL, as

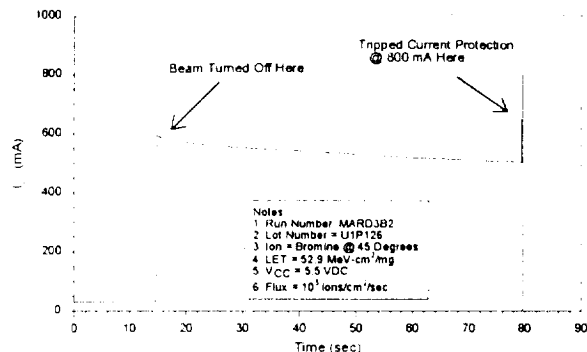

Figure 9. One effect of prolonged latchup on an A1020B. Large current jumps were observed on many devices; this run showed that, while the current was decreasing and the part appeared stable, I_{CC} rapidly increased, hitting the current limit of 800mA programmed for that run.

there is insufficient data and no analysis to give a solid position. Mostly, damage consisted of slight current increases with an unknown effect on reliability. Initial latchup currents varied from 80 to over 800 mA and some of the test samples that exhibited an initial latchup current of over 500 mA were allowed to remain latched, in vacuum, for several minutes. Note that our test pattern does not have 100% fault coverage of the device. Figure 9 is a plot of the operating current

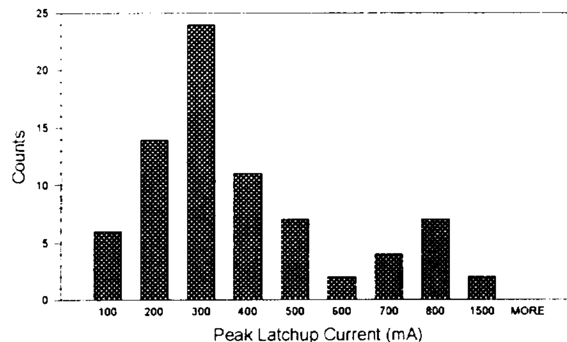

Figure 10. Distribution of peak latchup currents for the A1020B (MEC). Each label shows the maximum value for its bin. A wide range of latchup currents shows the need for large test sets if a latchup detection and removal circuit is contemplated. DC current shifts from TID exposure and transient current surges from normal operation must be distinguished from latchups with low current values. High latchup currents may blow fuses, trigger overcurrent protections, or place a supply into constant current mode, dropping the voltage, possibly affecting additional circuits and system performance.

during a prolonged latch. Although the part appears to be stable in the latched condition, and is in fact decreasing, there was a sudden I_{CC} "runaway." This shows that intervention to remove power from a latched device must be on-board and autonomous.

Table 2. SEL Summary for A1020B. A large set of parts from multiple lots were tested, showing a wide range of SEL LET_{TH} and latchup currents. Some latchups were destructive with either higher I_{CC} or functional failure.

S/N	Lot No.	D/C	Threshold	Cross Section (cm²)	Prolonged Latchup Allowed?
A1	U1P126	9646	52.9	1.5×10^{-6}	no
A4	U1P061	9402	52.9	4.50×10^{-6}	no
B1	U1P054	9851	52.9	3.4×10^{-7}	no
B2	U1P054	9851	43.2	2.0×10^{-6}	no
B3	U1P054	9851	52.9	3.0×10^{-6}	yes
B4	U1P054	9851	52.9	1.5×10^{-6}	yes
B5	U1P054	9851	> 74.7	no latchup	-
B6	U1P054	9851	> 74.7	no latchup	-
C1	U1P054	9844	52.9	3.0×10^{-6}	no
C2	U1P054	9844	43.2	no data @75	yes
C3	U1P054	9844	74.7	no data @75	no
D1	U1P126	9704	43.2	6.7×10^{-6}	no
D2	U1P126	9704	43.2	9.4×10^{-6}	no
D3	U1P126	9704	43.2	no data @75	yes
D4	U1P126	9704	< 37.4	no data @75	yes
D5	U1P126	9704	< 43.2	no data @75	yes

The distribution of peak latchup currents for the A1020B (MEC) is shown in Figure 10. It is seen that a wide range of latchup currents was observed. This shows the need for large test sets if a latchup detection and removal circuit is contemplated. On the low end of the peak current distribution, DC current shifts from TID exposure and transient current surges from normal operation must be distinguished from latchups with low current values, to prevent false triggering of detection circuits. On the other end, high latchup currents may blow fuses, trigger overcurrent protections in power supplies, or place a power supply into constant current mode, dropping the voltage, possibly affecting additional circuits and system performance. This can result in deadlock if the detection and removal circuits are on the same supply as the device that is latching.

This data shows the importance of performing latchup testing on a significant number of test samples to accurately determine the latchup characteristics, particularly if a latchup detection and removal solution is being considered. Increasingly, devices that exhibit SEL are used in non-critical satellite systems, and the latchup characteristics must be fully understood to assess the risk of doing so and to properly apply the part and any support circuitry.

VI. Conclusions

This examination of the effects of architecture and process on the radiation hardness of programmable technologies makes it clear that this specialized technology class must be analyzed and tested carefully, on a case by case basis. Antifuse hardness, having been studied with low energy heavy ions, is seen to have similar critical bias voltages under exposure to high energy ions. Latchup for some programmable designs is a function of the feature size, with the closer structures in the shrunk design leading to latchup susceptibility. This testing showed no statistically significant difference whether high or low energy ions are used, with the lower energy ions being slightly more conservative. This may be important for failure rate predictions and test strategies, with the lower energy, more cost-effective beams being adequate for testing and qualification. Similar to the proton susceptibility study performed on DRAMs and the FPGA's [7], we see that a small sample set for detailed latchup studies may be inadequate. This is of increased importance if a latchup detection and removal circuit is being designed. Our study of commercial FRAM technologies shows that leakage current, an indicator of damage in typical CMOS digital circuits, can be a poor metric to judge damage to the overall chip, for total dose exposures. Additionally, porting the FRAM device to a new fabrication facility had a significant change in SEL performance, showing the effect of process. This is in direct contrast to the A1020x experiment, where it was shown that design was the key driver, not a change of process. Each of these unique devices must be evaluated and analyzed on a case by case basis. Rules of thumb and "proof by similarity" often do not apply to these technologies.

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