SRAM Based Re-programmable FPGA for Space Applications

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Abstract

An SRAM (static random access memory)-based re-programmable FPGA (field programmable gate array) is investigated for space applications. A new commercial prototype, named the RS family, was used as an example for the investigation. The device is fabricated in a 0.25μm CMOS technology. Its architecture is reviewed to provide a better understanding of the impact of single event upset (SEU) on the device during operation. The SEU effect of different memories available on the device is evaluated. Heavy ion test data and SPICE simulations are used integrally to extract the threshold LET (linear energy transfer). Together with the saturation cross-section measurement from the layout, a rate prediction is done on each memory type. The SEU in the configuration SRAM is identified as the dominant failure mode and is discussed in detail. The single event transient error in combinational logic is also investigated and simulated by SPICE. SEU mitigation by hardening the memories and employing EDAC (error detection and correction) at the device level are presented. For the configuration SRAM (CSRAM) cell, the trade-off between resistor de-coupling and redundancy hardening techniques are investigated with interesting results. Preliminary heavy ion test data show no sign of SEL (single event latch-up). With regard to ionizing radiation effects, the increase in static leakage current (static I_{CC}) measured indicates a device tolerance of approximately 50krad(Si).

I. INTRODUCTION

The antifuse FPGA has gained significant visibility in recent years as the programmable logic device choice for space applications. The antifuse switch is nonvolatile and insensitive to both single event and total dose effects. Compared to mask-wired ASICs (application specific integrated circuits), it has the advantage in turnaround, flexibility, and (hardware) cost per design, while maintaining the same radiation performance. However, there has been a tremendous interest in re-programmable FPGAs for the potential realization of a "re-programmable satellite" in the future. There are two re-programmable FPGA technologies in the market right now. One uses a FLASH/EEPROM (electrically erasable programmable read only memory) configuration switch and the other an SRAM switch. This paper will focus on the SRAM-based technology only. The development and radiation effects for FLASH-based FPGAs will be published elsewhere (see reference [1]).

Intrinsically, the SRAM-based FPGA is very sensitive to single events. The primary concern is the SEU of the SRAM configuration bits. Unlike the aforementioned nonvolatile switches, the volatile SRAM switch is prone to SEU. Figure 1 shows the simplified schematics of the SRAM controlled switch. Each design is implemented into an FPGA by the configuration of many switches like this. CSRAM is used in this paper as the acronym for this configuration-SRAM cell. SEUs in the CSRAM will change the design configuration, and cause functional failure at the device level. Without reloading the corrupted configuration bits, the device cannot regain its functionality. Also, the corruption of the configuration may induce driver contention and locally cause abnormally high current. The SEU upset rates due to CSRAM switches on a single FPGA device are very high because of the large number of CSRAM switches. For example, in a fine-grained architecture (see Figure 12 in [2]), there are approximately one million configuration-bits in a 50k-gate device. Without introducing a process hardening technique, or employing SEU mitigation techniques, the utilization of SRAM-based FPGAs will be prohibitive for many space applications.
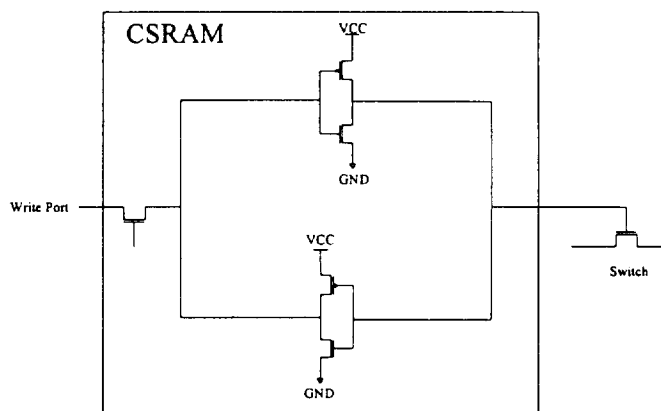

Figure 1. The schematics of the CSRAM controlled switch.

There have been serious efforts to develop a viable, radiation-hard SRAM-based FPGA. The most significant recent venture is a NASA/Honeywell/Atmel joint effort using SOI (silicon on insulator) technology to implement an existing low (6k) gate count product. While the radiation performance is still in development, the proposed approach will not satisfy the cheap, large gate count needs of commercial satellites. Many more efforts are still needed to make a re-programmable FPGA meet the performance, cost and radiation requirements for the space market.

This paper presents results of the investigation of an SRAM-based FPGA for its radiation performance and potential enhancement. A commercial prototype, named the RS product family is used as the starting point. Both SEE (single event effects) and total ionization dose (TID) effects

are investigated. Focus is on the SEU of memory bits in the device.

The scope of this paper is relatively wide by nature. Because of the publishing limitation, only details for those fresh data and new findings are presented. The well-known materials will be kept short and the interested reader should consult the references for further details.

II. DEVICE TECHNOLOGY

The Actel product presented in this paper is called RS. It is fabricated on the advanced 0.25μm CMOS technology in commercial foundries. Key wafer-fabrication elements [3] relevant to radiation effects are listed in Table 1.

Table 1. Key fabrication parameters

Technology	0.25μm CMOS
Substrate	Bulk silicon
Device Tub	N-Well
Isolation	Shallow Trench Isolation (STI)

III. DEVICE ARCHITECTURE AND SEU

This section gives a brief introduction of the device architecture. The main purpose is to identify different types of memory in the device for their SEU ramifications.

A. Architecture Overview

The architecture has three (3) levels of hierarchy [4]. Within each level of hierarchy, the structure is a two dimensional array. In the device investigated, the top level of the routing hierarchy is called B4 (Figure 2). It made out of a 4x4 rectangular array of tiles called B16x16, together with I/O (input/output) blocks on the periphery. It has approximately a 50k-gate capacity when counted as gate-array equivalent.

The B16x16 tile itself is the middle level of the hierarchy. It is composed of 16x16 arrays of block called B1. This array is served by a two-dimensional mesh routing structure. Each B16x16 tile also includes 9K bits of user SRAM (USRAM) and additional routing resources for its employment.

The lowest level of the hierarchy is the B1 block. As shown in Figure 3, B1 has four quads of functional modules and associated interconnect routing resources. Each quad has a trio, composed of two three-input lookup tables (LUT3) and a flip-flop (FF), and a two input look-up table (LUT2).

The routing tracks are populated with CSRAM switches. A user design is defined by specifying the state of every CSRAM in the device.

B Memory Types

If the device architecture is surveyed from a functional building block point of view, it is composed of logic modules, USRAM (user SRAM), I/O blocks, and is interspersed with

routing tracks and configuration switches. Three memory types identified from functional blocks are listed in Table 2. The effect of the SEU in each memory type is discussed separately in the following subsections.
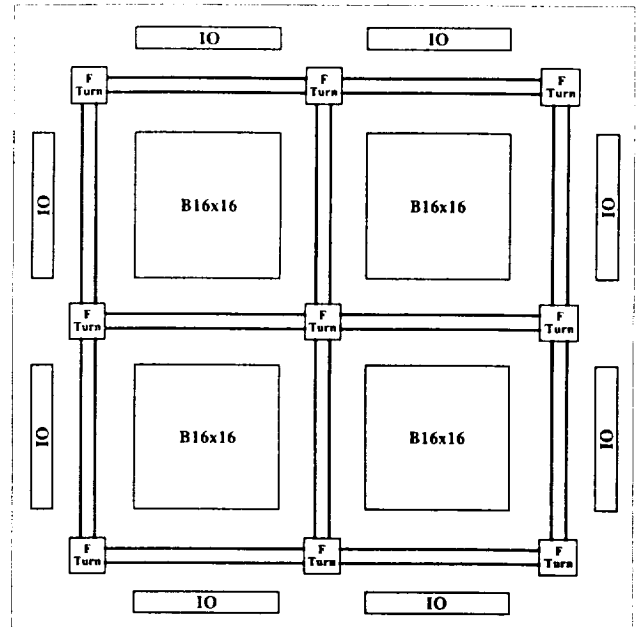

Figure 2. Floor plan of a four B16x16 tile (B4) RS device

C. CSRAM SEU

CSRAM is a five-transistor SRAM, designed for fast read and small die area. Since the N-well (P-substrate) process is used, the N+ junctions (N-hit) are more vulnerable than P+ junctions (P-hit). The upset of any one CSRAM bit potentially will cause a functional failure at the device level. This functional failure is considered *soft* if the errors in CSRAM configuration are corrected quickly. The simplest error correction approach is to reload the configuration states from an uncorrupted storage.

There are potential high current modes in the device due to CSRAM SEU. For example, when two inverter outputs with different states are connected erroneously due to the CSRAM upset (Figure 4), there is a static current through transistors and interconnects from V_{CC} to GND. This situation is close to a micro-latch-up. However, the current is through well-designed transistors while latch-up occurs in parasitic structures. A permanent damage in metallization, for example, is unlikely.

D. USRAM SEU

The user SRAM is the same design as the CSRAM except extra transistor logic is added for fast read and write. Its SEU sensitivity is the same too. However, the SEU ramification is totally different. The upset of a USRAM can only cause a soft data error. The functionality of the device is still intact. However, there is a potential latent functional failure mode. When the USRAM is used for storing a configuration state, an

SEU will induce a functional failure at a later time when that erroneous configuration datum is then loaded into the CSRAM.
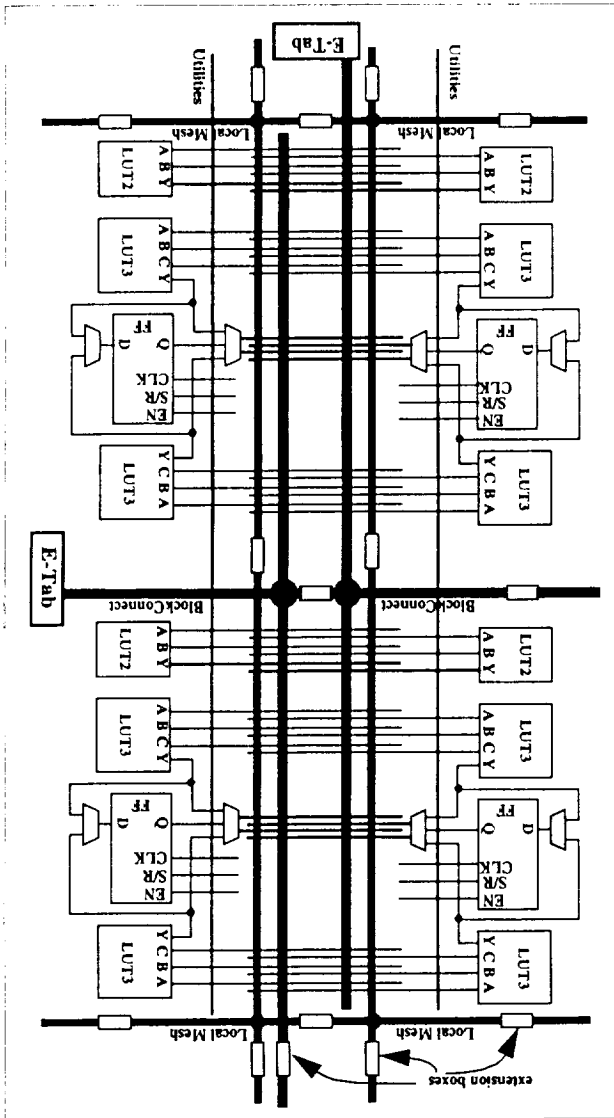

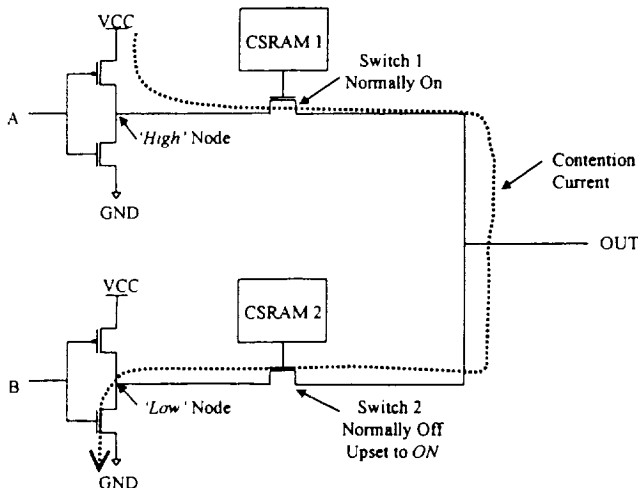Figure 3. The logic blocks and routing in B1.

Figure 4. Drive contention due to CSRAM SEU

E. User FF SEU

The user FF in the logic module (see Figure 3) is an edge-triggered master-slave with preset design. It also has logic for controlling the programming and testing. An SEU in the user FF will only cause a soft data error.

F. Control Logic SEU

In-flight programming will expose all shift registers in the control logic for SEU. But the programming period is short compared to the mission duration. Once programming is complete, the control logic used for programming is disabled by a hardwired reset and thus the SEU sensitivity is eliminated. The IEEE 1149 standard also known as JTAG is implemented in RS products for the board level testing. SEU in the TAP (test access port) controller will cause functional failures very similar to the failure due to CSRAM SEU. To eliminate this problem, the optional TRST (test rest input) input will be implemented to 'hard-reset' the TAP controller. Reference [2] presents a well summarized discussion regarding to JTAG SEU in the FPGA devices.

IV. SEU IN MEMORIES

A. Heavy Ion Testing Results and SPICE Simulation

In the SPICE simulator, the heavy ion effect is modeled by injecting a hit current pulse at the (reverse-biased) active junctions. This current pulse is of a triangular shape with rise time and fall time equal to 100ps. The injection node is clamped to either GND or V_{CC} by a variable capacitor during charge collection. This method assumes the hit pulse is much faster than the circuit response and ignores the detailed timing information carried in the pulse shape. It is the-worst-case-design simulation to generate a relatively conservative critical charge for SEU. The resulting critical charge (Q_{crit}) is an approximation of the Q_{sig} (the charge significant to the upset process) in reference [5].

The junction depletion depth, approximately 0.3μm, is calculated from direct measurement of the junction capacitance. To find the funnel length, heavy ion testing data measured on a 0.25μm flip-flop is used to derive the charge collection depth.

The charge collection depth (d_{coll}), is extracted by:

$$Q_{crit} = LCT_{th} \cdot d_{coll} \qquad (1)$$

Where Q_{crit} is the critical charge for upset. It is generated from SPICE simulation by the method mentioned above. LCT (linear charge transfer) is the charge equivalent of LET. Its value is:

$$LCT = \rho_{Si} \cdot LET / 3.6eV \qquad (2)$$

Where ρ_{Si} is the density of silicon, and 3.6eV is the energy needed to generate an electron-hole pair in silicon. LET_{th} was measured by heavy ion testing at Brookhaven National Laboratory (BNL). For this flip-flop, Q_{crit} was found

Table 2. The upset rates of different memory types in GEO environment.

Memory Type	Population per Device	Q_{crit} (pC)	LET_{th} (MeV-cm^2/mg)	Cross-Section (cm^2)	Upset Rate per Day	
					per Bit	per Device
CSRAM	1.0×10^6	0.027	2.7	1.20×10^{-8}	1.14×10^{-8}	1.14×10^{-2}
USRAM	3.7×10^4	0.027	2.7	1.20×10^{-8}	1.14×10^{-8}	4.22×10^{-4}
User FF	4.0×10^3	0.040	4.0	1.22×10^{-7}	8.19×10^{-8}	3.28×10^{-4}

equal to 0.05pC by simulation, and LCT was measured 0.05pC/μm experimentally, making d_{coll} equal to 1μm. Hence the funnel length is approximately 0.7μm. Note that the diffusion collection mechanism is neglected and all the charges collected are folded into the depletion and funnel collection. Once the charge collection depth is known, we can derive the LET_{th} for any memory circuit when Q_{crit} is acquired using a SPICE analysis.

The critical charge for different memory types in RS are simulated and listed in Table 2. The device populations of the different memory types are calculated using the 50k-gate, B4 device (Figure 2) in the RS family.

B. SEU Rate Prediction

To evaluate the radiation tolerance at the device level, the upset rate of each memory type is calculated using Space Radiation 4.0. The space environment is the Geosynchrous orbit with the solar minimum condition. Spacecraft shielding is assumed as 100mil aluminum.

For device parameters, the LET is converted from Q_{crit} by equation 1. The saturation cross section is measured from the layout design. The Weibull shape of 2 and width of 10MeV-cm^2/mg are assumed. These numbers are believed to be conservative based on the fact that there are several active junctions in every single event, and also from previous heavy ion test data on Actel FPGA devices. Usually much more gradual Weibull curves were measured.

The result of the upset rate for each memory type is listed in Table 2. It is clear that the CSRAM dominates the SEU issue at the device level. Actually during real operations, not all USRAMs nor all user FFs in one device, will be active and prone to SEU at any instant.

V. SINGLE EVENT TRANSIENT ERRORS IN COMBINATIONAL LOGIC

Compared to the 0.35μm technology, V_{CC} is reduced from 3.3V to 2.5V for 0.25μm. The digitized signal noise margin is significantly reduced and the device becomes particularly susceptible to combinational logic soft errors.

In the case of an SRAM-based FPGA, an important transient upset mode (called mode 2 in the following) due to the heavy ion hitting on the CSRAM is identified. For comparison, a well-known transient upset mode (called mode 1, see, for example, references [6,7]) is also evaluated. The

error rate at the device level due to transient upset is timing and design dependent. The quantitative evaluation of this highly complex task is the subject of future work.

A. Mode 1 Single Event Transient

As shown in Figure 5, two inverters are in series. A heavy ion hits the first inverter and induces a transient pulse. If this pulse passes the second inverter and still has a peak over half V_{CC} (1.25V), which is approximately the threshold voltage of the inverter, it will propagate through the logic chain and has the possibility of causing an error in the storage unit. For the most sensitive node, the Q_{crit} to cause a propagating pulse is 0.02pC and the threshold LET is 2MeV-cm^2/mg.
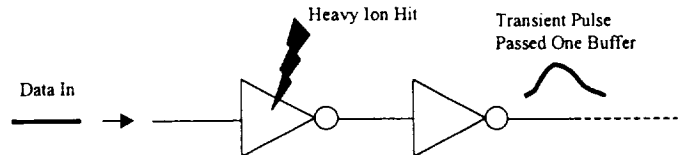

Figure 5. Mode 1 single event transient in combinational logic.

B. Mode 2 Single Event Transient

When the CSRAM is hit by an ion with deposited charge less than Q_{crit}, the state of the bit will be in a metastable state for a period of time and then recover to the original state. During the transient period, a signal passing through the pass transistor controlled by the CSRAM will be modified and soft data errors may occur. SPICE simulation results have shown that for a non-hardened CSRAM-switch, this may not be an issue, because the metastable period is very short (<1ns). However, the hardened CSRAM-switch will have long enough metastable period to generate a significant erroneous pulse. In the following scenarios, a hit pulse with 0.31pC and a resistor hardened CSRAM with 500kΩ resistors are used for demonstrating this issue.

Figure 6a shows one scenario. A CSRAM switch is gating the data path. A square wave signal is input from the left. Assuming the CSRAM switch is normally *on*, a heavy ion hitting on the CSRAM will leave the pass gate temporarily *off* for a short period of time, depending on the charge generated and collected. If the CSRAM transient is not near the signal transition edges, there is no effect. As shown in Figure 6b, the pulse will be narrowed down if the CSRAM transient falls on the front edge of the signal, and the pulse

widened if the CSRAM transient falls on the trailing edge. Narrowing may cause the disappearance of the signal and widening may cause racing issues.
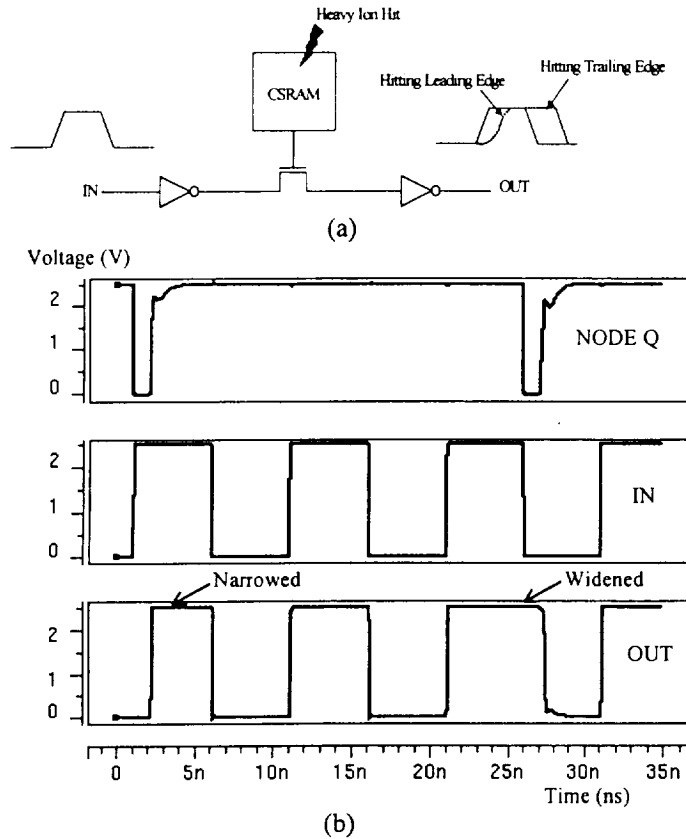

(a)

(b)

Figure 6   Mode 2 single event transient, metastability in CSRAM modifies the data signal.

Another scenario involves CSRAM controlling a multiplexer. Figure 7a shows the circuit schematic. Depending on the CSRAM state, either A or B will be selected. Assume A is *low* and B is *high*, and A is normally selected. An ion hit induced CSRAM transient will temporarily select B and generate a pulse.

Using the aforementioned hit pulse and resistor-hardened CSRAM, a pulse of more than 2V high and 2ns wide resulted (Figure 7b). It is strong enough to propagate through the circuitry and cause a soft data error.

VI. SEU MITIGATION

A. Memory Hardening

There are basically two strategies to harden a latch type of storage element. The objective of each strategy is to increase the threshold LET. Referring to equation 1, one way is to increase the Q_{crit} by circuit design techniques. The other is to reduce charge collection (d_{coll}) by technology changes such as SOI (silicon on insulator), or wafer fabricating process changes such as thin epitaxial silicon or double well.
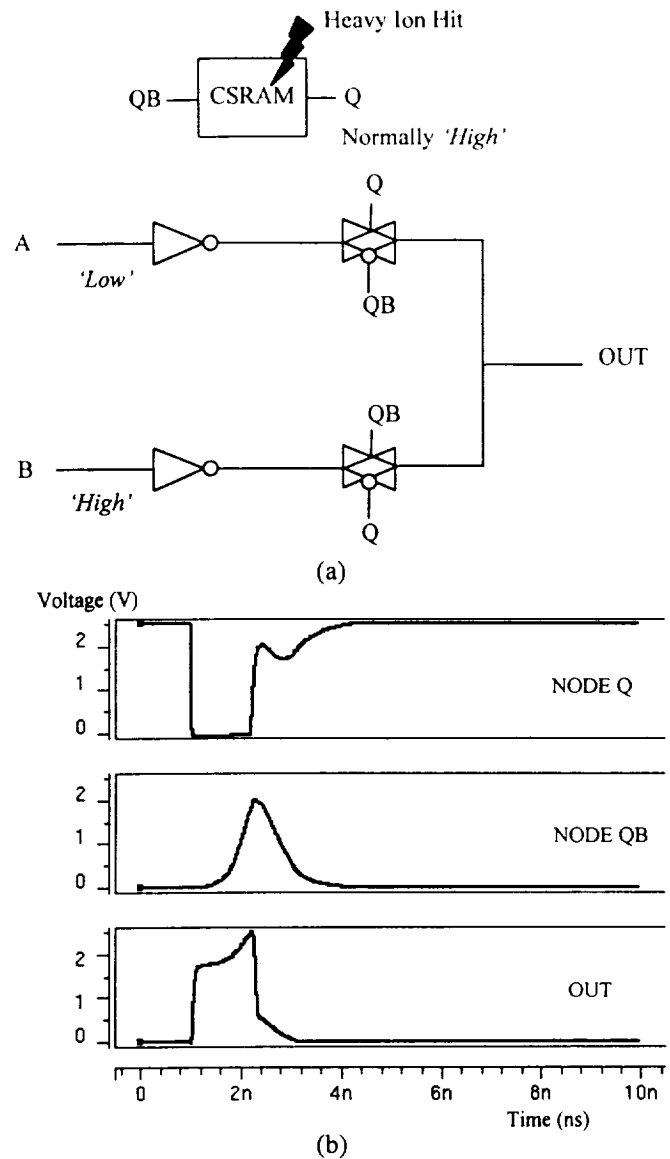

(a)

(b)

Figure 7. Mode 2 transient SEU, single event induced metastability in CSRAM controlled MUX.

Two circuit techniques are investigated. Figure 8 shows the schematic of the resistor-decoupling technique. The effectiveness depends on the resistor value. SPICE simulations were done and the correlation between LET_{th} and the resistor value is listed in Table 3.

Table 3. Upset rates for resistor hardened SRAMs.

Resistor (MΩ)	LET_{th} (MeV-cm²/mg)	GEO Error Rate (Upset/bit-day)
0	2.7	1.14×10^{-8}
0.5	30	5.05×10^{-11}
1	59	4.90×10^{-14}
1.5	87	7.10×10^{-15}

The other technique is to use redundancy for the circuit elements (see for example, reference [8,9]). However, the small geometry of a 0.25μm technology renders the

redundancy design prone to single strike double-bit upsets (SSDU) [10].

The DICE redundancy design in reference [9] is chosen as an example to illustrate the SSDU issue. Figure 9 shows the schematic of the DICE design. Each state in the memory is held by two nodes. For example, X1 and X3 are holding *high*, while X2 and X4 are holding *low*. If only one of the two nodes holding the same state (e. g. X1 and X3) has single event charge collection, the LET_{th} of this circuit is very high. The SPICE simulation results show that the 0.25μm version of the DICE SRAM is practically SEU-immune if only one node has been hit by the simulation heavy ion pulse mentioned in sub-section IV A.
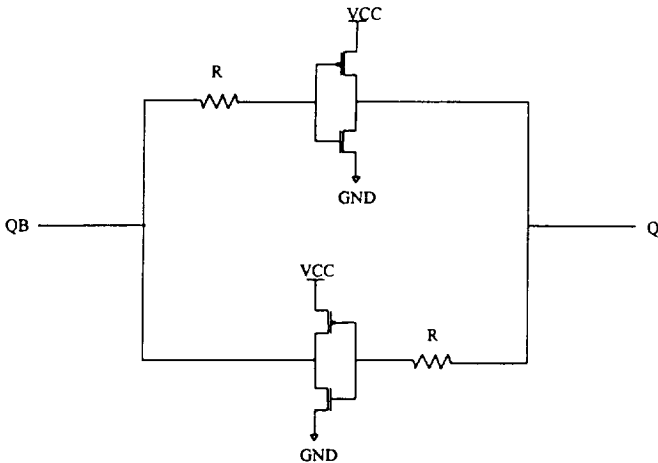

Figure 8. Resistor hardened SRAM.

The probability of two different ion hits on two nodes within the circuit response time is insignificantly small. However, an ion coming at a glancing angle may hit on the two nodes almost simultaneously and flip the memory.
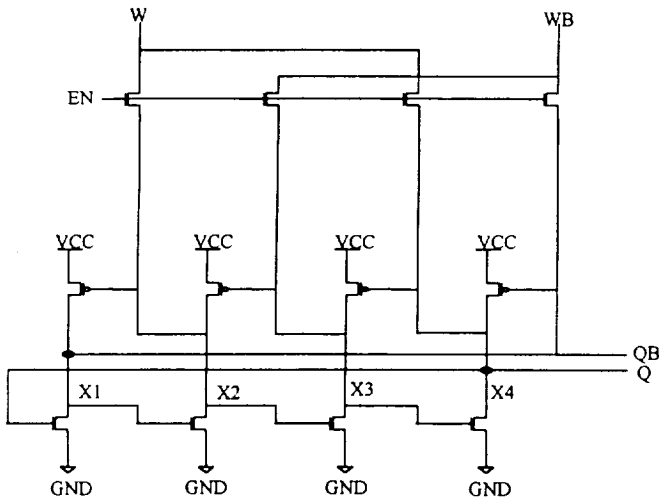

Figure 9. Schematic of the DICE SRAM.

Space Radiation 4.0 has a module based on Edmonds theory [10] to predict the SSDU rates. This module is basically applied to two independent memory bits. Two key input parameters are LET_{th} and the physical separation of the bits. However, the two nodes in DICE are not independent. SPICE has to be used to simulate the LET_{th} for SSDU in

DICE by injecting the same hit pulse at nodes X1 and X3 simultaneously. The resulting LET_{th} for SSDU in DICE is 2.7MeV-cm²/mg, the same as the original memory cell without implementing any hardening technique. The rate calculation was done for several different physical separations. Results are listed in Table 4. If a normally sized DICE cell is designed, the separation is close to 2μm.

Table 4. Upset rates of DICE SRAM for SSDU process.

Separation (μm)	GEO Error Rate (Upset/bit-day)
2	1.48×10^{-10}
10	5.69×10^{-12}

For comparison, the SSDU rate calculation is also performed for the resistor hardened SRAM. Again, SPICE is used to derive the LET_{th}. In this case the simultaneously active nodes are one P+/N-well junction and the other N+/P-substrate junction. The injection pulses for the P+ and N+ are of opposite polarity. Also, since the P+ is inside the N-well, compared to the N+, only about half the injected charge will be collected. Thus the injection pulse for the P+ is always half that of the N+. The LET_{th} of SSDU process is listed in Table 5. The rate calculation (results also listed in Table 5) is done by using a 2μm separation, which is a realistic layout dimension.

Table 5. SSDU process for resistor hardened SRAMs.

Resistor (MΩ)	LET_{th} (MeV-cm²/mg)	GEO Error Rate (Upset/bit-day)
0.5	18	8.60×10^{-12}
1.0	36	7.06×10^{-13}

Comparing the error rates in Table 5 and Table 3, it indicates that the SSDU process dominates the error rates when a hardening resistor value of 1MΩ is used.

The present analysis draws the conclusion that the SSDU process will limit both resistor and redundancy hardening. If the layout design doesn't pay special attention to this issue, the redundancy hardening is less effective than the resistor hardening by about two orders in upset rate. However, the major disadvantage of the resistor hardening is that the poly-resistor has a large negative temperature coefficient. The temperature coefficient is larger for larger resistance (lower poly doping). The memory cell employing resistor hardening will have a very large upset-rate variation through the specified operation temperature range. As the feature size shrinks to 0.18μm, the effectiveness of both resistor and redundancy hardening will be further compromised and more ingenious designs will be needed to mitigate SEU at the circuit level.

B. Device Level Mitigation by EDAC

Using EDAC to correct the corrupted CSRAM bits during operation will convert the device functional failure to a semi-soft error mode. It is highly desired for a moderately tolerant device. However, the method involves proprietary logic and circuit design information, which cannot be presented here.

VII. SINGLE EVENT LATCH-UP (SEL)

For space applications, SEL immunity ($LET_{th} > 100MeV$-cm^2/mg) is necessary. A non-programmed B4 device was powered on and tested for SEL by using heavy ions at BNL. The SEL sensitivity for a non-programmed device is not necessarily less than a programmed one, as long as the device is powered on. After powered on, in a non-programmed device, all the CSRAM-switches are turned off (closed), and every logic module is at a well-defined state. The active junctions are either at GND or V_{CC}, and many parasitic SCR (silicon controlled rectifiers) structures potentially susceptible to SEL are active. It was also confirmed at the layout level that many minimum-sized parasitic SCR structures were active for a powered, non-programmed device.

Figure 10 shows the standby (static) current of the power supply during heavy ion testing. The current increases monotonically with time. Finer resolution (not shown here) showed many small current jumps of approximately 1mA. The current increase is believed primarily due to driver contentions resulting from the upset of the CSRAMs, mentioned in section II C. SEL has the characteristic of a sudden current surge of a few hundreds of mA in previously measured FPGAs. Of course, once SEL occurred, the device had to be rebooted to regain functionality. None of these SEL characteristics were observed using ions with effective LET up to 74 MeV-cm^2/mg. This result is not surprising because latch-up prevention has been designed in the device.

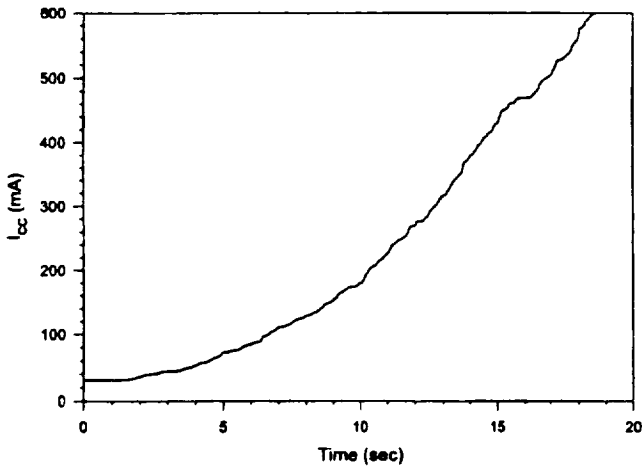Figure 10. I_{CC} of a non-programmed B4 part during Br ion (LET = 37MeV-cm^2/mg) bombardment.

VIII. TOTAL DOSE EFFECTS

Contrary to intuition, the deep sub-micron development in recent years actually alleviated the TID problem. As the feature size shrunk, the total dose tolerance improved. Very thin (<100 A°) gate oxide practically has negligible total dose effects. The test data of advanced CMOS technology based FPGAs indicated that the TID tolerance is limited by radiation-induced leakage current. To be more specific, the static I_{CC} test is usually the determining parameter for the TID tolerance. The leakage current may come from the parasitic-

NMOSFET leakage between source and drain (sometimes called edge leakage), or between two N+ junctions across the field (field leakage). The basic mechanisms causing these leakage currents are well-published (see, e. g., reference [11]). It is due to radiation-induced holes trapped at the Si/SiO_2 interface, thus inverting the P-well (or substrate) to form a leakage channel. The static I_{CC} usually has a threshold total dose. This threshold characteristic corresponds to the channel inversion threshold voltage of the parasitic NMOSFET.

As the technology advances, the feature size shrinks. The smaller feature requires thinner field oxide (FOX), higher P-well doping and lower V_{CC}. Thinner field oxide reduces the hole generation and trapping. Higher P-well doping (to alleviate the punch-through) increases the threshold voltage of the parasitic NMOSFET. Lower V_{CC} for smaller geometry also reduces the hole trapping in the field oxide.

Table 6. TID tolerance for different technologies

Technology	Isolation	FOX Thickness	TID Tolerance
0.6μ/5V	LOCOS	7000A	5krad(Si)
0.35μ/3.3V	LOCOS	3500A	35krad(Si)
0.25μ/2.5V	STI	3000A	50krad(Si)

Table 6 lists the key TID processing parameters of typical commercial foundries. TID tolerance is defined as the total dose when static I_{CC} reaches 20mA, the specified limit for the device. It is rationalized that the significant improvement from 0.6μm/5V to 0.35μm/3.3V is due to thinner FOX, higher P-well doping and reduced V_{CC}. Shallow trench isolation didn't severely impact the total dose tolerance of 0.25μm/2.5V. The better performance compared to 0.35μm/3.3V is probably because of the increased P-well doping and lower V_{CC}.
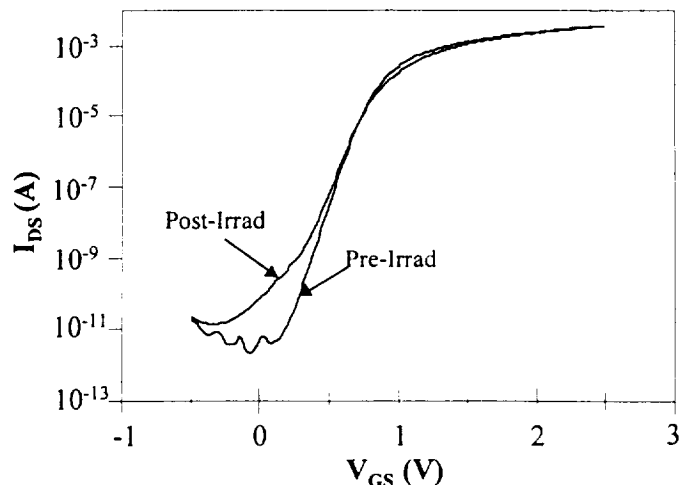

Figure 11. I_{DS}-V_{GS} of a 0.25μm NMOSFET pre- and post-100krad(Si) irradiation

Figure 11 shows the I_{DD}-V_{GS} curves of a 0.25μm N-channel transistor before and after 100krad(Si) irradiation. The radiation source is the ARACOR 4100. I_{off} (I_{DS} defined at $V_{GS} = 0$) increased only to 0.1nA after irradiation.

A simplified TID test was performed on a non-programmed B4 device. Only static I_{CC} was measured during irradiation by using a gamma cell. By the similar argument as stated in section VII, the non-programmed part had all the active junctions in well-defined states, thus many relevant parasitic NMOSFETs were active, and the results of radiation induced static I_{CC} change should be very close to a programmed device. Figure 12 shows the static I_{CC} versus the accumulated total dose. Using a static I_{CC} spec of 20mA, the tolerance is approximately 50krad(Si).
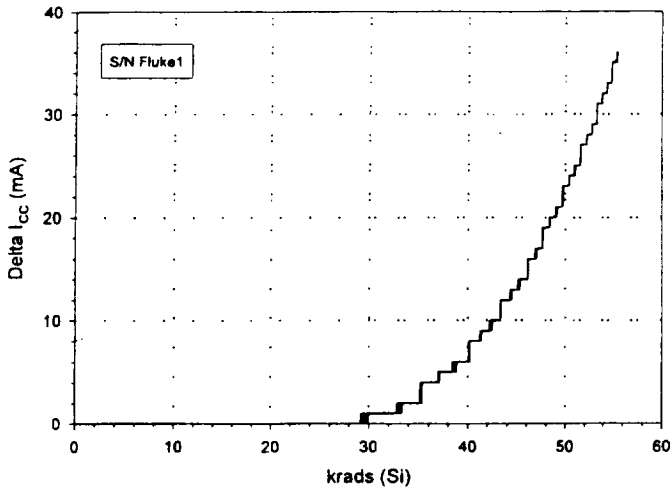

Figure 12. Static I_{CC} versus total dose of a 0.25μm B4 device.

IX. CONCLUSIONS

For single event effects, the 0.25μm SRAM based re-programmable FPGA presented in this paper needs to be hardened for space applications. The critical issue is the SEU hardening of the configuration SRAM (CSRAM) to avoid functional failure (or interrupt). CSRAM hardening is particularly difficult because of the constraint of its large population and small size. The traditional methods including resistor and redundancy hardening have their limitations, and the penalties paid for hardening are higher for smaller feature size. At high LET ranges, the hardened CSRAMs will induce single event transient glitches, and may increase the soft error rate of the device. SEL appeared to be not a big issue for this particular device. The data show that it at least has relatively good SEL tolerance ($LET_{th} > 74MeV\text{-}cm^2/mg$).

The TID issue is alleviated when feature size shrinks in the sub-micron regime. Several process parameters changed for scaling, such as thinner field oxide, higher well/substrate doping, and lower V_{CC} helped to reduce the TID induced leakage current, and consequently improved the TID tolerance. The present device has TID tolerance of approximately 50 to 100krad(Si).

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