b 4/16/96

## Summary of Proton Test on the Quick Logic

## QL3025 at Indiana University

June, 1998

Prepared by: R. Katz,
NASA/GSFC

Date: June 16, 1998

### Test Facility

A pAsic3 QL3025 was tested at the Indiana University Cyclotron Facility (IUCF). The proton energy was ~ 193 MeV and the flux was set at approximately 1 x $10^9$ p/cm$^2$/sec. The total fluence for the run was 5.12 x $10^{11}$ p/cm$^2$ corresponding to a total dose of 32.1 kRads (Si). The device was irradiated normal to the beam.

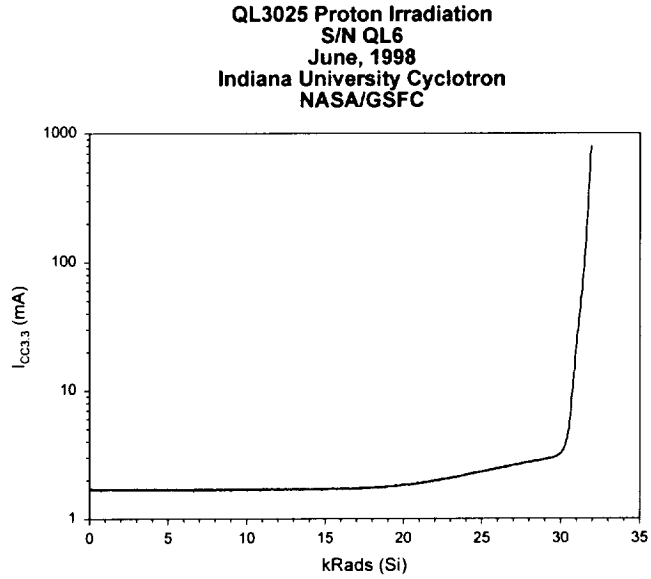
### Device Under Test

The device was in a PQFP208 package and was active during irradiation. Upsets and currents were monitored in real-time with the device active at 1 MHz. The stimulation pattern was a 500 kHz square wave. Both internal hard-wired flip-flops and I/O module flip-flops were tested. This pattern contains 500 internal flip-flops with 300 in a TMR configuration and 200 in a shift register. 50 I/O module flip-flops were tested.

### Test Results

No upsets were detected for this one sample, consistent with our quick-look heavy ion data, taken at an LET of 18.8 MeV-cm$^2$/mg. The total fluence for the heavy ion data was limited and complicated by the device's latchup characteristics. No evidence of latchup or any unusual current disturbances were observed.

The device showed a moderate increase in current at approximately 20 kRads (Si) and a current runaway at approximately 31 kRads (Si). This is thought to be a consequence of a charge pump failure. The total dose data, shown in the chart below, is comparable to our Cobalt-60 data where the device exhibited runaway at approximately 37 kRads (Si), while dosed at the relatively low rate of 0.5 kRads (Si)/hour in a static configuration. Dose rate during the proton irradiation was at the much higher rate of ~ 247 kRads (Si)/hour.




---

### Functional Failure of EEPROMs in the Heavy Ion Environment

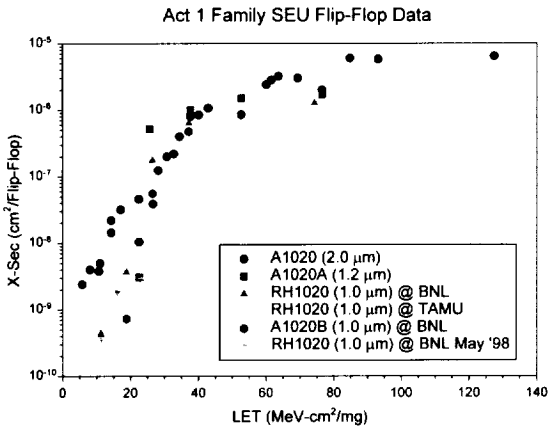
It has been demonstrated that devices, including EEPROMs, may lose functionality when upset by a single heavy ion. The Atmel AT28C010 is one example. Additionally, excess current was observed in the device. No permanent damage was detected. For the AT28C010, three types of SEUs were identified. one type was an upset in the output register, causing a read operation to fail. Additionally, there were two types of upsets where the device lost functionality over multiple cycles and entering a non-operating state.

This phenomena was covered in a good overview in "Single Event Functional Interrupt (SEFI) in Microcircuits," published in RADECS 97, Proceedings of the Fourth European Conference on Radiation and its Effects on Components and Systems. The authors are R. Koga, S. Penzin (Crain), K. Crawford, and W. Crain from the Aerospace Corporation.

Recently, a similar effect was demonstrated and analyzed in FPGAs utilizing IEEE 1149.1 JTAG circuitry, in an implementation without the optional TRST- pin. An application note on use of JTAG is in preparation and will be published shortly.

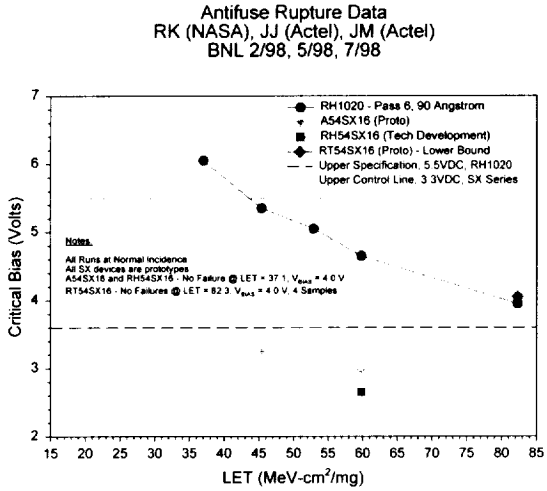
## Act 1 SEU Summary

The Act 1 architecture has been fabricated in a number of technologies, many of which are utilized in space flight hardware. These consist primarily of the MEC foundry 2.0, 1.2, and 1.0 µm devices as well as the RH1020 built at Lockheed-Martin. The following chart summarizes the SEU performance of these devices. Some other variants are being flown, such as the TI A1020B, but this is relatively infrequent and the data is not included here.




## Antifuse Hardness

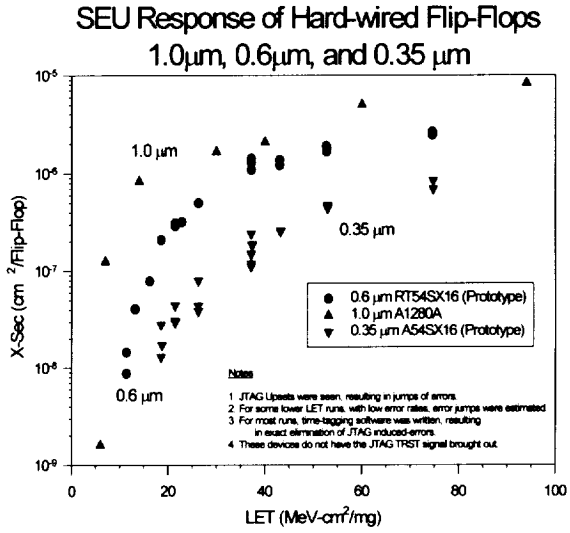
The following chart gives an update on antifuse hardness testing. Shown here is data on the RH1020 devices as well as prototypes from the SX series of FPGAs. Please note that these are prototypes used for technology assessment and development. Characteristics of production devices will differ and the user should be sure to obtain up-to-date data.




None of the antifuse 'recipes' showed any problems at an LET of 37 MeV-cm$^2$/mg with the ions normal to the device, which is worst-case for this effect. Note that the usual cosine law for SEU and SEL do not apply here. Of particular note is antifuse recipe 'M', which was hard (four sample devices) at an LET of 82.3 MeV-cm$^2$/mg with $V_{DD}$ = 4.0 VDC; maximum rated voltage for this class of device is 3.6 VDC.

## SEU Comparison of 1.0, 0.6, and 0.35 µm *Hard-wired* Flip-Flops

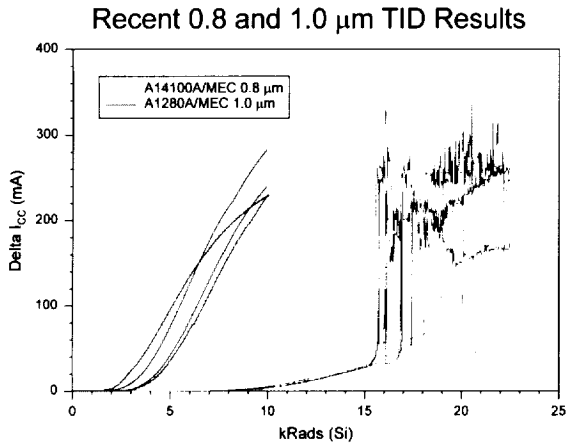
The following chart shows the SEU response of *hard-wired* flip-flops from an A1280A (5V/1.0 µm) and prototype RT54SX16 (3.3V/0.6 µm) and A54SX16 (3.3V/0.35 µm) devices. The hard-wired flip-flops are dedicated on the chip and are not formed by feedback connections in the routing channels. These are called 'S-Module flip-flops' in the A1280A and 'R-Cell' in the SX architecture.




As can be seen, the smaller feature-sized parts, operating with the lower bias voltage, had improved single event upset (SEU) performance over its older, higher voltage predecessors. As can be seen from the proton data, and limited heavy ion data, the QL3025 3.3V/0.35 µm device also performed well. Modern FPGAs will continue to scale and we expect to have test 0.25 µm feature size in the near future.

### Recent Act 2 and Act 3 Total Dose Results

Below is a chart showing total ionizing dose (TID) test results for flight lots of A1280A/MEC (left) and A14100A/MEC (right). Static $I_{CC}$ is plotted against accumulated dose.




As can be seen, these lots of devices are performing worse that 'typical' lots of these device types. While our database is not large enough to declare a trend, the decrease in TID performance is being watched, closely. A second batch of A14100A's are being qualified to 11 ± 10% kRads (Si) and are currently in high-temperature annealing.

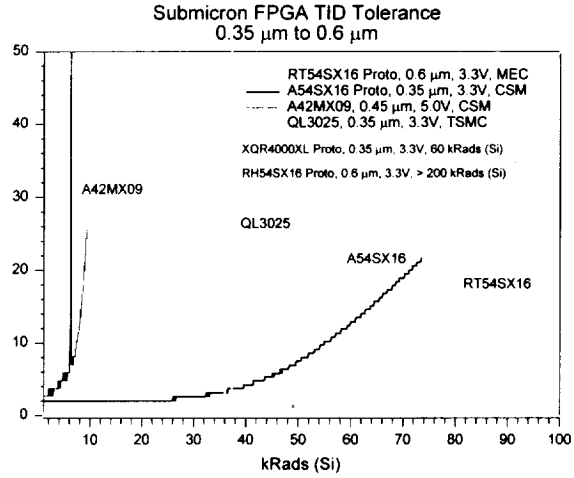
Additional data sets will be obtained in the near term, with lots of A1425A/MEC, A1460A/MEC, and A1280A/MEC being queued for test.

---

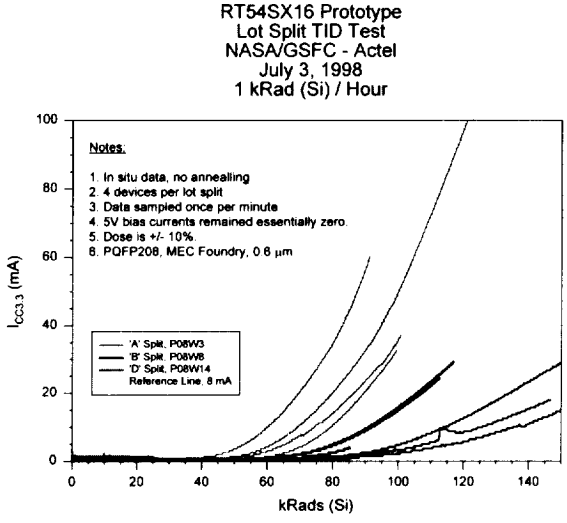
### Recent Sub-micron Total Dose Results

The graph below summarizes the performance of sub-micron devices recently testing. Data on the prototype XQR4062XL, using a modified process, was supplied by Xilinx Corporation. Note that heavy ion test data for this prototype devices showed no latchup at an LET = 100 MeV-cm$^2$/mg, at a temperature of 100°C.

The 5.0VDC/0.45 µm A42MX09 sample did poorly, with less than 10 kRads (Si) performance. All of the 3.3V/submicron devices did well, showing radiation-tolerant performance. All devices, except for the XQR4062XL, used unmodified processes. The RH54SX16 prototype, previously published, showed no degradation to 200 kRads (Si), with the results limited by available test time.




The following chart shows the results from modifications made to prototype RT54SX16's, with the results for three lot splits shown. The reference line is arbitrary and is used as a very conservative estimate of performance and a means for making comparisons between the lot splits. Even without annealing, performance levels exceeding 100 kRads (Si) were achieved on a commercial fabrication line.




### Miscellaneous

A number of items of interest are on the www site. This includes data, such as heavy ion and total dose tests on Chip Express devices, presentations from the SEE Symposium (April, 1998 in LA), and more research papers on topics such as antifuse reliability and efficiently supporting fault-tolerance in FPGAs. TID papers on EEPROMs are also being posted.