**Electrical Impact of SiC Structural Crystal Defects on High Electric Field Devices (Invited)**

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As illustrated by the invited paper of M. Dudley at this conference and other works, SiC wafers and epilayers contain a variety of crystallographic imperfections, including micropipes, closed-core screw dislocations, grain boundaries, basal plane dislocations, heteropolytypic inclusions, and surfaces that are often damaged and contain atomically rough features like step bunching and growth pits or hillocks. Present understanding of the operational impact of various crystal imperfections on SiC electrical devices is reviewed, with an emphasis placed on high-field SiC power devices and circuits.

The degree to which of each kind of crystal defect impacts a given device is quite application-specific, strongly dependent on a combination of both the electrical operating requirements and the physical layout of each particular SiC device structure. Because almost all useful semiconductor integrated circuit (IC) electronics require rectifying junctions to function properly, the primary failure mode discussed here is loss of junction rectifying characteristics. SiC electronics designed to operate all junctions within the device at low electric fields are least affected by crystal defects. SiC pn junction diodes, field-effect transistors (FET's) and integrated circuits have all demonstrated an ability to function despite the presence of micropipes running through key rectifying junctions as long as applied voltages are kept to a small percentage of the SiC critical breakdown field and device metalizations do not deposit into the micropipe core so as to physically short-circuit the junction.

As pointed out by Fazi et. al. [1], crystal defects are clearly much more harmful to devices that operate junctions at high electric fields (i.e., power devices), especially when the crystal defects perpendicularly cross the high-field metallurgical junction boundaries as is the case with micropipes and closed-core screw dislocations on commercially available c-axis oriented SiC wafers and epilayers. Until recently micropipes were recognized as the most detrimental junction failure defect that has severely hindered the development and utilization of SiC-based electronics simultaneously rated for high off-state blocking voltage with high on-state current ratings. Steady reductions in SiC micropipe densities from several 100's per $cm^2$ in 1993 to less than 1 per $cm^2$ have now enabled initial prototype demonstrations of high current SiC diodes in the neighborhood of 100 A. It is important to note, however, that most high-current SiC power devices reported to date have been significantly voltage derated, in that the experimentally demonstrated blocking voltages in these devices are usually significantly less than the theoretical blocking voltages calculated from blocking voltage layer doping and thickness. Similarly, the highest reported blocking voltage SiC devices (> 5 kV) have been very small-area (< $10^4$ $cm^2$) with low on-state current rating well under 1 A. If micropipes are the only defect limiting SiC high power devices, much better experimental results combining optimum high voltage and high current in a single large-area device should be obtainable.

While SiC devices promise some of the largest operational benefits to electric power conversion and motor-drive systems, the inductive components of such systems also impose the harshest operational stresses on semiconductor switches. Solid-state devices in these circuits are often subject to demanding overvoltage and/or overcurrent stresses not found in other applications, which they must withstand without damage or degradation in order for the system

to function reliably. Thus, it is possible that non-micropipe crystal defects, which appear relatively harmless when subjected to conventional characterization methods and used in less-demanding applications, could cause device failure when operated in demanding high-power circuits, as historically is the case with silicon-based power devices whose design specifications today are still primarily governed by safe operating area (SOA) reliability considerations. In silicon power electronics experience, undesired lateral nonuniformities in electrical material properties across the high field area of a power device, (e.g., nonuniformities caused by crystal dislocation defects and impurity clusters) have historically often led to reliability problems (i.e., reduced SOA) in demanding high-power systems, with higher voltage devices being most susceptible failure.

Because present-day commercial SiC wafers and epilayers contain plenty of non-micropipe crystal defects in densities as high as thousands per square cm, virtually all multi-amp SiC power devices manufactured in the near term seem guaranteed to contain electrical nonuniformities that could potentially impact SiC high-power device operation. It is therefore critical to understand the impact of these various non-micropipe defects on the SOA of various SiC power device structures, as understanding of device SOA is necessary for high-power circuit design. Significant changes in high-power circuit topologies and device derating practices may be required if these defects are found to greatly reduce the SOA of SiC-based power devices.

SiC has strong material property advantages that should make it inherently more durable to electrothermal stresses that govern SOA than silicon, such as higher thermal conductivity, higher melting temperature, lower impurity diffusion, etc. It is therefore quite possible that SiC-based high power devices may be able to much-better tolerate the presence of localized currents and crystal defects than silicon power devices. Previous works indicate this is the case for properly fabricated SiC pn junction diodes with voltage ratings of less than 400 V. Closed-core screw dislocations were recently shown to cause undesirable degraded reverse I-V and highly localized breakdown microplasmas in such diodes. Yet when subjected to reverse-breakdown avalanche energy testing, no significant difference was noted between devices with and without closed-core screw dislocations, apparently due to the fact that space-charge effects restrict the breakdown power density and temperatures at the dislocation-related microplasmas.

Unfortunately however, other SiC power device structures, particularly Schottky diodes, exhibit catastrophic localized breakdown and/or degraded operating properties that seem attributable to non-micropipe defects in SiC crystals. Many undesirable localized nonuniformities in electrical properties of SiC Schottky diodes observed by Electron Beam Induced Current (EBIC) have recently been conclusively correlated with closed-core screw dislocations, all of which formed morphological growth pit defects on the as-grown epilayer surface (see Schnabel et. al., this conference). However, a significant percentage of EBIC-observed nonuniformities could not be attributed to screw dislocations or surface morphological features such as growth pits unassociated with screw dislocations. The root electrical properties of closed-core screw remain under investigation at this time, with localized changes in band structure due to high crystal stress as well as enhanced impurity incorporation among the possible mechanisms being considered. Clearly, more work to better understand the electrophysical properties of closed-core screw dislocations and other SiC non-micropipe defects that will be present in high-power devices for the forseeable future is needed.

[1] C. Fazi, M. Dudley, S. Wang, and M. Ghezzo, IOP Conf. Ser. 137, p. 487-490 (1994).