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THIN FILM $Ba_xSr_{1-x}TiO_3$ Ku- and K-BAND PHASE SHIFTERS GROWN ON MgO SUBSTRATES

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We report measurements of gold circuits fabricated on four $Ba_xSr_{1-x}TiO_3$ films doped with 1% Mn grown on MgO substrates by laser ablation. Low frequency measurements of ε_r and $\tan\delta$ on interdigital capacitors are compared with high frequency measurements of phase shift and insertion loss on coupled microstrip phase shifters done on the same films. The variation in temperature of both high and low frequency device parameters is compared. Annealed and unannealed films are compared. Room temperature figures of merit of phase shift per insertion loss of up to 58.4°/dB at 18 GHz and 400 V dc bias were measured.

Keywords: $Ba_xSr_{1-x}TiO_3$; phase shifters; tunable microwave devices

INTRODUCTION

Major efforts are underway to develop new tunable microwave devices at frequencies above about 10 GHz where Si becomes too lossy. Inexpensive, compact low-loss devices are desired for a variety of communications and military applications. Recent improvements in the deposition of thin film ferroelectrics have made these materials a candidate for these roles. At ambient temperatures, the greatest attention has been given to the ferroelectric, $Ba_xSr_{1-x}TiO_3$ (BSTO). In BSTO, changing x from 0 to 1 causes the maximum of the dielectric constant to shift from 20 K to 395 K. Tunable ferroelectric devices are generally used above the Curie temperature (T_c) in the paraelectric regime, where a large dielectric constant is tuned with an applied dc electric field. BSTO films suffer from a high loss tangent, which can be lowered by introducing dopants[1,2]. Another avenue for improving films consists of annealing to remove lattice imperfections and increase tunability[3]. This paper examines four BSTO films as a function of temperature. The films were patterned with interdigital capacitors for low frequency measurements and coupled microstrip phase shifters (CMPS) for high frequency measurements.

DESIGN AND EXPERIMENTAL DETAILS

The Naval Research Laboratory deposited these BSTO ferroelectric films using on-axis laser ablation at a temperature of 750 C and a dynamic oxygen pressure of 100 mtorr. The BSTO was deposited to a thickness of 500 nm on substrates of 508 μm thick (100) single crystal MgO. All four films were doped with 1% Manganese. Two films had Ba:Sr ratios of 50:50 and the other two had 60:40. One films of each composition was bomb annealed at 1100° C for 6 hours[1]. The 60:40 composition samples have a higher T_c, which usually leads to higher tuning and loss at room temperature.

After BSTO deposition, the films were metallized using electron-beam evaporation at NASA Glenn Research Center with a 15 nm chrome (Cr) adhesion layer followed by a 2 μm thick Au film. Standard lift-off chemical etching techniques were used to fabricate Au/Cr/BSTO/MgO interdigital capacitors. two different circuits were patterned on these BSTO films. After measurements were complete, the Au was etched off with 1:1 KI:H_2O solution and the Cr seed layer was removed with perchloric acid. A second circuit consisting of a Au/Cr/BSTO/MgO four-element CMPS was patterned on the BSTO films in the same manner. Finally, a Cr/Au ground plane with the same metallic thicknesses was e-beam evaporated on the back of the substrate for the phase shifters.

The interdigital capacitors were measured at 1 MHz using a HP4192A LF Impedance Analyzer. The interdigital capacitor consisted of 100 identical fingers with a finger width of 25 μm and a gap between fingers of 15 μm. The finger length was 0.6909 cm long. The capacitance and tanδ measurements were made in a closed cycle He refrigerator at temperatures from 30 K to 330 K and excitation voltages of 50 mV or 100 mV.

The performance of the CMPS circuits at microwave frequencies was evaluated by measuring the transmission (S_{21}) and reflection (S_{11}) scattering parameters between 10 and 20 GHz using an HP 8510 C network analyzer. All loss measurements quoted here include the losses due to the SMA launchers which are estimated to be 0.25 dB. Two phase shifters were measured at temperatures down to 100 K in a closed cycle He refrigerator. The measurements were done in vacuum to protect from dielectric breakdown of the air in the large dc electric fields between coupled microstrip sections. However, tests of CMPS circuits in air have been done after coating the films in thin film bonding wax. No breakdown occurred and the wax had a negligible effect on device performance.

The phase shifter design consists of n-coupled microstrip sections in series. Each section functions as a single pole broadband filter whose passband shifts with dc bias applied to the ferroelectric. The phase shift is proportional to n. The circuits used in this study were four- coupled section phase shifters. A schematic of a single coupled microstrip section is given in Fig. 1. A photograph of the entire circuit is shown in Fig. 1. The dimensions of the coupled length, l = 457 μm, the gap between coupled section, s = 10 μm, and the coupled section width, w = 56 μm. The total circuit length is 1 cm. In Fig. 2, the dc bias is applied at the top two radial stubs while the bottom three stubs which include the input and output microstrips are held at ground. These phase shifters are fairly narrowband, about 12% bandwidth, and the optimal frequency of operation, f_{opt}, depends upon the ε_r and thickness of the ferroelectric film. A detailed discussion of the device properties has been given elsewhere[4].

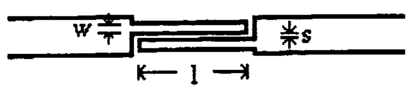


Figure 1. Schematic of a single coupled microstrip section for this design on 508 μm thick MgO, s = 10 μm, l = 457 μm, and w= 56 μm. The total length is 1 cm.

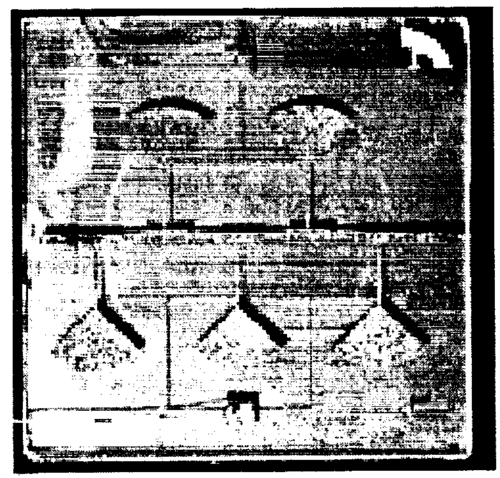


Fig. 2. A four element coupled microstrip phase shifter on a 508 μm thick MgO substrate.

The device was first successfully demonstrated using $YBa_2Cu_3O_{7-\delta}$ atop a 1 μm $SrTiO_3$ ferroelectric film on a 254 μm thick $LaAlO_3$ (LAO) substrate[4]. At 40 K and 16 GHz, those 1 cm long cryogenic devices demonstrated 484° of phase shift using 375 V dc bias with a figure of merit (K) of 80°/dB phase shift per maximum insertion loss. Transferring this exact LAO design to a room temperature Au/0.3 μm BSTO/ $LaAlO_3$ structure quickly achieved 200° phase shift and 43°/dB figure of merit (K) at 14 GHz and using 400 V dc bias[5].

RESULTS

The 1 MHz interdigital capacitor results are shown in Fig. 3 and Fig. 4. The dielectric constant of the film was then derived from the measured capacitance by using the conformal mapping and partial capacitance formulas of Gevorgian *et* *al.*[6] The relationship between C and ε_r for this 100 finger electrode configuration is,

$$C\,(\mathrm{pF}) = 28.969 + 0.19780\varepsilon_r \tag{1}$$

The error in the capacitance measurement and the uncertainties in the dimensions are about 5%. **Judging from test circuits on $LaAlO_3$ and MgO, the errors in the partial capacitance analysis of $C(\varepsilon_r)$ are probably less than 20%.** The tanδ measurements shown in Fig. 4 are more sensitive to stray capacitance and calibration errors, including those induced by changing temperature. These measurements have uncertainties of approximately ±0.003 except for Sample 1 which seems to suffer from an admixture of the capacitance.

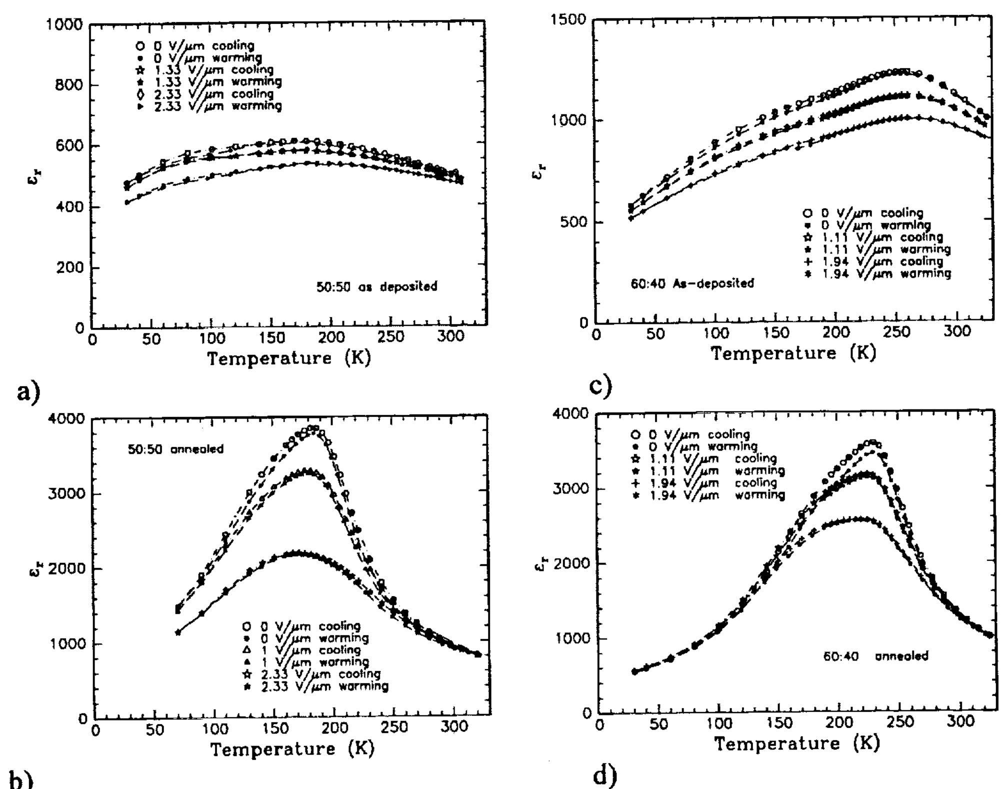


Figure 3. The dielectric constant as a function of temperature for all four samples as derived from the capacitance of an interdigital electrode at 1 MHz. a) Sample 1: BSTO 50:50 as deposited. b) Sample 2: BSTO 50:50 annealed. c) Sample 3: BSTO 60:40 as deposited. d) Sample 4: BSTO 60:40 annealed.

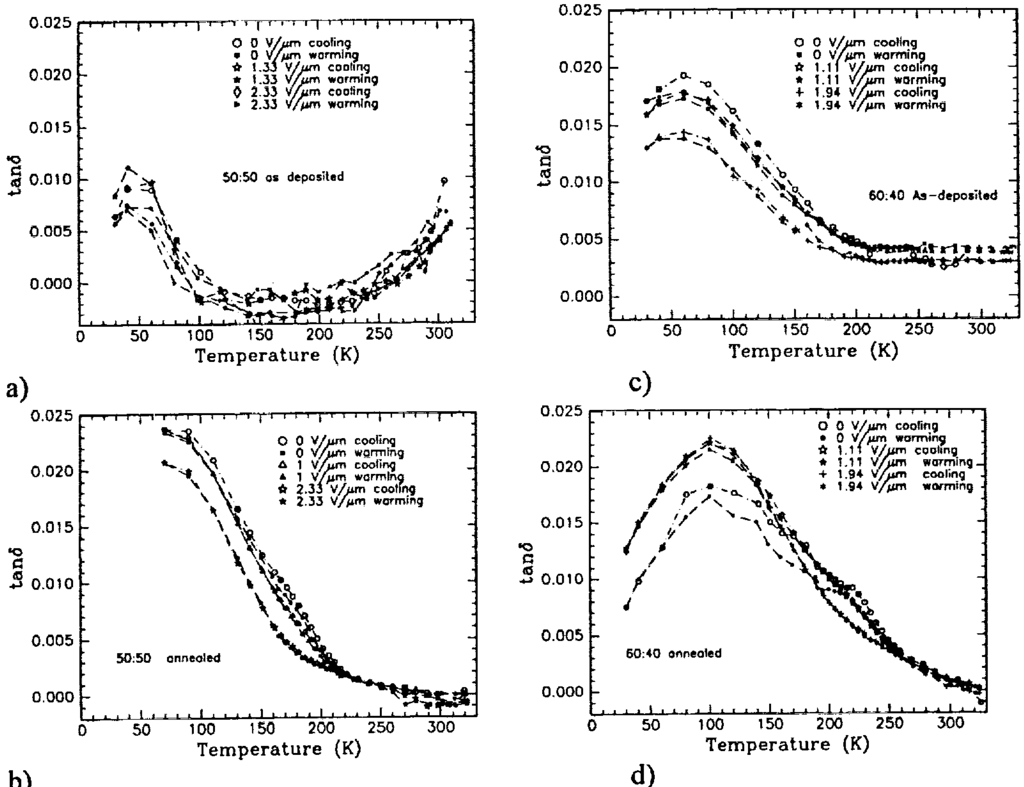
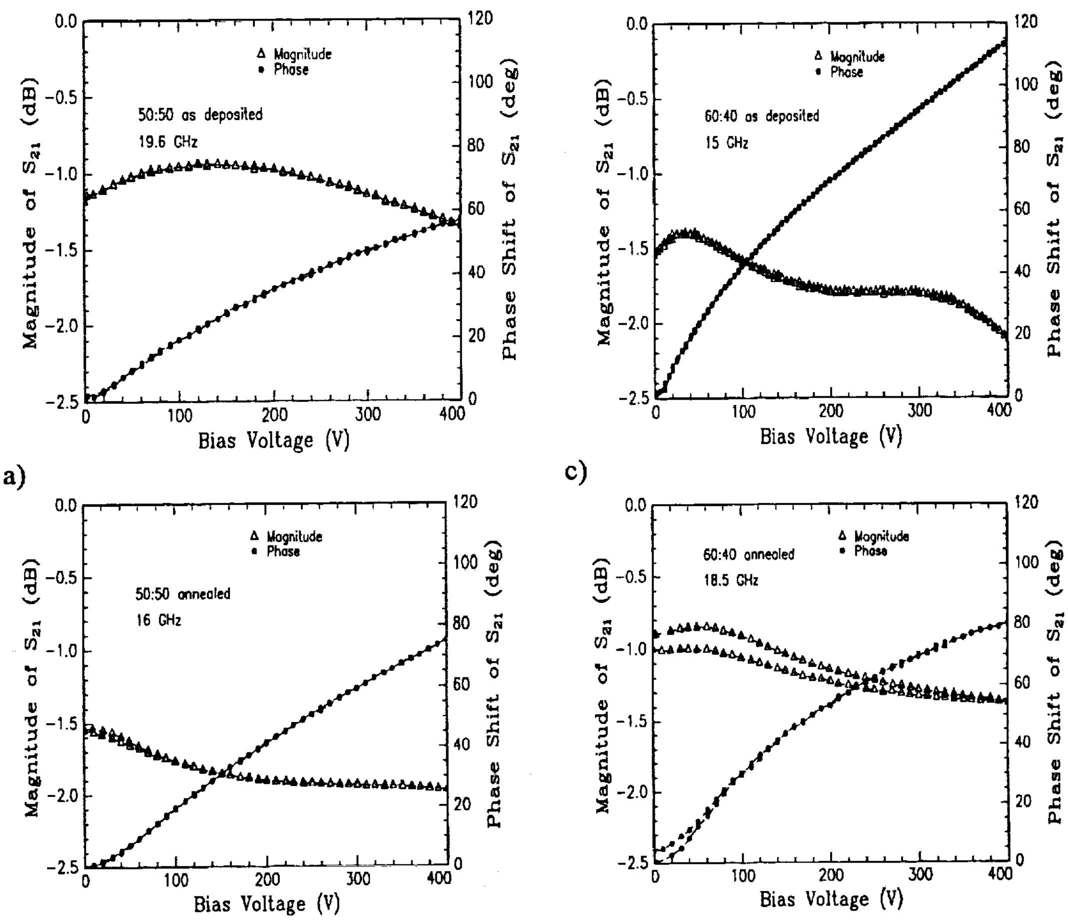


Figure 4. The loss tangent as a function of temperature for all four samples, measured using an interdigital electrode at 1 MHz. a) Sample 1: BSTO 50:50 as deposited. b) Sample 2: BSTO 50:50 annealed. c) Sample 3: BSTO 60:40 as deposited. d) Sample 4: BSTO 60:40 annealed.

There are several observations that can be made from these low frequency data. While the films certainly have varying dielectric properties before annealing, it appears that annealing increases the maximum dielectric constant of these films by more than a factor of 2. The tanδ is also increased, although only by 20% in the case of the 60:40 samples. The dielectric constant is quite high with a maximum in Sample 2 of 3850. Even higher than one would expect from an undoped BSTO sample. This result echoes that of Wu and Barnes[2] who found that bulk BSTO with 1% Mn doping had the largest value of ε_r amongst samples with 0, 0.5, 1.0, 2.5 and 5% doping. Another feature to note is that the temperature of maximum dielectric constant for the annealed samples of 50:50

(60:40) BSTO compositions, 183 K (230 K), is well below that of bulk T_c = 250 K (284 K).[7]

Figure 5 shows the results of insertion loss and phase shift measurements on the four-element coupled microstrip phase shifter circuits patterned on these same films. The results shown here are given at f_{opt}, the frequency of maximum tuning to insertion loss ratio, K, for each of these films. The tabulated maximum



b) d)

Figure 5. The phase shift and insertion loss through coupled microstrip phase shifters on each of the four samples at 298 K. Data is shown at f_{opt} for each sample. a) Sample 1 b) Sample 2 c) Sample 3 d) Sample 4.

phase shift and insertion loss for a 400 V dc biasing range are given in Table I. This frequency, f_{opt}, varies between these films because ε_r (E) differs for each film. The value of ε_r (0) in Ku-band frequency range determines the passband of the unbiased circuit. As the bias is increased and ε_r (E) drops, the device passband shifts to a higher frequency. Thus, ε_r (0) and ε_r (E_{max}) determine f_{opt}. The values of f_{opt} show some correlation with the measured $\varepsilon_r(0)$ at 1 MHz, with samples 1-3 following this trend of lower ε_r leading to higher f_{opt}. The fifth column lists f_{opt}, and the last column gives the maximum value of K. The tuning and loss at 16 GHz are also given so that one may compare films at the same frequency.

Table I. Four element CMPS measurements on 508 μm MgO substrates at room temperature. All values are given for tuning over a 400 V dc bias range.

	Ba:Sr ratio	Anneal at 1100 C for 6 hrs.	ε_r (0) at 1 MHz and 300 K	f_{opt} GHz	Tuning at f_{opt} w/ 400 V dc	Max. Loss (dB) at f_{opt} over 400 V range	Tuning at 16 GHz w/ 400 V dc	Max. loss (dB) at 16 GHz	Max K °/dB w/ 400 V dc
1	50:50	none	506	19.6	57°	-1.4	93°	-4.9	40.7
2	50:50	yes	946	16	75°	-1.95	75°	-1.95	38.5
3	60:40	none	1116	15	114°	-2.1	97°	-2.75	54.3
4	60:40	yes	1320	18	80°	-1.37	97°	-1.8	58.4

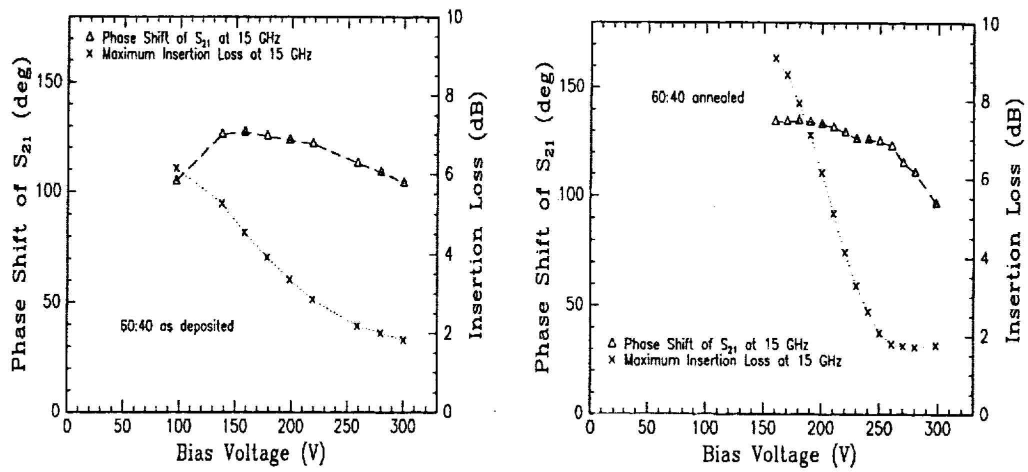
These two circuits are not ideal for comparisons between high and low frequency for several reasons. First, the electric fields in the capacitor measurements are limited to 2.33 V/μm by the 35 V dc maximum of the HP4291A. The CMPS devices act as dc blocks and are biased to 40 V/μm. Further tuning with higher voltages is possible and usually leads to higher values of K. None of these films broke down at field strengths of 40 V/μm. Second, the CMPS circuits are complicated and difficult to model causing considerable uncertainty in backed out values of ε_r and tanδ. However, the maximum phase shift of 114° seen in sample 3 roughly agrees with a change in ε_r of 700 (e.g. from 1000 to 300) while the phase shift in Sample 1 at 16 GHz can be modeled by shifting ε_r from 500 to 150. These values are illustrated in Table III which lists IE3D[8] em simulator modeled phase shifts assuming an unbiased $\varepsilon_r(0)$ of 1200. Note that phase shift of S_{21}, $\Delta\varphi(\varepsilon_r)$ is non-linear, this structure is a more efficient phase shifter at lower ε_r.

Table II. IE3D modeled phase shift through this four element CMPS circuit at 16 GHz assuming $\varepsilon_r(0) = 1200$ for the BSTO film at 16 GHz. Modeling assumes that the entire BSTO layer changes ε_r as a function of bias.

εr	1200	1000	800	600	500	400	300	200	150	100
Phase Shift	0°	17.2°	40.1°	70.7°	88.8°	110.5°	134.5°	163.2°	179.8°	196.8°

Furthermore, note that the CMPS losses listed in Table I are not solely due to the BSTO film. Mismatch losses vary from 0.15 dB to 0.45 dB for these devices. Conductor loss is estimated to be about 0.5 dB. The dielectric loss in the MgO should account for 0.1 to 0.2 dB of insertion loss. Radiation loss is presumed to be small with the BSTO film present. The remaining loss is due to the BSTO film. For Sample 4 with the lowest loss listed at f_{opt}, -1.37 dB, the BSTO film would then account for about 0.62 dB or 45%. For Sample 3, the most tunable film at f_{opt}, with losses of –2.1 dB, the ferroelectric could account for about 64% of the loss.

Figure 6 shows the temperature dependence of the CMPS phase shift and insertion loss as a function of temperature at 15 GHz and while applying 350 V dc for the two 60:40 samples. The as-deposited sample shows tuning increases with tuning that are roughly analogous to the changes in $\varepsilon_r(0)$ at 1 MHz. Both graphs indicate about 10% increases while cooling from 300 K to 250 K. The 15 GHz phase shift graph does peak at a lower temperature, however. The tuning in the annealed sample does not show the large increases of $\varepsilon_r(0)$ at 1 MHz. The change in $\varepsilon_r(0)$ from 300 K to 220 K was 168%, while the phase shift at 15 GHz increases only about 34%. Unfortunately non-linearity in $\Delta\varphi(\varepsilon_r)$ makes a



a) b)

Figure 6. The phase shift of S_{21} (Δ) and maximum insertion loss (x) vs. temperature of a) Sample 3 b) Sample 4. This data was taken at 15 GHz and using a 360 V dc bias.

conclusion about the value of at $\varepsilon_r(0)$ at 15-18 GHz difficult to draw. These phase shifter results are consistent with modeling where ε_r tunes from 1200 to 550 at room temperature, and from 3200 to 800 at 250 K

CONCLUSIONS

Four BSTO films of composition 50:50 and 60:40 Ba:Sr ratios doped with 1% Mn were measured at 1 MHz with interdigital capacitor circuits and at 15 to 20 GHz using coupled microstrip phase shifters. Two films were post-annealed at 1100 C. The capacitor measurements as a function of temperature showed that the BSTO 50:50 films had a Tc about 183 K, while the 60:40 films had a Tc of 230 K. The annealing was found to greatly increase ε_r of these films. The largest value of ε_r = 3850 was found in the annealed BSTO 50:50 film. Tanδ at 1 MHz were found to be below 0.004 for most of these films.

The high frequency phase shifter measurements found room temperature figures of merit, K, up to 58.4°/dB at 18 GHz and 400 V dc bias. The corresponding phase shift per length for a single phase shifter was 419°/cm.

Annealing of these films had little effect on the phase shift and losses at room temperature and Ku-band frequencies. Cooling the phase shifters on the 60:40 films to their Curie temperature, lead to increased phase shifts of 10% and 38% for the as-deposited and annealed samples, respectively. It is unclear whether this small increase compared to the increase in ε_r at 1 MHz is caused by lowered ε_r at high frequency or the non-linearity of the CMPS circuit phase shift with increasing ε_r.

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