Design and Testing of a Breadboard Electrical Power Control Unit for the Fluid Combustion Facility Experiment

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DESIGN and TESTING of a BREADBOARD ELECTRICAL POWER
CONTROL UNIT for the FLUID COMBUSTION FACILITY EXPERIMENT

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ABSTRACT
The *Fluid Combustion Facility* (FCF) Project and the Power Technology Division at the NASA *Glenn Research Center* (GRC) at Lewis Field in Cleveland, OH along with the Sundstrand Corporation in Rockford, IL are jointly developing an *Electrical Power Converter Unit* (EPCU) for the Fluid Combustion Facility to be flown on the *International Space Station* (ISS). The FCF facility experiment contains three racks: A core rack, a combustion rack, and a fluids rack.

The EPCU will be used as the power interface to the ISS $120V_{dc}$ power distribution system by each FCF experiment rack which requires $28V_{dc}$. The EPCU is a modular design which contains three $120V_{dc}$-to-$28V_{dc}$ full-bridge, power converters rated at $1kW_e$ each; bus transferring input relays and solid-state, current-limiting input switches; 48 current-limiting, solid-state, output switches; and control and telemetry hardware. The EPCU has all controls required to autonomously share load demand between the power feeds and—if absolutely necessary—shed loads. The EPCU, which maximizes the usage of allocated ISS power and minimizes loss of power to loads, can be paralleled with other EPCUs.

This paper overviews the electrical design and operating characteristics of the EPCU and presents test data from the breadboard design.

INTRODUCTION
The FCF facility experiments will number between 10 and twelve per year over a 15 year period aboard the ISS. Their long-term operational requirements, in conjunction with their undefined requirements for the power demands, mandates a flexible and readily re-configurable power interface.

FCF experiments require uninterrupted power for long periods of time, but the ISS is extremely power constrained. Therefore, the EPCU module is designed to maximize allocated-power usage. In addition to accommodating power allocation constraints the EPCU is designed to reduce experiment development and integration by providing a single, flexible power interface which is readily adaptable to changing experimental power requirements. Further discussion on this is provided in Reference 1 [Poljak and Soltis, 1997].

The EPCU concept achieves its goals by dynamically sharing the load demand between the ISS channels feeding the EPCU, by autonomously shedding loads, and by providing limited, internal-fault tolerance. A dynamic power controller parallels the LCUs such that the ISS power busses equally share load as long as channel allocations are not violated. If a channel allocation violation occurs, then the LCU(s) fed by the other ISS channel pick up the additional load. Load shedding occurs only if power demand cannot be dynamically reallocated to the another channel, if the bus voltage droops, if an LCU is lost, or if the total load exceeds the total allocation of the two ISS channels.

The EPCU has been bread-boarded and its operation verified in the *Power Systems Facility* (PSF) located at LeRC. The EPCU is connected to a distribution system consisting of ISS proto-type hardware, which conform to ISS electrical distribution system requirements, developed by Rocketdyne (RKD). The preliminary results for dynamic power sharing, prioritized load shedding, and converter synchronization of the EPCU operations are given in this paper.

EPCU CONFIGURATION
The EPCU is a $3kW_e$ module utilizing three independent $120V_{dc}$-to-$28V_{dc}$ *Load Converter Units* (LCUs) rated at $1kW_e$ each (see Figure 1). The LCUs are paralleled and synchronized. Each can be fed from one of two ISS power channels, allowing loads to simultaneously draw power from two ISS channels via dynamic load sharing of the input busses. Each LCU is interfaced to an ISS power channel with three paralleled RPCs (rated at $4A_{dc}$ @ $120V_{dc}$ each) and a
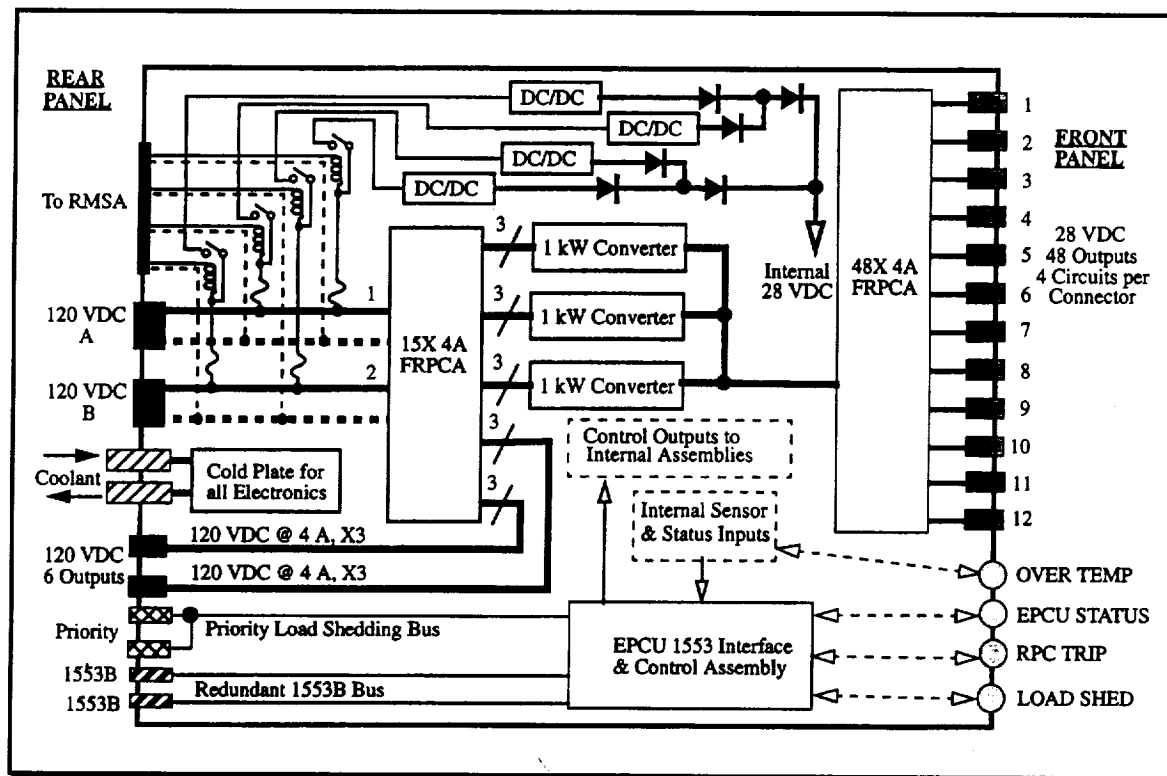
EPCU Block Diagram
Figure 1

dead-facing relay. (This allows an LCU to get power from one of two ISS channels without directly paralleling the channels.)

Within the EPCU are analog controls to dynamically parallel the LCUs and to shed loads under a variety of conditions. The EPCU contains a 1553b interface which allows EPCU telemetry to be uploaded (if required) and to download ISS channel-power allocations.

The EPCU faceplate has 12 power connectors (4 channels per connector) to which loads are connected via load-configured cable harnesses. The cable-harnesses can parallel $4A_{dc}$ channels as required for an experiment. This is possible because the EPCU output consists of 48 solid-state, current-limiting switches (referred to as *Flexible Remote Power Controllers*, FRPCs) rated at $4A_{dc}$ each.

DYNAMIC POWER SHARING
To maintain load sharing between the two input busses to the EPCU, the LCUs must be paralleled at a common output bus and the power share among them dynamically controlled. LCU paralleling is accomplished with a *Dynamic Power Share* (DPS) circuit which biases the converter sense voltages such that power demand, during normal operation, is shared equally between the two ISS power feeds to an EPCU rack. (Normal operation is defined as the total

load connected to the EPCU is serviced without interruption.) Then, as the allocation of a given channel reaches its limit, the LCU(s) connected to the other channel are forced to pick up the excess load (this is referred to as dynamic power reallocation), while the other channel is maintained at its allocation limit. The dynamic response of the power share controls is faster than that of the load shedding controls. Therefore, the power share circuit can reallocate load between channels before load shedding occurs. The LCU topology and circuit used to control the LCU power share are next detailed.

Dynamic Power Share Circuit
DPS results in EPCU loads being equally supplied by the two ISS channels as long as an allocation is not exceeded. This is accomplished as follows (see Figure 2):

1) The difference between the total bus current of each channel and the channel allocation is calculated. During normal mode operation, the difference amplifier output is negative.

2) Each of these "difference" signals is weighted (one positively and one negatively) and summed to produce an error signal. One channel allocation being exceeded leads to a positive error signal, while the other leads to a negative error signal. Under normal and ideal conditions, the error signal is zero.
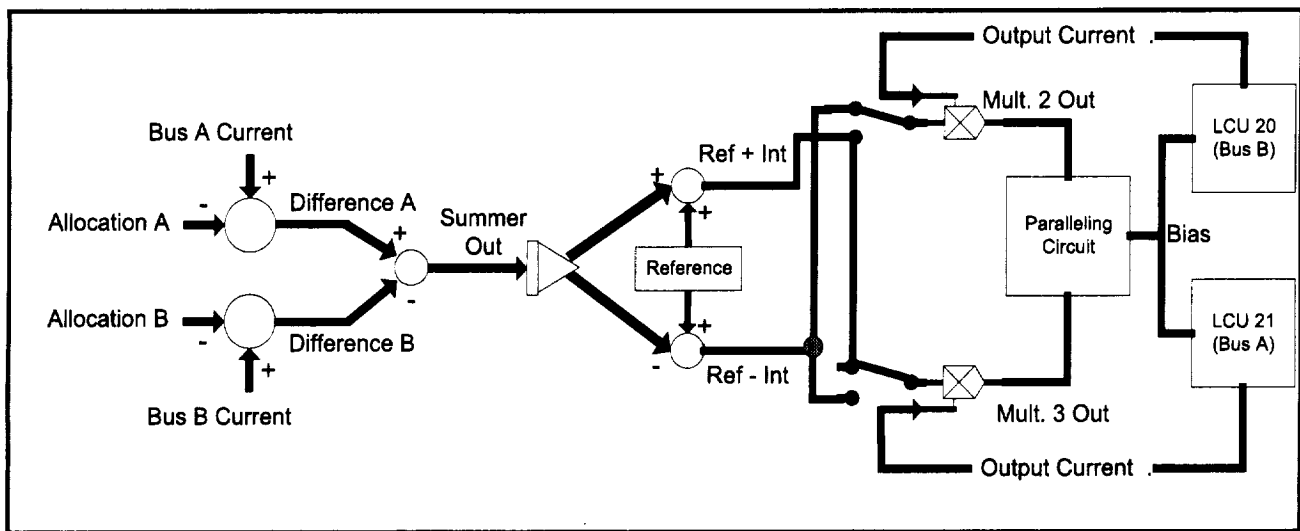
Dynamic Power Share Block Diagram for Two Load Converters
Figure 2

3) This single error signal is then integrated, inverted, and added to and subtracted from a reference signal of 5V. With zero error, the output will be $5V_{dc}$ and will result in control signals of 50/50 power share.

4) These control signals are then routed to two multipliers. The "Ref+int" is routed to those multipliers which receive current data from an LCU which is fed by a channel having negative weighting in step 2; the "Ref-int" control signal is fed to the multipliers which receive current data from an LCU which is fed by a channel having a positive weighting. In other words, the multiplier output is a product of the output current of an LCU and the control signal derived from the channel which does not feed the LCU.

5) The outputs of the multipliers are then fed to the actual paralleling circuit, which averages the total current supplied by the LCUs. The difference between a multiplier's output and this average value is the "bias voltage". Each bias voltage is added to the corresponding LCU output voltage sense circuit. Thus, the unit(s) which must supply more load receive a lower sense voltage, thus forcing the LCU to slightly increase its output voltage and thereby supply more load current. The converse holds for the LCU(s) which must decrease their share of load current.

It should be noted that, this paralleling scheme is easily extended to n-LCUs because the biasing circuit is connected in a star configuration, which results in an average voltage (based upon the output current of each LCU) at the common node. Also, the average should include only the current of active LCUs and, for this reason, the averaging bias resistor is enabled via a relay which is controlled by the "ON/OFF" status bit

of the LCU controller. However, in the event that the LCU does not shut off on an input undervoltage condition—whether by design or failure—then that LCU's zero current contribution is included in the averaging. The result of this inclusion is a bus voltage droop.

This bus voltage droop results from the paralleling controller attempts to increase the "off" converter's current share (by biasing its voltage sense lower) and to decrease the "on" converters' current share (by biasing the sense voltage higher). The increase in sense voltage causes a decrease of the LCU output voltage. Because the magnitude of current which the paralleling controller attempts to reallocate to the "off" converter affects the average value, the bus voltage droop is a function of total load. The droop is minimized by limiting the amount of bias to approximately $0.7V_{dc}$.

LCU Topology and Fault Tolerant Synchronization
Because the LCUs used in the FCF breadboard were designed as stand-alone $120V_{dc}$-to-$28V_{dc}$ converters, they have individual output LC filters. These output filters, in conjunction with non-synchronized operation, lead to a oscillating current between the tanks. This oscillating current adds to the ripple current (which will be present in an independently operating LCU) and resulted in an approximately 700mA peak-to-peak, tank-to-tank ripple. (It must be stressed that this ripple current is the ripple current associated with the individual LCU outputs. The total bus current ripple does not exhibit ripple of this magnitude.) Two solutions are available to synchronize and to reduce the ripple current of the converters.

1) Implement a master clock.

2) Affect the PWM comparator by superimposing a synchronizing signal on the individual ramps.

Option (1) suffers because a signal line disruption leads to one or more converters losing a clock. Option (2) is preferable because, even if the synchronization circuit fails, the worst case scenario is the converters will operate independently and exhibit higher than normal ripple current.

The synchronization of the converters over a small band of frequencies was accomplished via a circuit which produces three pulses, 120degrees out of phase. Each of these pulses is superimposed on the output-current ramp control signal of each LCU PWM controller, respectively. Test data verifies—but is not included within this paper--that the control ramps are forced to reset with the superimposed synchronizing signal. By synchronizing the converters, the peak-to-peak ripple current has been reduced by approximately 60%.

LOAD SHED CONTROL

A primary advantage of the EPCU is its ability to maintain the total load connected to it within the limits set forth by higher level ISS functions and downloaded to it via the 1553b bus. Load sharing redistributes power according to channel availability; however, in the event that load cannot be serviced without exceeding both allocations, load shedding is an essential function. Load shedding occurs for one of two reasons:

1) In the event that DPS cannot accommodate the total load (due to the loss of an LCU or too much

load) without exceeding both channel allocations, all load in excess of either allocation must be shed in a prioritized fashion. This is referred to as *Prioritized Load Shed* (PLS) control.

2) In the event that an input channel has been lost and the EPCU bus voltage has drooped significantly, then the EPCU must shed all but the most critical of loads. This is referred to as *Bus-Undervoltage* or *Fail-Safe Load Shed Control*.

Prioritized load-shed control is functionally accomplished by comparing each channel's current against a reference voltage corresponding to the allocation (see upper two diode-or circuits in Figure 3). If either allocation is exceeded, then the allocation comparator toggles high and the load shed-controller integrator, corresponding to that channel, begins to integrate down from its $+15V_{dc}$ normal state. (Recall that the load shed controller is slower than the dynamic power share, therefore the integrator will begin to integrate back up, if the excess load is reallocated to the other channel and the allocation is no longer exceeded.) These integrator outputs are tied together in a diode-or configuration so that the lower voltage (i.e., more overloaded channel) will initiate tripping of load. This diode-or node is fed to the inverting terminal of the load trip-control, "priority" comparator of each RPC channel.

The load priority level is connected to the non-inverting input of the "priority" comparator (Figure 3). The priority level voltage is a dip-switch selectable value. (There are 8 levels at $1.7V_{dc}$/priority level, and the lowest priority level has a $13.2V_{dc}$ voltage.) As a result, under normal operating conditions, the load trip-control comparator is low, and toggles high when the
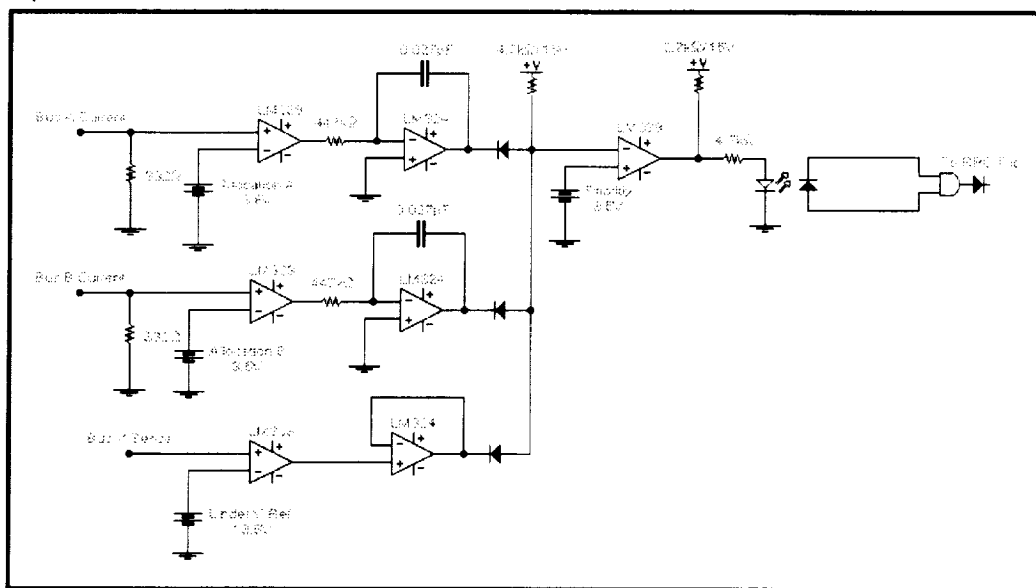
Load Shed Controller Pseudo-circuit
Figure 3

allocation is exceeded for a sufficient amount of time. The load shed controller comparator output is tied to the input of an HP2200 opto-isolator, which is normally low; the opto-isolator output is diode-or connected to the output of the RPC controller trip gate.

Lastly, the loss of an LCU impacts a fully loaded EPCU most drastically. In this case, the remaining two load converters—regardless of allocation setpoints—will result in a bus droop since the two remaining converters will enter current limit mode (foldback), while attempting to service 3kW$_e$. Granted, the load shed controls may shed some of the load; however, the response time of the load shed controller is much too slow for this condition.

As a result, bus-undervoltage load shed control is implemented (see lowest block in Figure 4). When the EPCU bus droops below 19.6V$_{dc}$, all but the most

output and have the load share control circuit having a closed-loop response of approximately 50mseconds.

2) One "Flex" *Remote Power Control* (RPC) unit having 20 channels rated at 4A$_{dc}$ each. The FLEX has two 120V$_{dc}$ input buses. Using a relay, an input bus can be selected, via a 1553 command, to be connected to an input RPC. Bus switching must be done with the solid-state switch in the "off" mode: hot switching cannot be accommodated. Using the FLEX, each LCU is connected to one of the 120V$_{dc}$ input buses, and each LCU within the EPCU is fed by four paralleled RPC Module channels.

3) Two Sundstrand "manual" RPCs having 14 channels, rated at 4A$_{dc}$ each, to service the EPCU loads. The loads connected to the Manual RPC Modules are purely resistive for these tests. The load shed control circuit is tied to all 14 channels on both RPCMs. The load shed controller has a time-to-first
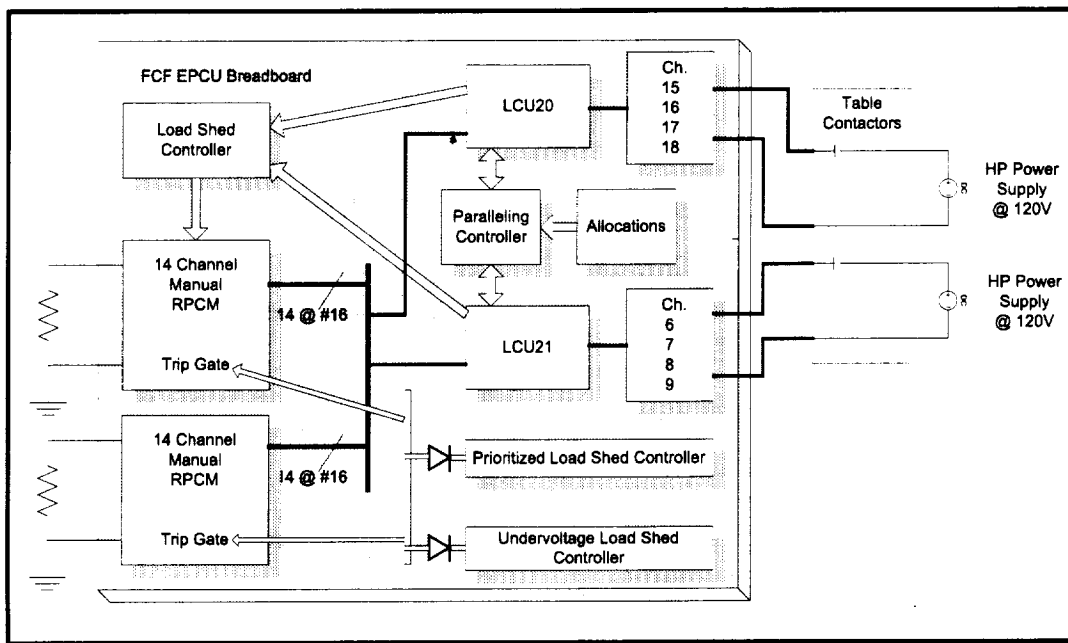
Breadboard & Test-bed Configuration
Figure 4

critical (i.e., initial position "on") loads are shed instantly, thus allowing the bus to recover and the EPCU to be operable. Again, this is fail-safe load shedding.

TEST-BED CONFIGURATION and RESULTS
The EPCU breadboard configuration consists of the following hardware and systems support hardware (see Figure 4):

1) Two Sundstrand 120V$_{dc}$-to-28V$_{dc}$ LCUs each rated at 1kW$_e$. These are paralleled at the

shed and a shed-interval time of approximately 55milliseconds.

4) Two HP power supplies to emulate 160V$_{dc}$-to-120V$_{dc}$ converters. The HP supplies are tied directly to the cold-table protective contactors which are tied to the input Flex RPC through 3feet of 1/0 cable.

5) A total resistive load of 70A$_{dc}$ of which approximately 20A$_{dc}$ is connected to the EPCU bus via the Manual RPC Modules, while the remainder is tied directly to the bus.

Tests were done to verify the functionality of and the required coordination between load sharing and load shedding; to verify EPCU operation in the event of the loss or droop of one ISS channels to the EPCU; to investigate the causes of and means to mitigate bus-voltage droop; and to verify the impacts of the LCU synchronization circuit.

Dynamic Power Share Test Results
Steady-state performance data for the paralleling circuit (refer to Figure 2) is given in Table 1. These data demonstrate the bias voltage differences and the resulting current share for equal and unequal allocations for the two channels.

The data in Table 2 was gathered by setting the two channel allocations to $3A_{dc}$ for channel A and $45A_{dc}$ for channel B, respectively. (Note that reflecting these values to the $28V_{dc}$ output of the LCUs results in current limits of 12A and $174A_{dc}$, respectively. Obviously, the channel B allocation cannot be exceeded because the maximum current output for an EPCU with three LCUs is approximately $105A_{dc}$.) Then the load was increased and the EPCU allowed to reach steady-state.

This steady-state data verifies that as the total load increases the two LCUs share data equally (data samples 1 and 2 in Table 2) until the allocation of the channel feeding LCU21 is exceeded. Further increases in total load are supplied by LCU20, and LCU21 continues to supply only $12A_{dc}$ of the total load.

	Allocation		
	A = B	A > B	A < B
Difference A	-0.016	1.721	-0.011
Difference B	-0.013	0.119	1.653
Summer Out	0.01	1.629	-1.634
Integrator Out	-0.02	-2.915	2.95
Ref + Int	5.18	2.47	7.92
Ref - Int	5.0	7.97	2.004
Multiplier 2 Out	4.26	3.511	2.639
Multiplier 3 Out	4.22	2.996	2.746
LCU20 Current	19.4	9.8	30.0
LCU21 Current	19.9	30.0	8.5

DPS Controller Data
Table 1

Total load [A]	I LCU 20	I LCU 21
17.22	8.78	8.44
22.45	11.42	11.03
34.3	22.45	11.85
45.29	33.2	12.09
53.15	41	12.15

**Dynamic Power Sharing Load Data**
Table 2

Figure 5 is the dynamic response of the EPCU to a load step change from approximately $30A_{dc}$ to $52A_{dc}$. The allocation of one channel is set to $17A_{dc}$ output current, and the other to a maximum of $105A_{dc}$ @ $28V_{dc}$. As seen, the two converters begin to share the increased load equally; however, the dynamic power share circuit limits LCU21 to $17A_{dc}$, and its share begins to roll-off. LCU20 continues to pick-up the remainder of the load. The steady-state share is LCU21 at $17A_{dc}$ and LCU20 at $35A_{dc}$.
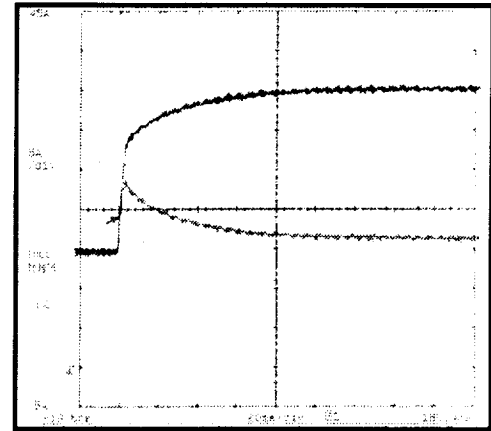
Dynamic Response to Load Step
Figure 5

Prioritized Load Shed Controller Test Results
Figure 6 is a trace of a priority load shed resulting from the loss of input power to LCU21. As seen, upon the loss of LC21, LCU20 picks up all of the load; however, the channel allocation (feeding LCU20) is set to a value which corresponds to an output current of approximately $19A_{dc}$. As a result, the excess load ($20A_{dc}$) is shed. The load priority controller sheds six priority levels in order to reverse the channel allocation violation.
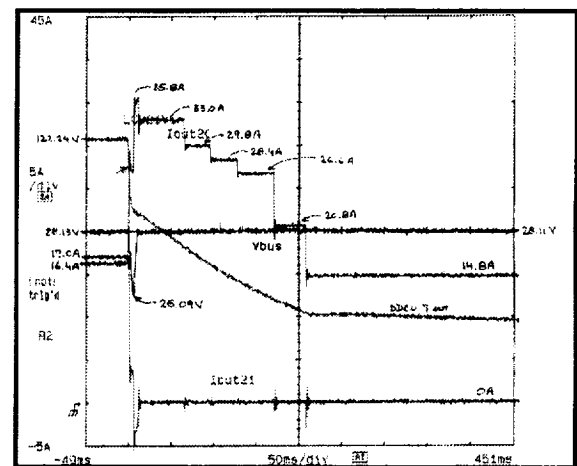
Prioritized Load Shed: Loss of Input Power
Figure 6

Also, because the bus undervoltage load shed controller is adjusted to shed upon a bus voltage below 19.6V$_{dc}$, it is seen that none of the load shedding occurs due to a bus undervoltage condition. This test scenario was selected to demonstrate that the loss of an input channel does not necessarily result in a severe bus droop and the resulting fail-safe load shedding associated with it.

Bus Undervoltage Load Shed Test Results
In this test (Figure 7) a purely resistive load is connected to the EPCU bus via the manual RPCs, and the allocation of both channels is set to 3kW$_e$ (i.e., 107Adc @ 28Vdc). Prior to the loss of input power to LCU21, the LCUs share the load equally at 29.6A$_{dc}$ and 28.4A$_{dc}$. Upon turning off the input RPCs feeding LCU21, the bus droops to 19.8Vdc and the bus recovers due to fail-safe load shed control.

Limiting Bus Voltage Droop Test Results
Figure 8 summarizes the steady-state bus voltage under various load conditions, after the loss of input power to LCU21. The test parameters are combinations of the input undervoltage shut-off status (enabled or disabled) of LCU21 with the droop-limiting diodes included or excluded in the paralleling circuit.

The impact of the undervoltage shut-off status is evidently most pronounced at light load conditions in the absence of droop-limiting diodes. The inclusion of droop-limiting diodes yields the flattest EPCU bus

voltage and yields the best results with undervoltage shut-off enabled. However the only case that impacts loads interface design and system efficiency is undervoltage shut-off disabled without droop-limiting diodes, because it leads to a significant EPCU bus-voltage droop at light loads. Thus, this is the only case which should not be implemented. (The bus recovers for all cases with loads greater than 55A$_{dc}$ due to fail-safe load shed control.)
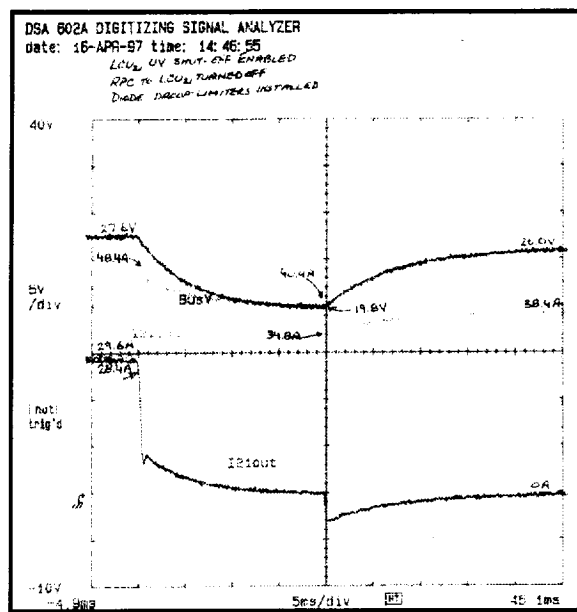
Bus Droop Limiting
Figure 7
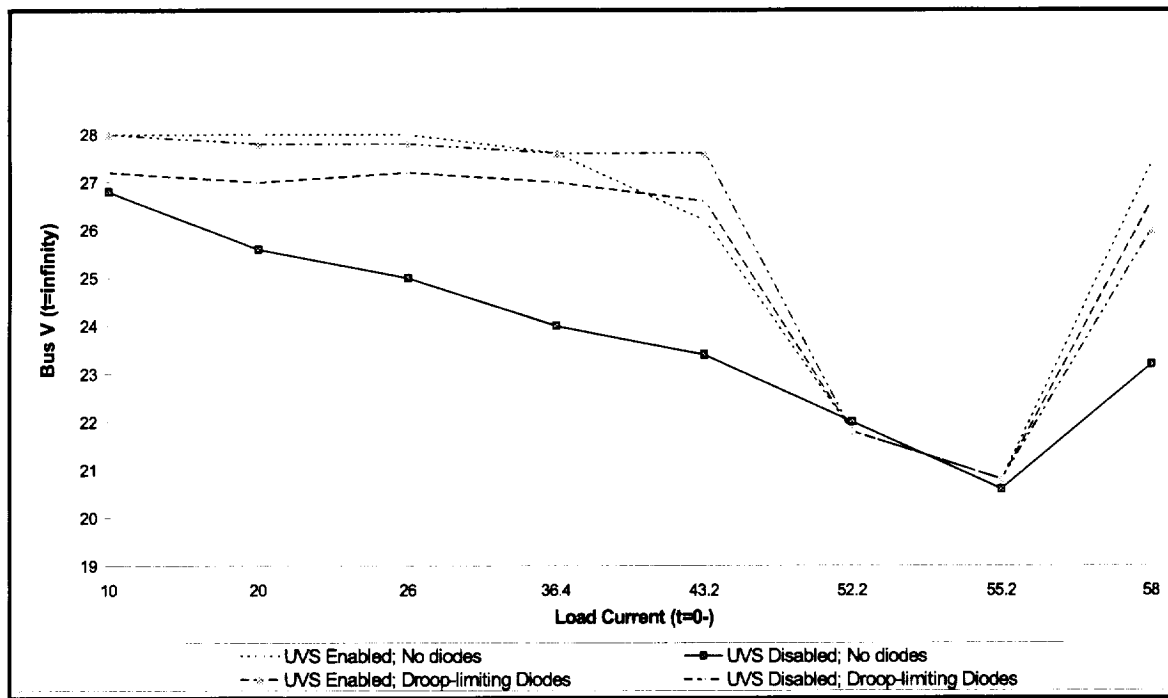
Bus Voltage as a Function of UVS and DLDs
Figure 8

CONCLUSIONS

The FCF EPCU concept proves to be a reliable, robust, and cost-effective power interface for the FCF experiments. It provides an intelligent interface through its ability to operate within ISS channel-power allocation limits under all conditions. The dynamic load sharing control ensures that the ISS channels are dynamically balanced to minimize channel allocation violations. And the load shedding schemes are implemented such that loads are shed in priority order only as necessary. As a result, this approach is very suitable—and recommended—for all ISS facilities and loads interfaces requiring $28V_{dc}$.

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13. ABSTRACT (Maximum 200 words)

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