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Design of a K-Band Transmit Phased Array For Low Earth Orbit Satellite Communications

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January 2000

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Abstract

The design of a light weight, low cost phased array antenna is presented. Multi-layer printed wiring board (PWB) technology is utilized for RF and DC/Logic manifold distribution. Transmit modules are soldered on one side and patch antenna elements are on the other, allowing the use of automated assembly processes. The 19 GHz antenna has two independently steerable beams, each capable of transferring data at 622 Mbps. A passive, self-contained phase change thermal management system is also presented.

Experiment Description & Objectives

Rapid deployment of low and medium Earth orbit (LEO/MEO) satellite constellations, which will offer various narrow to wide band wireless communications services, will require phased array antennas which feature wide-angle and super agile electronic steering of one or more antenna beams. Phased array antennas are perfectly suited for this application. A MMIC-based, K-band phased array antenna is in development, under a cooperative agreement between NASA Glenn Research Center and Raytheon Systems Company. The transmit array, operating at 19 GHz, is a state-of-the-art design that features dual, independent, electronically steerable beam operation (± 42°), a stand-alone thermal management system and a high-density tile architecture. The tile integration technology ("flip chip MMIC tile") represents a major advancement in phased array engineering and holds much promise for reduced manufacturing costs.

The antenna system is scheduled to be completed in mid-2000. The array will be a critical component of the Direct Data Distribution (D^3) flight experiment on a future Space Shuttle mission, as early as 2001, with the objective of down linking wide band data rates to a small, tracking Earth terminal. Phased array antennas capable of providing a rapid direct downlink of large volumes of data from various space platforms are high on NASA's and the communications industry's priority lists.

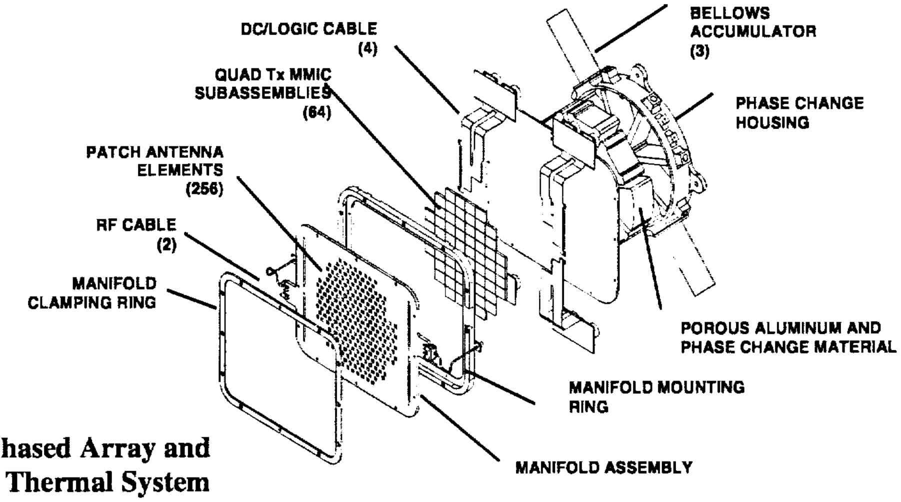


Figure 1. Phased Array and Thermal System

Array Requirements

Requirements for the D^3 Array were determined from a combination of functional needs of NASA's D^3 flight experiment and performance requirements taken from the experiment link budget analysis. Functional requirements of the experiment include: frequency/bandwidth, number of beams, scan limits, polarization, DC power and weight/volume. Performance requirements derived from the link budget include: EIRP, cross-polarization, and intermodulation. A summary of the phased array performance goals is listed in Table 1.

Table 1. Array Performance Goals

Parameter	Value
Frequency/Bandwidth	18.8 to 19.3 GHz
Transmit Power	20 Watts/beam
EIRP at max. scan	39.1 dBW
Number of Beams	2
Maximum Scan Angle	± 42° in Az and El
Polarization	RHCP & LHCP
Cross-polarization	-15 dB
Beamwidth	6.4° x 6.4°
Sidelobe level	-20 dB, peak
Intermodulation	-25 dBc
DC power	<390 Watts
Array Weight	< 3.8 kg
Array Volume	$<5000\ \mathrm{cm}^3$

Additional requirements due to the planned experiment on the Shuttle are environmental and safety related. The space environment requires special attention to thermal design of the active array. A separate thermal management system is required to handle the heat generated by the transmit modules. Special materials are used to accommodate the temperature and vacuum conditions. Space radiation is low at the Shuttle altitude, but radiation must be considered in selection of high speed digital circuits. Three levels of hardware and software interlocks are designed into the controller to eliminate the risk of RF radiation to the astronauts.

Array Description

The array aperture is circular with edges formed due to the use of quad modules as tiles for array construction. Microstrip stacked patch radiating elements are arranged in an equilateral triangular grid with a separation of 9.75 mm to allow the antenna to scan to 42° from boresight without grating lobes. To achieve the required 39.1 dBW effective isotropic radiated power (EIRP) at full scan, the array consists of 256 radiating elements. A 6 dB step taper has been implemented to control sidelobe levels. The 96 central and 160 outer elements are fed by 0.25 μm pHEMPT 150 mW and 37.5 mW MMIC amplifiers, respectively.

Each quad module contains 8, 4-bit phase shifters and 4 dual channel power amplifiers, allowing the array to form two independent, simultaneous beams. The output power is 20 Watts per beam. Array power dissipation is estimated at 346 Watts during the ON state with both beams active. The total dc power required by the array is estimated at 386 Watts.

The two beams are generated with opposite sense polarization, one right-hand circularly polarized, one as left-hand circularly polarized. This approach minimizes interference between beams and allows both beams to be simultaneously received by a single ground terminal. The current estimate is that the worst case polarization coupling level will be –15 dB. Predicted pattern performance is shown at the end of this paper.

As shown in Figure 1, the antenna is fabricated using a tile method of construction producing a high-density, low-profile assembly. The main internal assembly, the RF/DC manifold, is a multi-layer printed wiring board consisting of 27 metal layers separated by dielectric material of various thicknesses. These layers include the etched circuits for the two corporate feed RF divider networks for the two beams, the dc power distribution circuits, the logic and control networks, and the microstrip patch elements with their associated 90° branch-line hybrids to form circularly polarized waves. The layer count also includes all of the ground and joining layers required between sub-panels of the multi-layer board assembly. The quad modules are attached directly to the RF/DC manifold with a solder ball reflow process.

A beam steering computer (BSC) has been developed by Raytheon to control all operations of the antenna. The BSC consists of a commercially available VME processor card and a custom mezzanine card to control array functions in response to commands received from the payload control computer via the VME bus.

Tile Description

The D^3 Array is populated with 64 tile modules mounted to the RF DC manifold in a rectangular grid. Tile size is 16.4 mm W x 19.0 mm L x 2.67 mm H weighing approximately 3.5 grams. Each tile consists of a quad module as shown in Figure 2. The tile modules each contain 8 independently controlled RF paths partitioned in quadrants since each tile must feed the two independent beams to four radiating elements. The array 6 dB step taper is implemented with 24 high power modules in the center of the array and 40 low power modules around the periphery.

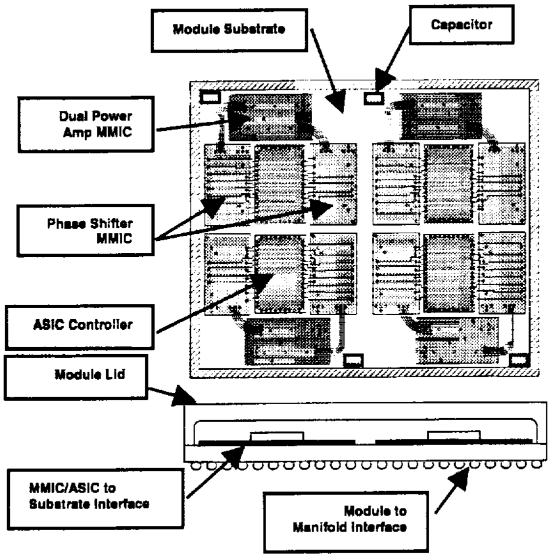


Figure 2. Module Layout

The D^3 tile module design evolved from RF and thermal performance, available area, fabrication/production issues and cost goals. The major module components are shown in Figure 2. The module mounts to the RF/DC manifold using a Ball Grid Array (BGA) using 0.508 mm diameter 90Sn/10Pb alloy solder balls. The module substrate is 0.381 mm thick Alumina with appropriate metallization for signal routing, thermal conduction and BGA attachment with 0.127 mm diameter filled through vias for RF/DC/logic I/O and thermal conduction. Each quadrant contains a silicon ASIC controller, a GaAs dual channel power amplifier MMIC, and two GaAs phase shifter/attenuator MMICs. The ICs are flip chip mounted to the substrate using 0.127 mm diameter 63SN/37Pb alloy solder balls. There are 4 surface mount chip capacitors for local energy storage and RF bypass. The MMICs and capacitors account for 60% of the substrate area demonstrating the increased packing density afforded by flip chip IC mounting. A copper alloy lid attached to the substrate completes the module package and serves as the main thermal interface.

Monolithic Microwave Integrated Circuit (MMIC)

The D^3 Array modules contain Embedded Transmission Line (ETL) MMICs on a GaAs substrate as shown in Figure 3 [1]. ETL MMICs utilize matching circuits, transmission lines, and lumped, passive components in a low loss dielectric with a topside ground plane. The ground plane reduces unwanted interactions between the MMIC and its surrounding environment producing more consistent RF performance during production process development.

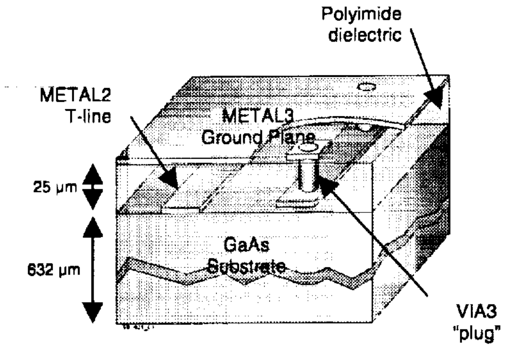


Figure 3. ETL MMIC

There are three MMIC designs: the phase shifter/attenuator, high power dual channel power amplifier and low power dual channel power amplifier. The phase shifter/attenuator

MMIC size is 4.47x2.47 mm. The RF signal enters the MMIC and travels through an amplifier followed by 4 attenuator bits, another amplifier stage, 4 phase shifter delay line and then exits the MMIC. The amplifier stages offset transmission line losses within the MMIC for a nominal net gain of 0 dB.

The dual channel high power amplifier MMIC size is 4.47x2.47 mm. Two RF signals enter the MMIC and each signal path travels through three amplifier stages before exiting the MMIC. Net gain is +21 dB with +22 dBm RF output power at 1 dB compression. The dual channel low power amplifier MMIC is similar to its high power counterpart except there are only two amplifier stages producing +15 dB gain with +16 dBm RF output power at 1 dB compression.

Thermal Management System

A phase change thermal management system has been developed to provide a platform independent heat management system. The system also provides the structural interface between the array and the Shuttle Hitchhiker canister. It is sized to maintain transistor junction temperatures below 100°C and to maintain an array thermal gradient below 10°C. The phase change system is a 20 cm diameter brazed housing with porous aluminum "foam" inside, as shown in Figure 1. The "foam" is filled with paraffin wax phase change material. As the antenna modules heat up, the solid wax absorbs the heat energy and changes to the liquid phase. During the phase change period, the wax temperature is maintained at approximately the melt point. This provides a constant-temperature interface for the array electronic modules. During periods in which the antenna modules are off, the wax releases its stored heat and changes back to the solid phase, thereby tempering extreme temperature excursions. Heat pipes are arranged radially to maintain the array temperature gradients at an acceptable level. This is made necessary due to the higher power center modules described above.

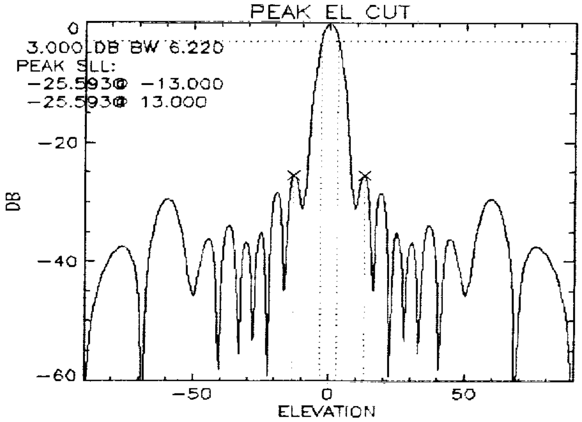
Conclusions

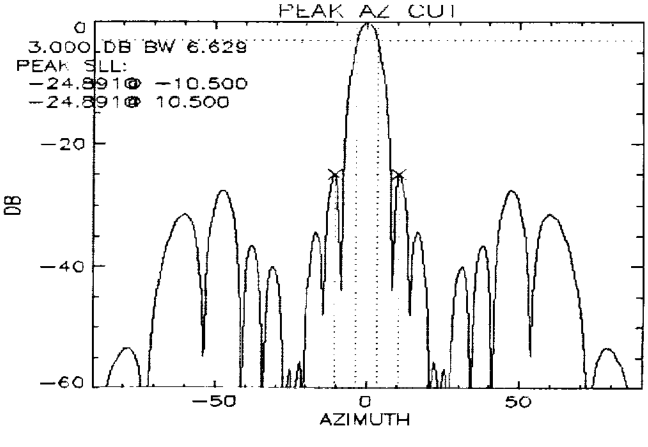
High performance, lightweight, low cost antennas are needed for future satellite communication systems. A recent advance has been the development of a two beam, K-band, transmit array to demonstrate high data rate link from the Shuttle to a NASA ground station. Many advanced technologies have been designed into this antenna in order to meet the requirements of the experiment. A successful demonstration will validate these technologies for future satellite applications.

References

[1] H. Tserng, *et. al.*, "Embedded Transmission-Line (ETL) MMIC for Low-Cost High-Density Wireless Communication Applications," IEEE Transactions on Microwave Theory and Techniques, vol. 45 No. 12, December, 1997.

Array Patterns on Boresight





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