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MEMS Reliability Assurance Guidelines For Space Applications

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The research described in this publication was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Preface

This guideline was developed as an aid to help in the understanding of Microelectromechanical Systems (MEMS) reliability and to facilitate the insertion of this technology into high reliability applications. Modeled after the GaAs MMIC Reliability Assurance Guideline for Space Applications by Kayali et al., it was felt that a guideline would be more advantageous to people than a strict specification. With the MEMS industry as diverse as it is today, it seemed presumptuous to lay out specific tests for every MEMS device inserted into space as that kind of document would be unduly constrictive to some applications. Rather this document was intended as a MEMS educational guide, offering descriptions of the most common devices and technologies and the steps required to meet the demands of the space environment.

The focus of this guide is upon methods rather than tests and as such, it is assumed that the ultimate responsibility for reliability lies in the hands of the user. Ultimately it is felt that the designers and the customers will have to reach an understanding as to the exact qualification needs of a particular device.

The guideline begins with a chapter on the recent developments in the field of MEMS and the need for an understanding of related reliability issues. Chapter 2 offers a basic review of reliability models and of semiconductor failure distributions. This chapter is intended to aid the reader in understanding the meaning of reliability tests in general, and how they may apply to MEMS.

Chapter 3 describes the known failure mechanisms that have been characterized in MEMS technology. While the bulk of the chapter is dedicated to mechanical fracture, it must be understood that each failure mechanism will have a different level of predominance on different devices. Chapter 4 describes the basic material properties of common MEMS materials and relates these to the theory presented in Chapter 3.

Chapter 5 provides a description of common MEMS processing techniques. Both the discrete steps used to make the devices and the combination of those steps into a coherent process are discussed. A description of common MEMS device elements is presented in Chapter 6, along with relevant reliability concerns.

Chapter 7 discusses methods for modeling structure using finite element analysis. Chapter 8 involves reliability issues in packaging. Chapter 9 describes common test structures used to characterize the materials properties and structures discussed in Chapters 3 and 6.

Finally Chapter 10 offers a summary of the ways to use the information from the previous chapters to develop a reliable, space qualified, MEMS device. The information

in this document is only a compilation of much deeper works and it is felt that users of this guideline should reference other documents listed throughout this guideline in the process of furthering MEMS reliability.

I would also like to thank the people involved in the production of this document. Sammy Kayali provided both technical advice and moral support throughout the arduous process of writing this guideline. Joseph Bernstein helped in the organization of the guideline and helped me to understand the material in Chapter 2. Bill Tang of the Micro Devices Laboratory at JPL gave great help in the processing area and lent his general expertise to improving the quality of the guideline. Dave Gerke, the resident packaging expert at JPL, was instrumental in producing the material on packaging issues in MEMS. Jim Newell and Kin Man in the Engineering Technology section at JPL provided invaluable modeling and dynamic testing material for the guideline. Finally, Thomas Kenny proofread the document and provided valuable feedback in the editing phase.

I would also like to acknowledge those people that did not contribute to the document itself, but who helped to make it possible through their encouragement. Russell Lawton, as the PI for MEMS Reliability at JPL, procured the funding for this document and acquired many of the images contained herein. Noel MacDonald, an electrical engineering professor at Cornell, provided the academic encouragement to enter into this emerging field and, without his teaching, this document would never have been produced. Norman Tien, also an electrical engineering professor at Cornell, helped by explaining some complicated issues in the field of surface micromachining. Rishi Khanna, Valdis Rigdon, and Dipak Srinivasan, also of Cornell, provided the incentive to start writing this document back in December of 1996. Greg Radighieri of Texas A&M also helped through his input and valuable insight into mechanical engineering issues.

Brian Stark
August 1998

Abstract

This guide is a reference for understanding the various aspects of microelectromechanical systems, or MEMS, with an emphasis on device reliability. Material properties, failure mechanisms, processing techniques, device structures, and packaging techniques common to MEMS are addressed in detail. Design and qualification methodologies provide the reader with the means to develop suitable qualification plans for the insertion of MEMS into the space environment.

Contributors

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Chapter 1: Introduction

B. Stark and W. C. Tang

This chapter offers a brief description of the MEMS industry as it stands today. Assuming no familiarity with the subject matter, it explains the basic concepts behind MEMS and how they are being applied to meet current technological challenges in different markets. This chapter also describes the basic methodology that will be applied throughout this book towards qualifying a high-reliability MEMS device.

I. A Brief Description of MEMS

MEMS is an acronym that stands for microelectromechanical systems. It is a broad term that encompasses a fairly nebulous group of products. Essentially, MEMS are any product, ranging in size from a micron to a centimeter, that combines mechanical and electrical structures. Although the possible scope of MEMS is fairly limitless, for the sake of conventions and the need for brevity, this book will only address the more common MEMS technologies.

Initially MEMS developed from technologies used in the semiconductor industry for the production of electronic circuits. Less than 10 years after the invention of the integrated circuit, H. C. Nathanson used microelectronic fabrication techniques to make the world's first micromechanical device.[2] By the early 1980s, due to massive improvements in processing technologies, micromechanical devices grew in popularity. In the ensuing years, a new industry was born, where electromechanical systems could be realized on micrometer scales. The result was a whole new class of sensors and actuators that performed common tasks on smaller scales that were ideally suited for mass production.

MEMS, in its most conventional sense, refers to a class of batch-fabricated devices that utilize both mechanical and electrical components to simulate macroscopic devices on a microscopic scale. This guideline focuses upon the conventional definition of MEMS. The essence of MEMS is that they are small devices that perform mechanical tasks in ways and, more importantly, in quantities that conventional devices cannot.

II. The Potential of MEMS

In the wake of the explosion of the microprocessor in the early eighties, the semiconductor industry revealed its immutable law that smaller is better. With economies of scale turning tiny firms into industrial behemoths, it became evident that mass miniaturization, along with mass distribution, could produce huge revenues and

substantively change the daily lives of average citizens. Given the unmitigated success of the microcircuit, it became only a matter of time before technologies would emerge that could bring machines to the microscopic world and produce similar results. With MEMS poised to do for machines what the transistor did for computers, there has been a vast explosion of interest, and thus funding, in MEMS research.

MEMS are used to perform the tasks of macroscopic devices at a fraction of the cost and with, occasionally, improved functionality and performance. By using simple mechanical structures and tailoring integrated circuits to suit specific tasks, designers have seen a drastic reduction in device scales and the implementations of functions that were previously unrealized. Their size alone makes them attractive for limited mass applications, with the automotive, biomedical, communications, data storage, and aerospace industries taking a keen interest in MEMS developments. Far more promising, though, is the possible reduction in costs offered by MEMS. By combining increasing throughput with fixed cost structures, manufacturers can linearly reduce prices by a comparable production increase. Offering economies unique to the semiconductor industry, MEMS have the potential to revolutionize the industrial age.

The effects of MEMS could enact sweeping reforms within the space industry. NASA hopes to eventually phase out the large satellites that it employs to reach the farthest points in the solar system. With every kilogram sent to Mars costing upwards of one million dollars, the potential of sending a fully integrated spacecraft weighing a few

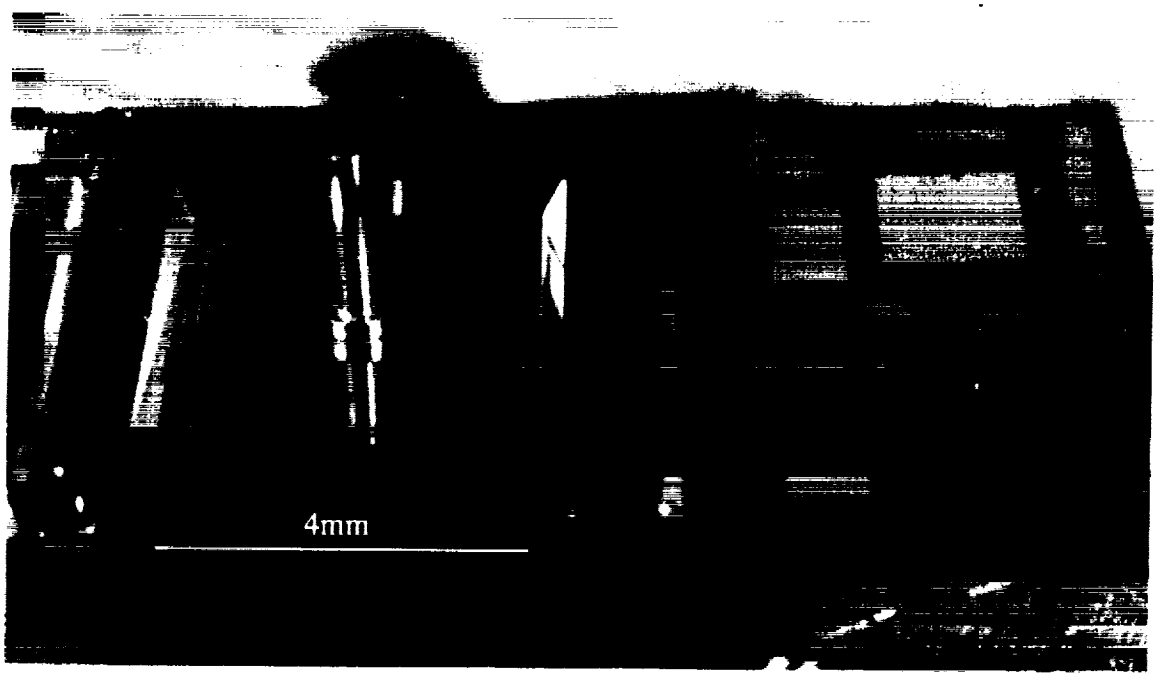


Figure 1-1: A partially packaged microgyroscope developed at JPL.

kilograms instead of the thousands of kilos offers significant monetary benefits. With MEMS capable of performing certain functions of macroscopic devices, the benefit of cutting the cost of research missions cannot be understated given this era of shrinking budgets. Space applications of MEMS are only a small part of their full potential. MEMS are also capable of revolutionizing the information age by changing the daily fabric of our terrestrial existence.

III. Current MEMS Technologies

Understanding the stated advantages of MEMS, designers have started developing a range of products to suit their needs. The first major MEMS to hit markets were pressure sensors for engine control in cars. This development was followed by the introduction of microaccelerometers, which were pioneered to provide zero-fault air bag deployment systems. Integrating a diagnostic circuit into a sensor, engineers were able to produce a device that could not only sense acceleration but that could also detect internal failures. Replacing a faulty system based on ball bearings and plastic tubing that was prone to misfire, these devices swept through the automotive industry. Building from the technological, as well as commercial, success of these initial designs, engineers have developed MEMS to act as a wide variety of motion sensors. Recently intense research has been conducted into producing microgyroscopes as part of a fully integrated inertial reference unit. Development has also commenced, seismometers, anemometers, temperature sensors, pressure sensors, and hygrometers which, when incorporated with accelerometers, could provide miniaturized weather stations.

MEMS have also shown promise for aerospace applications. Research into magnetometers shows that it may be possible to build devices that far outperform traditional solid-state sensors, which could provide cost saving reductions in the weight of spacecraft. Furthermore, the bulky propulsion systems in modern satellites will be phased out by advances in micropropulsion coming from new generations of ion drives and microthrusters. Recent developments at universities have shown that MEMS microactuators, when placed upon the leading edge of aircraft, can offer significant drag reduction and thus increase fuel efficiency.[182] Some even more interesting research has led to the design of a MEMS controlled aircraft, where control surfaces are replaced by micromachines, which could offer unprecedented control and diagnostic capabilities.

One of the more promising fields within MEMS is the concept of optical MEMS. Using micromirrors placed on top of memory arrays, researchers have developed a television projection unit on a semiconductor wafer that has all the functionality of a cathode ray tube.[3] Another promising development is in the field of optical switches. Conventional optical switching networks are costly and, with the forecasted growth in optical communications systems, cheaper alternatives are at a premium. Multiple groups have developed MEMS-based optical switches that can be produced at a fraction of the cost of conventional systems.

With the digital age largely upon the American public, MEMS are poised to offer greater improvements in computer technology. Given that power dissipation of the average microprocessor increases with every generation of microchip, microtubules research has been initiated to attempt to find better ways to conduct heat away from integrated circuits. MEMS structures have also been developed as microprobes for integrated circuits.[10] Using MEMS, it may be possible to take point contact voltage and current measurements on microprocessors. Another exciting development has been the pioneering of nanometer scale data storage. With miniaturized tunneling tips now possible, engineers have developed systems that could eventually store information at commercially competitive speeds in an area twenty nanometers on a side.

Another field that shows promise is the development of biological sensors. MEMS provides an opportunity for the development of new sensors to monitor the human environment. Researchers at JPL have begun to develop MEMS-based pills that can provide information about the digestive system. Another interesting application of MEMS has been in the development of new biological instruments. Researchers have, among other developments, produced probes to measure the strength of the human heart cell.[183]

While the potentials of MEMS are almost limitless, production of commercial parts has been heretofore limited. MEMS, as products of a young industry, remain largely prototypical. While their potential have been demonstrated their actual implementation has been relatively scarce, with commercial successes still the exception rather than the rule. In order for this rapid growth to be realized, the field of MEMS reliability will need to rapidly mature.

IV. The Need for, and Role of, MEMS Reliability

With MEMS still in their infancy, the question has been posed as to the need for reliability issues in MEMS. The goal of this book is not just to provide reliability information for the current designers but to set the standard for reliability in MEMS for the foreseeable future. Given the almost unstoppable commercialization of MEMS, reliability issues that have previously been ignored are destined to become of paramount importance. Researchers at NASA feel that these issues must be raised in unison with the development of MEMS in order to assure their rapid insertion into industrial and space applications. Understanding the future of the MEMS industry, it would be shortsighted to ignore the importance of reliability.

In confronting the issues of MEMS reliability assurance, users will certainly have different requirements and this book could not hope to address them all. Undoubtedly a Martian probe will have a different set of requirements and specifications than a communications satellite, but there will be similar methodologies for assessing qualification for both. This book is designed to utilize basic similarities in design

requirements to provide a means of developing high-reliability MEMS parts. In order to produce a high reliability, or high-rel, part one must not only examine the device itself, but one must also examine the entire process surrounding the part, from conception to finish. This means that the process must be qualified, with the supplier fully investigated, the design verified, and the packaging certified. This book lays out the methods to perform this task in an efficient manner that ensures the development of a high reliability part without enforcing cumbersome specifications.

V. Additional Reading

Helvajian, H. ed. Microengineering Technology for Space Systems, The Aerospace Corporation Report Number ATR-95(8168)-2, El Segundo, CA (September 30, 1995).

O'Rourke, L. Space Applications For Micro & Nano-technologies, European Space Agency, Noordwijk, The Netherlands (April 1997).

Chapter 2: Reliability Overview

B. Stark and J. Bernstein

Reliability is understood in modern times as the probability that an item will perform its required task for a set amount of time. Reliability is ultimately a measure of the rate at which things fail and can be used to make intelligent predictions about the performance of a system. If the assumption is made that a system is operating at time t = 0, and a time T is defined as the time to failure, then it is possible to define the complementary failure and reliability rates as:

$$F(t) \equiv P\{T \leq t \tag{2-1a}$$

$$R(T) \equiv P\{T > t\} = 1 - F(t) \tag{2-1b}$$

where

P{a} = The probability that the event 'a' will occur

F(t) = The probability that a system fails in [0,t]

R(t) = The probability that a system survives until time t

From probability theory, it is known that F(t) and R(t) are non-negative and that F(0) = 0 and F(∞) = 1, since all parts will eventually fail. A good measure of reliability in the interval (t,t+Δt] is the probability that a system does not fail in the internal (t,t+Δt], given that it has not failed by time t, which is written as:

$$P\{T \notin (t, t + \Delta t] \mid T > t\} \tag{2-2}$$

this quantity is known as the conditional reliability of a system of age t, represented by the expression R(Δt|t) and is related to R(t) by Equation 2-3.

$$R(\Delta t \mid t) = \frac{R(t + \Delta t)}{R(t)} \tag{2-3}$$

It should be apparent that R(Δt|0)=R(Δt), since R(0)≡1, as defined earlier.

I. Reliability Measures

The main challenge of reliability analysis is to quantify a system's reliability. This can be done in a number of ways by utilizing some important probability principles. When data from a reliability test is first collected, it is plotted as failure versus time. This plot is usually smoothed by fitting the reliability data to established reliability models, which are discussed later in the chapter. After this is done, the probability density function, or pdf, is determined.

A. Probability Density Function

The measure of the probability of failure around a point in time, t, is represented by the probability density function of T:

$$f(t) \equiv \frac{dF(t)}{dt} = \lim_{\Delta t \to 0} \frac{F(t+\Delta t) - F(t)}{\Delta t} \tag{2-4}$$

f(t) is, for a small Δt, approximately equal to the probability of failure in the time interval $[t,t+\Delta t]$. Once f(t) is found by whatever approximation is made for the failure function, one can determine the failure rate, which is the same as the reliability rate.

B. Failure Rate

The instantaneous failure rate is defined as:

$$\lambda(t) \equiv \lim_{\Delta t \to 0} \frac{P\{t < T \le t + \Delta t \mid T > t\}}{\Delta t} \tag{2-5a}$$

which can be rewritten as:

$$\lambda(t) = \lim_{\Delta t \to 0} \frac{P\{t < T \le t + \Delta t\}}{\Delta t P\{T > t\}} \Rightarrow \tag{2-5b}$$

$$\lambda(t) = \frac{1}{R(t)} \lim_{\Delta t \to 0} \frac{F(t+\Delta t) - F(t)}{\Delta t} = \frac{f(t)}{R(t)} \tag{2-5c}$$

Since $\lambda(t) = f(t)/R(t)$, it is also possible to define $\lambda(t)$ by:

$$\lambda(t) = -\frac{1}{R(t)} \frac{dR(t)}{dt} \Rightarrow \tag{2-6a}$$

$$\lambda(t) = -\frac{d}{dt}(\ln R(t)) \tag{2-6b}$$

This can be rearranged to give:

$$\ln(R(t)) - \ln(R(0)) = -\int_0^t \lambda(T)dT \tag{2-6c}$$

Thus, given that R(0) = 1, it is possible to determine R(t) as a function of λ as:

$$R(t) = e^{-\int_0^t \lambda(T)dT} \tag{2-7}$$

So, if λ is constant for a period of time, the reliability function is:

$$R(t) = e^{-\lambda t} \tag{2-8}$$

which is the exponential model of reliability. However, for most systems, the failure rate is not constant with time. In fact, the change of λ with time becomes one of the most important reliability measures. A decreasing λ indicates improvement with time, while an increasing λ indicates wear-out and a reduction in reliability over time.

C. The Bathtub Curve

By looking at a plot of failure rate over time, it is possible to derive substantive information about reliability. From experience in the semiconductor industry, it has been shown that most devices, including MEMS,[50] have a failure rate λ(t) that is shown in Figure 2-1. This model is known as the bathtub curve and was initially developed to model the failure rates of mechanical equipment, but has since been adopted by the semiconductor industry.

The bathtub curve can be reduced to three regions of reliability. The failure rate of a successful part is initially high and falls off as latent defects cause devices to fail until a time, t_{infant}, at which point the failure rate levels off. A decreasing failure rate will typically justify initial testing and burn-in. The failure rate remains constant for a period of time specified as the useful life, t_{useful}. Failures that occur during this period of time may be considered random and, for high-rel operations, λ should be exceedingly small. Finally, after $t_{operation}$, devices begin to exceed their lifetimes and wear-out causes the curve to rapidly increase. From this data it is evident that t_{useful} can be defined as:

$$t_{useful} = t_{operation} - t_{infant} \tag{2-9}$$

As indicated by the bathtub curve, manufacturers aim for the failure rate to remain fairly constant over t_{useful}, which justifies using the exponential reliability model for each part to be used in system reliability models. The time scale is often plotted logarithmically, although the values of t_{useful} and t_{infant} are rarely well defined.

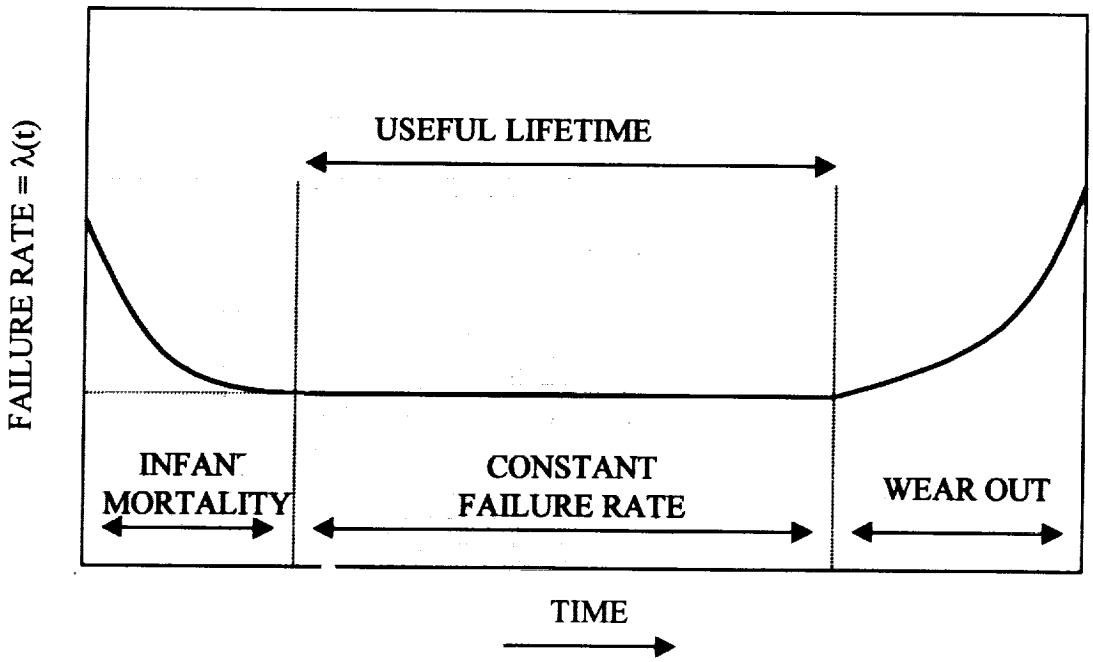


Figure 2-1: The Bathtub curve.

Consequently, every manufacturer has its own specific test and burn-in procedure to maximize the reliability of each product.

D. Predicting Time to Failure

Sometimes it is desirable to discuss the average time to failure instead of the probability of failure. This value, called the mean time to failure (MTTF) is defined as:

$$MTTF \equiv \int_0^\infty tf(t)dt \tag{2-10a}$$

It is also possible to prove[108] that the MTTF equals

$$MTTF = \int_0^\infty R(t)dt \tag{2-10b}$$

Once a device is operational, a more useful value is the mean residual life, or MRL. This quantity is derivable as:

$$MRL(t) = \frac{1}{R(t)} \int_t^\infty R(T)dT \tag{2-11}$$

It should be noted that MRL(0) = MTTF.

E. Failure Rate Units

Since, for most systems, $\lambda(t)$ is a small quantity, special units are used to describe reliability. The failure rate is given as the number of units failing per unit time. In common operation, this number, when expressed as the number of devices failing per unit time, K, is a fraction of a percent. To make this function more useful, the values are scaled to a more meaningful time frame. Thus $\lambda(t)$ is expressed as tenths of a percent of devices failing per 1×10^6 hours or as the total number of devices failing in 1×10^9 hours. This latter quantity is known as the failure in time, or FIT, and is the common unit of reliability defined as:

$$1\ \text{FIT} = \frac{1\ \text{failure}}{1\times10^9\ \text{device hours}} \tag{2-12}$$

A FIT is an approximate rate measure over the useful life of a part, assuming a constant failure rate, given the bathtub curve model, the FIT rate = $\lambda/10^9$, where λ is the constant failure rate shown in Figure 2-1.

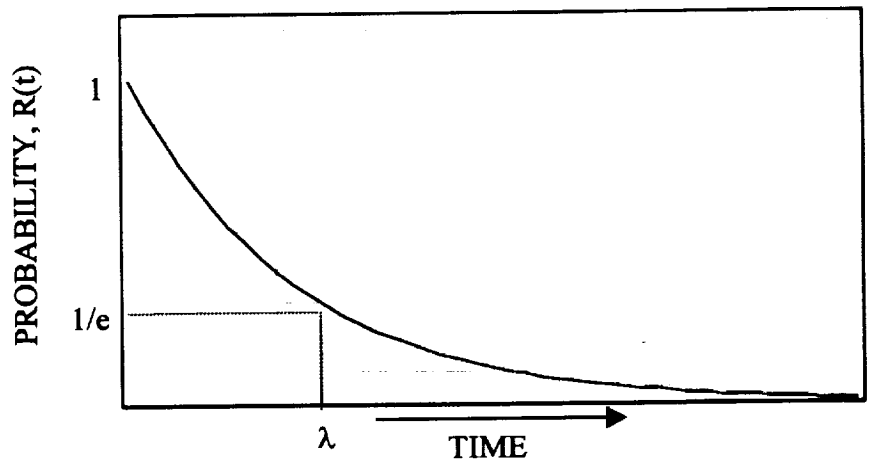


Figure 2-2: Probability of survival to time t.

II. Probability Models

Several standard probability models are often used to model failure of systems.

A. The Uniform Distribution

The uniform model is the most common probability model used to predict the lifetime of systems. For a system with multiple components with distinct MTTF and λs, it is often only possible to model the entire system as having a combined failure rate λ_c,

Assuming that the failure rate of a single component will constitute a total failure, then it is possible to directly determine λ_c by:

$$R(t) = \prod_{i=1}^{n} R_i(t) = e^{-\lambda_1 t} e^{-\lambda_2 t} \ldots = e^{-\left(\sum_{i=1}^{n} \lambda_i\right) t} \Rightarrow \tag{2-13a}$$

$$\lambda_c = \sum_{i=1}^{n} \lambda_i \tag{2-13b}$$

where λ_i = failure rate of the *i*th component of a system. A system that has any redundancy or error tolerance will be more difficult to model in detail, but generally, a series system will have a reliability determined by Equations 2-13. The pdf of this model is:

$$f(t) = \lambda_c e^{-\lambda_c t} \tag{2-14}$$

which is shown in Figure 2-2. This model is often the only available predictor of reliability for multi-component systems.

B. The Weibull Distribution

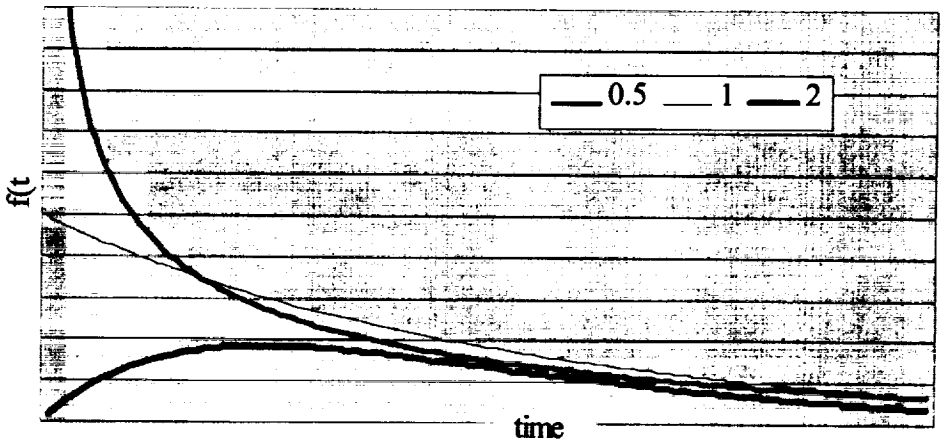


Figure 2-3: The pdf of the Weibull function with different b values.

In a system composed of n components, the probability of the first component failing is determined by:

$$F(t) = \prod_{i=1}^{n} F_i(t) \tag{2-15a}$$

where F_i is the probability of failure of the *i*th component. For systems where all components exhibit uniform failure rates, the probability of failure of the system can be expressed as:

$$F(t) = \left(1 - e^{-\lambda t}\right)^n \tag{2-15b}$$

This model is called the Weibull model. It is conventionally written as:

$$f(t) = \alpha^{\beta} \beta t^{\beta-1} e^{-(\alpha t)^{\beta}} \text{ and } \lambda(t) = \alpha^{\beta} \beta t^{\beta-1} \tag{2-16}$$

where

α = the scale parameter

β = the shape parameter

The shape parameter enables the Weibull distribution to model multiple aging trends:

- If $0 < \beta < 1$, then $\lambda(t)$ is decreasing with time
- If $\beta = 1$ then $\lambda(t)$ is constant ➔ the exponential model
- If $1 < \beta < \infty$ then $\lambda(t)$ is increasing with time.

For the Weibull distribution, the MTTF is given as:

$$MTTF = \frac{1}{\alpha} \Gamma\left(1 + \frac{1}{\beta}\right) \tag{2-17}$$

where Γ is the gamma function, which is defined as:

$$\Gamma(x) = \int_0^{\infty} t^{x-1} e^{-t} dt \text{ for } x>0 \tag{2-18}$$

C. The Normal Distribution

Physical data often fits a Normal, or Gaussian, distribution. This distribution is derived from the central limit theorem, which states that the distribution of a large number of random values usually results in a normal distribution, no matter what their individual distributions were.

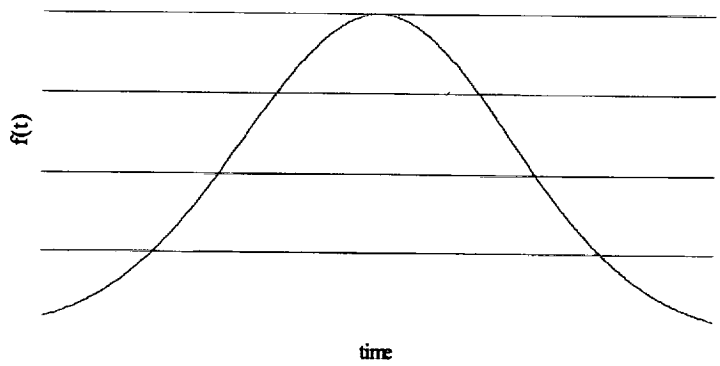


Figure 2-4: pdf of the normal distribution.

The normal distribution is expressed by the equation:

$$f(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\left(\frac{t-t_0}{2\sigma}\right)^2} \qquad (2\text{-}19)$$

where

σ = the standard deviation

t_0 = the MTTF

For this model, F(t) and R(t) are given by the respective error and complimentary error functions, Φ and 1-Φ. This function is usually approximated by

$$\Phi(z) = \frac{1}{\sqrt{2\pi}} e^{-\frac{z^2}{2}} \qquad (2\text{-}20)$$

D. The Lognormal Distribution

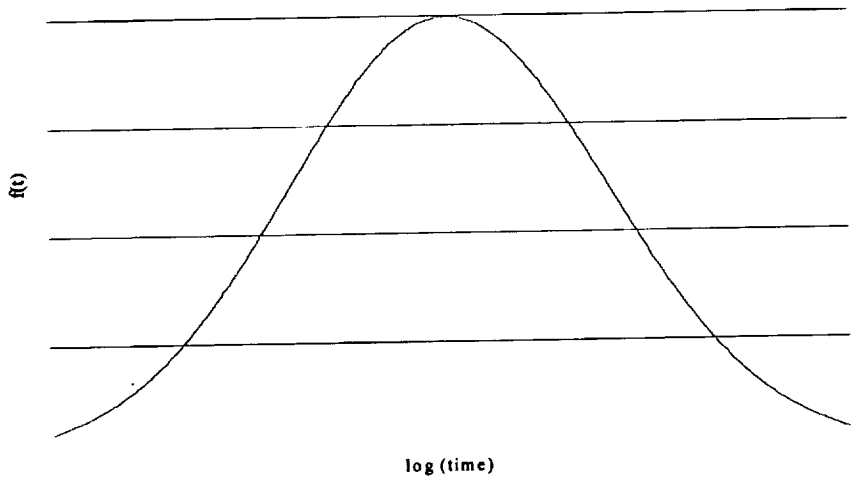


Figure 2-5: pdf of the lognormal distribution.

The logarithm of many failure times are found to be normally distributed in what has been termed a lognormal distribution. The physical justification for the lognormal model is that thermally activated systems will have a failure rate that is determined by the Arrhenius relation:

$$MTTF(T) = t_0 e^{-\left(\frac{E_a}{kT}\right)} \tag{2-21}$$

where:

E_a = the activation energy

k = Boltzmann constant (8.6×10^{-5} eV/K)

If the activation energy, E_a, is normally distributed in energy:

$$p(E) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(E-E_{a0})^2}{\sigma^2}}, \tag{2-22}$$

then the failure rate will have the form:

$$f(t) = \frac{1}{t\sigma\sqrt{2\pi}} e^{-\left(\frac{\ln(t-t_0)}{\sqrt{2}\sigma}\right)^2} \tag{2-23}$$

For this model, F(t) is given by

$$\Phi\left(\frac{\ln(t-t_0)}{\sigma}\right)$$

III. Application of Reliability Models

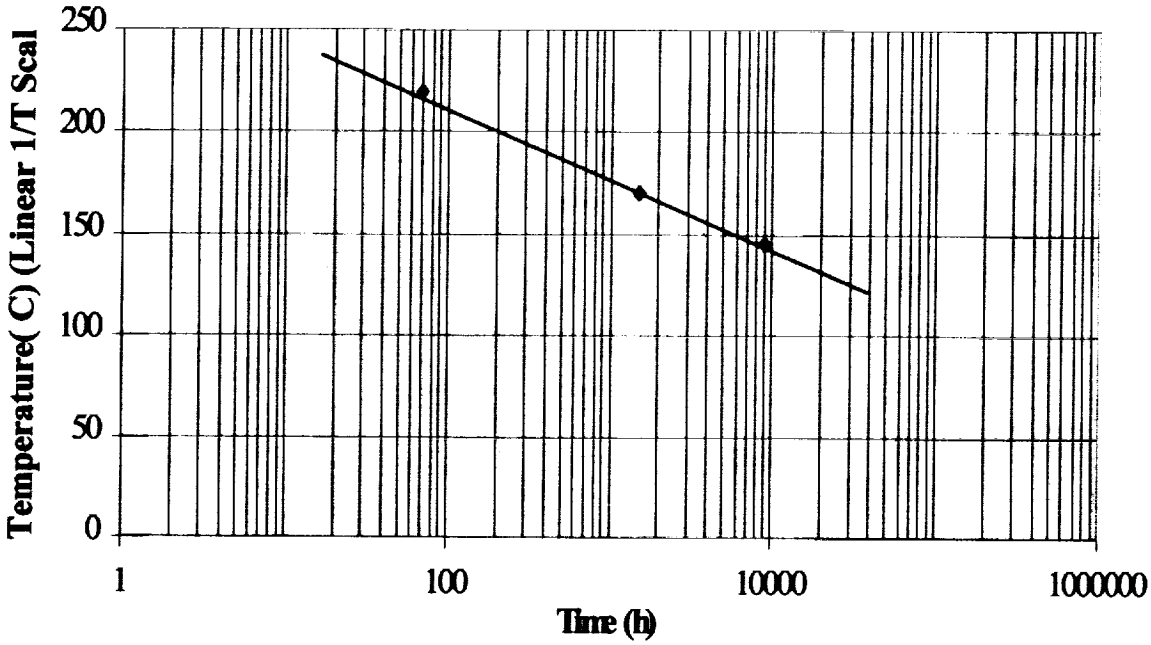


Figure 2-6: An example of using the lognormal distribution to predict lifetime in ICs. Each data point represents a life test and the line provides lifetime data at any given temperature.

While the above models offer a good basis for describing reliability, they must be accurately utilized to predict lifetime data. The simplest way to measure reliability is to submit a large number of samples to testing under normal operating conditions until failure occurs. However, since most high-rel applications utilize devices with lifetimes of several years, this approach is often too costly and time-consuming for most applications. Instead, devices are operated under accelerated conditions for a shorter period of time until failures occur and then, using probability theory, actual device lifetime is reconstructed.

While this kind of testing is relatively simple for purely electrical systems, it is significantly more difficult for MEMS, or for any mechanical system. Since failure mechanisms are not well understood, there is no simple test to accelerate lifetime. To further compound matters, the vast difference in types of MEMS devices means that each

set of devices may require unique acceleration conditions. These kinds of difficulties are not encountered in purely electrical systems because lifetime is determined almost exclusively by the rate of thermally activated processes. These interactions are easy to accelerate by increasing temperature. In MEMS, on the other hand, it may be temperature, humidity, vibration, or a number of other factors that limit device lifetime, and accelerating one failure mode may decelerate another.

Once life-test data is collected, it can be modeled with one of the above probability distributions. Take, for example, data that fits a lognormal distribution. This can be determined by plotting the data on a lognormal graph. If the life-test data fits into a straight line, then the data fits into a lognormal distribution. The intersection of this straight line with 50% cumulative failure indicates the MTTF.

To accurately predict lifetime at any operating conditions, at least three distinct high stress tests must be performed. The median lifetime from each of the three tests is then transferred onto a lognormal plot and fit with a line. Median life at any operating condition can then be determined.

In a world with limitless resources and time, lifetime test would be conducted with nearly infinite sample sizes. Since this is a practical impossibility, the size of the sample must be considered in determining the confidence in lifetime predictions. Confidence is expressed in terms of a percentage, where a confidence value says that for a given percentage of the time, a test would yield a result within the two limits of the test. Thus an upper and lower confidence of 90% on respective lifetimes of two and four years means that nine out of every ten tests would predict a lifetime between two and four years. The following equations yield confidence limits:[118]

$$\text{upper limit} = T_{test} \times e^{(t(df,\,alpha)\times\sigma/N)} \tag{2-24a}$$

$$\text{lower limit} = T_{test} \times e^{(-t(df,\,alpha)\times\sigma/N)} \tag{2-24b}$$

where

σ^2 = the standard deviation in the data

T_{test} = median life at test temperature

$t(df, alpha)$ = value from the Students' t distribution (see ref. [118] for more detail on this subject)

df = degrees of freedom (N-1)

$alpha$ = (1% confidence) / 2

N = sample size

Due to the variability of test data, it should be apparent that an understanding of failure mechanisms within MEMS is critical to determining device lifetime. This kind of information can only be determined from further research into MEMS reliability. As stated above, the diversity of MEMS technologies on the market almost necessitates an individualized approach to a statistical lifetime study. One of the great obstacles to space qualifying MEMS is the individuality of the devices. MEMS manufacturers do not have the luxury of ASIC and MMIC designers, who can use a great deal of prior work and knowledge in space qualifying their products. Despite these obstacles, it is inevitable that MEMS will eventually work their way into high-rel applications and this methodology will provide the means for realizing that goal.

IV. Failure

While this chapter has devoted a lot of time to quantifying reliability, it has not discussed the roots of reliability, namely failure. The time dependence of reliability, R, and failure, F, are complimentary, so the rates are both equal to the failure rate, λ. In order to accurately study MEMS reliability, the nature of failures must be quantified. Failure may be separated into two distinct categories:

(1) Degradation failure, which consists of device operation departing far enough from normal conditions that the component can no longer be trusted for reliable operation

(2) Catastrophic failures, which are, as the name implies, the complete end of device operation.

Failures occur when the stresses on a device exceed its strength. While the most prevalent failure mechanisms in MEMS are not yet fully understood, there is a great deal of knowledge about failure mechanisms within more common semiconductor devices, which should have a bearing upon failure within MEMS.

In order for a device to be classified as high-rel, it must meet some basic criteria. The most significant of these is that a device cannot exhibit a dominant failure mechanism. This ensures that there is no inherent design flaw that prohibits long-term reliable device operation. In order to make this assessment, the failure mechanisms with a device must be understood.[109]

The identification and mitigation of failure mechanisms in MEMS is both one of the most important and one of the newest issues in MEMS. The most relevant way to keep abreast of the failure mechanisms within MEMS is to search the current literature, as data contained within this manual is almost sure to be revised after publication. With this in mind, Chapter 3, "Failure Modes and Mechanisms" provides a description of the most commonly observed failure mechanisms and associated failure modes in MEMS.

V. Additional Reading

E. A. Amerasekera and F. N. Najm, Failure Mechanisms in Semiconductor Devices: Second Edition, John Wiley & Sons, New York, 1997.

C. C. Montgomery and G. C. Runger, Applied Statistics and Probability for Engineers, John Wiley & Sons: New York, 1994.

Chapter 3: Failure Modes and Mechanisms

B. Stark

A critical part of understanding the reliability of any system comes from understanding the possible ways in which the system may fail. In MEMS, there are several failure mechanisms that have been found to be the primary sources of failure within devices. In comparison to electronic circuits, these failure mechanisms are not well understood nor easy to accelerate for life testing. In any discussion of failures, the definition of failure mechanisms, or causes of failure, often overlaps with the definition of failure modes, or observable failure events. To alleviate this confusion this chapter has been roughly organized by failure modes, with mechanisms being described within the sections on the modes they cause. Failure mechanisms that do not have clearly associated modes are discussed at the end of this chapter.

I. Mechanical Fracture

Mechanical fracture is defined as the breaking of a uniform material into two separate sections. In MEMS it will usually lead to the catastrophic failure of a device, although there are some structures that will have more moderate performance degradations.[5,8] No matter what the actual outcome, any fracturing is a serious reliability concern. There are three types of fractures, ductile, brittle, and intercrystalline fracture. Ductile fracture, as the name implies, occurs in ductile materials. It is characterized by almost uninterrupted plastic deformation of a material. It is usually signified by the necking, or extreme thinning, of a material at one specific point. Brittle fracture occurs along crystal planes and develops rapidly with little deformation. Intercrystalline fracture is a brittle fracture that occurs along grain boundaries in polycrystalline materials, often beginning at a point where impurities or precipitates accumulate. For MEMS the latter two types of fracture are more common. To understand the actual causes of fracture and the methods for predicting it, several terms must be first defined.[27]

A. Definitions

Mechanical failure in a crystal lattice occurs when an applied stress exceeds the failure stress of the structure. Stresses are separated into the two categories of normal and shear stress. Normal stress is defined as stress perpendicular to a plane in a material, while shear stress occurs parallel to a plane, as shown in Figure 3-1. In solid materials, stress is linearly related to a concept called strain, which is the fractional elongation of a material. The proportionality constant between stress and strain is, for small normal

loads, called the modulus of elasticity, or Young's modulus. The actual deformation of a cubic volume will depend upon all the stresses applied to it:

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{xy} \\ \tau_{xz} \\ \tau_{yz} \end{bmatrix} = \begin{bmatrix} E_{11} & E_{12} & E_{13} & E_{14} & E_{15} & E_{16} \\ E_{21} & E_{22} & E_{23} & E_{24} & E_{25} & E_{26} \\ E_{31} & E_{32} & E_{33} & E_{34} & E_{35} & E_{36} \\ E_{41} & E_{42} & E_{43} & E_{44} & E_{45} & E_{46} \\ E_{51} & E_{52} & E_{53} & E_{54} & E_{55} & E_{56} \\ E_{61} & E_{62} & E_{63} & E_{64} & E_{65} & E_{66} \end{bmatrix} \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{xz} \\ \varepsilon_{yz} \end{bmatrix}$$

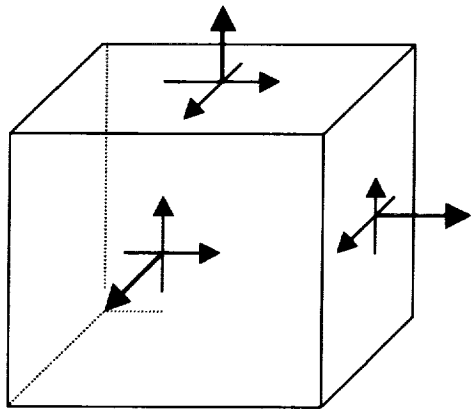
where

σ = normal stress

τ = shear stress

ε = strain

E = Elastic Modulus



One important aspect of this tensor is that $E_{ij}=E_{ji}$, so that there are actually only 21 independent constants. Further simplifying this effect is the internal symmetry of most crystals. In cubic crystals, such as Si and GaAs, the tensor reduces to:

$$\begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{xy} \\ \tau_{xz} \\ \tau_{yz} \end{bmatrix} = \begin{bmatrix} E_{11} & E_{12} & E_{12} & 0 & 0 & 0 \\ E_{12} & E_{11} & E_{12} & 0 & 0 & 0 \\ E_{12} & E_{12} & E_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & E_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & E_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & E_{44} \end{bmatrix} \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{xz} \\ \varepsilon_{yz} \end{bmatrix} \tag{3-1b}$$

While not all materials have just three independent elastic constants, it is unlikely to find even highly anisotropic crystals with more than nine elastic constants.

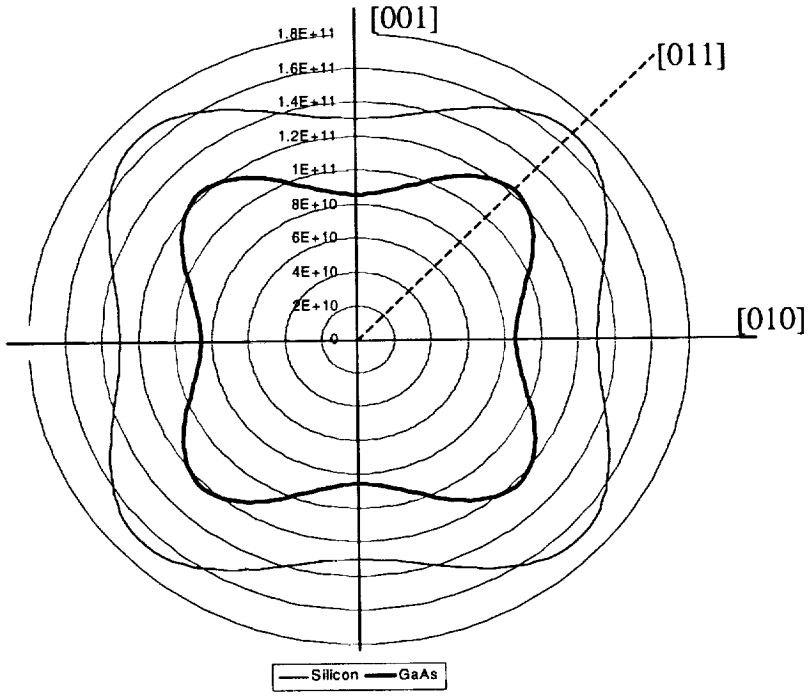


Figure 3-2: Young's modulus as a function of crystalline orientation for Si and GaAs along the <100> axis.

One of the difficulties in using Equation 3-1b is that, in an anisotropic crystal, the elastic modulus will vary with crystalline orientation. To account for this variation a plane modulus is defined with the crystal orientation by

$$E_{[hkl]} = \frac{\sigma_{[hkl]}}{\varepsilon_{[hkl]}} \tag{3-2}$$

In order to relate the modulus of a crystalline plane to the elastic constants in Equations 3-1, the following equation is used:

$$E^{-1}(\theta,\phi,\psi) = s_{11} - 2(s_{11} - s_{12} - 0.5s_{44})(l_1^2 l_2^2 + l_2^2 l_3^2 + l_1^2 l_3^2)) \qquad (3\text{-}3)$$

where

$$s_{11} = \frac{E_{11} + E_{12}}{(E_{11} + 2E_{12})(E_{11} - E_{12})}$$

$$s_{12} = \frac{-E_{12}}{(E_{11} + 2E_{12})(E_{11} - E_{12})}$$

$$s_{44} = \frac{1}{E_{44}}$$

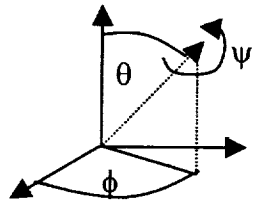


Figure 3-3: Euler's angles.[91] These are the angles formed between the <100> axis and an arbitrary <hkl> axis.

θ, ϕ, ψ = Euler's angles, defined in Figure 3-2

l_1, l_2, l_3 = the direction cosines defined by the following matrix

$$\begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} = \begin{bmatrix} \cos(\theta)\cos(\phi)\cos(\psi) - \sin(\phi)\sin(\psi) & \cos(\theta)\sin(\phi)\cos(\phi) - \sin(\phi)\sin(\psi) & -\sin(\theta)\cos(\psi) \\ -\cos(\theta)\cos(\phi)\sin(\psi) - \sin(\phi)\sin(\psi) & -\cos(\theta)\sin(\phi)\cos(\phi) - \sin(\phi)\sin(\psi) & \sin(\theta)\sin(\psi) \\ \cos(\theta)\cos(\phi) & \cos(\theta)\cos(\phi) & \cos(\theta) \end{bmatrix}$$

The modulus of Si and GaAs as a function of crystalline orientation is shown in Figure 3-2.[32]

In common nomenclature the constants, s_{11}, s_{12}, and s_{44} are called compliance coefficients. This equation reveals that the {100} planes of Si have an elastic modulus of 130 GPa, while the {110} planes have a modulus of 165 GPa. For the {111} planes, with a θ and ϕ angle of 45° and a ψ angle of 0°, the value of $E_{\{111\}}$ is 187 GPa, which is the stiffest plane in silicon. As a result, wear effects will be most severe in the[100] direction because it has the lowest stiffness of any crystal planes in silicon. It must also be noted that E_{11}, E_{12}, and E_{44} are usually defined relative to the <110> planes, while s_{11}, s_{12}, and s_{44} are generally defined relative to the <100> planes.

Poisson's ratio is also orientation-dependent, with the basis vector given along with the value of the number. Poisson's ratio is normally defined in terms of the elastic compliance coefficients as $\nu = -s_{12}/s_{11}$. If a longitudinal stress is considered in a direction that is displaced from the {100} planes by angles θ, ϕ, and ψ, it has been proven [48,49] that

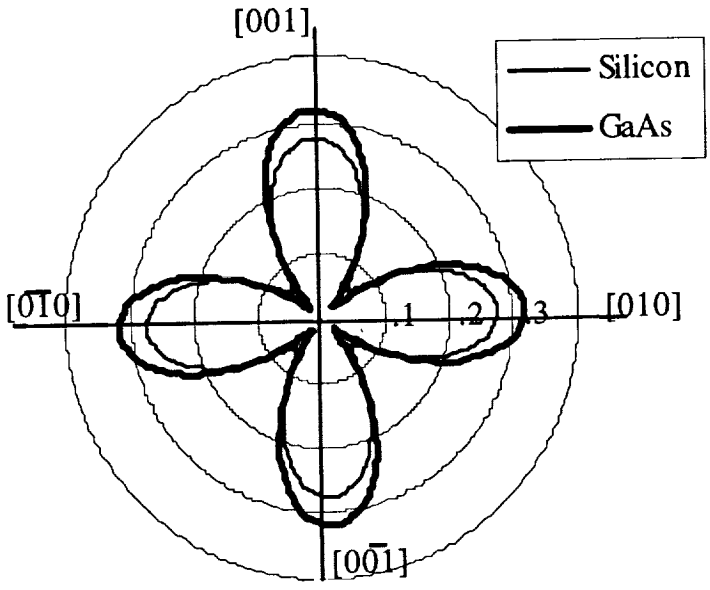


Figure 3-4: Poisson's ratio as a function of angle in the (100) plane with l and m varying in the (100) plane.

$$\nu = -\frac{s_{12} + (s_{11} - s_{12} - .5s_{44})(l_1^2 m_1^2 + l_2^2 m_2^2 + l_3^2 m_3^2)}{s_{11} - 2(s_{11} - s_{12} - .5s_{44})(l_1^2 l_1^2 + l_2^2 l_3^2 + l_1^2 l_3^2)} \tag{3-4}$$

While these considerations are important in the study of MEMS, they are difficult to resolve analytically. For simplicity's sake, researchers design structures that will only be forced in orthogonal directions, so that Young's modulus and Poisson's ratio can be treated as uniform values. For this reason, the remainder of this guideline will treat Young's Modulus and Poisson's ratio as a single value, with the implicit understanding that these quantities are actually dependent upon crystal structure.

Once the definitions of stress and strain are understood, it is possible to understand how stress leads to failure.

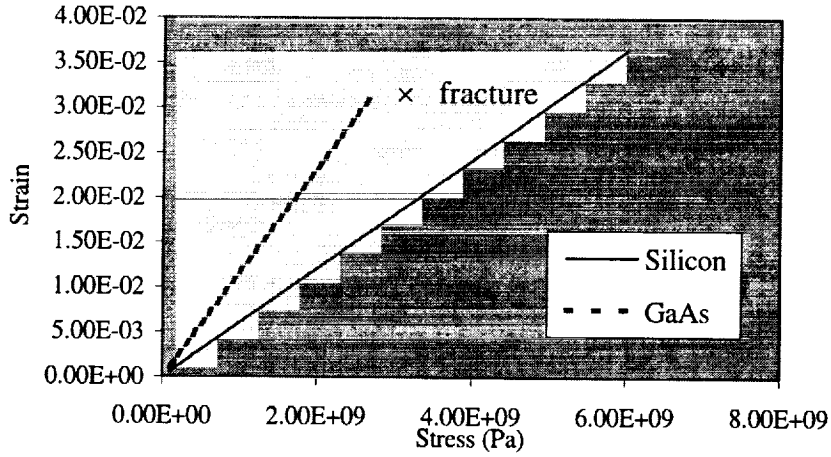


Figure 3-5: Stress versus strain relationships for bulk Si and GaAs[1].

B. Stress-Induced Failure

In Figure 3-2, the process of crystal lattice failure is illustrated through a diagram of stress versus strain. As can be seen, the application of stress causes a linear increase in strain until fracture. This is a function of the brittle properties of these materials; brittle materials deform elastically until fracture occurs. To understand the fracture tolerances of a MEMS device, as in any mechanical structure, one needs to determine the maximum stresses.

The maximum stress in a device usually occurs near stress risers, or concentrators. Stress concentration occurs when there is a sudden change in the cross section of a material. At these points, stress is usually non-uniformly distributed and somewhat difficult to analytically resolve. Since most engineers are more concerned with maximum stress rather than average stress, this value can be calculated by defining the stress concentration factor K as:

---

[1] This chart is idealized. In actuality there is a small curvature to the stress strain curve of any material.

$$K = \frac{\sigma_{max}}{\sigma_{ave}} \tag{3-5}$$

where

σ_{max} = maximum stress at a stress concentration point

σ_{ave} = average stress at a stress concentration point

K is a function of the geometry of the stress riser and is typically graphically represented. σ_{ave} can be calculated from basic structural analysis, which allows σ_{max} to be determined.

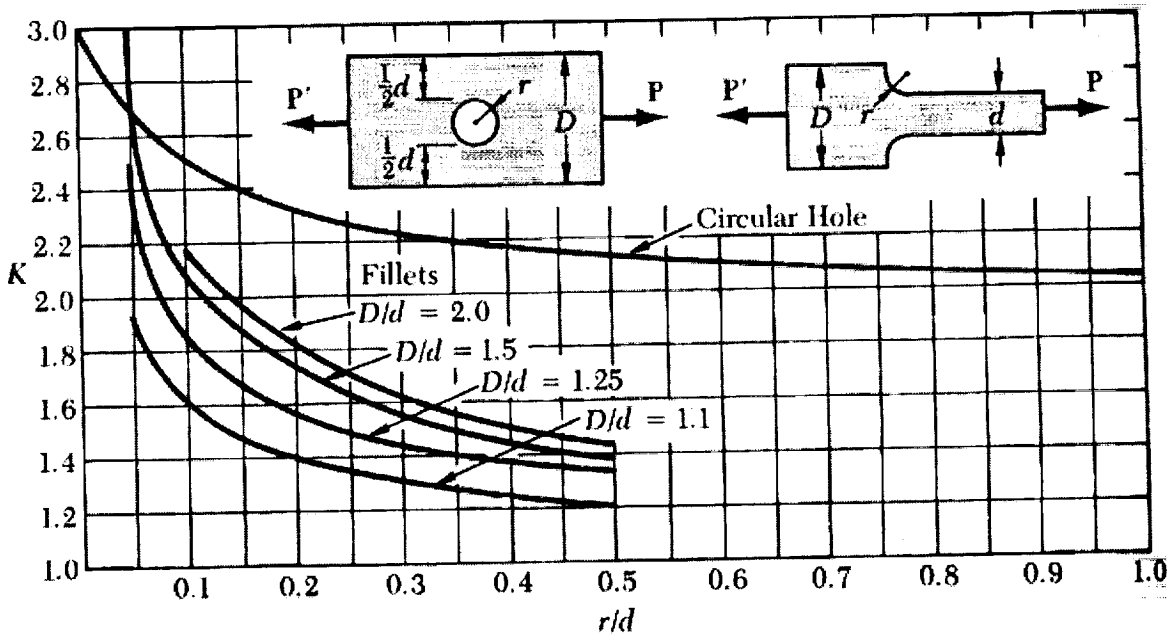


Figure 3-6: Stress concentration factor as a function of geometry for thin beams. (from [11])

While analysis of stress will determine if a material has exceeded its fracture strength, some new concepts will have to be introduced to understand what factors limit the strength of materials. Many of the mechanical failures in crystalline solids occur as the result of defects in crystal structures. These defects are the result of imperfect techniques in crystal growth and are critically important to the study of the properties of crystals. While a modern silicon wafer will have relatively few defects,[46] other materials used in MEMS have significant defect densities. There are several kinds of defects that need to be examined.

C. Point Defects

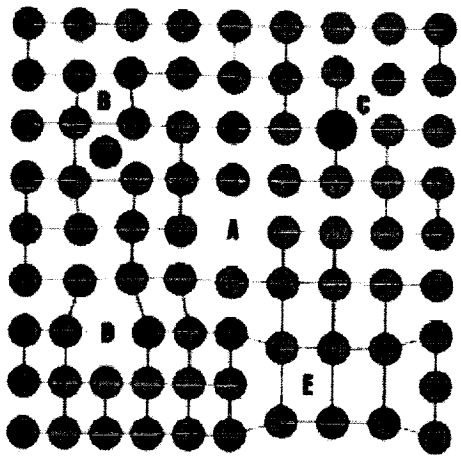


Figure 3-7: Different point defects. A is a vacancy, B is an interstitial. C is a Point replacement while D and E are 2-D mappings of an edge and screw dislocation, respectively.

Point defects are faults at a single point in a crystal. They tend to create very localized internal strains and do not usually have the magnitude of an impact upon crystal lattice integrity that is common to dislocations, which are discussed in the following section. Point defects are categorized into the following groups:

i) Vacancies

A vacancy is the lack of an atom at a specific point in a lattice where one would otherwise be expected. This has the result, as most defects do, of limiting electron mobility. More important for MEMS is the fact that a vacancy will lower the yield strength of the material, as it weakens the lattice strength. The missing atom causes the lattice to compress around the vacancy, which creates an internal stress field that is described by Equation 3-5.

$$\sigma_{rr} = -2\sigma_{\varphi\varphi} = -2\sigma_{\theta\theta} = \frac{g_0}{\pi}\frac{1-2\nu}{1-\nu}\frac{1}{r^3} \tag{3-6}$$

where

$$g_0 = 2G\Delta V\frac{1-\nu}{1-2\nu}$$

G = the shear modulus of a material (E_{44} for cubic crystals)

ΔV = the change in the volume of the solid due to the vacancy.

ii) Interstitial

An interstitial is an additional atom which has become wedged between the atoms of a lattice. An interstitial will have, to a first order approximation, the same stress field as a vacancy, except that the strength factor, g_0, becomes

$$g_0 = \frac{8\pi G}{3}\frac{1+\nu}{1-2\nu}\eta r_0^3 \tag{3-7}$$

where

$$\eta \approx \frac{r_0}{A} - 1$$

r_0 = the radius of the foreign atom

A = the lattice parameter

iii) Point Replacement

In this case a single atom has been replaced by an atom of a different element. Often this is done intentionally for doping purposes, but sometimes it occurs accidentally as the result of disorder in the lattice or impurities in the melt. Theses defects will have differing effects on the mechanical properties of solids, but will usually not be as large in magnitude as vacancies or interstitials.[53]

D. Dislocations

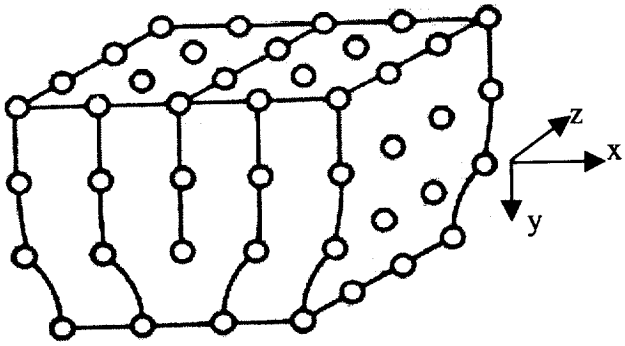


Figure 3-8a: Edge dislocation. (from [37])

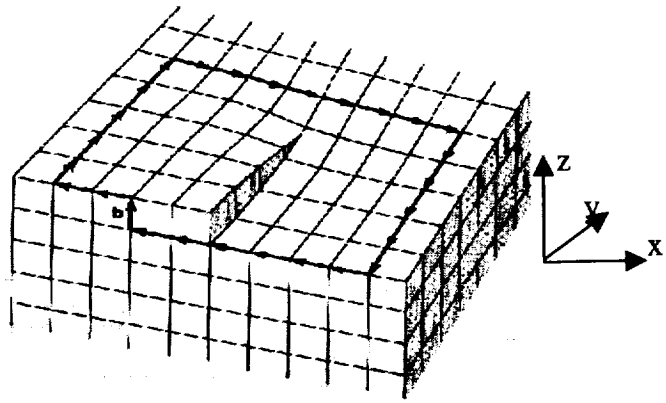


Figure 3-8b: Screw dislocation. (from [37])

A dislocation is a one-dimensional array of point defects in an otherwise perfect crystal. They occur when a crystal is subjected to stresses that exceed the elastic limits of materials. Dislocations are usually introduced into a crystal through the presence of a temperature gradient during crystal growth. Modern wafer processing techniques produce extremely low dislocation densities on wafers. Dislocations can be separated into two types:

i) Edge Dislocation

In this case a whole row of atoms is out of phase with respect to the rest of the lattice, as shown in Figure 3-8a. The result of this phenomenon is a physical barrier in the crystal that scatters electrons and weakens the crystal. An edge dislocation creates a stress field that is defined by Equations 3-8a-e:

$$\sigma_x = \frac{Gb}{2\pi(1-\nu)} \frac{y(3x^2 + y^2)}{(x^2 + y^2)^2} \tag{3-8a}$$

$$\sigma_y = \frac{Gb}{2\pi(1-\nu)} \frac{y(x^2 - y^2)}{(x^2 + y^2)^2} \tag{3-8b}$$

$$\sigma_z = \nu(\sigma_x + \sigma_y) \tag{3-8c}$$

$$\tau_{xy} = -\frac{Gb}{2\pi(1-\nu)} \frac{x(x^2 - y^2)}{(x^2 + y^2)^2} \tag{3-8d}$$

$$\tau_{xz} = \tau_{yz} = 0 \tag{3-8e}$$

where

x, y, z = distance from edge dislocation, with the dislocation in the plane of x and the z axis is tangent to the dislocation.

b = The magnitude of the Burgers vector of the dislocation ~ a few lattice spacings.

ii) Screw Dislocation

This fault is much the same as an edge dislocation except that it is shaped like a spiral staircase, as shown in Figure 3-8b. Screw dislocations also create stress fields in solids, as defined below:

$$\tau_{xz} = \frac{Gb}{2\pi} \frac{y}{x^2 + y^2} \tag{3-9a}$$

$$\tau_{yz} = -\frac{Gb}{2\pi} \frac{x}{x^2 + y^2} \tag{3-9b}$$

$$\sigma_x = \sigma_y = \sigma_z = \tau_{xy} = 0 \tag{3-9c}$$

The essential feature to recognize from these equations is that dislocations introduce stresses internal to materials that will significantly weaken crystal lattices. While these stresses decrease quadratically with distance from the dislocation, there clearly will be a strong local internal stress created by these features. Another factor to consider is that the stress fields from different dislocations will interact, creating internal forces. From a MEMS reliability standpoint, this means that using high quality wafers with smaller numbers of dislocations will ultimately increase device reliability and lifetime. For more information on this subject, Reference [37], "Elementary Dislocation Theory" by Weertman and Weertman offers a good, in-depth discussion of dislocation theory.

E. Precipitates

In metals containing another element in a supersaturated solid solution, this solution tends to precipitate in the form of a compound with the solvent metal.[53] In the presence of a dislocation, atoms will precipitate into the dislocation, which will occur at the rate:

$$n(t) \propto \left(\frac{t}{T}\right)^{2/3} \tag{3-10}$$

where

n(t) = the number of atoms precipitating in a time, t.

T = temperature

This phenomenon is used to harden materials by allowing precipitates to lock dislocation and prevent them from moving through the lattice. While this is found to be useful in construction materials, it creates problems for MEMS devices using metallic compounds, such as GaAs. The formation of precipitates creates an internal stress, which can significantly weaken crystal lattices and is discussed in great detail in Reference [53].

F. Fracture Strength

The impetus for studying defects is that, for brittle materials, the fracture strength is a function of the largest crystal defect. For a defect of length c, the fracture strength can be determined by:[114]

$$\sigma_F = \frac{K_{Ic}}{Y\sqrt{c}} \tag{3-11}$$

where

K_{Ic} = Fracture toughness

σ_f = fracture strength

Y = dimensionless parameter that depends on the geometry of the flaw

It is sometimes useful to approximate the defect as being penny shaped with a radius, c, in which case the fracture strength is:[17]

$$\sigma_F = \frac{1.6K_{Ic}}{\sqrt{\pi c}} \tag{3-12}$$

Normally, a Gaussian distribution of crystal defects is assumed for a given volume. This would imply that there is also a normal distribution of fracture strengths, as described below:

$$f(\sigma) = (2\pi d^2)^{-1/2} e^{-\frac{(\sigma-\bar{\sigma})^2}{2d^2}} \tag{3-13}$$

where

d^2 = standard deviation in fracture strength

$\bar{\sigma}$ = mean fracture strength

For this kind of fracture stress distribution, the probability of failure of a body exposed to a stress field is modeled by the Weibull probability distribution function of:

$$P_f = 1 - e^{-\int_V \left(\frac{\sigma-\sigma_u}{\sigma_0}\right)^m dv} \text{ [40]} \tag{3-14}$$

where

V = the volume of the stressed body

σ_u = a lower stress limit which is usually equal to zero in brittle materials (Pa)

σ_0 = a parameter related to the average fracture stress (Pa)

m = the Weibull modulus, a measure of the statistical scatter displayed by fracture events

For simple geometries, Equation 3-14 can be simplified to:

$$\ln\left[\ln\left(\frac{1}{1-P_f}\right)\right] = m\ln\sigma + const \tag{3-15}$$

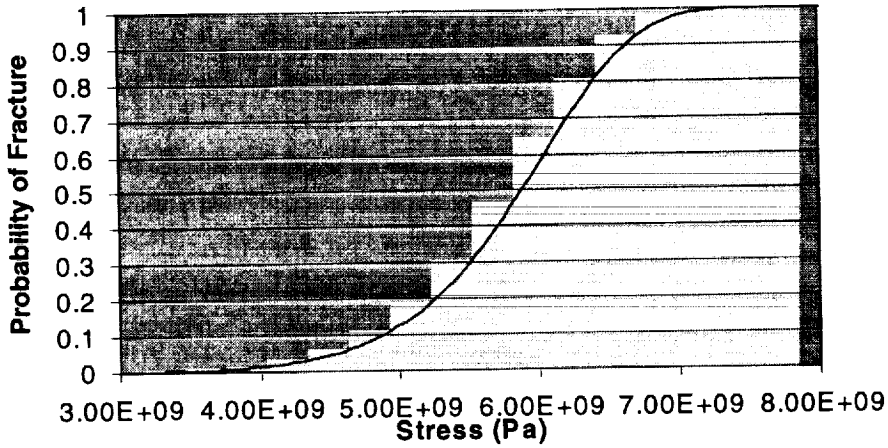


Figure 3-9: Representative plot of the probability of the fracture of silicon under applied stress.

The Weibull modulus, which can be used to measure the reliability of an engineering material, can be determined by a linear curve fit on a simple ln/ln-ln plot. Thus, the probability of fracture will be randomly distributed by a Weibull model, as shown in Figure 3-9. As such, the fracture strength of a material can only be expressed as a probability distribution and not as a specific value, which presents a challenge for reliability engineers. Since it is not known what the ultimate failure strength of a device will be, testing must be done on all devices prior to insertion into the market to eliminate devices with unacceptably low fracture strengths.

For common MEMS materials, several fracture studies have been conducted. The median fracture strength of silicon beams has been reported to be on the order of 6 GPa with a Weibull modulus of 10.1, although these values are strongly dependent upon the finished composition of the beam.[40] GaAs had a fracture strength of less than half that

of silicon, at 2.7 GPa. These values compare favorably to construction steel, which fractures under 1 GPa. While this study provides a baseline for the strength of Si and GaAs, they are not universally applicable. Fracture studies need to be conducted on every process, as mechanical properties of materials are highly dependent on processing conditions.

G. Fatigue

Fatigue is a failure mechanism caused by the cyclic loading of a structure below the yield or fracture stress of a material. This loading leads to the formation of surface microcracks that cause the slow weakening of the material over time and create localized plastic deformations. While brittle materials do not experience macroscopic plastic deformation, they will still experience fatigue, albeit in a much longer time frame than in ductile materials.

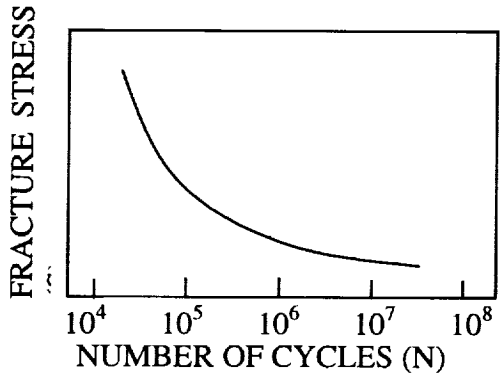


Figure 3-10: Typical SN curve for a ductile material.

Fatigue is typically modeled with a plot known as the SN curve. The plot, shown in Figure 3-11, relates the fracture stress, S, to the number of cycles of loading and unloading a material. As shown in the figure, the fracture stress decreases with time and can eventually fail.

Fatigue also causes a gradual change in the properties of a material. After repeated cycling, which is often on the order of billions of cycles, Young's modulus will gradually shift. This shift will change the resonant frequency of many devices and degrade sensor outputs. Also affected is the dampening coefficient, which will increase over time and change the resonant frequency and Q factor of a structure. Electrical resistance of many structures will also increase over time. The combined effect of these changes can lead to degradation failure. Table 3-1 provides order-of-magnitude estimates in the changes that might be expected in these values over the lifetime of a device.[95]

Property	P+ Silicon		P+ Silicon coated with aluminum		P+ Silicon coated with nitride		P+ Silicon coated with oxide	
	original	aged	original	aged	original	aged	original	aged
Young's Modulus (GPa)	129	136	117	113	134	125	127	123
Dampening Coefficient (Hz)	600	770	741	779	436	588	631	685
Resistance (Ω)	9.9	15.3	19.9	22.7	4.93	9.55	10.3	12.5

Table 3-1: Fatigue induced materials degradations.[95]

While this table is only indicative of one study, it does show that fatigue is a real concern for MEMS.

II. Stiction

One of the biggest problems in MEMS has been designing structures that can withstand surface interactions. This is due to the fact that, when two polished surfaces come into contact, they tend to adhere to one another. While this fact is often unimportant in macroscopic devices, due to their rough surface features and the common use of lubricants, MEMS surfaces are smooth and lubricants create, rather than mitigate, friction.[19] As a result, when two metallic surfaces come into contact, they form strong primary bonds, which joins the surfaces together. This is analogous to grain boundaries within polycrystalline materials, which have been found to be often stronger than the crystal material itself. However, adhesive boundaries are usually not as strong as grain boundaries, due to the fact that the actual area of contact is limited by localized surface roughness and the presence of contaminants, such as gas molecules.

Adhesion is caused by van der Waals forces bonding two clean surfaces together. The van der Waals force is a result of the interaction of instantaneous dipole moments of atoms. If two flat parallel surfaces become separated by less than a characteristic distance of z_0, which is approximately 20 nm, the attractive pressure will be:

$$P_{vdw} = \frac{A}{6\pi d^3} \text{ [110]} \qquad (3\text{-}16)$$

where

A = Hamaker constant (1.6 eV for Si)

d = the separation between the surfaces

While this equation, since it ignores the repulsive part of surface forces, overestimates the force of adhesion by at least a factor of 2, it is a good order of magnitude approximation for adhesive forces. Typical values of d are on the order of several Ångstroms.

In most MEMS devices, surface contact causes failure. With the noted exception of the small contact areas in microbearings, when surfaces come into contact in MEMS, the van der Waals force is strong enough to irrevocably bond them. Although some devices, such as microswitches, are designed to combat this problem through strong actuator networks, most devices must be designed to eliminate any surface interactions, in order to avoid the effects shown in Figure 3-11.

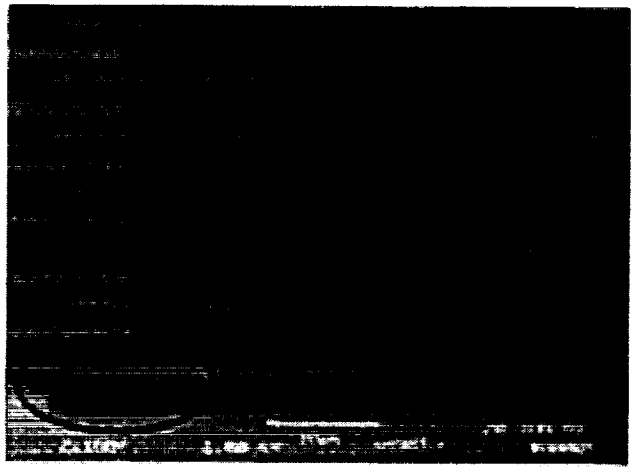


Figure 3-11: Polysilicon cantilever adhering to substrate.

III. Wear

Wear is an event caused by the motion of one surface over another. It is defined as the removal of material from a solid surface as the result of mechanical action.[27] While there are some mechanical operations, such as polishing and sharpening, that utilize wear in a constructive manner, wear is generally considered an undesirable effect in MEMS. There are four main processes that cause wear. They are called adhesion, abrasion, corrosion, and surface fatigue.

Adhesive wear is caused by one surface pulling fragments off of another surface while they are sliding. This is caused by surface forces bonding two materials together. When the bonds break, they are unlikely to separate at the original interface, which

fractures one of the materials. The volume of a material fractured by adhesive wear is determined by the relationship:[27]

$$V_{AW} = \frac{k_{AW} F x}{3\sigma_y} \tag{3-17}$$

where

σ_y = yield strength of the material

k_{AW} = material dependent wear constant

x = sliding distance

F = load on the material

k_{AW} is material dependent. Several useful approximations have been developed for non-metallic wear between different types of materials:

	Nonmetal on identical nonmetal	*Nonmetal on like nonmetal*	*Nonmetal on unlike nonmetal*	*Layer-lattice nonmetal on unlike material*
Unlubricated	1.8×10^{-5}	9×10^{-6}	4.5×10^{-6}	1.5×10^{-6}
Poor lubricant	6×10^{-6}	3×10^{-6}	1.5×10^{-6}	6×10^{-7}
Good lubricant	3×10^{-6}	1.2×10^{-6}	6×10^{-7}	3×10^{-7}
Excellent lubricant	1.5×10^{-6}	6×10^{-7}	3×10^{-7}	9×10^{-8}

Table 3-2: Wear coefficients for nonmetals[1].[120]

As a general rule, adhesive wear will be minimized with dissimilar hard materials.

Initial studies on the long-term effects of adhesive wear have been completed, with some interesting results being discovered. A study at Sandia National Laboratories found that wear related failures had a high initial infant mortality rate, followed by a decreasing failure rate over time. An interesting part of their discovery was that both the lognormal and the Weibull model of failure rates described wear equally well. While this seems a bit counterintuitive, upon close inspection both of these models have fairly similar shapes of probability density and cumulative distribution functions over the ranges in question.

[1] Traditionally the factor of 3 is dropped from Equation 3-15 and these values are expressed as 1/3 of the values in this chart.

Abrasive wear occurs when a hard, rough surface slides on top of a softer surface and strips away underlying material. While less prevalent in MEMS than adhesive wear, it can occur if particulates get caught in microgears and can tear apart a surface. Also defined by Equation 3-15, the constant k_{AW} for abrasive wear is usually on the order of 10^{-3} to 10^{-6}.

Corrosive wear occurs when two surfaces chemically interact with one another and the sliding process strips away one of the reaction products. This type of wear could cause failure in chemically active MEMS. Certain types of microfluidic systems and biological MEMS are susceptible to corrosive wear. Corrosive wear is dependent upon the chemical reactions involved, but it can be modeled as:

$$h_{CW} = \frac{k_{CW} x}{3} \tag{3-18}$$

where

h_{CW}= depth of wear

k_{CW} = corrosive wear constant, on the order of 10^{-4} to 10^{-5}

Surface fatigue wear occurs mostly in rolling applications, such as bearings and gears. It affects highly polished surfaces that roll instead of sliding. Over time, the continued stressing and unstressing of the material under the roller will cause the appearance of fatigue cracks. These cracks then propagate parallel to the surface of a structure, causing material to flake off the surface. Surface fatigue wear tends to generate much larger particles than other wear mechanisms, with flakes as large as 100 nm being common in macroscopic applications.[27]

In many actuator technologies, wear will increase the voltage required to drive a device. Due to the polishing of the contact surfaces caused by wear, the adhesive forces will increase. The increase in adhesion will require larger input signals to drive a device. The increase in drive signal will, in-turn, increase to force, and thus wear, on a structure. As a result, many structures that have contact surfaces prone to wear, will experience a positive feedback loop between wear and driving voltage that will eventually lead to the catastrophic failure of a device. Either the increase in voltage will create a power drain that exceeds the available power to the system or the increase in voltage will decrease the stability of the actuator until stiction occurs.

IV. Delamination

Delamination is a condition that occurs when a materials interface loses its adhesive bond. It can be induced by a number of means, from mask misalignments to particulates on the wafer during processing. It can also arise as the result of fatigue

induced by the long term cycling of structures with mismatched coefficients of thermal expansion.

No matter what the actual cause, the effects of delamination can be catastrophic. If the material is still present on the device, it can cause shorting or mechanical impedance. Furthermore, the loss of mass will alter the mechanical characteristics of a structure. While the exact changes will depend upon the amount of material that has fallen off, recent work[87] has reported shifts of up to twenty five percent in resonant frequency in some devices.

V. Environmentally Induced Failure Mechanisms

In addition to device operation, there are external effects that can also cause failure in MEMS. Many environmental factors can lead to the development of failure modes. As discussed in the next section, environmental failure mechanisms are one of the biggest challenges facing the insertion of MEMS into space.

A. Vibration

Vibration is a large reliability concern in MEMS. Due to the sensitivity and fragile nature of many MEMS, external vibrations can have disastrous implications. Either through inducing surface adhesion or through fracturing device support structures, external vibration can cause failure. Long-term vibration will also contribute to fatigue. For space applications, vibration considerations are important, as devices are subjected to large vibrations in the launch process.

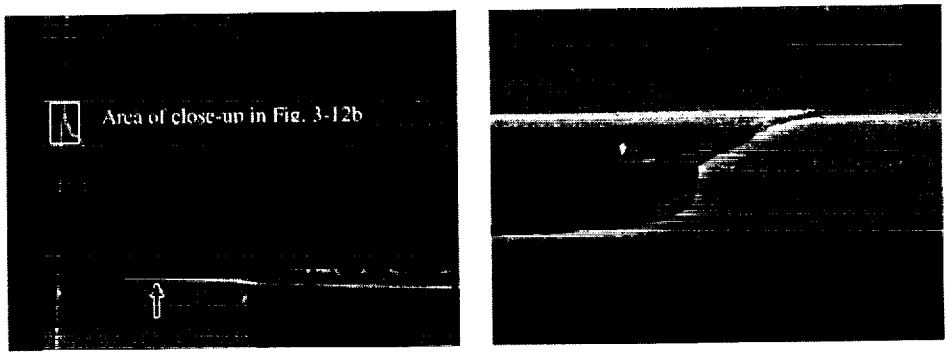


Figure 3-12 (a, b): Cracks in single crystal silicon support beams caused by vibrations from a launch test.[5]

B. Shock

Shock differs from vibration in that shock is a single mechanical impact instead of a rhythmic event. Shock creates a direct transfer of mechanical energy across the device.

Shock can lead to both adhesion and fracture. Shock can also cause wire bond shearing, a failure mode common to all semiconductor devices.

C. Humidity Effects

Humidity can be another serious concern for MEMS. Surface micromachined devices, for reasons related to processing, are extremely hydrophilic. In the presence of humidity, water will condense into small cracks and pores on the surface of these structures. When the surface equalizes with the atmosphere there will be a curved meniscus of liquid on the surface, with the two radii of curvature of the meniscus, r_1 and r_2, determined by the expression:

$$\left(\frac{1}{r_1}+\frac{1}{r_2}\right)^{-1} = \frac{\gamma v}{RT\log\left(P/P^{sat}\right)} \tag{3-19}$$

where

γ = surface tension

v = molar volume

P/P^{sat} = relative vapor pressure of water in the atmosphere

R = gas constant (1.98719 cal/mol-K)

T = temperature

Recent work has shown that condensation on surface micromachined surfaces will lead to an increase in residual stress in the structures.[28] For two surfaces that come into close proximity with each other, the condensation will also create a capillary pressure between the surfaces equal to:

$$P_{cap} = \frac{4\gamma r_1 \cos^2(\theta)}{d^2} \tag{3-20}$$

where

d = the separation between the two plates

θ = contact angle between the surfaces and the liquid

Thus, a hydrophilic surface in a humid atmosphere will experience both condensation, which will create bending moment in structures, and capillary forces, which will create stronger adhesive bonds than Van der Waals forces alone.[110,114]

D. Radiation Effects

While still in its infancy, the field of radiation effects on MEMS is becoming increasingly important. It has long been known that electrical systems are susceptible to radiation and recent research has raised the possibility that mechanical devices may also be prone to radiation-induced damage. Especially sensitive to radiation will be devices that have mechanical motion governed by electric fields across insulators, such as electrostatically positioned cantilever beams. Since insulators can fail under single event dielectric rupture, there is a distinct possibility that these devices will have decreased performance in the space environment. A further complication is the fact that radiation can cause bulk lattice damage and make materials more susceptible to fracture.

Recent work indicates that dielectric layers will trap charged particles, creating a permanent electric field. This permanent field will change resonant characteristics and alter the output of many sensors.[122,123] This may indicate that radiation-tolerant designs will have to limit the use of dielectrics, which could be a challenging design problem. One radiation issue that has received some notice without generating a lot of research is the impact of large atomic mass particles on MEMS. It is known that high Z radiation can lead to fracturing by creating massive disorder within the crystal lattice. Since this radiation source is common in the space environment, it needs to be investigated before MEMS to launch into space.

On one of the few radiation tests to date, one group of surface micromachined devices exposed to gamma ray doses in excess of 25 krad had severe performance degradation. While certainly this reveals no substantive information about the overall radiation tolerance of MEMS as a technology, it raises the possibility that radiation can cause failure within these devices. While more studies need to be conducted before any conclusions can be made, it is important to understand that radiation effects in MEMS is a non-trivial issue that has yet to be fully addressed.[13]

E. Particulates

Particulates are fine particles, that are prevalent in the atmosphere. These particles have been known to electrically short out MEMS and can also induce stiction. While these particles are normally filtered out of the clean room environment, many MEMS are designed to operate outside the confines of the clean room and without the safety of a hermetically sealed package. As a result, devices must be analyzed to ensure that they are particle-tolerant before they can be used as high-rel devices in environments with high particulate densities.

Another area in which contaminants cause problems is in adhesion. Proper device processing requires most materials interfaces to be clean in order to have good adhesion. If dust particles are present, then the two materials will be weakly bonded and are more likely to have delamination problems.

F. Temperature Changes

Temperature changes are a serious concern for MEMS. Internal stresses in devices are extremely temperature dependent. The temperature range in which a device will operate within acceptable parameters is determined by the coefficient of linear expansion. In devices where the coefficients are poorly matched, there will be a low tolerance for thermal variations. Since future space missions anticipate temperatures in the range of –100 to 150°C, thermal changes are a growing concern in MEMS qualification efforts.

Beyond these issues, there are other difficulties caused by temperature fluctuations. Thermal effects cause problems in metal packaging, as the thermal coefficient of expansion of metals can be greater than ten times that of silicon. For these packages, special isolation techniques have to be developed to prevent the package expansion from fracturing the substrate of the device.

Another area that has yet to be fully examined is the effect of thermal changes upon the mechanical properties of semiconductors. It has long been known that Young's modulus is a temperature-dependent value. While it is more or less locally constant for a terrestrial operating range, it may vary significantly for the temperature ranges seen in the aerospace environment.

G. Electrostatic Discharge

Electrostatic discharge, or ESD, occurs when a device is improperly handled. A human body routinely develops an electric potential in excess of 1000V. Upon contacting an electronic device, this build-up will discharge, which will create a large potential difference across the device. The effect is known to have catastrophic effects in circuits and could have similar effects in MEMS. While the effects of ESD on MEMS structures have not been published to date, it can be assumed that certain electrostatically actuated devices will be susceptible to ESD damage.

VI. Stray Stresses

Stray stresses are a failure mechanism that are endemic to thin film structures. Stray stresses are defined as stresses in films that are present in the absence of external forces. In MEMS small stresses will cause noise in sensor outputs and large stresses will lead to mechanical deformation.

Thermal and residual stresses are the two sources of stray stress in MEMS. Thermal stress is a process-induced factor caused by bimetallic warping. Thin films are grown at high temperature and, in the process of cooling to ambient temperature, they contract. While these effects are desirable for the thermocouples, they can cause problem in common MEMS devices. Thermal strains on the order of 5×10^{-4} are commonly

observable in MEMS. Residual stresses are a result of the energy configuration of thin films. Caused by the fact that these films are not in their lowest energy state, residual stress can either shrink or expand the substrate. While there are high-temperature techniques for annealing out residual stress, these methods are not always compatible with MEMS processing.

In bulk micromachined devices, stray stresses can cause device warping, while the effects can be much more serious in surface micromachined devices. Since they are made entirely of thin films, surface micromachined devices are exceptionally sensitive to stray stresses. Large residual stresses can cause warping and even the fracturing of the structural material. For this reason, the materials used in surface micromachining are often selected for their ability to be grown with little stray stress.

VII. Parasitic Capacitance

Parasitic capacitance is another failure mechanism in MEMS. Parasitic capacitance does not cause failure in and of itself, but it can be a contributing factor to failure. Parasitic capacitance is defined as an unwanted capacitive effect in a device. While parasitics are unavoidable in devices, they must be minimized for devices to work properly. Parasitic capacitance can cause unwanted electrical and mechanical behavior in devices.

The most common source of parasitics in MEMS is between a device and the substrate. Most MEMS devices consist of a conducting device suspended over a conducting substrate. These two devices have a capacitance between them that is inversely proportional to the distance separating them. This capacitance will exert a force upon the device, creating non-planar displacement and a current flow through the substrate. While some devices use this effect for non-planar actuation, often parasitic capacitance will impinge device performance by causing unwanted mechanical stresses and motion. To limit these effects, devices should be sufficiently removed from the substrate that large z-axis motion cannot be detected. While this definition is fairly loose, it is ultimately up to design and reliability engineers to determine how much parasitic capacitance is tolerable.

The second major source of parasitics comes from within the device. Many new bulk micromachined devices are designed with a silicon base, a reactively grown oxide layer, and a metallization top layer, as shown in Figure 3-14.

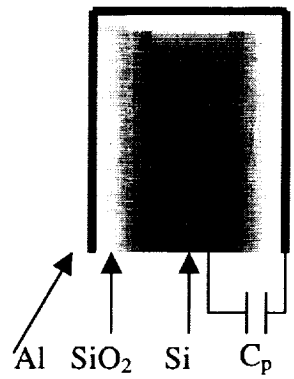


Figure 3-13: Diagram of parasitic capacitance between silicon base and metallization layer on a bulk micromachined beam.

These parasitic capacitances will have varying effects based upon device design. On some devices their effects may be negligible, while on others they can cause severe problems with device output. To limit the influence of parasitic capacitances, many engineers alter their designs to electrically isolate much of their structure. This is done by limiting the amount of metal coated structures and by using thin wires to supply voltages to many structures.

VIII. Dampening Effects

Many MEMS devices are operated in resonant modes, which has some interesting performance implications. All mechanical systems will have specific frequencies at which amplitude, velocity, and acceleration are maximized. They also have an undamped natural frequency, ω_n, which is the oscillating frequency of an unforced system. While in many analyses, this frequency is called the resonant frequency, resonance actually differs from the undamped natural frequency by the relationships below:

$$\text{Displacement resonant frequency}, \omega_d = \omega_n \sqrt{\left(1 - 2\zeta^2\right)} \tag{3-21a}$$

$$\text{Velocity resonant frequency}, \omega_v = \omega_n \tag{3-21b}$$

$$\text{Acceleration resonant frequency}, \omega_a = \frac{\omega_n}{\sqrt{\left(1 - 2\zeta^2\right)}} \tag{3-21c}$$

$$\text{Damped natural frequency}, \omega_d = \omega_n \sqrt{\left(1 - \zeta^2\right)} \tag{3-21d}$$

where ζ is the fraction of critical dampening, which is defined as the system dampening, or dampening coefficient, divided by the critical dampening coefficient, c_c. The critical dampening coefficient describes the minimum amount of dampening required for a forced system to return to equilibrium without oscillation, and, for a given system

mass, m, and stiffness, k, the mathematical expression for the critical dampening coefficient is given as:[54]

$$c_c = 2\sqrt{km} \tag{3-22}$$

Thus, the resonant frequency is influenced by the system dampening and, if system degradation leads to increased dampening, there will be decreases in resonant frequency.

The typical reason to operate a device at resonance stems from the fact that there is an amplification of system output from the natural response of a structure. The magnitude of this amplification is quantified by the quality factor, Q, which is defined as

$$Q = 2\pi \frac{W}{\Delta W} \tag{3-23}$$

where W is the energy stored in a system and ΔW is the energy dissipated per cycle. The quality factor also describes the sharpness of the resonance peak. One common method to measure Q is to determine the frequency range for a system at which $v_{out} = v_{max}/\sqrt{2}$, as shown in Figure 3-14. For $\zeta << .1$, the quality factor can be approximated as:

$$\frac{\Delta\omega}{\omega_n} = \frac{1}{Q} = 2\zeta \tag{3-24}$$

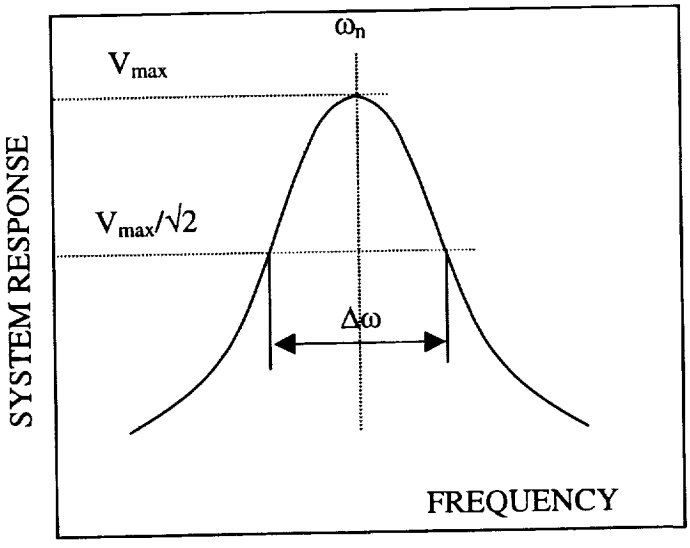


Figure 3-14: Definition of resonance and Q.

As a result, operating a device at resonance, allows greater displacements, which leads to an increase in sensitivity in many systems. However, large structural dampening can cause changes in resonance that will alter output, which can be a long term reliability concern.

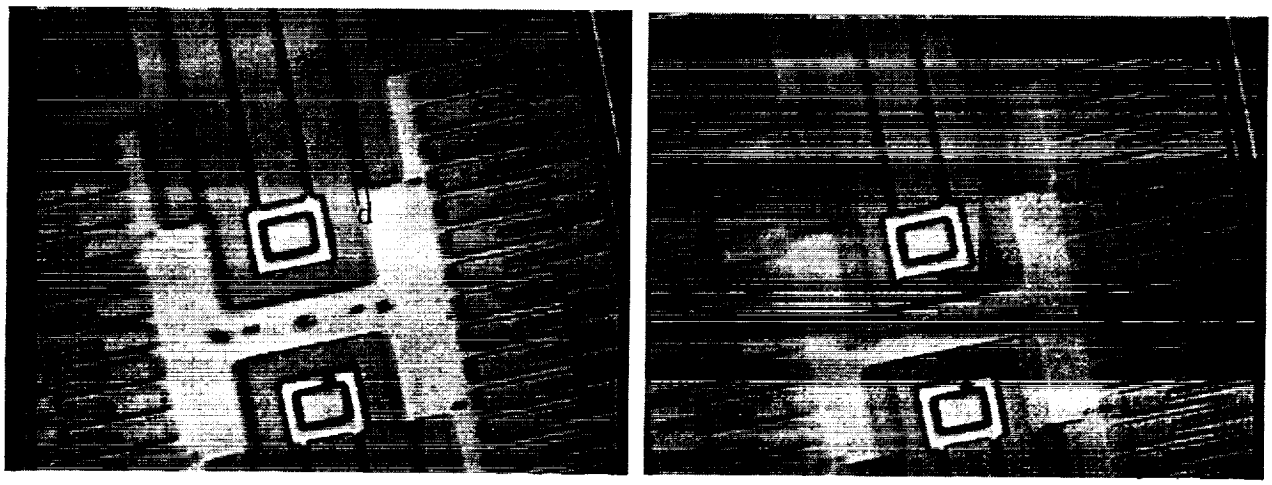


Figure 3-15 (a,b): The difference in amplitude between a linear resonator operating in resonance, right, and operating at a non-resonant frequency, left. As can be seen, the device on the right has a much larger displacement, d, than the device on the left.

MEMS damping is usually caused by the presence of gaseous molecules. There are multiple kinds of damping caused by the atmosphere and the type of damping depends largely upon device geometry. For closely packed parallel surfaces, squeeze film dampening will be predominant. For a rectangular plate of width, 2W, and length, 2L, the squeeze film fraction of critical dampening is, for small displacements[1]:[135,136]

$$\zeta = \frac{8\mu f(W/L)W^3 L}{h_0^3\sqrt{mk}} \tag{3-25}$$

where:

f(W/L) = a function of aspect ratio

m = mass of the moving surface

h_0 = distance between the two surfaces at rest

μ = absolute viscosity of air (1.8×10^{-5} Ns/m^2 at 1 ATM)

[1] The derivation of this equation assumes that $\omega h^2\times$(fluid density)$/\mu << 1.0$.

For a device moving in plane, with an area A, and a separation from the substrate, h, there will be a structural dampening factor due to Couette flow of:[24]

$$\zeta = \frac{\mu A}{2h\sqrt{mk}} \tag{3-26}$$

Since the dampening is proportional to the viscosity of air, which is a function of pressure, some MEMS utilize vacuum packaging to increase performance. The degree to which a package holds a seal will determine the operating characteristics of these MEMS. Thus changes that lead to increased dampening of a system will alter output by shifting resonant frequency and lowering the quality factor.

IX. Additional Reading

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E. Rabinowicz, Friction and Wear of Materials: 2nd Edition, New York, John Wiley & Sons, 1995.

A. T. DiBenedetto, The Structure and Properties of Materials, McGraw-Hill, United States of America, 1967.

Chapter 4: Material Properties

B. Stark

MEMS are constructed out of a multitude of materials, each of which has unique reliability implications. Different materials have different responses to failure mechanisms that need to be understood to better device reliability. To help clarify the purposes of the myriad of MEMS materials, this chapter offers a brief overview of the materials used in MEMS and provides a listing of their properties.

One of the great debates within the MEMS community has focused upon whether to use the thin film or the bulk properties of materials in performing structural analysis. The problem with treating many of these materials as bulk materials is that, when samples become as small as they do in MEMS, crystal defects are no longer small in comparison to the size of the structure being analyzed. While most testing is performed on macroscopic samples, these properties probably do not scale well enough to be used for MEMS, but are often employed anyway for lack of better numbers. For ultimate reliability statistics to be determined, the actual properties of a given material made on a given process line will have to be characterized. Lacking this, approximations can be made with the available data. This chapter offers the common bulk materials properties that are generally accepted. For thin films the applicability of these properties is still somewhat in doubt.

I. Single Crystal Silicon

Silicon is the most common material used in semiconductor devices. In crystalline form, silicon aligns in a diamond structure, which consists of a face-centered cubic lattice with a basis of two atoms, as shown in Figure 4-1. The atomic structure of silicon determines many of its physical properties, which are listed in Table 4-1.

Property	Value
Crystal structure	Diamond
Lattice constant	5.43 Å
Atoms/cm^3	5.0×10^{22}
Density	2.32 g/cm^3
Melting point	1412 °C
Specific Heat	.7 J/g-°C
Young's modulus <100>	130 GPa
Stiffness Constants:	
E_{11}	165.6 GPa
E_{12}	63.98 GPa
E_{44}	79.51 GPa
Poisson's ration <100> orientation	0.28
Tensile strength	3790 MPa
Fracture toughness	.9 MPa m^.5
Thermal conductivity	1.5 W/cm-°C
Coefficient of thermal expansion	4.2×10^{-6} °C^{-1}
Heat Capacity	20.07 (J/mol-K)
Breakdown Field	~3×10^5 V/cm
Piezoresistive coefficients	
n-type: π_{11}	6.6×10^{-11} Pa^{-1}
π_{12}	-1.1×10^{-11} Pa^{-1}
π_{44}	138×10^{-11} Pa^{-1}
p-type π_{11}	-102×10^{-11} Pa^{-1}
π_{12}	53.4×10^{-11} Pa^{-1}
π_{44}	-13.6×10^{-11} Pa^{-1}
DC dielectric constant	11.7
High frequency dielectric constant	11.7
Resistivity	2.3×10^5 Ω-cm
Energy Gap	1.12 eV
Electron mobility	1500 cm^2/V-s
Hole mobility	450 cm^2/V-s
Index of Refraction	3.42

Table 4-1: Room-temperature properties of single crystal silicon.[6,17]

As its atomic similarities to diamond might imply, single crystal silicon is a very hard substance. It exceeds the mechanical strength of steel, but is decidedly more brittle. Its strength makes silicon ideal for many MEMS structures, as it has the highest fracture strength of any material commonly used in MEMS. Due to well controlled processes that yield high purity crystalline structures, silicon has the desirable quality that its mechanical properties are very reproducible.[6] For these reasons, silicon is often used for high-quality microstructures.

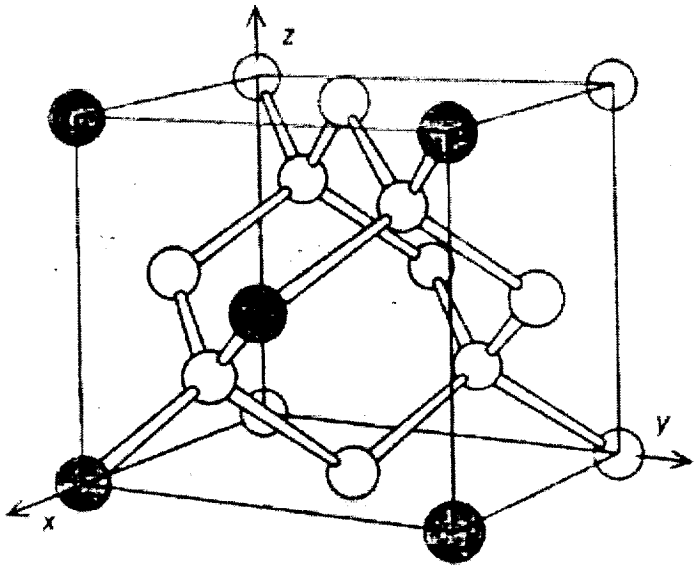


Figure 4-1: Crystal structure of silicon. (from [96])

The science of silicon growth has developed extensively over the past few years. Silicon wafers are now produced with dislocation densities on the order of .1 dislocations/cm^2, which helps to explain the high fracture strength of the material. These wafers also have impurity densities less than .03 particles/cm^2.

In a diamond cubic lattice, like that of silicon, fracture will normally occur along the {111} planes. This is due to the fact that these planes have the lowest surface energy to resist crack propagation. Although fracture along the other crystal planes is certainly possible, it generally will not occur without the aid of a dislocation to lower its strength.[47]

As technology progresses, the fact that silicon does not have the superior electrical and optical properties of other materials has been a minor drawback. Silicon has a lower electron mobility than some other common semiconductor materials, which impedes high frequency operation. While this is a concern for digital designers, it is of little import to MEMS designers, as there are relatively few applications that need mechanical structures to run at the frequency limits of silicon. On the other hand, the electrical properties of

silicon have the advantage that they are sensitive to stress, temperature, magnetic fields, and radiation, which is a characteristic that has been taken advantage of in a number of solid-state sensors.

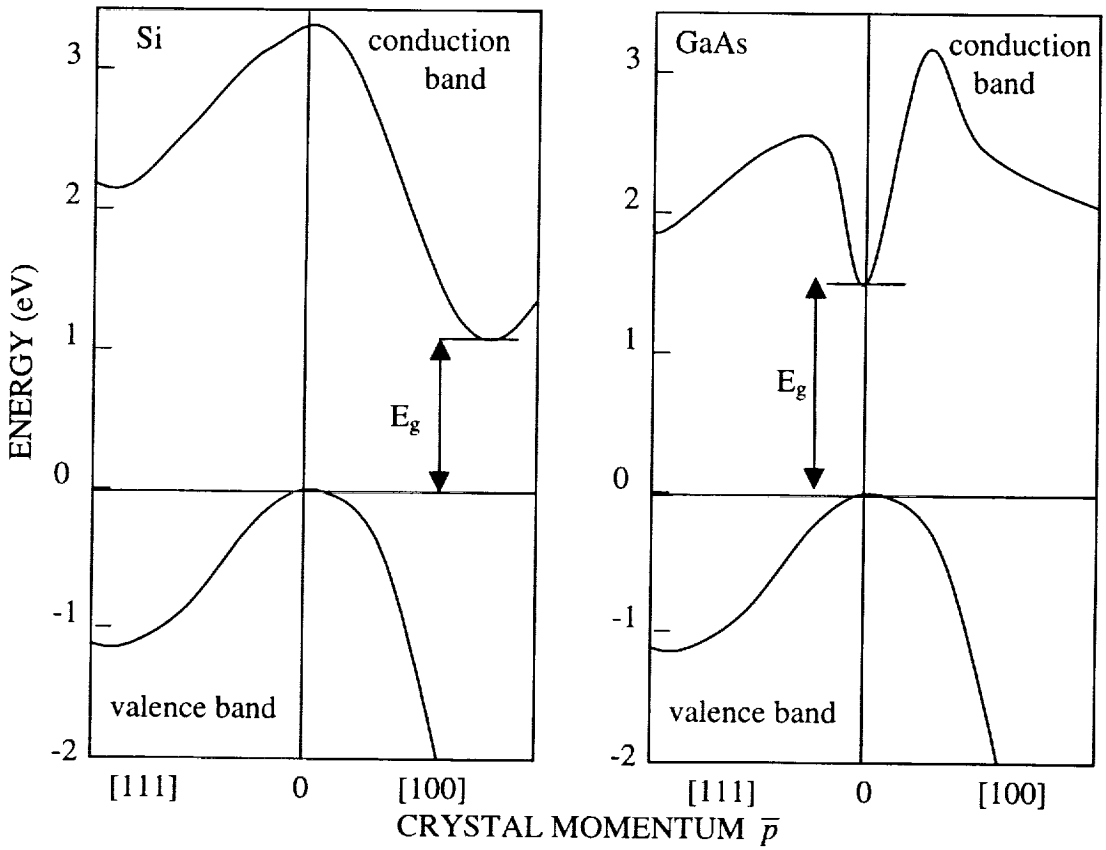


Figure 4-2: Energy band structures of Si and GaAs.

An issue of great importance in silicon is its energy band structure. In the first half of the twentieth century, scientists researching quantum mechanics discovered that electrons in solids can only have discrete energy levels. These energies are separated into distinct bands. At the lowest potential, all electrons in a solid occupy the valence band, which corresponds to the valence orbits in the atoms. After some energy, often in the form of light or heat, has been added to the solid, electrons will transition into the conduction band. The distance between these two energy levels, called the bandgap, determines the fundamental electrical properties of a material. In insulators, such as glass and rubber, the bandgap will be on the order of several electron-volts. Conversely, in good conductors, such as most metals, the bandgap will be less than an electron-volt. Semiconductors occupy the region in between these two areas, with a medium sized bandgap. As such, intrinsic silicon has a moderate resistivity of 2×10^5 Ω-cm.

While the bandgap determines the electrical properties of a device, it also affects the optical properties. The energy level of the valence and conduction bands varies

within a semiconductor material. The bandgap is calculated by subtracting the minimum of the conduction band from the maximum of the valence band. In some materials, such as GaAs, these two points line up. Materials in which this occurs are called direct bandgap semiconductors and have the property that electrons only need to change energy levels to switch band levels, which causes a photon to be emitted when an electron drops from the conduction to the valence band. Materials, like silicon, where this does not occur, are called indirect bandgap semiconductors. Electrons in indirect bandgap semiconductors need to change both momentum and energy to switch band levels, as shown in Figure 4-2.

Thus, intrinsic silicon, as an indirect band-gap material, cannot be used in the production of semiconductor lasers and light emitting diodes. This limitation in silicon has led to research into whole new classes of semiconductor materials that are capable of emitting light.

II. Polycrystalline Silicon

In applications involving surface micromachining, thin films of silicon are needed as a structural material. Since it is difficult to grow thin films of single crystal silicon, thin films of polycrystalline silicon are grown instead.[6] These materials are now finding extensive use in the MEMS industry.

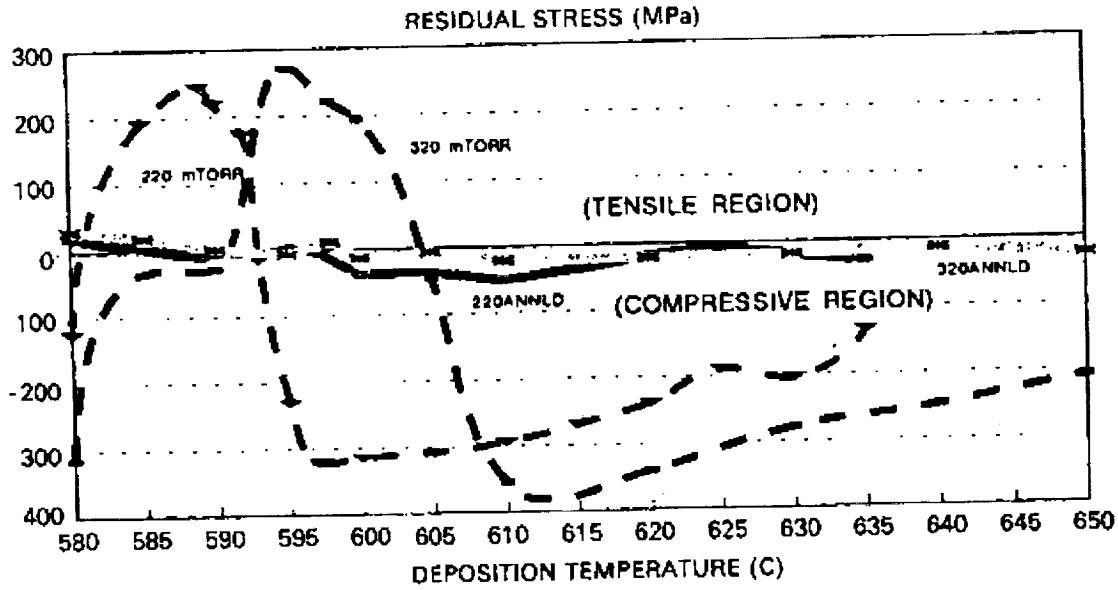


Figure 4-3: Residual stress as a function of deposition conditions. (from [104])

The mechanical properties of polysilicon films depends greatly upon the process used in deposition. The residual stress can be controlled almost entirely by varying deposition pressure and temperature, as shown in Figure 4-3. It has also been discovered that there is a direct link between the presence of <110> oriented grains and residual stress in films, although the reasons for this are not entirely clear.[45]

The strength of polycrystalline silicon is less well understood. Different researchers have reported a Young's modulus ranging between 140 to 210 GPa,[130] with these values having a dependence on crystal structure and orientation. Recent research has shown that the Young's modulus of polycrystalline films is highly dependent upon deposition conditions. The films exhibit preferential grain orientations that vary with temperature. Since an ideal film does not exhibit orientation dependence for its mechanical properties, researchers have found that depositing films at 590 °C, which is the transition point between polycrystalline and amorphous silicon, is an effective method of producing an isotropic film of polysilicon. At this temperature, the amorphous silicon will recrystalize during annealing, which produces films with a nearly uniform Young's modulus of 165 GPa.

In polycrystalline materials, the fracture strength is dependent upon two factors, the grain size, d, and the fracture surface energy, γ_s. This stems from the fact that the size of a dislocation is usually governed by the grain size, which, by Griffith's equation, shows that the fracture strength of this material is:[103,119]

$$\sigma_f = \sqrt{\frac{4E\gamma_s}{\pi d}} \qquad (4\text{-}1)$$

As shown by the equation, the fracture strength is also dependent upon the fracture surface energy, γ_s. For small grained polycrystals, the energy needed to fracture a grain surface increases with grain size.[44] As a result, larger grains will be stronger due to the increased energy needed to propagate a crack across the material.

In several studies, the mean fracture strength of polysilicon has been found to be between 2 to 3 GPa, which is clearly less than that of single crystal silicon. Polysilicon fracture samples have been reported to have a Weibull modulus similar to that of single crystal silicon, which would indicate a similar reliability of the two materials.[40,44,103]

III. Silicon Dioxide

Silicon dioxide is commonly used as an insulator in integrated circuits. In MEMS it is used to electrically isolate components and has been used in some recent applications as a structural material.[7] Its basic properties are listed for reference in Table 4-2.

Property	Value
Density	2.65 g/cm^3
Melting point	1728 °C
Young's modulus	66 GPa
Tensile strength	69 MPa
Thermal conductivity	1.4 x10^{-2} W/°C-cm
Thermal coefficient of expansion	7 x 10^{-6} °C^{-1}
Dielectric constant	3.78
Resistivity	10^{12} Ω-cm
Energy gap	8 eV
Index of refraction	1.46

Table 4-2: Room temperature properties of silicon dioxide.[85]

In the crystalline form of Quartz, silicon dioxide exists in the trigonal trapezohedral class of the rhombohedral system. This class has one axis of three fold symmetry and three polar axes of two-fold symmetry. Quartz, due to its high piezoelectric coupling, is occasionally used in MEMS. However, as a result of its high anisotropy, quartz is more difficult to etch than silicon.[124,125]

Silicon dioxide is a common component of glasses and is, as such, a very weak and brittle material. Thin films of oxide have a compressive internal stress on the order of 1 GPa. Despite this, due to the fact that silicon dioxide is less stiff than other thin film materials and that it has unique electrical properties, it is occasionally used as a mechanical material in high sensitivity applications. Silicon dioxide, with its low thermal conductivity, is a natural thermal insulator, a property which has been exploited for the production of integrated thermal detectors. With a low tensile strength, silicon dioxide is susceptible to mechanical fracturing.

One major feature of silicon dioxide is its properties as an insulator. With a bandgap of 8 eV, silicon dioxide can effectively separate different layers of conductors with little electrical interference. Due to the inherent advantages in being able to integrate such an effective insulator, silicon dioxide has helped to make silicon the semiconductor material of choice for most applications.

IV. Silicon Carbide

In recent years there has been a growing interest in the use of silicon carbide as a material for MEMS. SiC has many properties that make it well suited for MEMS applications, although the SiC wafer growth technology has not matured enough to make it a common MEMS material. Polycrystalline silicon carbide exists in about 180 different polytypes, with the four dominant structures listed in Table 4-3.

Modification	Polytype
α-SiC	6H
(High-temperature modification)	15R
	4H
β-SiC	
(Low-temperature modification)	3C

Table 4-3: Dominant SiC types.[112]

Due to the fact that SiC exists in its beta form at temperatures below 2000 °C, this is called its low-temperature modification. Above this temperature, only hexagonal and rhombohedral polytypes are stable.

The properties of SiC are highly dependent upon the processing conditions and can vary quite dramatically. These properties are listed for a few different SiC preparation techniques.

SiC type	SiC content	Density (g/cm^3)	Young's modulus (GPa)	Thermal expansion coefficient (10^{-6} °C^{-1})	Thermal conductivity (W /m-K)	Flexural strength (MPa)
Ceramic bonded	up to 95%	2.55	100	5.8	16	30
Recrystallized	100%	2.55	240	5.0	28	100
Sintered	95%	2.55	410	4.9	50	450
Hot-pressed	98%	2.55	450	4.5	55	650

Table 4-4: Room temperature properties of SiC.[112]

While not all of these methods are compatible with wafer growth, it should be apparent that the properties of SiC can vary significantly depending upon processing.

Silicon carbide is used for its extreme hardness and high temperature resistance. SiC does not have a defined melting point, instead it has a breakdown point of 2830 °C. At this temperature, SiC decomposes into graphite and a silicon rich-melt. Many SiC structures are less elastic than silicon, which is useful in certain MEMS applications. SiC also has a Poisson's ratio that varies between .183 and .192. The main drawback to SiC in MEMS has been that the technology used to grow SiC wafers still results in high

dislocation densities. This lowers the strength of SiC, which prohibits its use in many applications. For silicon carbide to find widespread use, the techniques used to manufacture it must continue to mature.[112,113]

Silicon carbide, with a band-gap around 3eV, is a wide-bandgap semiconductor material. While the exact width of the bandgap depends on the polytype, SiC is a better natural insulator that Si or GaAs. Intrinsic SiC has a resistivity of 10^8 Ω-cm, although doping can vary this value from .1 to 10^{12} Ω-cm. Silicon carbide also oxidizes readily above 600 °C to form silicon dioxide by the reaction:[112]

$$SiC + 2O_2 \rightarrow SiO_2 + CO_2 \qquad (4\text{-}2)$$

V. Silicon Nitride

Silicon nitride is a material that is employed in a variety of applications. Since it does not react well with many etching solutions, silicon nitride is often used to prevent impurity diffusion and ionic contamination. Its basic properties are listed in Table 4-5.

Property	Value[1]
Density	3.1 g/cm^{-3}
Melting point	1900°C
Young's Modulus	73 GPa
Fracture strength	460 MPa
Coefficient of thermal expansion	3×10^{-5} °C^{-1}
Thermal conductivity	0.28 W /cm-°C
Resistivity	10^{15}Ω-cm
Dielectric constant	9.4
Breakdown field	1×10^{7} V/cm
Index of refraction	2.1
Band gap	3.9-4.1 eV

Table 4-5: Room temperature properties of silicon nitride.[18]

The silicon nitride films used in most MEMS devices are amorphous and are usually either sputtered or deposited by CVD. These films are made with the following reaction, which occurs between 300-500 mT and 700-900°C.

$$3SiH_2Cl_2(g) + 4NH_3(g) \xrightarrow{heat} Si_3N_4(s) + 6HCl(g) + 6H_2(g) \qquad (4\text{-}3)$$

[1] Varies with processing conditions.

Stoichometric nitride films have tensile stresses on the order of 1-2 GPa, which causes large warping. To maintain the structural integrity of the films, they are usually only grown a few hundred nanometers thick. To avoid this limitation, silicon-rich nitride films are often used. A common film of $Si_{1.0}N_{1.1}$ has been developed that has a Young's modulus on the order of 260-330 GPa, a Poisson's ratio of 0.25, and a fracture strain on the order of 3%.[45]

The stress of silicon nitride films can be controlled simply by adjusting the deposition temperature and the ratio of dichlorisilane to ammonia. As shown in Figure 4-4, nearly zero stress films are grown with a ratio of 4:1 at a temperature of 835 °C.

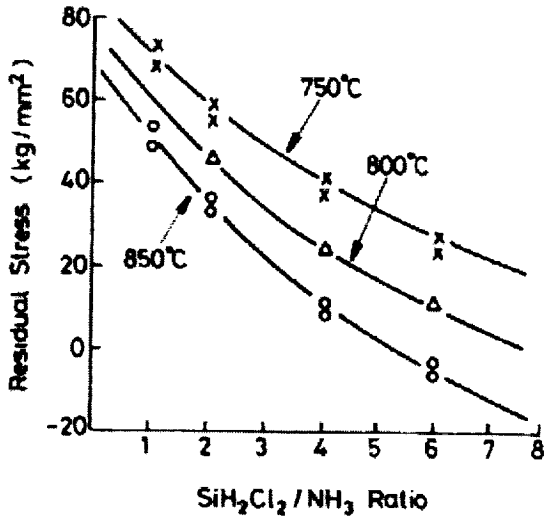


Figure 4-4: Residual stress in silicon nitride films as a function of processing conditions. (from [105])

Silicon nitride has many mechanical properties that make it a desirable material to work with. It is a better thermal insulator than polysilicon, which can be important for isolating surface micromachined structures. Also, its high mechanical strength makes it an ideal film for friction and dust barriers.

One of the unfortunate properties of silicon nitride is that it is not as good an insulator as silicon dioxide. With a bandgap 40% smaller than SiO_2's, the electrical isolation provided by silicon nitride is significantly less than that of silicon dioxide. Furthermore, Si_3N_4 forms a low energy barrier towards silicon and metals, which facilitates the injection of holes into the dielectric at electric fields greater than 2×10^6 V/cm. This results in a hysteresis appearing in the capacitance-voltage curve of metal-insulator-semiconductor structures after the voltage has been swept to large values. Due to these concerns, some designers like to form most of an insulator with SiO_2 and then seal its surface with Si_3N_4.[18]

VI. Gallium Arsenide

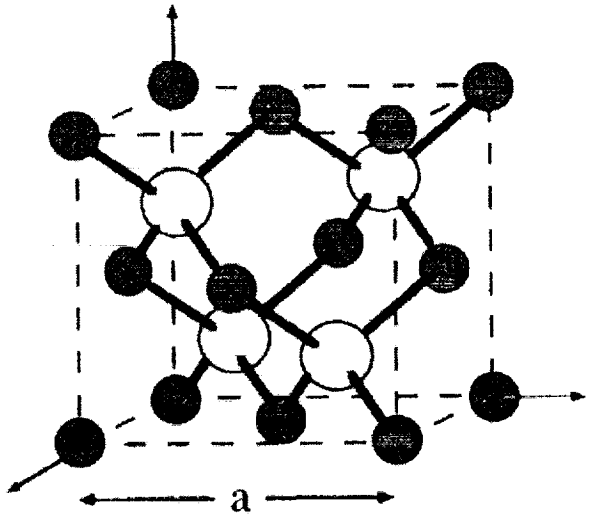


Figure 4-5: Crystalline gallium arsenide. (from[17])

Gallium arsenide is the second most common semiconductor material. It has some unique properties that make it ideal for use in applications that silicon is ill-suited for. Initially finding a niche in the Monolithic Microwave Integrated Circuit market, gallium arsenide, due to its optical properties, has recently been used in the production of optical MEMS, or OMEMS.

Gallium arsenide forms a face centered cubic lattice with a basis of one gallium and one arsenic atom in what is called a zincblende structure, as shown in Figure 4-5. The basic material properties of gallium arsenide are listed in Table 4-6.

Property	Value
Crystal structure	Zincblende
Lattice constant	5.65 Å
Atoms/cm^3	4.42 x 10^{22}
Density	5.32 g/cm^3
Melting point	1237 °C
Specific heat	.35 J/g-°C
Young's modulus <100> orientation	85.5 GPa
Stiffness constants:	
E_{11}	118.8 GPa
E_{12}	53.8 GPa
E_{44}	58.9 GPa
Poisson's ratio <100> orientation	0.31
Fracture toughness	.44 MPa m^.5
Thermal conductivity	.46 W/cm-°C
Coefficient of thermal expansion	6.86 x 10^{-6} °C^{-1}
Heat capacity	47.02 J/mol-K
Breakdown Field	~4 x 10^5 V/cm
DC dielectric constant	13.18
High frequency dielectric constant	10.89
Resistivity	10^8 Ω-cm
Energy Gap	1.424 eV
Electron mobility	8500 cm^2/V-s
Hole mobility	400 cm^2/V-s
Index of Refraction	3.66

Table 4-6: Room temperature properties of gallium arsenide.[6,17]

AlGaAs has also become an integral part of GaAs processing. New technologies have started to use this ternary compound in GaAs based MEMS systems. AlGaAs is an attractive compound because it exhibits many properties that complement GaAs:

Property	Value
Crystal structure	Zincblende
Lattice constant	5.66 Å
Atoms/cm^3	4.42 x 10^{22}
Density	3.76 g/cm^3
Melting point	1467 °C
Specific heat	.48 J/g-°C
Stiffness constants:	
E_{11}	120.2 GPa
E_{12}	57.0 GPa
E_{44}	58.9 GPa
Fracture toughness	1.7 MPa m$^{.5}$
Hardness	5 GPa
Thermal expansion coefficient	5.2*10^{-6} °C^{-1}
Thermal conductivity	.9 W/cm-°C
DC dielectric constant	10.06
High frequency dielectric constant	8.16
Energy Gap	2.168 eV (indirect)

Table 4-7: Room temperature properties of AlAs.[17]

Gallium arsenide is not used in the semiconductor industry for its mechanical characteristics. While sharing many of the same mechanical properties of silicon,[6] it is significantly weaker, with its Young's modulus only 54% that of silicon. It, like silicon, is also very brittle and thus offers no advantages in terms of mechanical performance.

GaAs contains more crystal defects than high quality silicon and, of these, arsenic precipitates are of paramount importance in determining fracture strength. For a normal distribution of arsenic precipitates in a large sample, such as a wafer, there will always be at least one defect large enough to cause small load fracturing. However, for small samples of materials, it is quite common to have limited defect size, which allow the manufacture of high stress structures out of macroscopically low stress materials.[17]

Due to the fact that GaAs is not an elemental structure, it exhibits some mechanical properties that would not be expected from other materials. In GaAs, the electron cloud tends to shift towards the arsenide atoms, which creates a dipole moment along the [111] axis. This causes the eight {111} surfaces to have differing concentrations of Ga and As atoms. As a result, the {111} planes are much tougher than expected. This toughening causes the {110} planes to be the primary fracture points.[17]

Gallium arsenide also has a thermal conductivity that is less than one-third that of silicon and one-tenth that of copper, which makes it a poor conductor. The consequence of this poor conductivity is that the packing density of GaAs devices is limited by the thermal resistance of the substrate. Another thermal concern is the fact that brittle materials becomes ductile at around 35% of the melting point. Corresponding to 250 °C in GaAs, this marked drop in hardness and increase in fatigue could present serious problems for high temperature device operation.

Gallium arsenide finds most of its applications due to its superior optical and electrical properties. As shown in Tables 4-1 and 4-6, GaAs has close to six times the electron mobility of silicon. Electron mobility, which describes how strongly an electron is influenced by an electric field, is derived from the laws of basic physics and is related to Equation 4-4:

$$v_d = -\left(\frac{qt_c}{m^*}\right)E \tag{4-4}$$

where:

v_d = drift velocity

q = electron charge

t_c = mean free times between collisions

m* = effective electron mass

E = electric field

In Equation 4-4, the bracketed proportionality constant is called the electron mobility. As the equation clearly indicates, electron mobility is directly proportionate to the mean free time between collisions, t_c. This number is in turn a function of the lattice and impurity scattering of electrons. The lattice scattering is a result of thermal vibration and increases with temperature until it becomes the dominant factor, as impurity scattering is a constant function of doping levels. Thus, the electron mobility is a function of temperature, which changes based on the intensity of device operation. As a result of this, the electron mobility of GaAs is not always six times that of silicon, as it may often only be double that of silicon.[1]

With the electron mobility determining maximum operating frequency and with GaAs always having a greater electron mobility than silicon, GaAs can operate at higher frequencies than silicon, which has made it an ideal material for many communications applications. However, for MEMS, these factors are limited in their import. While some high frequency GaAs systems are attempting to integrate MEMS components, most GaAs MEMS devices will operate at significantly lower frequencies due to the mechanical limitations of the systems.

Gallium arsenide also has a larger energy band gap than that of silicon, which means that it is a better natural insulator. Through the introduction of either oxygen or

chromium to the GaAs melt, it can further be turned into a semi-insulating material. This provides a substrate that isolates components and performs many of the same tasks, albeit not as effectively, as silicon dioxide.

The other significant advantage that GaAs has over silicon is that it is, as discussed previously, a direct band gap semiconductor material. This has enabled whole classes of optomechanical devices to be developed. It is this property that allows semiconductor lasers and LEDs to be made out of GaAs and it will undoubtedly be exploited more in the future.

While gallium arsenide does have significant advantages over silicon there are also some major drawbacks. There are no stable insulating oxides and nitrides in GaAs technology. This means that it is difficult to manufacture reproducible passivation layers.

VII. Metals

Metals are used in MEMS as electrical conductors and occasionally as structural material. The metals used in MEMS are, unlike the materials discussed previously, ductile. That means that they will plastically deform if stressed past the yield strength. Plastic deformation results in a non-zero strain with zero applied stress, which appears as a shift in the stress strain curve, as shown in Figure 4-6.

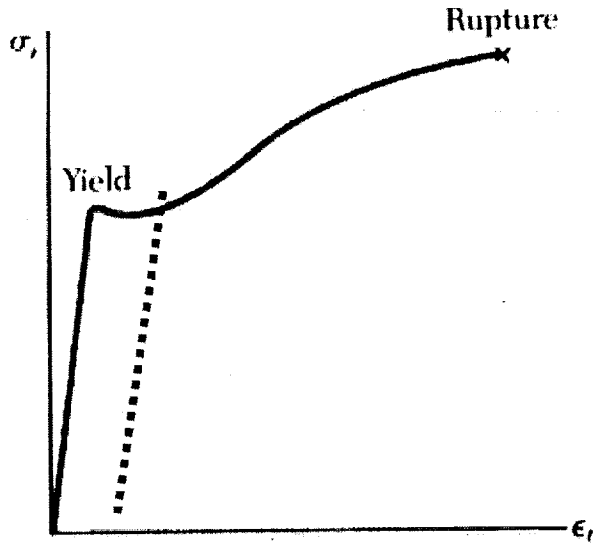


Figure 4-6: Stress versus strain curve for a ductile material. There is a clearly marked yield point, after which plastic deformation occurs. If the material is stressed past this point and then unstressed, the curve will decrease parallel to the elastic deformation section, as illustrated by the dotted line.

A. Aluminum

Aluminum is commonly used in MEMS as a sputtered film placed over a processed structure. By covering a structure with a conductive film, equipotential surfaces are created on a device, which are critical to the operation of many electrostatic device. Aluminum is also commonly used as an electrical conductor in semiconductor technologies.

Aluminum, like most metals, is often alloyed with other substances to improve its structural properties. The alloys of aluminum are numerous and are offered in great detail in Reference [111]. Pure aluminum has many properties that distinguish it from other materials used in MEMS. Listed in Table 4-8, the properties of aluminum have been both a boon and an area of concern for researchers over the past decades.

Property	Value
Density	2.71 g/m^3
Melting Point	659°C
Specific Heat	0.90 J/g-°C
Young's modulus (bulk value)	70 GPa
Poisson's ratio	.35
Ultimate tensile strength	110 MPa
Ultimate shear strength	70 MPa
Yield tensile strength	100 MPa
Yield shear strength	55 MPa
Thermal conductivity	2.37 W/cm-°C
Coefficient of thermal expansion	23.6×10^{-6} °C^{-1}
Resistivity	2.82×10^{-6} Ω-cm

Table 4-8: Room temperature properties of 99.6% pure aluminum.[46,101,111]

The mechanical properties of aluminum are considerably poorer than Si and GaAs. With a Young's modulus that is less than half that of silicon, it is clearly a more ductile material. However, since the yield strength of aluminum, at 100 MPa, is at least an order of magnitude below the fracture strength of Si and GaAs, aluminum is rarely used as a structural support in MEMS.

For a considerable amount of time, aluminum was the only good conductor that could easily be integrated into ICs. Since aluminum forms Al_2O_3 bonds with SiO_2, it is simple to adhere it to passivation layers. This fact lead to its widespread implementation, despite the fact that materials existed with better electrical properties.

B. Gold

Gold is a substance that is finding increasing use in the MEMS field. While not as common as aluminum, it has many of the same features with some added advantages. Its properties are listed below for reference.

Property	Value
Density	19.3 g/m^3
Melting Point	1063°C
Specific Heat	0.13 J/g-°C
Young's modulus (bulk value)	75 GPa
Poisson's ratio	.42
Ultimate tensile strength	125 MPa
Thermal conductivity	3.15 W/cm-°C
Coefficient of thermal expansion	14.2×10^{-6} °C^{-1}
Resistivity	2.44×10^{-6} Ω-cm

Table 4-9: Properties of gold.[46,102,111]

Gold is not a material known for its strong mechanical properties. It is a soft, ductile material that is easily deformed. As a result, it is not used as structural material. Instead, it will almost always be layered on top of a more rigid material or be used in applications that do not require mechanical motion. Gold does have problems adhering to SiO_2, but there are some established methods to circumvent them. One method employed is to use an intermediary layer of chromium as an adhesive, since it forms Cr_2O_3 with SiO_2 and also strongly bonds to gold.

The main impetus for the use of gold in MEMS applications has been the fact that it is a better electrical conductor than aluminum. In applications where high conductivity is of paramount importance, gold is often the material of choice. One of the attractive properties of gold is that it is a fairly inert material. This means that its surface does not readily oxidize in atmosphere, which helps to maintain its conductivity in atmospheric applications.

C. Copper

With the recent integration of copper into ICs, it will only be a matter of time before copper becomes integrated into MEMS. Since many designers hope to eventually place MEMS in system-on-a-chip devices, it is of paramount importance that low power systems, that must therefore employ copper, can be developed. Copper has some unique properties that make it worth the effort to integrate, as shown on the following page.

Property	Value
Density	8.89 g/m^3
Melting Point	1083°C
Specific Heat	0.39 J/g-°C
Young's modulus (bulk value)	115 GPa
Poisson's ratio	0.36
Ultimate tensile strength	220 MPa
Ultimate shear strength	150 MPa
Yield tensile strength	100 MPa
Thermal conductivity	3.98 W/cm-°C
Coefficient of thermal expansion	16.6×10^{-6} °C^{-1}
Resistivity	1.72×10^{-6} Ω-cm

Table 4-10: Properties of 99.99% copper.[46,101,111]

Copper is actually a slightly stronger material than pure aluminum. However, it is unlikely to be used as anything but a conductor in the near future due to the fact that it does not adhere especially well to silicon, which makes it likely to delaminate. The ability of copper to find a niche in the MEMS community will largely hinge upon the strength of the adhesive bonds that can be formed. Copper is an excellent thermal conductor, which will prove useful in many applications.

The main reason that large investments have been made into the development of copper in ICs and MEMS is that it has a higher conductivity than aluminum and gold. This means that it will dissipate lower amounts of heat and waste less power. Thus, there is a great incentive to integrate copper into the MEMS industry in general and in the space MEMS industry in particular.

VIII. Polyimides

Polyimides are a class of organic films that have proven promising as a possible replacement for SiO_2 as an insulator in microelectronics. There are a number of different commercially available polyimide films used in the semiconductor industry and their properties vary significantly. The main reason for the investigation of polyimide films is that they offer a new generation of low permittivity dielectrics, some of which have been reported to have a permittivity of less than $2\varepsilon_0$. Since lower dielectric constant insulators dissipate less power in FETs, these materials may begin to find their way into the MEMS community. The materials properties of a PMDA/BPDA/TFMOB polyimide film have been fairly well investigated and are offered below.

Property	Value[1]
Young's Modulus (in plane)	7.5 GPa
Young's Modulus (out of plane)	8.0-15.0 GPa
Shear Modulus	1.0-10.0 GPa
Poisson's Ratio(in plane)	0.35
Poisson's Ratio (out of plane)	0.1-0.45
Dielectric coefficient	2-4
Coefficient of thermal expansion	6.0×10^{-6} C^{-1}

Table 4-11: Properties of PMDA/BPDA/TFMOB polyimide.

Polyimides are a weak class of materials. Their main function in MEMS has been in circuits and as a layer of chemically active sensor materials on membranes and cantilevers. As such, polyimides are generally not considered for structural applications.

The main impetus for developing polyimides was that they could have a lower dielectric constant than SiO_2, which could represent a major reduction in power consumption on integrated circuits. Thus, much like copper, polyimides are likely to find introduction into the MEMS market through their inclusion in the consumer electronics market. As good insulators, polyimide films have a myriad of possible uses in the semiconductor industry.

IX. Additional Reading

Michelle M. Gauthier, Engineering Materials Handbook ASM desk edition. Materials Park, OH, November 1995.

K. Hjort, J. Söderkvist and J. -Å. Schweitz, "Gallium Arsenide as a Mechanical Material" *Journal of Micromechanics and Microengineering*, Vol. 4, No. 1, 1994.

D. Bloor, R. J. Brook, M. C. Flemings and S. Mahajan, eds. The Encyclopedia of Advanced Materials, Elsevier Science, Ltd., New York, 1994.

[1] These values will vary by manufacturer.

Chapter 5: MEMS Device Processing

B. Stark and W. C. Tang

The growth of MEMS has largely been due to innovations in processing technologies. Adaptations in the processes used to manufacture integrated circuits have led to the development of MEMS and will continue to define the dimensional limitations in devices. It is ultimately these technologies that determine the specifications and reliability characteristics of any given device. As such, they are critically important to understanding MEMS. This chapter offers a brief overview of the most common processing techniques used today. It then describes the integration of these techniques into micromachining.

In the fabrication of common MEMS devices, there are two basic techniques employed. Devices can be constructed by patterning the bulk material of a wafer into a desired structure or, alternatively, by patterning thin films of material deposited on the surface of a wafer. These two processes, respectively called bulk and surface micromachining, are the basis for any MEMS fabrication technology.

I. Microfabrication Processing Steps

There is a variety of processing techniques that are often used in all MEMS processes.[6] The degree to which they are successfully implemented in any given technology determines the viability of the technology. They are listed below to give a basic description of MEMS processing.

A. Thin Film Growth and Deposition

Thin films are an essential building block of semiconductor devices. Surface micromachined devices are constructed entirely out of successive layers of thin films and bulk micromachined devices that employ thin films of silicon dioxide for electrical isolation. There are several common methods for placing thin films on MEMS that are discussed in this section.

i) Spin Casting

In this process, a material is in a solution with a volatile liquid solvent. The solution is poured onto a wafer, which is rotated at high speed. As the liquid spreads over the surface of the wafer, the solvent evaporates, leaving behind a thin film of the solid material, which can be anywhere from .1 to 50 μm thick. Spin casting is useful for depositing organic materials, such as photoresist, as well as inorganic glasses. Spin

casting blurs the underlying topography of a structure, yielding a smooth surface. Spun cast materials are susceptible to severe shrinkage whenever the film coalesces, either from solvent removal or post-bake. This means that spin cast films have an inherently high residual stress. Spin cast films are also less dense and more susceptible to chemical attack than materials deposited by other means.[6]

ii) Evaporation

Another way to place a material in a thin film on a wafer is to evaporate them from a hot source. The evaporation system uses a vacuum chamber, which is pumped down from 10^{-6} to 10^{-7} Torr. A crucible is then heated to flash-evaporate material onto a sample. This process is controlled by a shutter, which limits the amount of time in which the wafer is exposed to the crucible. The thickness of the film is governed by the length of time that the shutter is open and is also a function of the vapor pressure of the material. Thus materials with a high melting point, such as tungsten, require high temperatures to evaporate, which can burn organic films that are on the wafer. Since evaporated films originate from a point source and the vaporized materials travel in a straight path, they suffer from shadowing effects that yield non-uniform thickness and poor step coverage.[6] A second factor affecting the coverage is the surface mobility of the species on the substrate. As a general rule, evaporated films are highly disordered, which causes a large residual stress and limits the thickness of the films.

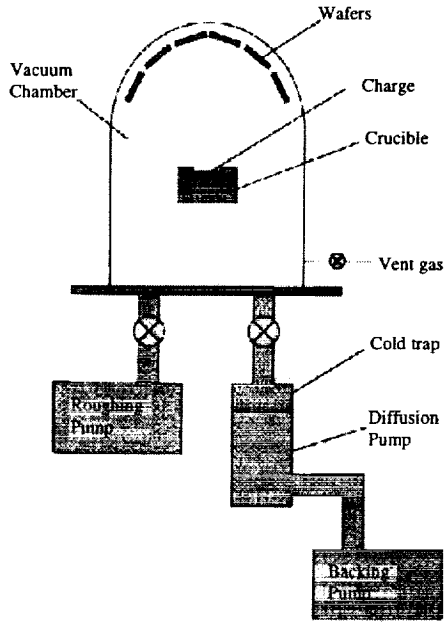


Figure 5-1: A typical evaporation system. (after [46])

iii) Sputtering

Sputtering is a thin film growth technique that eliminates many of the problems inherent to flash-evaporation. Sputtering works by inserting a wafer into a vacuum chamber that is subsequently pumped down to between 10^{-6} and 10^{-8} Torr. Then an inert gas of a few mTorr of pressure is introduced into the system, which is then ignited into a plasma. The highly energetic ions of the plasma strike a target of sample material and tear atoms off its surface. These atoms then form a thin film across the wafer. This process creates a continuous planar flux of the species landing on the wafer, which makes preferable for mass production.[6] Another desirable aspect of sputtering is that the high energy plasma does not have the same temperature problems inherent to evaporation. Most elements and many inorganic and organic compounds can be sputtered. Refractory materials that are difficult to evaporate can be easily sputtered as well. Sputtering can also be done with more than one target, which allows control of the atomic composition of thin film alloys. Sputtered films have better step coverage and uniformity than evaporated films, but they are disorganized structures whose mechanical properties and residual stresses are sensitive to sputtering conditions. Problems also arise from the inert gas used in the sputtering process, which can become trapped in the film and cause inconsistencies in the mechanical properties of the films.[46]

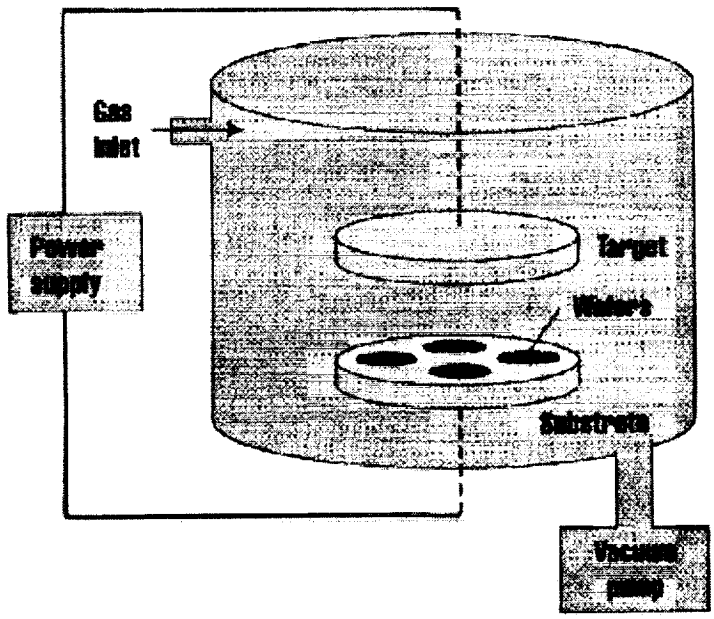


Figure 5-2: Basic sputtering system. (from [46])

iv) Reactive Growth

Reactive growth differs from the previously mentioned methods in that it utilizes chemical reactions with the substrate to construct thin films on wafers. The most common example of this process is with the growth of oxide films on silicon wafers. In this process, a wafer is placed into a furnace with oxygen gas (dry oxidation) or steam (wet oxidation). The silicon is gradually oxidized at a highly predictable rate that depends upon temperature and crystalline orientation.

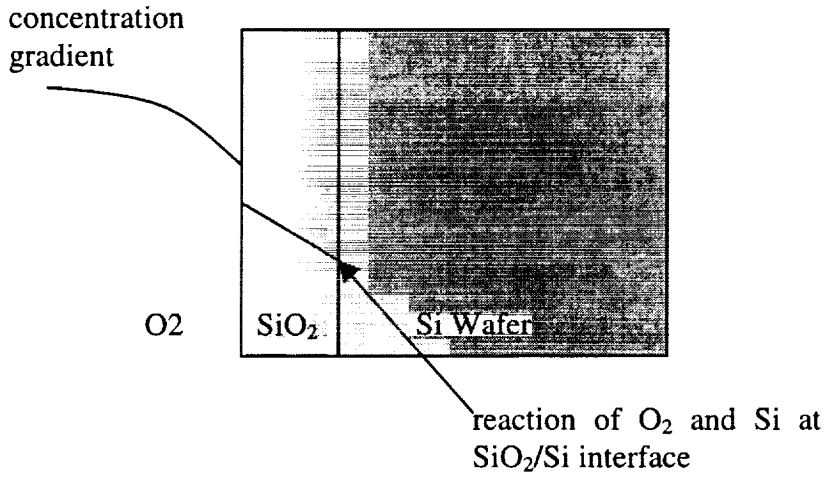


Figure 5-3: Reactive growth process.

Reactively grown films are usually of excellent quality but suffer from large residual stresses due to volume changes in the processed sample. In silicon dioxide growth, there is a volume change of about 45%, which causes mechanical warping.

v) Chemical Vapor Deposition

Chemical vapor deposition, or CVD, involves thermally breaking down gaseous compounds into their components. When they impact a wafer, some of these components nucleate onto it, which grows a thin film. CVD is limited by both the mass transport and reaction-limited processes, with the latter method being preferable due to its better uniformity. This process can be used to deposit many common semiconductor materials, including silicon dioxide, silicon nitride, polycrystalline silicon, and refractory metals. In low pressure thermal CVD, or LPCVD, films with the most desirable mechanical properties are produced. Unlike other methods, CVD films can be deposited conformally on a sample. This property allows CVD films to seal cavities, which can be advantageous in many devices. The stresses and mechanical properties of CVD films can be controlled through the deposition conditions and subsequent annealing. A CVD process called epitaxial growth can be utilized to grow single crystal films on crystalline substrates. Since these films have the same properties as bulk crystals, they could find a multitude of applications in the MEMS industry.

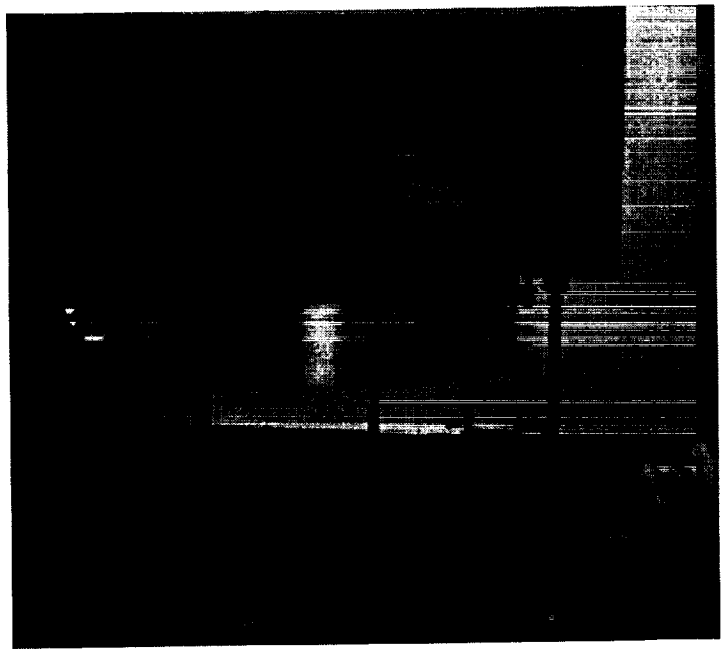


Figure 5-4: A chemical vapor deposition system. (from [179])

vi) Plasma Deposition

Plasma-induced reactions are commonly used for the deposition of MEMS materials. The decomposition of gaseous compounds into reactive species can be induced by the presence of a plasma. This process is known as plasma-enhanced CVD or PECVD. This process utilizes a plasma that contains many ionized species. Some of these species are then deposited on the substrate, which forms a solid film. PECVD films are deposited at a faster rate and require a lower deposition temperature than thermal CVD films, which permits deposition on low-melting point substrates. A number of organic films can also be deposited through PECVD. These films find use as resists for nonplanar substrates. However, PECVD films contain cracks and pinholes. Accurate control of the stoichiometry is difficult as these films contain trapped byproducts from the reaction (especially H_2) that affect the film's mechanical integrity and residual stress.

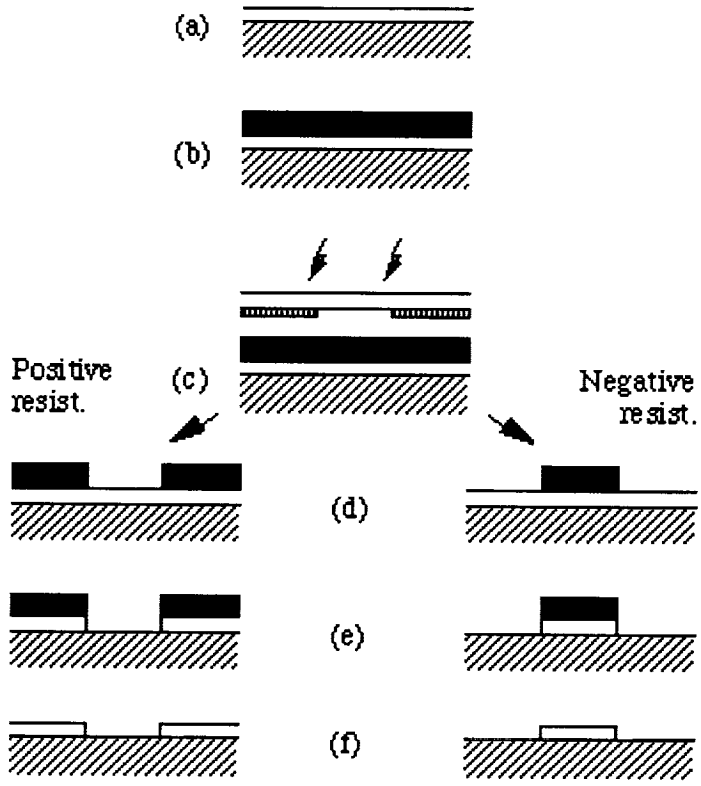


Figure 5-5: The basic photolithographic process in a cross sectional view. First a thin film is deposited on the substrate in (a) followed by the photoresist in (b). UV rays are then focused through a mask onto the surface in (c). Depending upon the type of photoresist, the exposed resist is either removed or left intact in (d). Next, the film is stripped away in places that it is not covered by resist in (e). Finally all of the resist is removed in (f). (from [158])

B. Photolithography

Photolithography is the process by which patterns are transferred onto a wafer. It is accomplished by spinning a thin layer, usually 1 μm thick, of photosensitive organic material, called photoresist, onto the wafer. Then a light source, which typically has an ultraviolet wavelength, is flashed through a computer generated quartz mask and focused onto the photoresist. Then, in a process similar to photographic picture development, the photoresist that has been exposed to light is washed off with the aid of a chemical developer. The remaining resist then acts as a barrier for the underlying regions for further processing. After the processing on the exposed layers has been completed, the resist is washed off and a clean processed wafer is left. This process is typically repeated many times with different mask sets for many of the most common integrated circuits fabrication processes. There are several critical sub-processes in photolithography that need to be addressed as well.

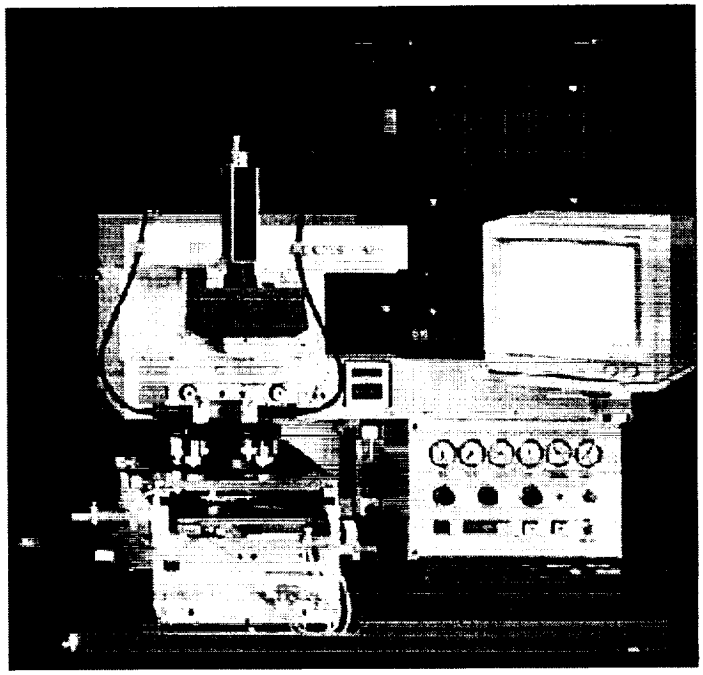


Figure 5-6: Typical alignment machine.

i) Mask Fabrication

The quartz mask is generated by photolithography as well. This process utilizes a glass plate with chromium or emulsion patterns and entails the use of a computerized mask making machine. It starts with a pattern for the mask being entered into the computer through commercially available CAD tools. The pattern is then broken down into small rectangular regions transferred to a mask-making machine. Then a glass plate coated with light blocking chromium or emulsion and photoresist is exposed. The data on

the computer is used by the mask maker to position the mask and determine the size of a variable aperture shutter on the ultraviolet light source. Each of the rectangular boxes is then individually exposed onto the plate. Depending upon the design, this process may be repeated over one hundred thousand times before the mask is finished. After this exposure step, the photoresist is developed and the chromium or emulsion patterns are etched.

ii) Alignment and Exposure

In processes that require multiple masks, each mask layer must perfectly match the features on the substrate. This is done by aligning the mask to special features, called alignment keys, on the wafer prior to exposure. A typical mechanical alignment utilizes a sample, mask holder, a stereoscopic microscope, an ultraviolet light source, and a precision positioning stage, as shown in Figure 5-6. This can either be done with a stepper aligner, which exposes one die at a time, or with a contact aligner, which exposes the whole wafer at once. Often in MEMS, the fabrication process requires photolithography to be performed on both sides of a wafer. To accomplish this, two masks are aligned with each other inside a secure assembly. Then the wafer is inserted and aligned with one of the two masks before being exposed to the ultraviolet light source. There is also an alternative method employed that uses an infrared microscope to locate alignment keys on the back-side, which could offer better alignment precision.[6]

C. Etching and Patterning Techniques

After a pattern has been transferred onto a wafer, it is often necessary to strip away unwanted sections of materials. This process, called etching, determines the dimensions of a MEMS structure. Invariably the reliability of a device will be related to how well the etching is performed and, as such, it must be well understood before a device can be qualified. There are several standard etching techniques used throughout MEMS processing that will be discussed in the following sections.

i) Lift-off

Lift-off is a simple patterning technique. It is accomplished by depositing a layer of sacrificial material, like photoresist, on a substrate. This layer is then patterned, which usually involves the photolithographic processes discussed above. Then a layer of structural film is evaporated onto the substrate. The pattern on the sacrificial layer is then transferred to the structural layer by removing the sacrificial layer. This has the effect of removing all of the structural material that is on top of the sacrificial layer, thus leaving a patterned structural film.

ii) Wet Etching

Wet etching involves immersing a wafer patterned with photoresist or other etch masks in a chemical bath. The chemical etchant selectively removes material not covered with the mask. The exact profile of the patterning depend on the anisotropy of the etch. Wet etchants all exhibit a degree of isotropic behavior. This has the effect of undercutting the patterned structure, making it smaller than the resist mask. The degree to which the etchants etch the <100>:<110>:<111> directions is responsible for determining the maximum aspect ratio of many structures. Another important aspect of many etchants is their ability to selectively etch one material over the other. Called selectivity, this ratio determines how thick etch stops must be and provides dimensional limits on many technologies.

There are several different chemicals used in wet etching. Acidic etches are used for isotropic release etches. These are usually completely isotropic etches that are designed to separate suspended structures from the underlying substrate. Common acidic etchants are HF, HNO_3, and CH_3COOH. These chemicals etch from 50 to 150 μm/h. SiO_2 is often used as an etch stop for these materials, as it is usually etched at a rate of 2 μm/h.

For an anisotropic etch, alkaline etchants are commonly used. These exhibit different degrees of selectivity and etch rates. Typically these chemicals etch <111> planes much slower than the <100> and <110> planes. This effect and its impact upon MEMS devices is discussed in greater detail in Section 5-IIA. Some etchants can also be influenced by the introduction of boron into the bulk material, which can greatly reduce the etch rate. It is also possible to influence etch rates in a process known as electrochemical etching, which involves applying a voltage across a p-n junction.

iii) Dry Etching

Dry etching, also referred to as reactive ion etching, or RIE, involves using etchants in a gaseous state. The etchant is converted to a highly ionized plasma. Dry etching is performed in a chamber pumped down to a pressure between 10 mTorr and 1 Torr. A wafer is placed between two electrodes, which are then exposed to an RF voltage, which creates a plasma in the chamber. Etching occurs when highly reactive free radicals in the plasma react with the solid-phase material of the film. The anisotropy of the etch is a result of the chemical reaction being preferentially enhanced on the side of the wafer parallel to the electrodes by bombardment from ions in the plasma. The ions impinge the surface of a film and expose underlying material, which is then etched away by the gas. The ions accelerate the etching process considerably, which means that the vertical sidewalls of the wafer, which do not interact with the ions, are not affected by dry etching.

GaAs anisotropic etching is usually performed in chlorinated gasses. One of the problems with GaAs etching is that, due to differences in the etch rates of group III and group V halides, the speed of etching in GaAs varies with crystal planes. In low power, high pressure Cl_2 gasses, significant faceting can occur. There are several methods that can be used to avoid this problem. It is possible to add certain compounds to form polymers in the plasma and passivate the side walls, thus preventing the problem. Another possibility is to use hydrides to etch arsenic and methane to etch gallium. A mixture of AsH_3 and between 5 to 25% methane has been shown to be an effective anisotropic etchant.[46]

One of the major drawbacks to reactive ion etching is residual damage caused by the etch. With ion fluxes of 10^{15} ions/cm^2 delivered at 300 to 700 eV, substrate damage and chemical contamination are serious issues to consider. Another problem is gas phase particle deposition and metallic impurities originating from the RIE chamber and electrodes. Several more complex techniques have been derived to remove these problems, but they come at added expense and preparation time. It is also known that the RIE can drive impurities into the bulk material to depths of 30 nm, which can limit the fracture strength of a structure.[46]

II. MEMS Fabrication Processes

A. Bulk Micromachining

The distinguishing characteristic of bulk micromachining is that it fabricates micromachined devices out of the bulk of a substrate. In recent years, several variants of this procedure have appeared that utilize different etching and patterning techniques. In this section, a brief overview on bulk micromachining will be offered that will include the most prevalent processing techniques.

Bulk micromachining begins with a single crystal substrate. A thin film of material that is inert to the chemical etchants is then deposited on the substrate. For silicon substrates, silicon oxide or nitride are most commonly used as an etch mask. Then the film is patterned so that the undesired portions of the film are removed. This leaves the bare substrate exposed.

At this point, the bulk material is etched. The etching of the bulk material can either be performed with a wet or a dry chemical etchant. Since the processes associated with these etches are substantively distinct, they will be individually addressed.

i) Bulk Micromachining with a Wet Etch

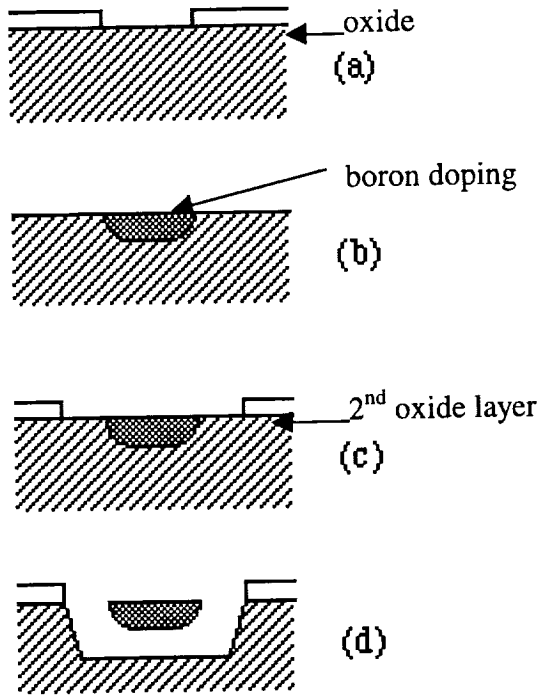


Figure 5-7: A side view of a generic bulk micromachining process. (a) an oxide layer is grown and patterned on top of a <100> silicon wafer. (b) Boron is ion implanted and annealed to the suitable depth. (c) a second oxide layer is grown and patterned. (d) KOH anisotropic etch.

The process associated with the wet chemical etching of silicon is illustrated in Figure 5-7. As the figure shows, this anisotropic etch occurs in diagonal direction. This is a common feature of wet anisotropic etches. Since the early 1960s, alkaline solutions have been used to etch silicon along crystalline planes. The etch rate is slowest in the <111> direction and fastest in the <100> and <110> directions. The result of this uneven etch rate is that the bulk material is etched at an angle of 54.74°, which is the angle between the (100) surface and the four {111} planes. The ratio between the etching in the desired directions and the etching in the undesirable directions is defined as the selectivity. An etchant that has a better selectivity will yield a more defined, and hence better, finished structure.

There are several characteristics of anisotropic etches that lead to important design considerations. The major constraint is that designed features must be bound by the {111} planes thus the resulting structures are necessarily rectangular, with sidewalls sloping away at 54.74°. The use of less popular <110> oriented Si wafers yields vertical sidewalls but the planar features can only be long parallel strips on the substrate, which have limited use. In recent years a number of groups have begun exploring dry etching processes that offer the possibility of anisotropic etchings.

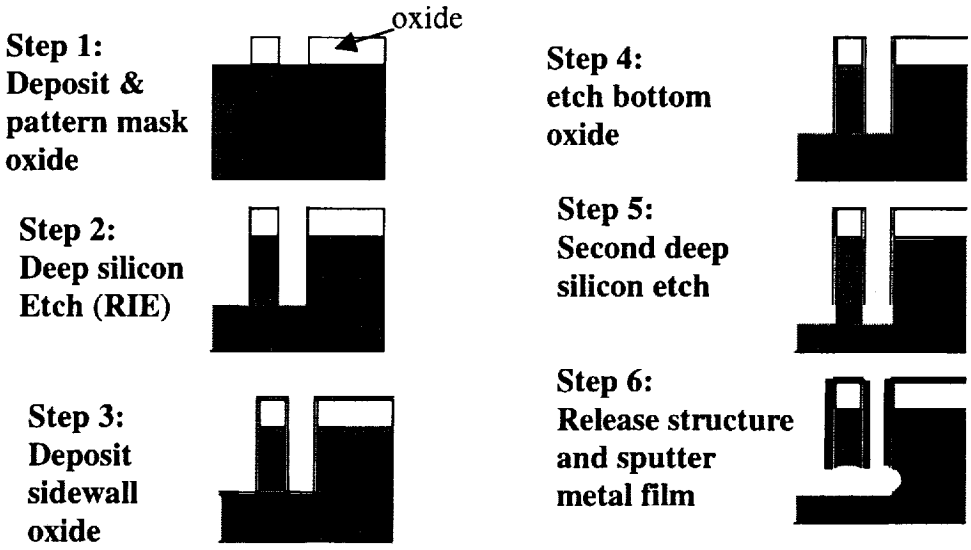


Figure 5-8: A side view of one of the dry etch micromachining processes. In Step 1, an oxide coating is grown on top of the substrate and patterned. Then, in Step 2, a reactive ion etch removes silicon and transfers the pattern from the oxide. Step 4 exposes the bottom of the wafer for Step 5, etches a small amount of substrate. This allows Step 6 to proceed, which is an anisotropic etch that releases that structure from the substrate and often deposits a layer of metallization to create an conductive surface.

ii) Bulk Micromachining with a Dry Etch

Bulk micromachining involving dry etching is performed in much the same way as bulk micromachining with a wet etch. One example of a dry etching process is the SCREAM process, which was developed at Cornell under the supervision of Noel MacDonald and is illustrated in Figure 5-8. This process is conducted by transferring a pattern onto the substrate. Then, a reactive ion etch is performed. Normally after this, a second deep etch is performed to expose oxide-free silicon. From this point, an isotropic etch can be performed to release the whole structure, which creates high aspect ratio structures suspended above the substrate.[180]

There are multiple methods employed to produce finished devices through a reactive ion etch. While the processes vary by research group, all employ a deep reactive ion etch that can create aspect ratios higher than 20:1. It is the ability to produce these high aspect ratio structures, which can have higher mass and capacitance per silicon surface area than many other MEMS technologies, that has helped to drive the development of RIE in MEMS production.

In the production of bulk micromachined devices, it has proven useful to layer devices. The most common method of achieving layered bulk micromachined devices is by bonding two wafers together. For this reason, different wafer bonding techniques will be addressed.

iii) Wafer Bonding

Wafer bonding has been used in recent years for both sealing microsensors and for the construction of composite sensors. There are several kinds of wafer bonding techniques commonly employed, which are discussed below.

(1) Anodic Bonding

Anodic, or electrostatic, bonding is a process that bonds a conductive substrate, which is usually silicon, to a sodium rich glass substrate. This is done by putting the two substrates into direct contact. They are then heated to between 350-400 °C, which mobilizes the sodium ions in the glass. Then a voltage of 400-700 V is applied between the two substrates, with the glass substrate being made negative with respect to the silicon wafer. This repels the sodium ions from the interface and creates an ion-depletion region about a micron thick with electric fields on the order of 7×10^6 V/m. This creates an electrostatic pressure of several atmospheres, which pulls the two wafers together while a thin layer of SiO_2 is formed. The end result of this process is a hermetically sealed bond with a strength that exceeds that of the individual substrates.

There are several reliability concerns in producing these bonds. The high temperature at which the bond is formed can induce thermal mismatch warping in a processed device. There can also be warping at the bonding interface from unmatched thermal coefficients of expansion. Currently, Corning glass 7740 offers the closest match to silicon. Another concern is the introduction of the large voltages and electric fields inherent to the bonding process. It is possible to destroy the device in the bonding process if these factors are not considered.[6]

(2) Low-Temperature Glass Bonding

Low-temperature glass bonding offers a viable alternative to anodic bonding for applications where high voltages are unacceptable. In this process, the bonding interface is covered with a thin film of low-temperature glass. The wafers are then placed into contact under pressure and heated to create the bond. The low-temperature glass then either melts or crystallizes, depending upon the actual glass used, which bonds the two substrates. In general, these bonds are not as strong, and thus less reliable, as anodic bonds.

In some applications, glass frits are used to form bonds. These frits are solutions of metal oxides that form a paste. Under pressure, the frit will form a film that seals rough surfaces. This film can be hardened by heating it to between 300-600°C. The thermal expansion coefficient of these frits can range between two to five times more than that of silicon, which can lead to warping problems.

(3) Fusion Bonding

Fusion bonding is a technique that fuses two materials together through high temperature. This process is used commonly in the production of silicon-on-insulator devices and pressure sensors. It is accomplished by taking two clean wafers and placing them on top of one another. This bonds the two wafers through Van der Waals forces. They are then placed into a furnace to create the final bond at temperatures in excess of 1000 °C.

While this process creates strong bonds it has some serious drawbacks. High furnace temperatures prohibit the use of active devices in the wafer prior to bonding. Furthermore, the weak initial bond makes the final bond strength very sensitive to the surface topology of the wafers and the presence of contaminants. For these reasons, these bonds are not always the most reliable and are often difficult to use.

iv) Reliability Issues

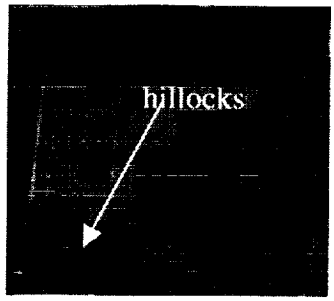


Figure 5-9: Hillocks caused by wet etchants.

Bulk micromachined devices have reliability concerns that vary with the processes used to fabricate them. One problem with using wet etchants is that they create sharp corners in silicon. These corners are natural stress concentration points that will weaken the strength of a structure. The use of chemical etchants can also lead to rough features on the surfaces of processed structures. The features, called hillocks in the literature, are a periodic undulation in the silicon. The presence of hillocks, which has been measured as high at 10μm, precludes many electrostatic devices from operating properly. Furthermore, hillocks create natural stress concentation points that are more likely to fragment over time, which can create destructive free particulates in the MEMS device.

Dry etching can have reliability problems caused by the reactive ion etch. While the sidewalls created by these etches are intended to be vertical, they often have irregular features. Poor control over the conditions inside the etching machine can lead to unintended geometric effects on finished devices, as shown in Figure 5-10. A study conducted at Carnegie-Mellon University[168] has shown that the O_2 flow rate, pressure, and RF power density of the RIE machine can influence the formation of different sidewall features. Devices produced that have these uneven sidewall features will have questionable reliability characteristics, as these features are indicative of a poorly

controlled process line. Devices with these features will also depart from predicted operational characteristics and, as a result, devices made with dry etches need to be screened for these characteristics. One positive feature of using an RIE system is that it produces more rounded corners than wet etching. As a result, these structures are not as prone to fracturing as wet etched devices.

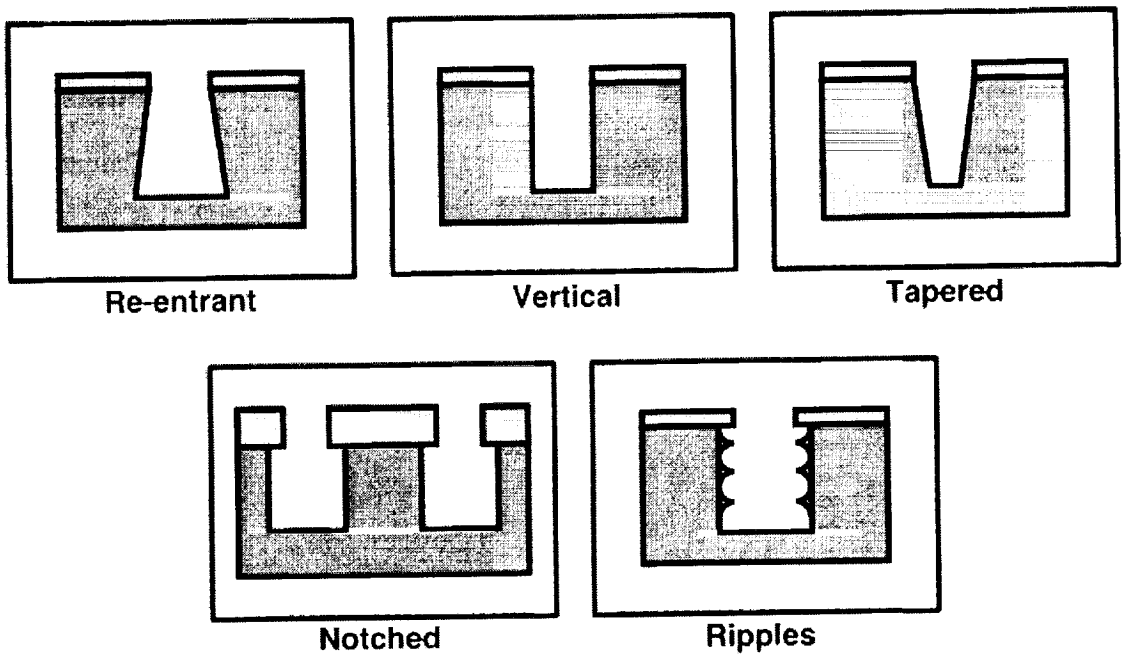


Figure 5-10: Possible sidewall features created by a poorly controlled RIE. (from [181])

B. Surface Micromachining

Surface micromachining is a process that offers many advantages and disadvantages different from bulk micromachining. Surface micromachining differs from bulk processes in that devices are fabricated entirely out of thin film materials. One of the most attractive features of this process is that it, like reactive ion etching, does not suffer from the 54.7° feature enlargement common to bulk micromachining with wet etchants. A key design feature of surface micromachining is the choice of structural and sacrificial thin films.

A typical surface micromachining process starts with a silicon substrate passivated by silicon nitride. Upon this substrate, a thin film of sacrificial oxide is deposited. This film is then patterned according to the device's design. After this, a layer of thin film polysilicon is deposited to form the structural material. The most common method of deposition is through LPCVD, which can either produce polycrystalline or amorphous silicon films depending upon reaction temperature. This process allows tight control over the residual stress in the films. After this, the oxide layer is often removed by immersing the structure in a HF solution. For most surface micromachining, the process of depositing a layer of oxide, followed by a layer of polysilicon will be repeated several

times to produce multi-layered structures. Figure 5-11 shows a common process developed by MCNC that uses three layers of polysilicon.[144]

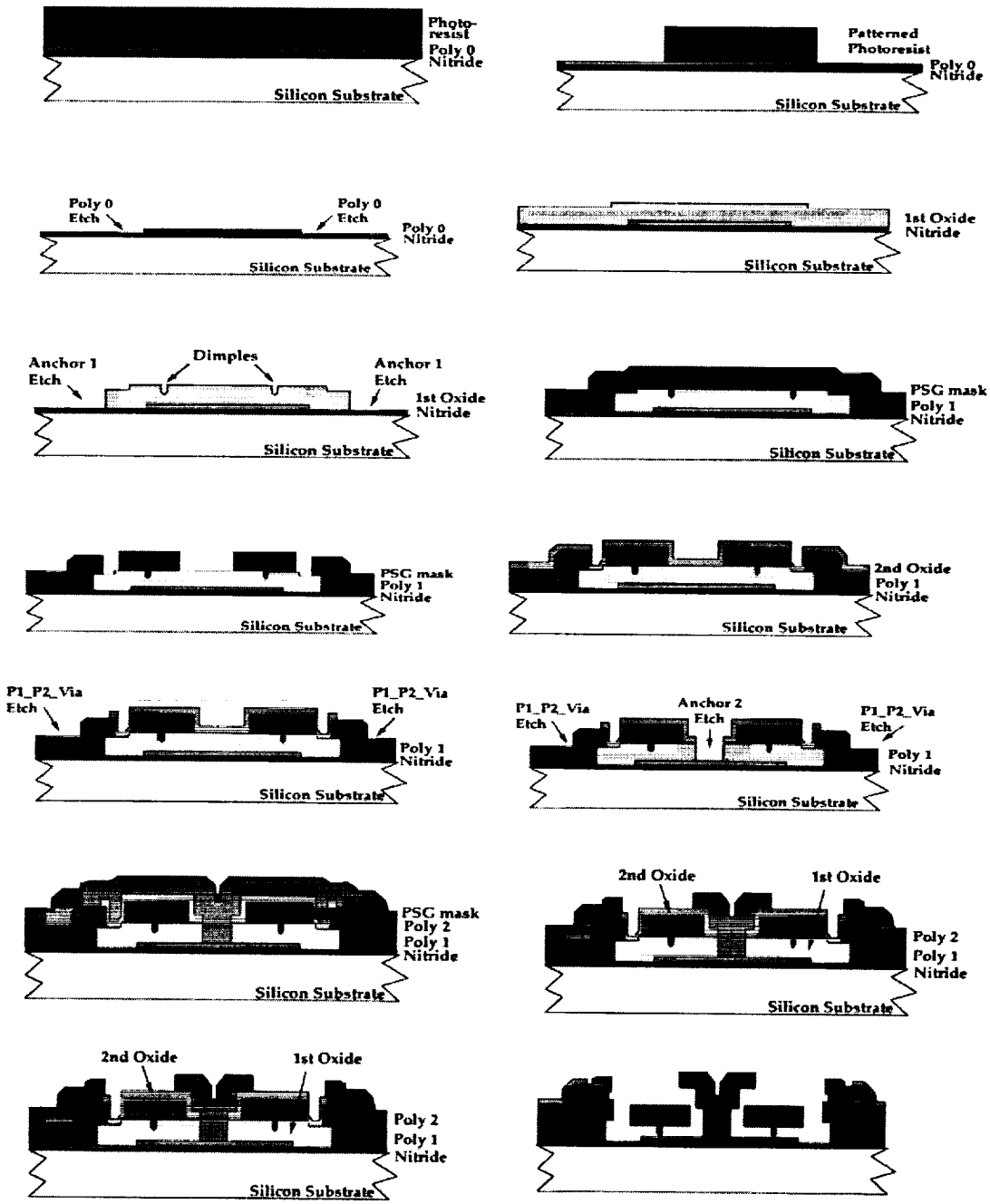


Figure 5-11: The surface micromachining process using three layers of polysilicon. (from [144])

The ability to layer structures in surface micromachining has piqued the interests of many researchers. It allows for the construction of structurally complex sensors that are difficult to fabricate with bulk processes.

i) Reliability Issues

Another consideration that needs to be addressed in these devices relates to their mechanical properties. While bulk materials have well understood properties, the mechanical attributes of surface micromachined devices depend upon thin film processing conditions. To ensure reproducible devices, these conditions must be well controlled. In particular, many of the materials used in these devices have large built-in stresses which affect the performance of the device to a variable degree (Figure 5-12).

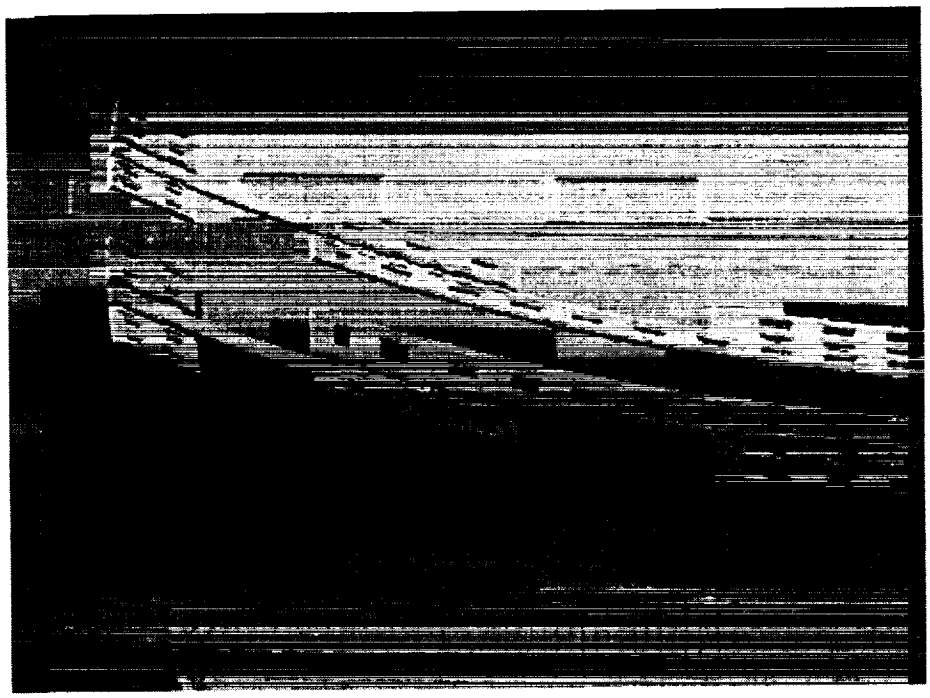


Figure 5-12: MEMS structure with a large residual stress. (from JPL)

Surface micromachined devices also have adhesion problems that are inherently worse than bulk micromachining. Cantilever beams are produced in surface micromachining on top of a sacrificial oxide layer, which is removed by immersion in an HF bath. Then the structure is cleaned in de-ionized water. After this, a of 5-30Å thick oxide layer will form on the surface of the polysilicon. There will also be hydroxyl groups in the oxide layer, which have a high surface energy. This makes the oxide layer extremely hydrophilic, which creates a strong capillary force between the beams and the substrate. This capillary force will pull the beam to the substrate and create an adhesive bond between the beam and the substrate.

There are several methods now used to prevent released structures from bonding to the substrate. Several groups, including those led by R. Howe at Berkeley and N. Tien at Cornell, utilize a thin film of self assembled monolayers on the surface micromachined device. The monolayers are hydrophobic, which creates a repulsive force between the substrate and the suspended structures, which effectively prohibits adhesive bonds from forming. However, it remains unclear what impact the monolayers will have on the long term reliability of these devices. Another method that prevents the creation of adhesive bonds involves using polyimide as a sacrificial material. This technique, developed by Gregory Kovacs at Stanford University, utilizes aluminum structures that are released in an oxygen gas. Since this process does not utilize any liquids, no adhesive bonds are formed.

C. LIGA

LIGA is a German acronym that stands for lithography, electroplating, and molding. LIGA was developed to produce high aspect ratio structures. LIGA offers some unique properties that makes it an interesting technology. LIGA enables the construction of structures with the thickness of bulk micromachining with a degree of design freedom similar to surface micromachined devices. This technology offers structures several hundred microns thick, with a minimum feature size of only a few microns.

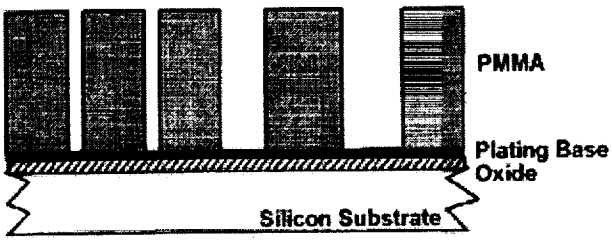


Fig. 1 Fabrication is done on a (100) silicon wafer with a 0.5μm oxide layer. A plating base is formed by sputtering 300nm of Ti and 5000A of Cu with a top layer of 300A Ti. The Ti and Cu also act as a release layer. Thick photoresist is applied and exposed using x-rays from a synchotron and developed with a solvent.

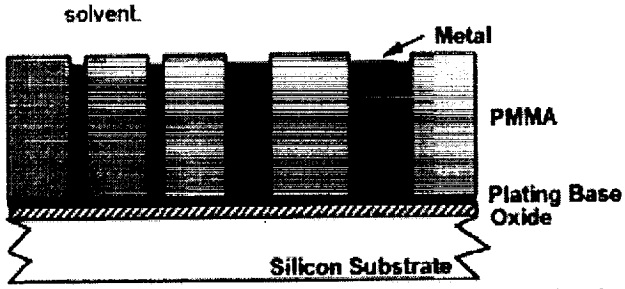


Fig. 2 The desired metal, in this case nickel, is electroplated onto the substrate, filling the voids in the PMMA.

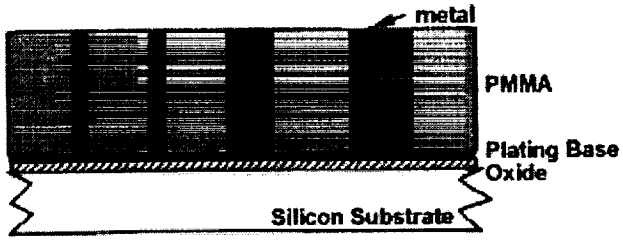


Fig. 3 The metal and PMMA are milled back to produce a uniform top surface.

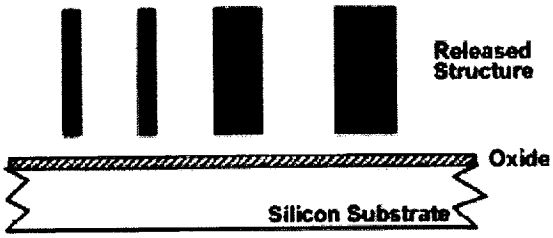


Fig. 4 Finally, the PMMA is removed. If desired, the customer can release the structures from the substrate by etching away the plating base in an NH_4O_2/H_2O_2 solution.

Figure 5-13: The basic LIGA process. (from [144])

The LIGA process begins by depositing a layer of thick photoresist, usually polymethyl methacrylate, or PMMA, that is between 300 and 500 μm thick onto a conductive substrate. The PMMA is then patterned with short wavelength radiation from an X-ray synchrotron source for several hours. Then a layer of metal is electroplated onto the

exposed area of the conductive base plate, which fills in the open areas created by the patterning. Then the metal structure is separated from the PMMA mold, as shown in Figure 5-13. This metal structure can in turn be used as a mold insert for injection molding to form multiple plastic replicas of the original plating base. These plastic replicas can then be used to make multiple copies of the original structure.

The LIGA technique involves some advances beyond semiconductor processing. The X-ray source must be capable of delivering at least 1 GeV of energy at wavelengths shorter than 7 Å. To withstand this bombardment, the opaque part of the mask must be constructed out of a material with a high atomic number. Furthermore, the transparent part of the mask must have a low atomic number to allow the photons to pass through without heavy absorption and scattering. Successful masks have been made with 3 μm thick gold in the opaque region and 1 to 2 μm thick silicon nitride or titanium foil in the transparent region. Another hurdle to overcome is the electroplating of the patterned structure. This step requires accurate controlling of current density, temperature, concentration, and composition of the plating solution to prevent the formation of hydrogen bubbles, which can ruin a structure. These conditions also determine the internal stress of the device and thus must be well understood and controlled to ensure reliable device operation.

i) Reliability Issues

LIGA, as a relatively costly technology, has not been researched as fully as other MEMS processes. As a result, the LIGA process can have great variability across process runs. Another problem with LIGA is that the injection molding process and mold separation processes require almost perfectly vertical structures. This issue has become a strong factor in the device yield of LIGA technology.

D. GaAs Processing

The processing of gallium arsenide can be as varied as silicon processing. While there are many GaAs processes that are very similar to those of silicon, there are some techniques that are unique to GaAs. These GaAs processing techniques are an offshoot of bulk micromachining that utilizes the unique properties of GaAs and its ternary alloy AlGaAs to produce structures.

One method of processing GaAs wafers is to use ion implantation. The first step is to layer an implantation mask. Then a layer of N ions is implanted into the substrate. The depth that they travel into the substrate is a function of accelerating voltage. Then the mask is removed and the sample is annealed at 750°C for about 30 minutes while covered with PECVD Si_3N_4. This process recrystalizes the buried layer to a $GaAs_{1-x}N_x$ layer. Then a SiO_2 etch mask is evaporated onto the surface of the wafer. Then an

anisotropic etch is performed to expose the buried layer. Finally a selective etch is used to remove the buried layer. This process is illustrated in Figure 5-14.

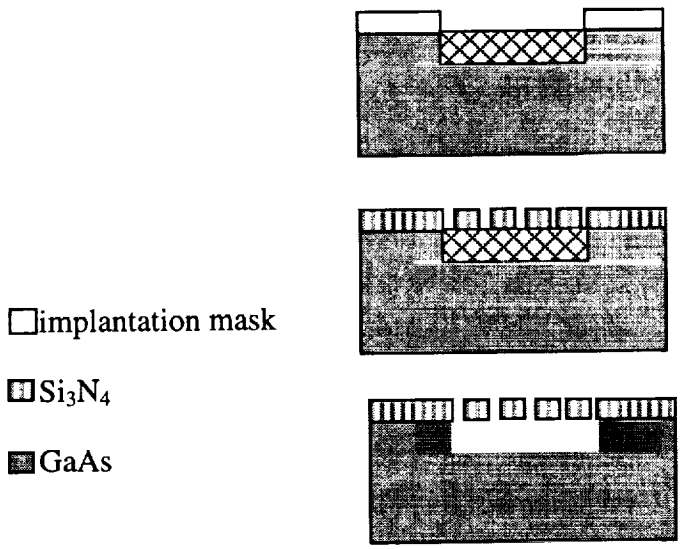


Figure 5-14: Fabrication of a suspended structure in GaAs. First a layer of N ions is implanted into the substrate, then a Si_3N_4 structure is patterned on top. Finally the N ion layer is selectively removed, leaving a suspended structure.

Another GaAs process used in producing microstructures is to micromachine through the use of epitaxy. This process utilizes the chemical difference between GaAs and $Al_xGa_{1-x}As$ in order to gain the desired results. The first step to this process is to use epitaxial growth to produce an undoped $Al_xGa_{1-x}As$ layer on top of a GaAs wafer. Then a Si_3N_4 etch mask is applied to the back side of the wafer. This mask then allows the full removal of the GaAs by using an H_2O_2/NH_4OH solution, which leaves only a thin membrane of $Al_xGa_{1-x}As$ as shown in Figure 5-14.[21]

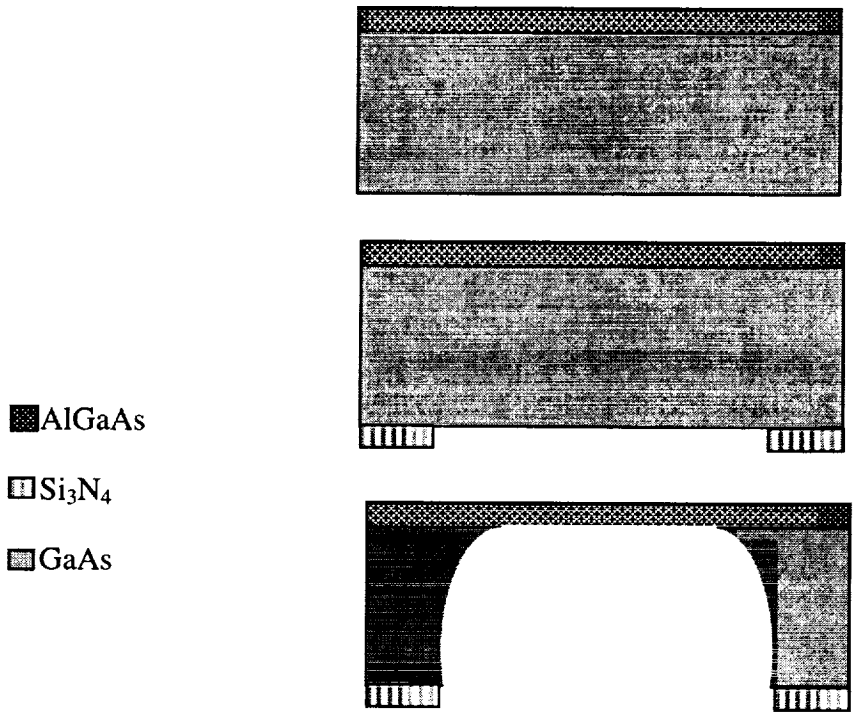


Figure 5-15: Fabrication of an AlGaAs membrane. The first step in this process is to epitaxially grow a AlGaAs layer on the GaAs substrate. Then a Si_3N_4 etch mask is used to etch away the back side of the structure.

i) Reliability Issues

One issue that is an area of concern in GaAs processing is the internal film stresses created by thermal mismatch in GaAs-$Al_xGa_{1-x}As$ heterostructures. Epitaxial growth is a high temperature process which will, even though the lattice parameters of these two compounds are well matched, create a strain from differing expansion coefficients.

III. Additional Reading

Sze, S. M. ed., Semiconductor Sensors, Wiley Inter-Science, New York, 1994.

S. A. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, Oxford, 1996.

Chapter 6: Common Device Elements

B. Stark

While a completed MEMS is a complicated device, the individual components of any given system are much simpler to understand. Due to the nature of MEMS processing, no single component can be very complex. This in turn means that understanding of a MEMS device can be gained through knowledge of a few simple parts and understanding how they interact. To ensure the reliable operation of a MEMS device it is sufficient to ensure the reliable operation of all the constituent parts.

One of the difficulties in writing a guideline is trying to select material that will not be dated before the book goes to press. To preclude this problem, this chapter does not address specific sensor technologies, but rather it deals with device elements. It is assumed that a knowledgeable reliability engineer can construe all the necessary information on, for example, a capacitive accelerometer by examining the sections on structural beams and parallel plate capacitors. It is felt that this arrangement of the material will increase its useful lifetime.

This chapter has been loosely organized into three sections. The first three subchapters discuss structural elements in MEMS. The next two subchapters, along with part of the third, discuss transducer elements. The remainder of the chapter is dedicated to actuator technologies.

I. Structural Beams

Structural beams are a basic building block of most MEMS devices. A beam is, as the name implies, a long thin piece of material that often serves as the supporting basis for a structure. While this is fairly self-evident, there are also some commonalities specific to MEMS beams that are useful to understand. The majority of beams used in MEMS have the rectangular cross section defined below:

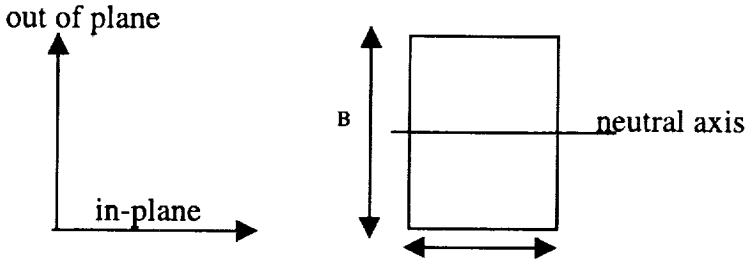


Figure 6-1: Cross section of common MEMS beams. Dimension A is planar and is limited by the minimum feature size of the processing technology. Dimension B is non planar and is limited by the aspect ratio of the etching technology.

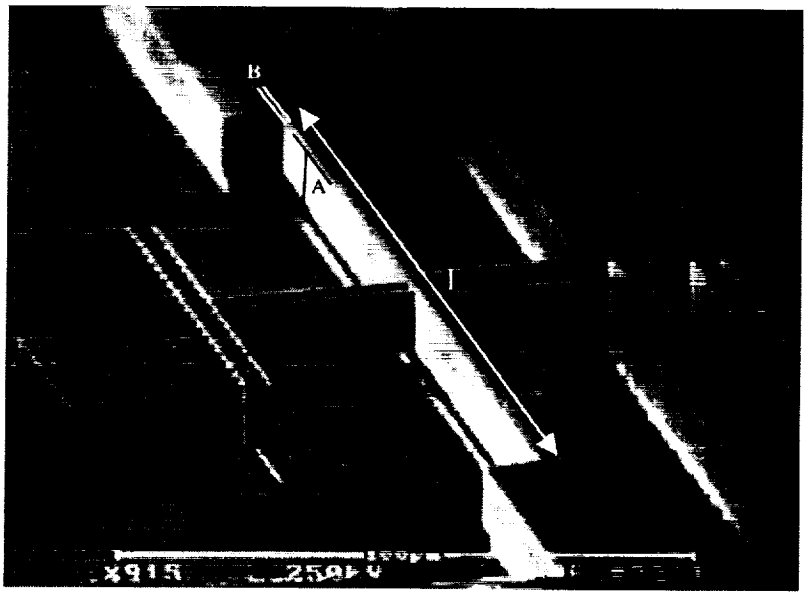


Figure 6-2: SEM picture of beam with all dimensions labeled. (from [155])

A SEM picture of a beam is included in Figure 6-2 to show the usual labels given to each beam dimension. It should also be noted that the rectangular cross section is a

generally accepted approximation, as there are multiple non-uniform features introduced in device construction. In some cases, such as beams made with wet etching and certain CMOS processes, the cross section is more trapezoidal than rectangular. However, once the basic shape of the beam is determined, it is relatively simple to construe its mechanical properties.

A. Structural Analysis of Support Beams

i) Static Deflections

Support beams are analyzed for both reliability and performance using techniques common to most engineering students. One issue critical to understanding beams is understanding how they bend under different loadings. The most common method to determine this involves the Euler-Bernoulli equation:

$$\frac{d^2y}{dx^2} = \frac{M(x)}{EI} \tag{6-1}$$

where

x = direction along the neutral axis

y = direction along the transverse axis

E = Young's modulus

I = area moment of inertia

M(x) = the bending moment in the beam, which is usually a function of x.

As this definition may be a bit obtuse, Figure 6-3 illustrates the concept being described.

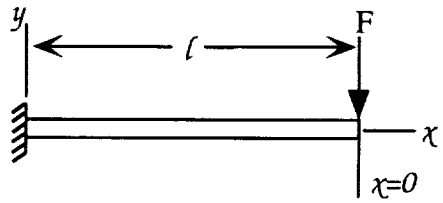
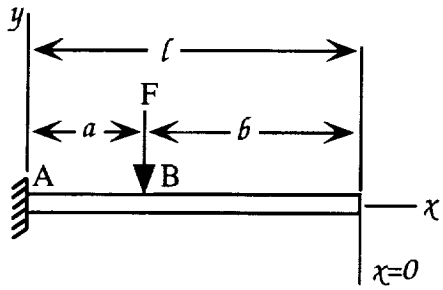
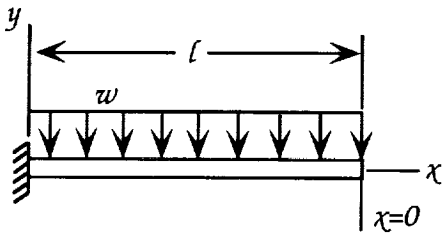
Beam Configuration	Vertical (y) Displacement
	$y(x) = -\frac{F}{EI}\left(\frac{x^3}{6} - \frac{l^2 x}{2} + \frac{l^3}{3}\right)$ $y_{max} = -\frac{Fl^3}{3EI}$
	$y_{AB} = -\frac{F}{EI}\left(\frac{(x-b)^3}{6} - \frac{a^2 x}{2} + \left(\frac{la^2}{2} - \frac{a^3}{6}\right)\right)$ $y_{BC} = -\frac{F(b-x)}{EI}\left(\frac{a^2}{2}\right) - \frac{F}{EI}\left(\frac{ba^2}{2} + \frac{la^2}{2} - \frac{a^3}{6}\right)$ $y_{max} = -\frac{Fb}{EI}\left(\frac{a^2}{2}\right) - \frac{F}{EI}\left(\frac{ba^2}{2} + \frac{la^2}{2} - \frac{a^3}{6}\right)$
	$y = -\frac{w}{24EI}(x^4 - 4l^3 x + 3l^4)$ $y_{max} = -\frac{wl^4}{8EI}$

Figure 6-3: Displacement of loaded cantilever beams.

To analyze the deformation of a beam under transverse loading, Equation 6-1 is integrated twice using the appropriate boundary conditions. This yields the result:

$$y(x) = -\frac{1}{EI}\iint M(x)dxdx + Cx + D \qquad (6\text{-}2a)$$

$$y'(x) = -\frac{1}{EI}\int M(x)dx + C \tag{6-2b}$$

where C and D are constants determined by the boundary conditions.

For a cantilever beam, which is one of the most structural beams in MEMS, with the boundary conditions of y(l)=0 and y'(l)=0 and a force, F, applied at one end, the equation yields:

$$y(x) = -\frac{F}{EI}\left(\frac{x^3}{6} - \frac{l^2 x}{2} + \frac{l^3}{3}\right) \tag{6-3}$$

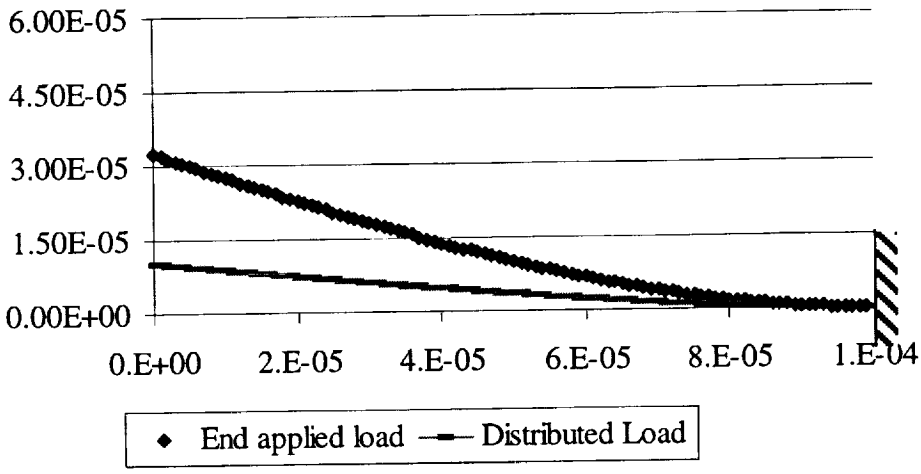


Figure 6-4: Graphical representation of a cantilever beam deforming under a transverse load.

Figure 6-3 contains the equations describing cantilever deflections under other common loading conditions. This analysis also leads to another piece of information that is useful to understand. Since Equation 6-3 describes a linear force-deflection relationship, it is essentially describing a spring reacting to an applied load. This means that it is possible to extract a spring constant, k, from this expression. Evaluating y(x) at a specific point will determine the spring constant. For this example y(0), which is equal to $-Fl^3/3EI$, will be used. Rearranging this equation yields:

$$\frac{F}{y(0)} = -\frac{3EI}{l^3} \tag{6-4}$$

and, since F/y = k, this gives the result:

$$k_y = \frac{3EI}{l^3} \tag{6-5a}$$

The value of I can either be determined by integration or by tables. For rectangular cross sections and planar bending, I is $a^3b/12$ and Equation 6-5a is rewritten as 6-5b. If a non-homogenous beam is used, then the method introduced in Chapter 5-2C describes how to normalize this beam to a uniform cross section.

$$k_y = \frac{Ea^3b}{4l^3} \tag{6-5b}$$

While this expression is useful for predicting displacement under a given load, there are some limitations to it that must be understood. Hooke's law of $F_x=kx$ only applies for small displacements. For larger displacements, non-linear terms will appear in the force-displacement equations. The degree to which this equation applies thus depends largely upon how large a force is applied to the structure. Often, to simplify the development of devices, designers will construct structures that will operate solely within the linear regime. However it is important to understand that the linear force-displacement equation is only a first order approximation of the actual relationship between force and displacement.

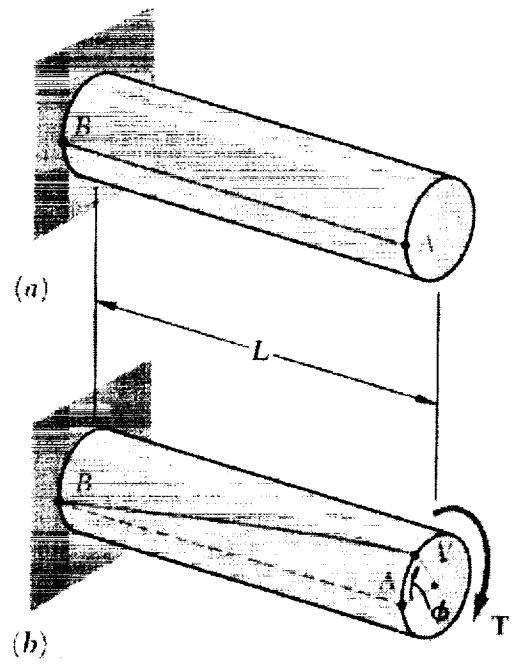


Figure 6-5: Beams displacing an angle, ϕ, due to an applied torque. (from [11])

For some applications, especially those involving non-planar displacements, it is necessary to subject structural beams to a torque. There are methods for analyzing rigid bodies under a torsional load, an example of which is shown in Figure 6-5. For these applications, it is useful to relate a torque to the angle of twist, ϕ, which can be accomplished with the expression:

$$\phi = \frac{TL}{c_2 G a^3 b} \tag{6-6}$$

where

T = applied torque

c_2 = a constant defined in Table 6-1

b/a	c_1	c_2
1.0	0.208	0.1406
1.5	0.231	0.1958
2.0	0.246	0.229
2.5	0.258	0.249
3.0	0.267	0.263
4.0	0.282	0.281
5.0	0.291	0.291
10.0	0.312	0.312
∞	0.333	0.333

Table 6-1: Constants for rectangular cross sections under a torsional load.[11]

As might be expected, there is also a torsional stiffness related to beam geometry that is useful in analyzing non planar actuators. This stiffness, k_ϕ is defined by:

$$k_\phi \equiv \frac{T}{\phi} = 2c_2 G \frac{a^3 b}{l} \tag{6-7}$$

ii) Oscillatory Motion

As structural beams are often operated in resonant modes, it is necessary to analyze the oscillatory motion of beams. Resonant frequency[1] is determined by the equation:

[1] The terms "resonant frequency" and "natural frequency" are used interchangeably in this section. Although this is common in the literature, these are actually two distinct quantities. The relationship between resonant and natural frequency is discussed in detail in Section 3-VII.

$$\omega_0 = \sqrt{\frac{k}{m_{eff}}} \qquad (6\text{-}8)$$

where

k = stiffness or spring constant

m_{eff} = moving mass

The only two quantities required to determine the natural frequency of a beam are k and m_{eff}. Since k has already been derived, it is necessary to calculate the moving mass. The moving mass can be analytically determined using Rayleigh's method. However, this method exceeds the scope of the guideline. It suffices to know that, for a cantilever beam, the moving mass is roughly 23% of the total mass. This can be analytically described by

$$m_{eff} = .23\rho abl \qquad (6\text{-}9)$$

where ρ is the mass density of the beam. This leads to a final expression for resonant frequency:

$$\omega_0 = 1.043\frac{a}{l^2}\sqrt{\frac{E}{\rho}} \qquad (6\text{-}10)$$

In cases when beams oscillate in torsion, the torsional resonant frequency is:

$$\omega_0 = \sqrt{\frac{k_\phi}{I_\phi}} \qquad (6\text{-}11)$$

Since beams driven by harmonic transverse loads behave similarly to strings in tension, the wave equation can describe analytically how a beam moves in resonance:

$$\frac{\partial F}{\partial x} = -\frac{m}{l}\frac{\partial^2 y}{\partial t^2} \qquad (6\text{-}12a)$$

Through a substitution of the force for an expression involving the moment, this equation becomes:

$$-\frac{\partial^2}{\partial x^2}\left(EI\frac{\partial^2 y}{\partial x^2}\right) = \frac{m}{l}\frac{\partial^2 y}{\partial t^2} \qquad (6\text{-}12b)$$

This equation describes the curvature of a beam as a function of time. Through the study of differential equations, Equation 6-12b is solved as:

$$y = (A_1 \sin(Kx) + A_2 \cos(Kx) + A_3 \sinh(Kx) + A_4 \cosh(Kx))\cos(\omega t + \Theta) \qquad (6\text{-}13)$$

where

A_n = constant determined by the boundary conditions

$$K^4 = \frac{\omega_n^2 m}{EIl}$$

This reveals that, at resonance, a beam will oscillate in a sinusoidal fashion, with the shape of the beam determined by the boundary conditions:

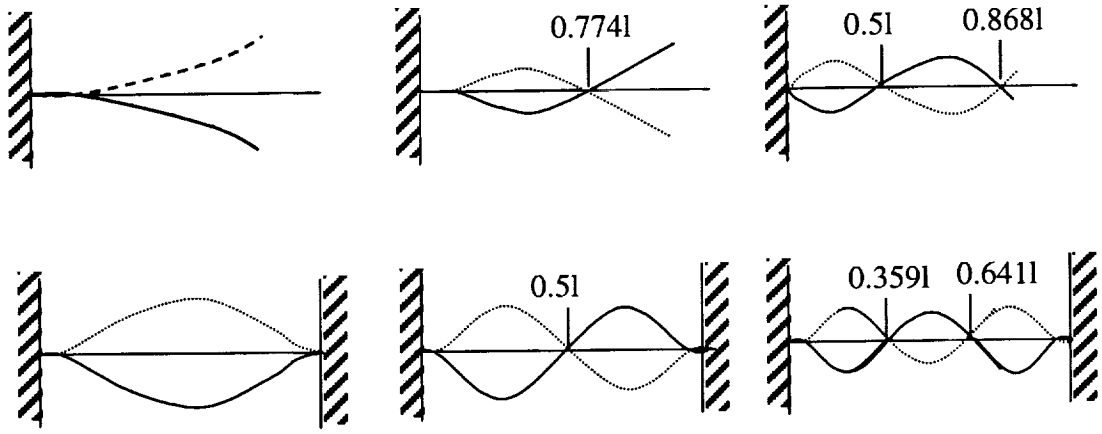


Figure 6-6: Oscillatory modes for cantilever beams (top) and built-in beams (bottom).

While using the above techniques will determine the shape of beams under a variety of loads, different methods will have to be introduced to insure that the beams will not fail under the stresses caused by these loads.

B. Failure of Structural Beams

A structural beam will fail when the maximum allowable stress has been exceeded. For different types of materials, different failure modes are exhibited, as discussed in Chapter 3. However, for reliable operation, the stresses in materials should not approach either yield or ultimate stress. There are several methods useful for calculating stresses in materials.

The normal stress, σ_x, is easy to calculate. It can be determined by the relationship:

$$\sigma_x = \frac{My}{I} \tag{6-14}$$

where y is the vertical distance from the neutral axis.

While this equation is valid for small deformations, for large deformations, the slope of a beam at the loading point[1], $\left.\frac{dy}{dx}\right|_l$, becomes important. For large deflections the maximum stress is:

$$\sigma_{\max}^{large} = \frac{y}{I}\sqrt{\frac{2EIM\left.\frac{dy}{dx}\right|_l}{l\left(1-\nu^2\right)}} \tag{6-15}$$

The ratio of $\sigma_{\max}^{small} / \sigma_{\max}^{large}$ is compared to get an estimate in the error in using the linearized approximation of Equation 6-14. One study [40] found the error to be 5% at $\tan^{-1}\left(\left.\frac{dy}{dx}\right|_l\right) = 30°$, 11% at 45° and 22% at 60°. So, the extent to which a linear approximation is valid depends upon the size of the deflection, as one would expect.

Determination of shearing stress is slightly more difficult. Shearing stress is calculated by examining a section of a beam and using the equation:

$$\tau_{ave} = \frac{VQ}{It} \tag{6-16}$$

where

τ_{ave} = average shearing stress in a section of the beam

V = vertical shear in a given cross section

t = thickness of the cross section

Q = 1st moment of the area defined as $Q = \int_{y=y1}^{y=C} ydA$

[1] This derivation assumes a concentrated load.

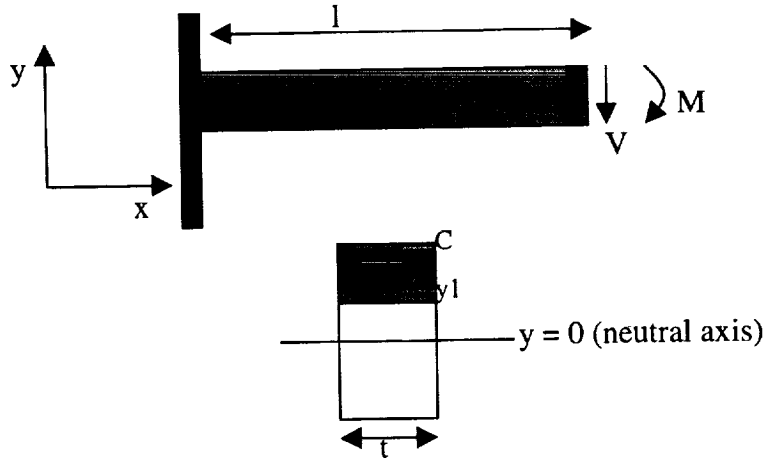


Figure 6-7: Side (top) and cross sectional (bottom) views of cantilever beam under shear force and bending movement.

The relationship among all of these values is presented in Figure 6-7. To determine $\tau_{max,}$ it is usually necessary to examine τ_{ave} as a function of y. For beams with the height > 4×width, the approximation of τ_{max}=1.5×V/(w×h) is useful. However, for planar bending in beams, where the b ≥ a relationship obviates this approximation, the full structural analysis will have to be performed. It is convenient to recognize that maximum shearing stress will always occur along the neutral axis, unless there are marked variations in beam thickness. Thus, determination of shearing stress in beams can usually be performed simply by examining τ_{ave} at y=0.

For rectangular beams subjected to a torque, there will be a shear stress that will vary as a function of horizontal and vertical position. However the study of mechanics reveals that the maximum stress, which is the most important in terms of structural analysis, occurs along the neutral axis of the wider face of the beam, which, in this discussion, is labeled as b. This maximum shearing stress is determined by the relation:

$$\tau_{max} = \frac{T}{c_1 a^2 b} \tag{6-17}$$

where c_1 is a constant defined in Table 6-1.

While using the above analysis leads to a good understanding of when fracture will occur, there are other failure modes in structural beams. Beams will usually fail if they come into contact with other structures, due to adhesive forces. To analyze the probability of this, the deflection of every beam must be considered under maximum load.

Another concern raised in Chapter 3 was the impact of fatigue in beams. Over long cycle times, the properties of beams will shift, which, as this section has shown, will change the static and resonant characteristics of the structures. These changes will alter the output of many sensors based upon measuring frequency and deflection. Another fatigue related mechanism is the gradual relaxation of the fracture strength of a material. Beams that were initially driven within stress tolerances of a material, can be driven past them, as the tolerances decrease. Although it should be noted again that this mechanism has yet to be observed in silicon.

Thermal changes can also have an impact upon beam reliability. Thermal stressing and unstressing creates mechanical fatigue in beams. In large temperature changes, as experienced in the space environment, most MEMS beams will also experience bimetallic warping due to the fact that they are made of different materials that have mismatched thermal coefficients of expansions. Thermal fatigue can also contribute to delamination.

C. Additional Reading

F. P. Beer and E. R. Johnston, Mechanics of Materials: Second Edition, McGraw-Hill. New York, 1992.

C. M. Harris and C. E. Crede, Shock and Vibration Handbook Volume 1: Basic Theory and Measurements, McGraw-Hill Book Company, Inc., New York, 1961.

II. Thin Membranes

In recent years, thin membranes have found increasing use in pressure and flow sensors. They provide a large sensing area coupled with low mass, which is advantageous in many applications. A membrane is commonly assumed to be any structure with a z dimension much smaller than its x and y dimensions. While the membranes used in MEMS do not fit the classic definition of plates, their thickness deformation can be influenced by in-plane tension. This term is also applied to these devices. A membrane structure is shown in Figure 6-8. The analysis of a membrane is more difficult than cantilever beams, but it is still tractable.

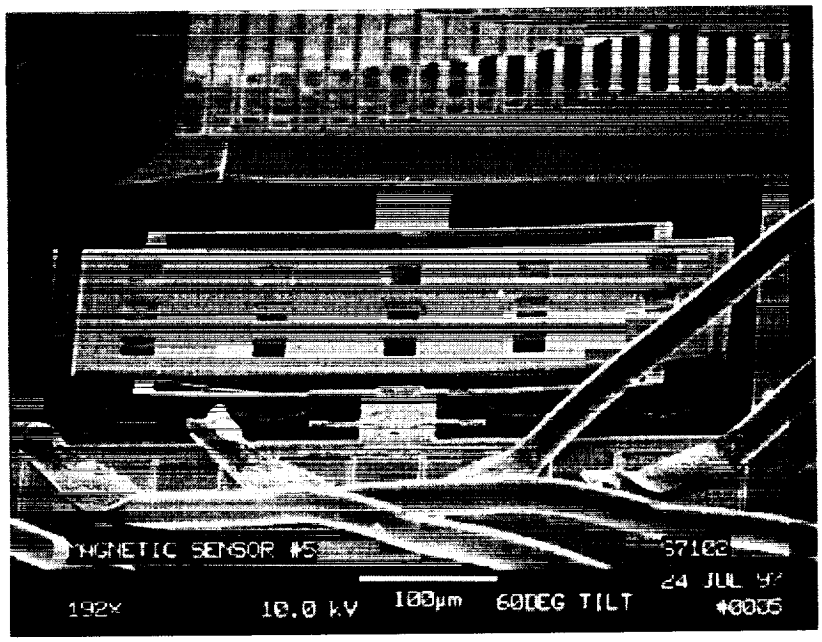


Figure 6-8: A thin plate viewed at 200x magnification. (from JPL)

A. Structural Analysis of Membranes

i) Static Deflection

There are several methods commonly employed in the analysis of thin plates or membranes. The most obvious method is to use the equations of motion to describe the plate, as was done for beams. This is accomplished by defining coordinates for the plate in the x and y axis and taking into account all shearing and bending forces. This analysis leads to a system of six equations and six unknowns which reduces to the result:

$$\nabla^4 w = \frac{q}{D} \tag{6-18}$$

where

$$\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2}$$

w = the plate deflection at any given point

q = the lateral load function

D = the plate stiffness = $\frac{Eh^3}{12(1-\nu^2)}$

h = the plate thickness

The solution of this equation clearly requires determining the function w, such that it satisfies both the loading and boundary conditions. Since empirical data shows that these models are not the most accurate, the method developed by J.Y. Pan[14] is often used. This method begins by determining the midpoint deflection of a membrane, w_0. For a square membrane there is a relationship between midpoint deflection and an applied pressure p given by:

$$p(w_0) = C_1 \frac{h\sigma}{a^2} w_0 + C_2 \frac{hE}{a^4} w_0^3 \text{ [14]} \tag{6-19}$$

where

σ = internal stress

a = plate width

w_0 = plate deflection at center point

C_1,C_2 = functions of Poisson's ratio, defined in Figure 6-9a

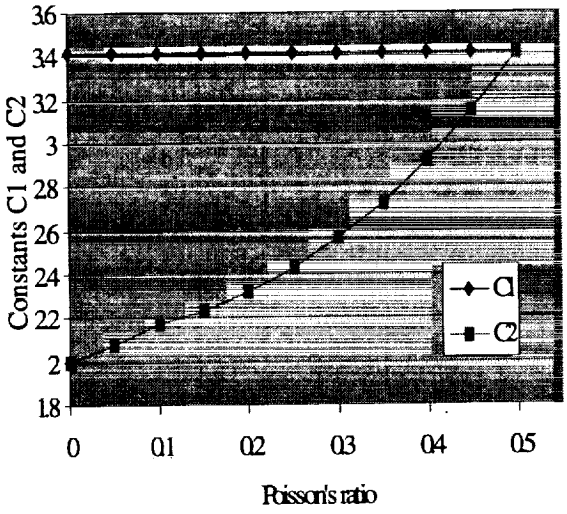


Figure 6-9a: Dependence of C_1 and C_2 upon Poisson's ratio.[15]

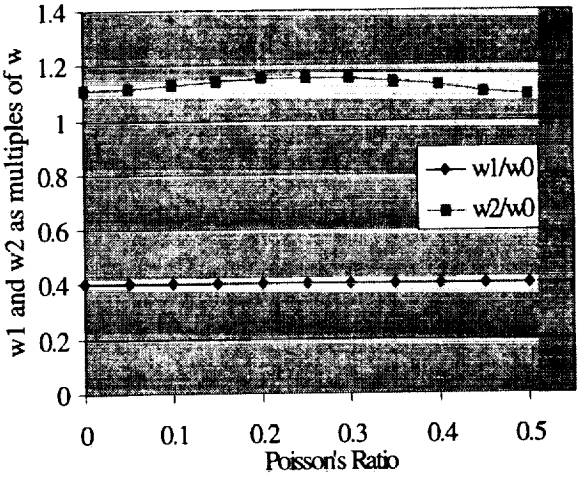


Figure 6-9b: w_1/w_0 and w_1/w_0 as a function of Poisson's ratio.[15]

Once w_0 is known, it is possible to determine the shape of the entire plate. If the origin of the plate is taken at its geometric center, then the deflection is described by:

$$w(x,y) = \left(w_0 + w_1 \frac{x^2 + y^2}{a^2} + w_2 \frac{x^2 y^2}{a^4} \right) \cos\left(\frac{\pi x}{2a}\right) \cos\left(\frac{\pi y}{2a}\right) \qquad (6\text{-}20)$$

where w_1 and w_2 are functions of Poisson's ratio related to w_0 by Figure 6-9b.

While this method has the attribute that it offers a closed form solution to the shape of the plate as a function of x and y, it is not always possible to solve the deformation of the plate so simply. In instances when the plate is not simply loaded or supported, it is often necessary to resort to other methods. Among the most common of these is to numerically model the membrane. This process, known as the method of finite differences, separates the plates into discrete points and analyzes the plate piecewise. This method is discussed in detail in Chapter 7.

ii) Lamb Waves

Engineers also utilize waves on plates as transducers. There are two kinds of waves that travel in plates. They are dilation waves, which involve changes in volume without rotation, and distortion waves, which do not change volume but instead result in rotation and shearing of a given material. In more common terminology, the dilation wave is referred to as a longitudinal wave, while the distortion wave is often called a

transverse or shear wave. These waves travel with a velocity that is material dependent and the respective velocities of each, c_1 and c_2, are related by the ratio:

$$\frac{c_2}{c_1} = \sqrt{\frac{(1-2\nu)}{2(1-\nu)}} \tag{6-21}$$

given that:

$$c_1 = \sqrt{\frac{\lambda + 2G}{\rho}} \tag{6-22a}$$

$$c_2 = \sqrt{\frac{G}{\rho}} \tag{6-22b}$$

where λ is Lamé's Parameter, defined by $\nu = \frac{\lambda}{2(\lambda + G)}$

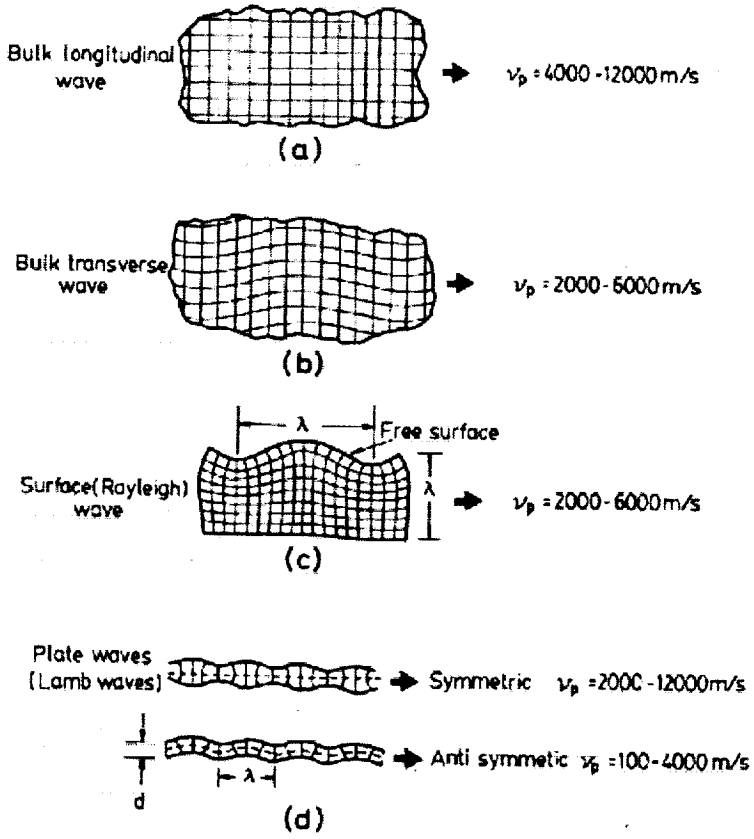


Figure 6-10: Wave propagation in solid media. (from [6])

In plates, these two waves interact in complex ways at the plate boundaries, which results in the formation of a plate wave, which is also called a lamb wave. These waves travel in either symmetric or anti symmetric modes as shown in Figure 6-10. The lowest order of these modes are very similar to surface acoustical waves, or SAW, that propagate along a semi-infinite medium. However, in thin plates, the lowest order symmetric mode is dispersionless and propagates much faster than a SAW on the same materials. The lowest order anti-symmetric mode, on the other hand, involves flexure and its wave velocity decreases monotonically to zero as the plate becomes infinitely thin.[51] Lamb waves travel with a phase and group velocity that is defined by:

$$v_{ps} = \sqrt{\frac{12D}{h^3\rho}} \quad v_{gs} = v_{ps} \tag{6-23a}$$

$$v_{pa} = \sqrt{wh\sqrt{\left(\frac{D}{h^3\rho}\right)}} \quad v_{ga} = 2v_{pa} \tag{6-23b}$$

where g and p represent group and phase, and s and a represent symmetric and anti-symmetric.

One of the interesting results of this analysis is that tension and wave velocity are coupled. If a small section of a plate is considered with dimensions, dx and dy, and a tension, T, in the x-direction, the out of plane force on the plate can be modeled by two forces, a stiffness and a tension:

$$dF_{zS} = -D\frac{\partial^4 w}{\partial x^4}dxdy \tag{6-24a}$$

$$dF_{zT} = T\frac{\partial^2 w}{\partial x^2}dxdy \tag{6-24b}$$

If these equations are combined and related to the acceleration of the membrane, the result is:

$$-D\frac{\partial^4 w}{\partial x^4}dxdy + T\frac{\partial^2 w}{\partial x^2}dxdy = Mdxdy\frac{\partial^2 w}{\partial t^2} \tag{6-24c}$$

where M is the mass per unit area of the membrane

If this equation is solved through separation of variables, one finds that the solution is:

$$w(x,t) = C_n e^{j(\omega_n t - k_n x)} \tag{6-25}$$

where

$$\omega_n = \frac{2\pi n}{P}\sqrt{\frac{1}{M}\left(t + \left[\frac{2\pi n}{P}\right]^2 D\right)}$$

P = period of the actuator that is oscillating the plate

n = integer representing the different modes of the device

This leads to the solution that the phase velocity is dependent on tension and mass:

$$v_p \approx \sqrt{\frac{T + \frac{2\pi n}{P} D}{M}} \tag{6-26}$$

As this analysis shows, the phase velocity is coupled to both the tension and mass density of the plate. This enables sensors that detect lamb waves to be sensitive to a wide range of different effects, with temperature and pressure changes being the more prevalent changes sensed. The advantage of using anti-symmetric lamb waves in sensors is that, on very thin plates, they have a phase velocity that is usually much slower than that of sound in most media. This allows these devices to transmit waves without dissipating large amounts of energy to the surrounding environment. In comparison to surface acoustic waves, which dissipate on the order of 1 dB per wavelength, lamb waves have extremely low loss mechanisms. In lamb waves, the disturbance to the surrounding medium only extends to a distance of $\lambda/2\pi$, which limits the acoustical energy loss. For an in-depth discussion of the physical properties of Lamb waves, Reference [115] treats the material more thoroughly.

iii) Modal Waves

While lamb waves have many applications in membranes, it is also useful to excite standing waves on plates. A standing wave, as opposed to a lamb wave, involves oscillations in fixed spots. These waves have maximum displacement at the resonant frequency of a device. On a resonating plate, there will be distinct spots called nodes, where vertical motion is essentially zero, and spots called anti-nodes, where oscillations are maximized. The analysis of standing waves begins with a dynamic version of Equation 6-18:

$$D\nabla^4 W = Mh\omega_n^2 W + N_x \frac{\partial^2 W}{\partial x^2} + N_{xy} \frac{\partial^2 W}{\partial x \partial y} + N_y \frac{\partial^2 W}{\partial y^2} \tag{6-27}$$

where

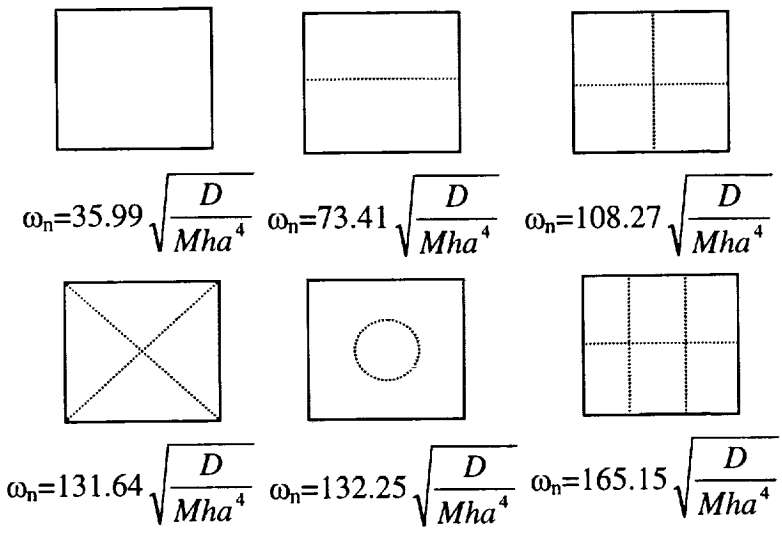


Figure 6-11: First six vibratory modes and resonant frequencies in a square plate with nodal lines shown.[54]

N_x, N_y = Normal loadings in the x and y directions

N_{xy} = shear loading

$W \equiv w = AW(xy)\cos(\omega_n t+\theta)$ where A is the oscillating amplitude

To solve this equation, the boundary conditions for W must be found that fit the end conditions. Since many square MEMS membranes are clamped on all sides, Figure 6-11 shows the modes and resonant frequencies of these structures. For other solutions to oscillating plate problems, Reference [54] offers an excellent analysis of plate mechanics.

B. Failure of Membranes

As membranes can be considered two dimensional equivalents of one dimensional beams, they have similar failure considerations. If Equation 6-18 is solved analytically, then the stresses on the plate are determined by the equations:

$$\sigma_x = -\frac{Ez}{1-\nu^2}\left(\frac{\partial^2 w}{\partial x^2}+\nu\frac{\partial^2 w}{\partial y^2}\right) \tag{6-28a}$$

$$\sigma_y = -\frac{Ez}{1-\nu^2}\left(\frac{\partial^2 w}{\partial y^2}+\nu\frac{\partial^2 w}{\partial x^2}\right) \tag{6-28b}$$

$$\tau_{xy} = \frac{Ez}{1+\nu}\frac{\partial^2 w}{\partial x \partial y} \tag{6-28c}$$

where z is the distance from the neutral axis of the plate

In order to determine the maximum stress in a plate, the following relationships are also useful:

$$M_x = -D\left(\frac{\partial^2 w}{\partial x^2} + \nu\frac{\partial^2 w}{\partial y^2}\right) \tag{6-29a}$$

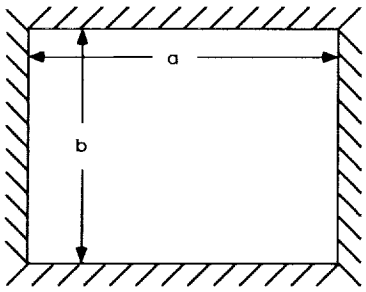
$$M_y = -D\left(\frac{\partial^2 w}{\partial y^2} + \nu\frac{\partial^2 w}{\partial x^2}\right) \tag{6-29b}$$

If the bending moments are known, the stress distribution can be calculated. Stress is zero along the neutral axis and rises linearly to a maximum at the surface. This maximum value is:

$$(\sigma_x)_{\max} = \frac{6M_x}{h^2} \tag{6-30a}$$

$$(\sigma_y)_{\max} = \frac{6M_y}{h^2} \tag{6-30b}$$

This analysis can be simplified for a membrane with a uniform loading, q, and fixed boundary conditions on all four sides. These structures will have the following stresses:



stress at center of long edge: $\sigma_{\max} = \frac{-\beta_1 q b^2}{t^2}$ (6-31a)

stress at center: $\sigma = \frac{\beta_2 q b^2}{t^2}$ (6-31b)

The parameters α, β_1 and β_2 are functions of the plate geometry and boundary conditions, and may be determined from the table below:

a/b	1.0	1.2	1.4	1.6	1.8	2.0	∞
β_1	0.3078	0.3834	0.4356	0.4680	0.4872	0.4974	0.5000
β_2	0.1386	0.1794	0.2094	0.2286	0.2406	0.2472	0.2500
α	0.0138	0.0188	0.0226	0.0251	0.0267	0.0277	0.0284

Table 6-2: Plate coefficients (four sides fixed)[1].

Solutions for other geometries and loading conditions are also available; the reader is referred to References [58] and [59] for additional information.

Another area of concern in plate mechanics is the effects of internal stress upon deflection and strength. As discussed in Chapter 3, thin films can often have large residual stresses. As this stress is coupled to temperature, changes in temperature will also affect the output of many membrane based sensors.

A problem with using lamb wave oscillators is that their sensitivity is coupled to a number of different changes. Using these devices in space applications will be especially difficult due to the fact that they are natural thermocouples. For lamb wave oscillators to have a future in the aerospace industry, it must be proven that they are sufficiently decoupled from many common aerospace phenomena, such as large temperature and pressure changes, to be effective transducers.

C. Additional Reading

Timoshenko, S. and Woinowsky-Krieger, Theory of Plates and Shells: 2nd edition, New York: McGraw-Hill, 1959.

I. A. Viktorov, Rayleigh and Lamb Waves: Physical Theory and Applications, Plenum Press: New York, 1967.

[1] The discussion on stresses on a bounded rectangular plate is adapted from work done by K. Man at JPL.

III. Hinges

In MEMS, there is a need for devices that can produce out of plane motion without the limitations of a torsional spring. In these instances, hinges are often used.

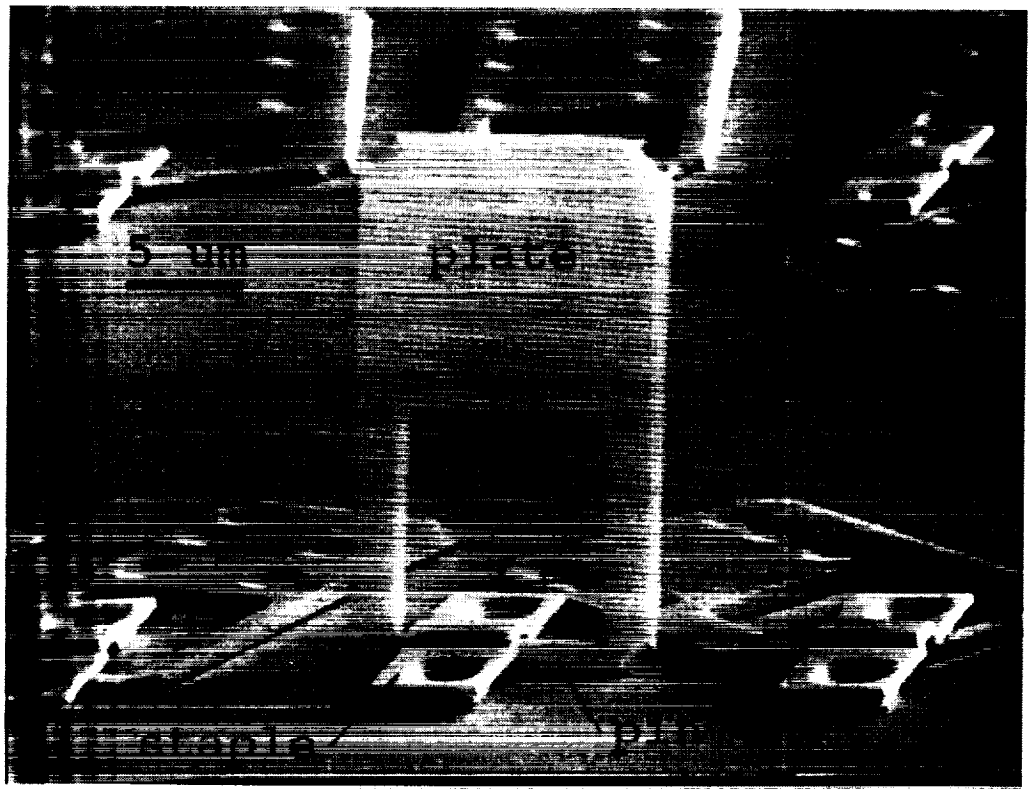


Figure 6-12: A typical hinge. (from [93])

In technical parlance, a hinge is an end condition that prevents translation of a structure, but allows free rotation. Often in MEMS, flexible structural beams that have hinged-boundary properties are called hinges. However, since the mechanical and reliability characteristics of these devices are similar to that of structural beams, there is no need to repeat that material here. It is enough to treat those devices as structural beams with narrow cross sections that create stress concentration at the interfaces with thicker beams.

This section will discuss surface micromachined non-planar hinges. These hinges can perform a multitude of tasks. One common implementation is to use hinges to hold structures, which were fabricated in a planar position, out of plane. Another common use of hinges is to bind non-planar structures together, as in the case of a cage or a box. This allows the fabrication of extremely high aspect ratio structures by common surface micromachining methods. This technology has enabled multitudes of new devices, such as optical devices and microgrippers. One of the biggest advantages of hinges is that they

enable devices to be both thermally and electrically removed from the substrate, which limits much of the noise common to planar sensors.[93]

A. Structural Analysis

A common hinge is depicted in Figure 6-12. These devices are simply constructed with only two parts. There are several types of hinges that were initially reported by Pister et. al. in [93], which are represented in Figure 6-13. 6-13a shows a substrate hinge, which is constructed out of a pin and a staple. The pin is a structural beam held down by the staple, which is a curved membrane. This hinge is often used to support non-planar structures and is fairly common in optical MEMS technologies. The other two hinges are called scissor hinges. They are constructed of interlocking beams, as shown, and usually have a wider range of motion. Scissor hinges are usually used to hinge released structures to each other. In many applications, hinges are not used to support large ranges of motion, but rather are used to support static structures. If the hinges are to be used in this static mode, a layer of material is deposited after assembly to bond the hinges into position.

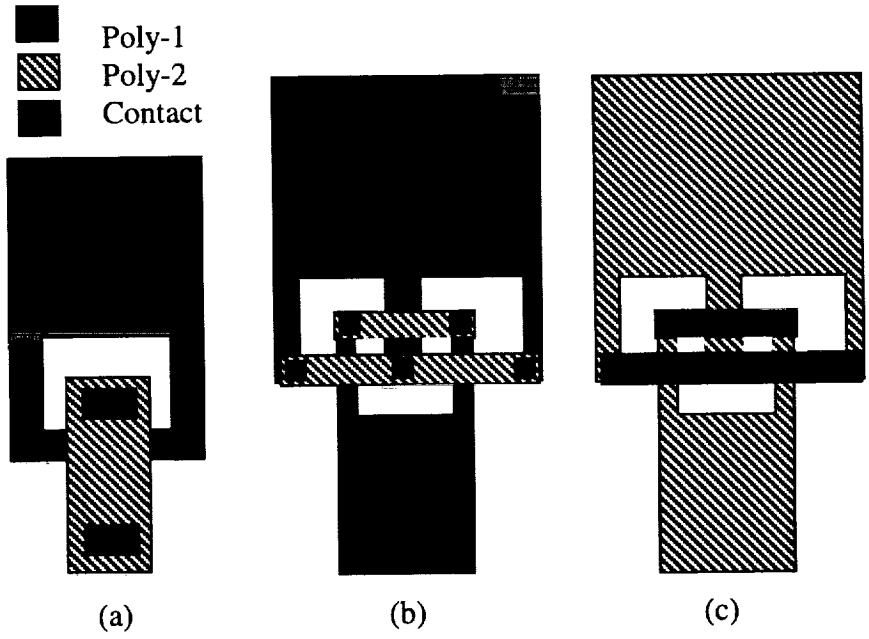


Figure 6-13 (a-c): Three basic hinges as presented by Pister et al.[93]

B. Reliability Concerns

One of the limitations in designing a substrate hinge is in designing the pin so that it is not wider than the allowable clearance of the staple. While this is an easy enough issue to address in design, it does provide some upper limits on the strength of the hinge. Scissor hinges, on the other hand, do not have limitations on the width of the beams. As a result scissor hinges are considered stronger structures than substrate hinges. If the hinge is anchored in place by the deposition of material after the device has been assembled, the adhesive strength of the deposited material will determine the hinge strength. Although Pister et al. reported a PECVD oxide layer that can withstand a torque of 10 nNm, this data would have to be independently determined by individual foundries.

Another area of concern in hinged devices is the issue of assembling hinged devices. While this is commonly done with micromanipulator stages in the laboratory setting, it may be extremely difficult to do this on a reproducible basis on a production line. As a result, membranes that are supported by hinges must be examined for damage caused in the assembly process.

C. Additional Reading

K. S. Pister, M. W. Judy, S. R. Burgett, and R. S. Fearing, "Microfabricated Hinges" *Sensors and Actuators A*, Vol. 33, pp. 249-256, 1992.

M. E. Motamedi, M. C. Wu and K. S. Pister, "Micro-opto-electro-mechanical Devices and On-chip Optical Processing" *Optical Engineering*, Vol. 36, No. 5, May 1997.

IV. Piezoresistive Transducers

Piezoresistivity is the property of a material whereby the bulk resistivity changes under the influence of a stress field. While all materials have varying degrees of piezoresistive responses, piezoresistors are commonly employed in semiconductor sensors because many semiconductor materials have large piezoresistive responses. The actual physics behind piezoresistive devices is slightly involved, but necessary to understanding its effects.

A. Formal Definition

To understand piezoresistivity, several other concepts must be first introduced. For a three-dimensional, anisotropic crystal, the electric field is related to a current by a three-by-three resistivity tensor given below.

$$\begin{bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \end{bmatrix} = \begin{bmatrix} \rho_1 & \rho_6 & \rho_5 \\ \rho_6 & \rho_2 & \rho_4 \\ \rho_3 & \rho_4 & \rho_3 \end{bmatrix} \cdot \begin{bmatrix} i_x \\ i_y \\ i_z \end{bmatrix} \tag{6-32}$$

If a Cartesian coordinate system is aligned to the <100> axis, then ρ_4, ρ_5, and ρ_6 become correlation coefficients, which relate the electric field in one axis to the current in a perpendicular direction. This leads to the result that in an isotropic conductor, such as unstressed silicon, $\rho_1=\rho_2=\rho_3=\rho$ and $\rho_4=\rho_5=\rho_6=0$. These values can be related to incremental changes in resistivity by the following equation:

$$\begin{bmatrix} \rho_1 \\ \rho_2 \\ \rho_3 \\ \rho_4 \\ \rho_5 \\ \rho_6 \end{bmatrix} = \begin{bmatrix} \rho \\ \rho \\ \rho \\ 0 \\ 0 \\ 0 \end{bmatrix} + \begin{bmatrix} \Delta\rho_1 \\ \Delta\rho_2 \\ \Delta\rho_3 \\ \Delta\rho_4 \\ \Delta\rho_5 \\ \Delta\rho_6 \end{bmatrix} \tag{6-33}$$

To define the piezoresistivity, all one needs to do is to relate the fractional change in resistivity, $\Delta\rho_i/\rho$ to the stresses in the crystal. In order to do this fully, a 6x6 matrix must be defined. But for a crystal, this matrix will exhibit the same symmetries as the crystal lattice itself, which will obviate the need for many of the matrix coefficients. If the coefficients are defined as π_{ij}, a cubic crystal structure will only have three non-vanishing coefficients. For a silicon lattice, the matrix becomes:

$$\frac{1}{\rho}\begin{bmatrix}\Delta\rho_1\\ \Delta\rho_2\\ \Delta\rho_3\\ \Delta\rho_4\\ \Delta\rho_5\\ \Delta\rho_6\end{bmatrix} = \begin{bmatrix}\pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0\\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & \pi_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & \pi_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & \pi_{44}\end{bmatrix}\begin{bmatrix}\sigma_x\\ \sigma_y\\ \sigma_z\\ \tau_{xy}\\ \tau_{xz}\\ \tau_{yz}\end{bmatrix} \qquad (6\text{-}34)$$

If all these equations are combined, it is possible to get an expression for the electric field as a function of stress[1]:

$$E_x = \rho i_x+\rho\pi_{11}\sigma_x i_x+\rho\pi_{12}(\sigma_y+\sigma_z)i_x+\rho\pi_{44}(i_y\tau_{yz}+i_z\tau_{xz}) \qquad (6\text{-}35a)$$

$$E_y = \rho i_y+\rho\pi_{11}\sigma_y i_y+\rho\pi_{12}(\sigma_x+\sigma_z)i_y+\rho\pi_{44}(i_x\tau_{yz}+i_z\tau_{xy}) \qquad (6\text{-}35b)$$

$$E_z = \rho i_z+\rho\pi_{11}\sigma_z i_z+\rho\pi_{12}(\sigma_x+\sigma_y)i_z+\rho\pi_{44}(i_x\tau_{xz}+i_y\tau_{xy}) \qquad (6\text{-}35c)$$

These equations clearly show that there is a direct relationship between stress and resistivity. It is also important to note that materials with small piezoresistive coefficients will have more limited responses than those with larger coefficients. One interesting aspect of Equation 6-34 is that it closely resembles Hooke's law. In fact, this tensor is relating a resistivity strain, instead of a mechanical strain, to the stresses upon a material. As such, there is also an orientation dependence on the piezoresistive coefficients similar to the one discussed for the elastic moduli in Section 3-IA. For an in-depth discussion of this material, Chapter 4 in Reference [6] offers a more complete mathematical description of piezoresistivity.

B. Piezoresistive Sensors

Devices that utilize the piezoresistive effect are designed so that mechanical stress occurs simultaneously with an event to be measured and that the stress is proportional to the magnitude of the event. Currently there are two kinds of piezoresistive sensors made. Membrane sensors are manufactured to measure pressure and flow while cantilever beams sensors are made for accelerometers.

Membrane sensors are usually designed as a thin single crystal silicon plates supported by a thick ring. Usually a piezoresistor is built into the edge of the device to utilize stress concentration. When the membrane deforms under an externally applied

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[1] This discussion assumes an infinite bulk lattice. For finite crystals there is a small correction factor due to dimensional changes.[6]

load, there will be stress on the piezoresistor. On cantilever beam sensors, the piezoresistor is, for similar reasons, placed on the surface of the beam near its support.

If it is assumed that the mechanical stress over the resistor is constant, the change in resistance can be given as:

$$\frac{\Delta R}{R} = \sigma_l \pi_l + \sigma_t \pi_t \tag{6-35d}$$

where

σ_l, σ_t = longitudinal and transverse stresses

π_l, π_t = longitudinal and transverse piezoresistance coefficients

For a resistor made of p-type material this expression reduces to

$$\frac{\Delta R}{R} = \frac{\pi_{44}}{2}(\sigma_l - \sigma_t) \tag{6-36}$$

For n-type resistors the expression becomes

$$\frac{\Delta R}{R} = \frac{\pi_{11} + \pi_{12}}{2}(\sigma_l + \sigma_t) \tag{6-37}$$

One important feature of these equations is that, due to the fact that they assume uniform stress fields, they are only valid for resistor sizes much smaller than the membrane or beam size.

Usually piezoresistors are configured in a Wheatstone bridge. Two resistors are placed to measure stress parallel to current flow, while two are placed to measure stress perpendicular to current flow. This arrangement works so that any decrease in resistance from tensile stress is balanced by a corresponding increase in resistance for compressive stress. This has the effect of creating a differential output of opposite signs on each side of the bridge. The total voltage change is defined as

$$\Delta V = \frac{\Delta R}{R} V_b \tag{6-38}$$

where V_b is the voltage applied to the bridge, as shown in Figure 6-14.

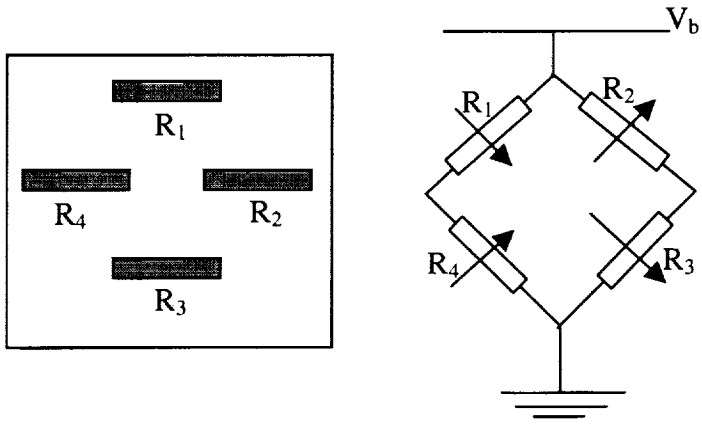

Figure 6-14 (a,b): Schematic representation of the position of four piezoresistors on a membrane (left) and accompanying circuit diagram (right). The arrows represent resistance changes when the membrane defects in the –z direction.[6]

C. Reliability Issues

One of the problems that will be encountered in using piezoresistors in high-rel applications is that they exhibit a temperature dependence. If the relationship between the piezoresistive coefficients and temperature is plotted, it becomes apparent that there is a roughly linear relationship between log(π) and log(T). For a generalized description, the piezoresistive coefficient can be determined as a function of both doping concentration, N, and temperature, T, by:

$$\pi(N,T) = \pi_0 P(N,T) \tag{6-39}$$

where π_0 is the low-doped room temperature piezoresistive coefficient.

P(N,T) is offered graphically in Figure 6-15. As can be clearly seen, at low doping concentrations, there is better sensitivity but a greater temperature dependence. As doping concentrations becomes greater than 10^{20} atoms/cm^3, the temperature dependence becomes indiscernible, but sensitivity decreases greatly. For space applications, with the great thermal ranges usually required, these devices will almost certainly have to balance the sensitivity requirements with the temperature dependence.

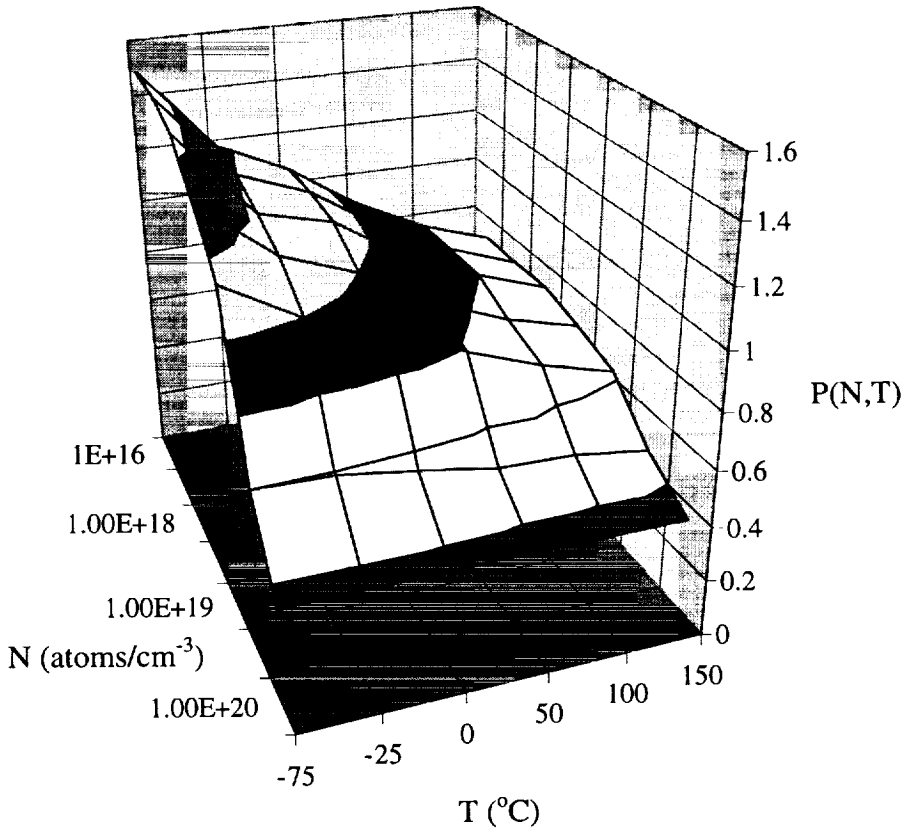

Figure 6-15: P(N,T) for n silicon. As can be seen, P(N,T) converges to a nearly uniform, albeit smaller, value versus temperature at doping levels above 10^{20} atoms/cm^3.

D. Additional Reading

Sze, S. M. ed., Semiconductor Sensors, Wiley Inter-Science, New York, 1994, Cp. 4.

Y. Kanda, "A Graphical Representation of the Piezoresistive Coefficients in Silicon", *IEEE Transactions on Electron Devices*, Vol. ED-29, No. 1, January, 1982.

V. Tunneling Tips

Electron tunneling is a concept that was developed in this century as an outcropping of quantum theory. Tunneling developed from the study of the energy of an electron in a confined space. Basic quantum theory entails Schrödinger's equation, which describes a particle's wave function, ψ, by the relation:

$$\nabla^2\Psi = -\frac{2m}{\hbar^2}(E-U)\Psi \tag{6-40}$$

where

h = Planck's constant of 6.62617×10^{-34} J-s

E = total energy of the particle

U = potential energy of the particle

m = mass of the particle

The wave function of a particle is usually not as informative as the value of the wave function multiplied by its complex conjugate, $\psi^2=\psi\times\psi^*$. This value represents the probability that a particle will be in a given point in space. If this equation is solved for the case of an electron that is in a one-dimensional energy well of width a, bounded by two infinite potential energy barriers, as depicted in Figure 6-16, the solution to Schrödinger's equation yields:

$$\psi^2(x)=0 \ \{x<0\}$$

$$\Psi^2(x) = \left(\frac{2}{a}\right)\sin^2\left(\frac{n\pi x}{a}\right) \ \{0<x<a\} \tag{6-41}$$

$$\psi^2(x)=0 \ \{x>a\}$$

where n is an integer.

This equation shows that the electron is bound by the infinite barriers, and can never escape from the well it is in. However if the barrier at a is replaced with a barrier of finite energy and width, then solving Schrödinger's equation shows that the electrons will actually tunnel through the barrier and there will be a non-zero probability that there will be an electron on the other side of the barrier. This means that it is possible for electrons to actually pass through areas in which, according to classical physics, they do not have the energy to penetrate. It is this phenomenon, called electron tunneling, that is utilized to produce tunneling tip sensors.

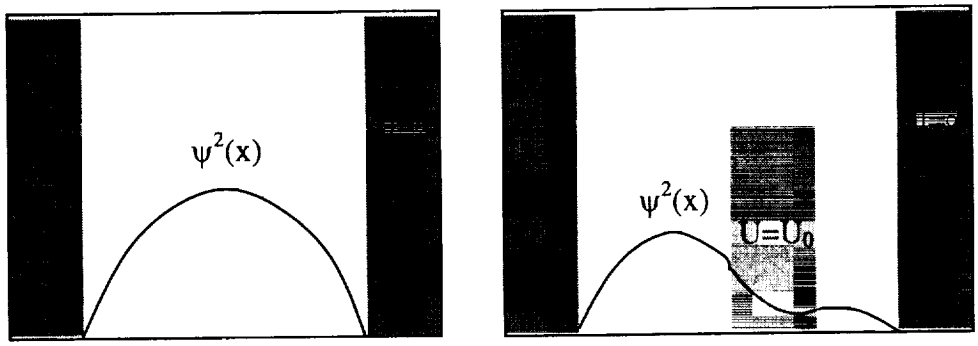

Figure 6-16: Probability distribution of an electron trapped in a well. The figure on the left shows an electron bounded by two infinite walls while the figure on the right shows an electron bounded by two finite walls with a finite energy barrier, which is greater than the energy of the electron, in the middle. As can be seen, there is a finite probability that the electron will penetrate the barrier and be on the other side. This diagram roughly corresponds to the device in Figure 6-18.

Tunneling tips are small pointed tips, shown below, that were initially developed for use in electron microscopy. They have since been adopted by the MEMS community because the tunneling effect is an extremely accurate way to measure displacements caused by external effects.

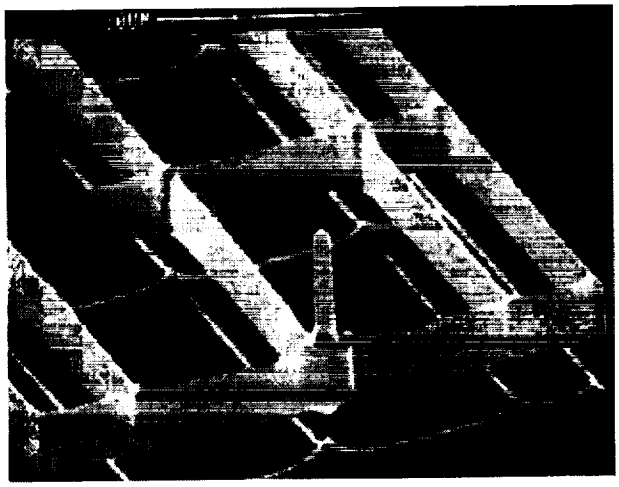

Figure 6-17: Tunneling tip on SCS beams. (from [154])

A. Physical Description

It has been shown that the current caused by tunneling across a narrow barrier is given by:

$$I \propto Ve^{\left(-\alpha x\sqrt{\phi}\right)} \tag{6-42}$$

where

V = bias voltage on the tip

$\alpha = 1.025\ \text{Å}^{-1}\text{ev}^{-1/2}$

ϕ = the effective energy height of the tunneling barrier = $-\frac{1}{\alpha I}\frac{\partial I}{\partial V}\frac{\partial V}{\partial x}$

x = the physical width of the energy barrier

This means that an electronic circuit capable of detecting a 1% variation in a 1 nA current from a 100 MΩ source would be able to detect deflections on the order of 0.003 Å. For this reason tunneling tips have started to be developed for use in high data storage applications and high sensitivity accelerometers.

Typically tunneling sensors are designed by suspending a mass above the tunneling sensor. An external force, which can be anything from infrared radiation to acceleration, pushes the mass downwards, which increases the tunneling current and becomes a measurable event, as shown in the diagram below.

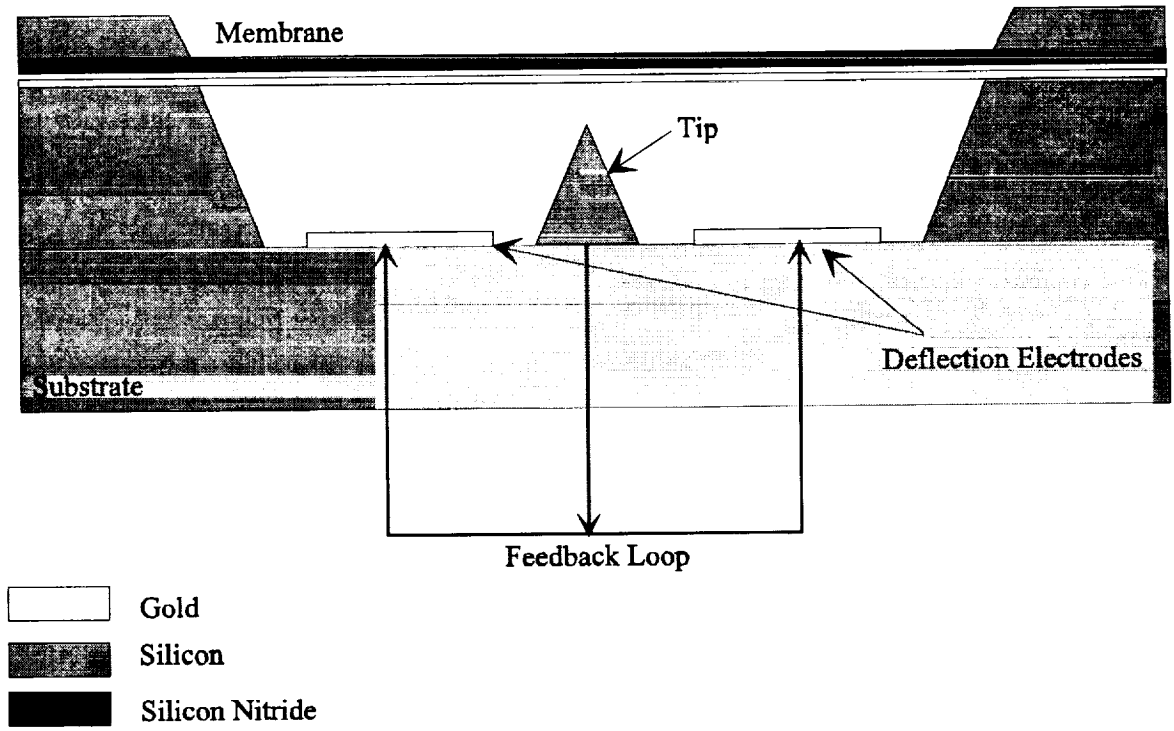

Figure 6-18: Typical layout for a tunneling sensor.

While tunneling sensors are among the most accurate sensors available in MEMS technology, they do suffer from a number of reliability problems.[41,43]

B. Reliability Concerns

One of the great difficulties in making tunneling accelerometers is in fabricating the devices. The tunneling tips need to be made of a conductive surface that does not react with the air. While conventional tunneling tips, since they operate under an Ultra-High Vacuum, can be made from a multitude of metals, microsensor tunneling tips are much more limited in the materials that can be used. Gold has been found to be useful in the production of sensors, but it is difficult to create good adhesion between a gold tip and an insulating substrate, which is usually SiO_2. This created a need for multiple layers of adhesive materials, which create processing problems and reduce yield.[42] While the fabrication of these devices is certainly not an impossible task, they do suffer from low yield rates.

Another problem that is more difficult to handle stems from the fact that the tunneling effect is highly displacement sensitive. Since, in order to get a tunneling effect, the tip must usually have a bias voltage, which is typically under 1 volt, and be within nearly ten Ångstroms of the moving mass, contact between tip and mass is unavoidable. This contact must be accounted for in design of mechanical system and circuit. On the mechanical side, it is important to place one of the electrodes on a compliant support to

limit the force to the tip during the inevitable contact. The circuit must also limit the current during contact. If both of these precautions are taken, the danger of tip crashes will be mitigated. For devices designed with these techniques, crashes have occurred at low frequency operation for months with no detectable change in operational characteristics. However, any tunneling tip designs need to have these issues thoroughly addressed for high-rel applications.

These devices, due to their extreme sensitivity, are also susceptible to thermal noise and mechanical vibration. It is typically these effects that limit device sensitivity and they need to be addressed for any tunneling sensor. There is also electrical noise in the measurements of the tunneling output. In many devices, the electrical noise spectrum exhibits a 1/f dependence. This noise creates an error in measurements that scales on the order of 10^{-3} Å/Hz^{½}. While this noise is fairly insignificant for many applications, it does provide a limit on the actual sensitivity of the device.[41]

C. Additional Reading

T. W. Kenny, W. J. Kaiser, H. K. Rockstad, J. K. Reynolds, J. A. Podosek, and E. C. Vote, "Wide-Bandwidth Electromechanical Actuators for Tunneling Displacement Transducers" *Journal of Microelectromechanical Systems*, Vol. 3. No. 3, September 1994.

VI. Electrostatic Actuators and Transducers

A. Parallel Plate Capacitors

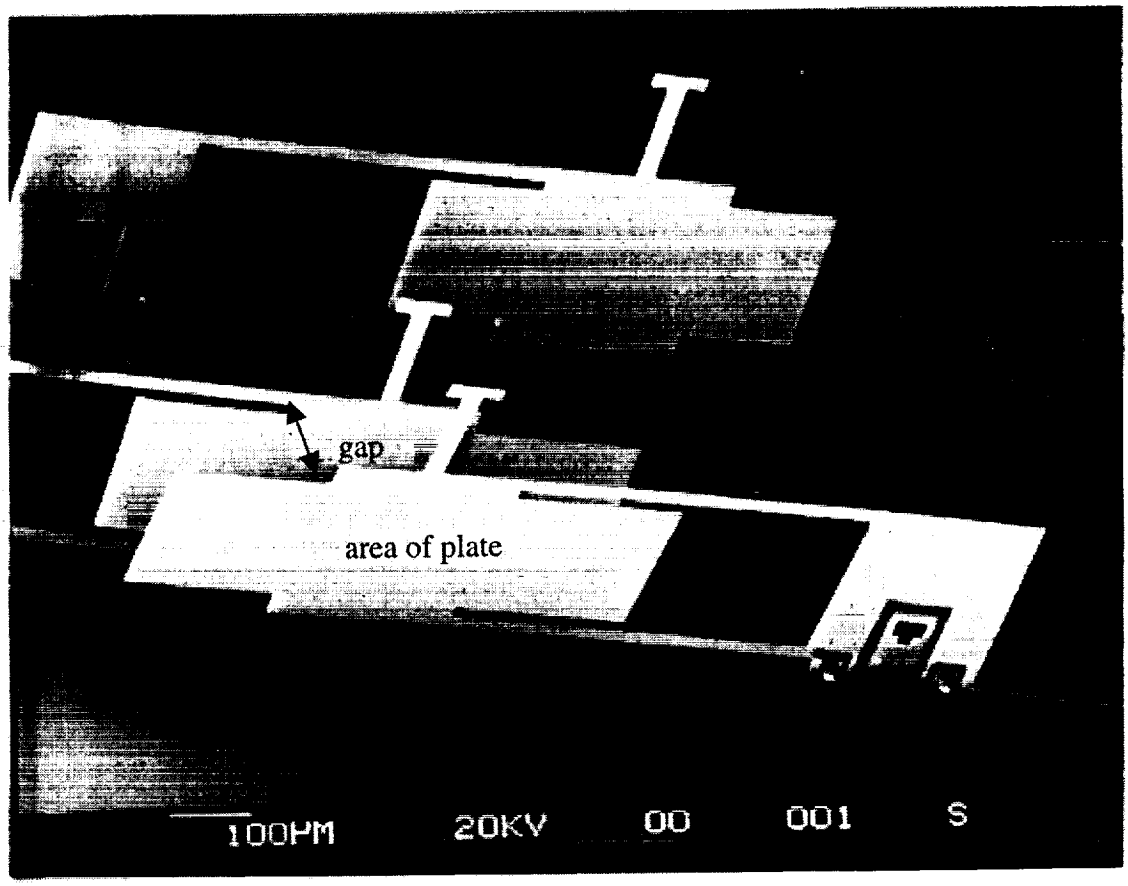

Figure 6-19: Closeup view of parallel plate capacitor with the area and gap labeled. (from[155])

Capacitors have been developed and understood for as long as any electronic device. They are both simple to construct and understand. As such, capacitors are fundamental to many devices and have been used extensively in the microelectronics industry. It has been estimated that a modern microprocessor has anywhere between seven and ten million recognizable capacitors in its design. A capacitor is simply two conductive objects separated by some distance, d, which store electrical energy by attracting and repelling free electrons within the conductors. For MEMS, a prevalent capacitors design consists of two parallel plates, as shown in Figure 6-19.

i) Electrical and Mechanical Analysis

The capacitance of an object is defined as the amount of electric charge that it can store per voltage. The common mathematical expression of a capacitor's ability to store energy or charge is related by the expressions:

$$q = CV \tag{6-43a}$$

$$U = \tfrac{1}{2}CV^2 \tag{6-43b}$$

where

q = electric charge

V = voltage

C = capacitance

U = energy

For capacitors constructed of two parallel plates a useful relationship has been derived that:

$$C = \varepsilon \frac{A}{d} \tag{6-44}$$

where

A = area of one of the plates

d = distance between the plates

ε = the permittivity of the material between the two plates

One reason that capacitors have become prevalent in MEMS is that capacitance is a function of distance. This means that a change in distance will result in a change in capacitance, which is a measurable event. If a capacitor immersed in air is assumed to have one fixed plate and one plate that displaces a distance, x, from the rest, the capacitance can be rewritten as:

$$C = \varepsilon_0 \frac{A}{(d - x)} \tag{6-45}$$

where

ε_0 = permittivity of a free space ($8.85*10^{-12}$ F/m)

If a sensor is to be fabricated out of parallel plate capacitor, there is a simple method to electrically detect a change in capacitance. Since a current, I, is related to the charge on a capacitor, Q_c, by the equation:

$$i_c = \frac{dQ_c}{dt} \tag{6-46}$$

Then using the circuit below,

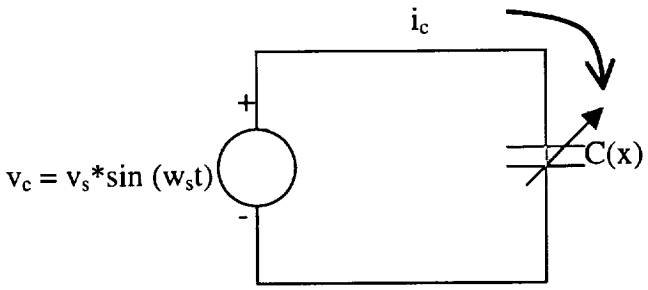

Figure 6-20: Basic circuit for detecting changes in capacitance.

a change in current will be approximately related to a change in displacement by the relationship[1]:

$$\Delta i_c(\Delta x) \approx \omega_s v_s C(d)\left[\frac{\Delta x}{d}\right] \tag{6-47}$$

Another useful feature of parallel plate capacitors is the fact that they can be made into actuators. Given that a force, F, is related to potential energy by the equation:

$$F = -\frac{\partial U}{\partial x} \tag{6-48}$$

it is possible to derive the relationship for parallel plate capacitors that:

$$F = \frac{\varepsilon_0 A V^2}{2d^2\left(1-\frac{x}{d}\right)^2} \tag{6-49}$$

This shows that an applied voltage will exert a force on the capacitor plates. It is this electrostatic force that is used to make actuators out of parallel plate devices.

[1] This is a linearized result that only applies for $\Delta x << d$.

ii) Limitations of Parallel Plate Capacitors

While parallel plate capacitors have good actuation and sensing abilities, they have some severe limitations. The greatest drawback to using these devices is that they are non-linear. While they can be treated as linear for small displacements, for large motions, parallel plate capacitors clearly exhibit non-linear behavior.

One of the dangers in these devices is the potential of the plates touching. As discussed in Chapter 3, when two metal surfaces come into contact, adhesive forces exert a strong bond that usually causes failure. This problem is especially prevalent in parallel plate devices because of the non-linear force that increases quadratically with distance. A common design rule used is that, if $\Delta x \geq 1/3$ d, the device will usually have sufficient force to transverse d. To prevent this, parallel plate devices must be designed to displace much less than this amount.[10]

Parallel plate capacitors could also be susceptible to electrostatic discharge. An ESD would have a similar effect as applying a delta function to the device. If the voltage spike is large enough, it could induce stiction by bringing the plates into contact. Unfortunately the scant research into ESD in MEMS has not provided any concrete data on the effects of ESD on parallel plate capacitors and these theories have not been experimentally verified.

iii) Additional Reading

W. S. Trimmer, K. J. Gabriel, and R. Mahadevan, "Silicon Electrostatic Motors", *Transducers '87, The 4th International Conference of Solid-State Sensors and Actuators*, pp. 857-860, June 1987.

W. S. Trimmer and K. J. Gabriel, "Design Considerations for a Practical Electrostatic Micro-Motor", *Sensors and Actuators*, Vol. 11, pp. 189-206, 1987.

B. Comb Drives

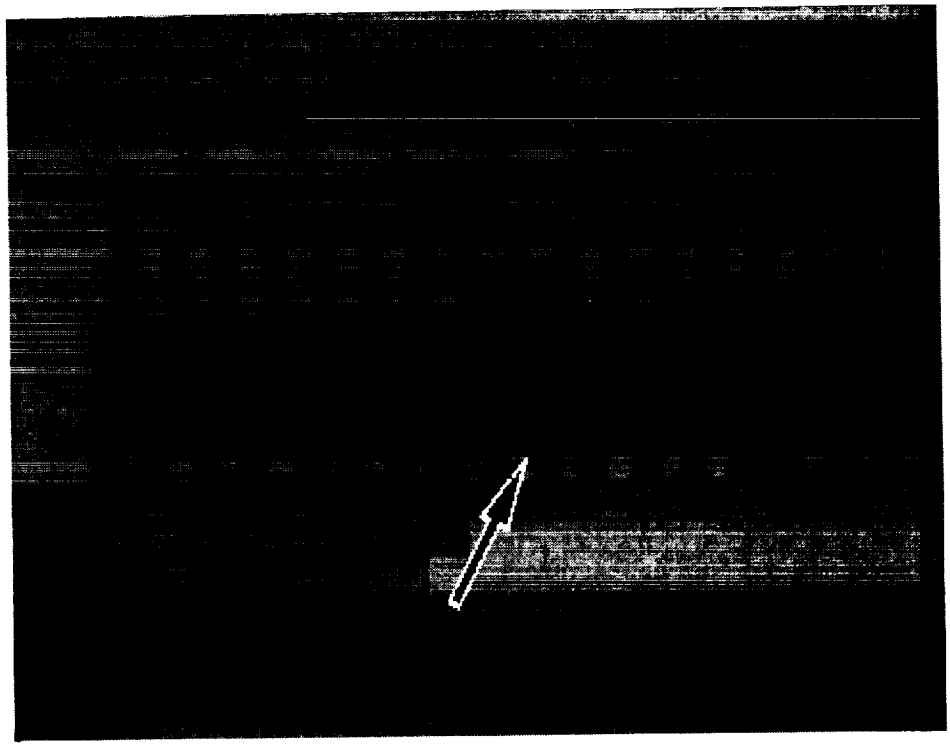

Figure 6-21: A standard comb drive. The arrow points to a particulate that landed on one of the electrodes.

Due to the problems discussed with making electrostatic parallel plate actuators, there have been attempts made to make devices that utilize electrostatics to produce motion while eliminating the relationship between force and distance. The most common device made to accomplish this is called a comb drive because of its overall comb-like appearance, as seen in Figure 6-16. Comb drives operate by using fringing fields to pull one set of the drive into the other. Actuation occurs in one dimension only and the equations of motion are derived in the next section.

i) Mechanical and Electrical Analysis

Essentially comb drives are composed of multiple structural beams and, as such, they are not difficult to analyze. As shown in the picture, there are two sets of interdigitated electrodes. Generally one of them is fixed while the other is mobile. The force generated by a voltage is described by:

$$F = \frac{\varepsilon_0 b V^2}{d} \tag{6-50}$$

where b is the vertical height of the cantilever beams.

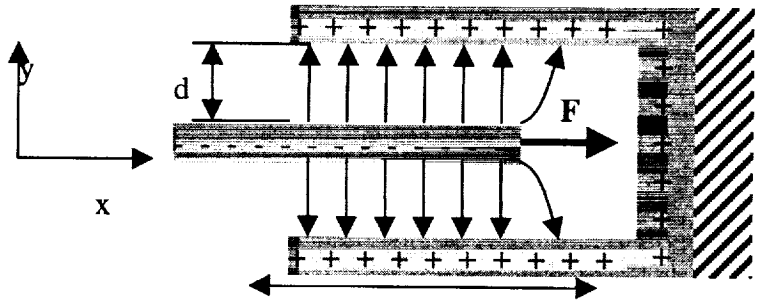

Figure 6-22: Overhead view of basic unit of a comb drive.

This equation shows that the force produced by this device is independent of the displacement of the middle electrode. As a result, comb drives are among the more common actuators in MEMS. The other fact that makes comb drives appealing is that n comb drives produce a force equal to n×F. This simple scaling makes it possible to produce macroscopic forces on the MEMS scale. It is not unreasonable to manufacture an array of comb drives to produce upwards of 30 Newtons with as little as 10 volts applied to the electrodes.[10] While these aspects of comb drives are quite appealing, there are also some serious limitations to their performance.

ii) Limitations on Design

One of the problems with comb drives illustrated by Figure 6-22 is that there is one electrode. For argument's sake, assume it to be negatively charged, surrounded by two positively charged electrodes. While the forces on the electrode are balanced by the equal spacing of the two gaps, clearly any perturbation of the center electrode will cause an offset of the forces and pull the electrode to one side or another. In engineering terms, the comb drive is an inherently unstable system. To combat this problem, several steps must be taken in the design to insure that the device does not fail at the first vibration. Since stability problems are problems in energy storage, the key to designing a stable comb drive is to design it to store more energy in the y direction than in the x direction. To make $U_y >> U_x$, the following condition must be met:

$$\tfrac{1}{2} k_y d^2 >> \tfrac{1}{2} k_x l_p^{\,2} \tag{6-51a}$$

where

k_y = spring constant in the y direction

k_x = spring constant in the x direction

l_p = The length of the electrode

which means that:

$$k_y >> \frac{l_p^2}{d^2} k_x \tag{6-51b}$$

This is illustrated in Figure 6-23.

While this is hardly an exact answer to the problem of stability, this solution does lend it some formalism. For high-rel applications, a large safety factor will have to be included to guarantee that the comb drive does not fail due to surface contact. If a comb drive is not entirely stable, it is possible for the drive to not completely fail but instead enter into chaotic oscillatory modes. While this phenomenon has applications in encryption, it is usually an undesirable event.

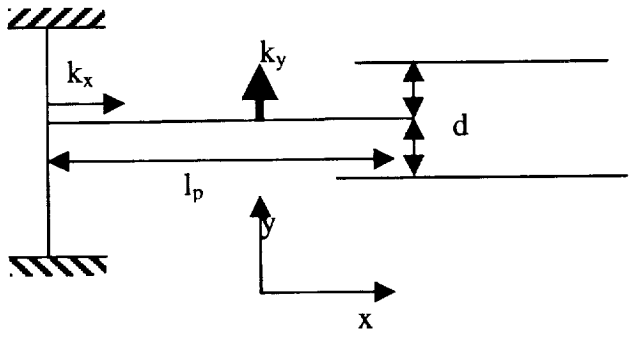

Figure 6-23: Overhead view of comb drive structure with spring constants and dimensions labeled.

Another limitation on comb drives is that they are typically limited in the amount of work they can do. With a maximum displacement of l_p and, with l_p being kept to a minimum due to Equation 6-51, comb drives are just not capable of producing large scale motion. While this problem can be designed around to a degree, it is nevertheless a serious limitation to comb drive usage.

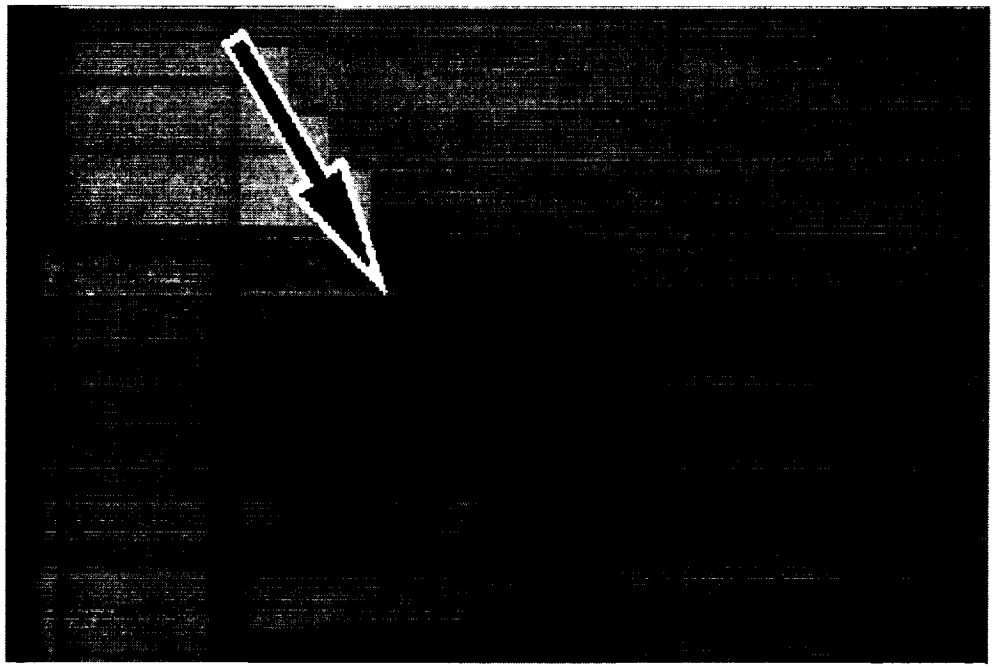

Figure 6-24: An example of the damage that results when two comb drive electrodes come into contact and short out the device.

An area that is also important to consider in comb drive operation is the effects of parasitic capacitance with the substrate. Since the comb drive is a fairly large conductive surface suspended over another large conductive surface, there is a considerable parasitic effect between the substrate and the drive. While this effect can be used to produce out of plane torsional microactuators, it is often an undesirable side effect of the comb drive design. It is possible to have such a large parasitic motion that the comb drive will actually touch the substrate, which will lead to the adhesion and possibly shorting problems. In a sound design, the comb drive should be far enough removed from the substrate that the parasitic capacitance will not cause stiction.

Particulates can also be problematic in comb drives. Conductive dust particles can electrically connect parts of a comb, which will short them out, producing catastrophic current flows. Comb drives could also be susceptible to electrostatic discharge. An ESD would have a similar effect as applying a delta function to the device. If the voltage spike is large enough, it could induce stiction by bringing the plates into contact. Unfortunately there is no published information on the effects of ESD on comb drives, which means that evaluating the ESD tolerance of a design is not yet possible.

iii) Additional Reading

W. C. Tang, T.-C. H. Nguyen, and R. T. Howe, "Laterally Driven Polysilicon Resonant Microstructures." *Proceedings of IEEE Microelectromechanical Systems*, February 1989.

W. C. Tang, T.-C. H. Nguyen, M. W. Judy and R. T. Howe, "Electrostatic-comb Drive of Lateral Polysilicon Resonators" *Transducers '89, Proceedings of the 5th International Conference on Solid-State Sensors and Actuators and Eurosensors III*, Vol. 2, pp. 328-331, June 1990.

C. Micromotors

A major area of research in MEMS in the past decade has been into the design and fabrication of micromotors. There are multiple kinds of micromotors being designed today. While most of these devices are electrostatically driven by side electrodes, as illustrated by Figure 6-25, there are also a number of other designs being implemented. However, for the sake of brevity, this discussion will be limited to electrostatically driven micromotors. The section on reliability will have implications to less conventional micromotors.

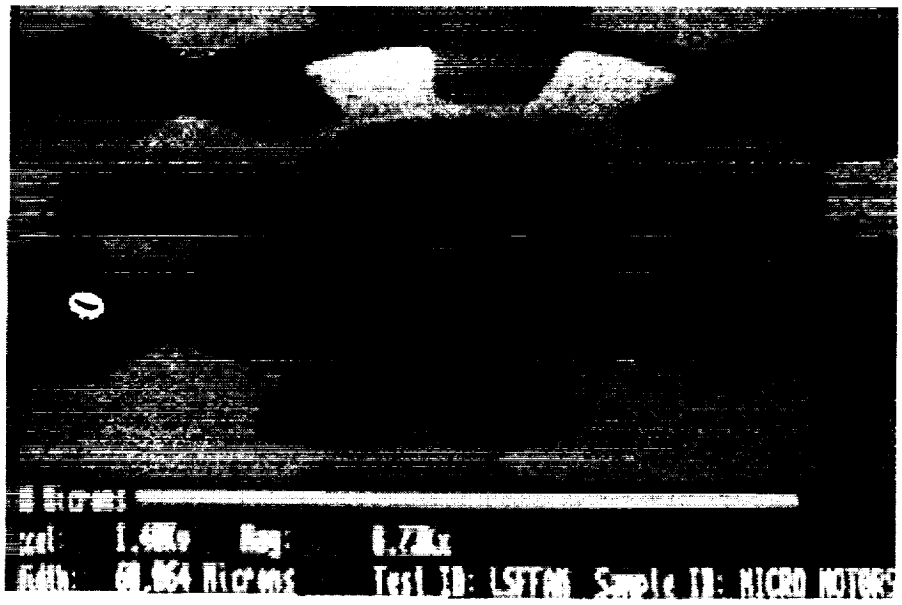

Figure 6-25: Electrostatically driven micromotor. (from [22])

i) Electrostatic Motor Analysis

Electrostatic micromotors utilize variable capacitance in a fashion somewhat similar to other electrostatic devices previously discussed. The main difference is that micromotors are typically driven by several different sets of drives, or stators, that are switched on and off to produce a torque. This torque is a function of the rotation angle of the drive:[22]

$$T(\theta) = \tfrac{1}{2} V^2 \frac{\partial C(\theta)}{\partial \theta} \tag{6-52}$$

Micromotors have a natural operating frequency, which is determined by the magnitude of torque applied to the motor. For a motor similar to the one depicted above, this frequency is:

$$f_N(V_p) = 1.5\left(\frac{V_p}{100}\right)^2 kHz \tag{6-53}$$

where V_p is the phase voltage applied to the stators. This leads to an equation for the maximum rotational speed of the motor, ω_{max}:

$$\omega_{max} = \frac{240 f_N}{n} rpm \tag{6-54}$$

where n is the number of steps per revolution determined by[1]:

$$n = \frac{1}{\left(\frac{1}{n_s} - \frac{1}{n_r}\right)} \tag{6-55}$$

where n_s and n_r are the respective numbers of stators and rotors.

These motors can be either used as microstepper motors or can be operated as a continuously rotating motor. While the actual design and fabrication of these devices varies depending upon application, most electrostatic motors are governed by the above physical laws.[22,23]

ii) Harmonic Motors

Harmonic motors are a kind of motor that utilizes the rolling motion of two bodies with different circumferences. Typically a motor contains a cylindrical hole, with a slightly smaller cylindrical rotor. These motors have a tribological interest as they utilize rolling instead of sliding friction, which eliminates many of the wear concerns common to other motors. Furthermore, since the stators and rotors are designed to touch in these devices, large amounts of force can be generated.

Using one of the original harmonic motors as an example, there are some basic facts of motor operation that are fairly common to all harmonic motors. If the stators are cycled at a frequency of ω_s, then it is possible to determine the steady state frequency of the harmonic motor, ω_r:[87]

$$\omega_r = \omega_s\left(\frac{R_s}{R_r} - 1\right) \tag{6-56}$$

where R_s and R_r are dimensions defined in Figure 6-24.

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[1] This derivation assumes a drive signal described by Y. –C. Tai et al. in [22].

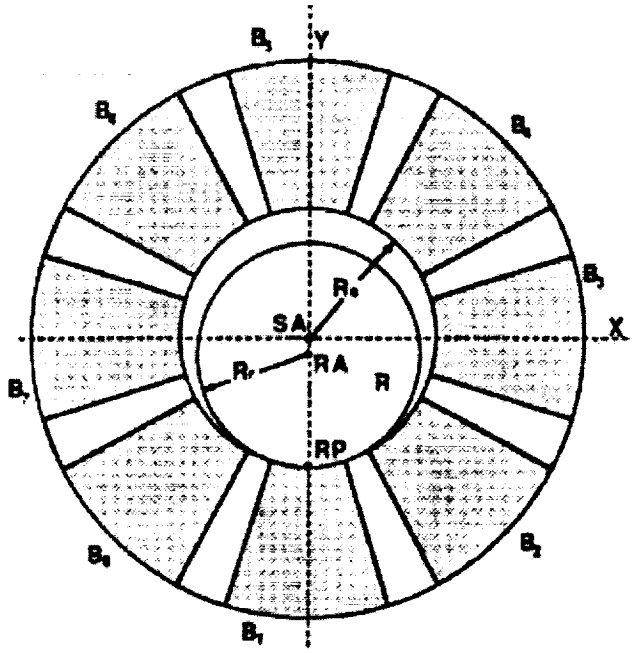

Figure 6-26: A basic harmonic motor layout. (from [88])

The unsymmetrical nature of the roll causes the rotor to effectively wobble inside the stator. One reliability concern of wobble motors is that the direct contact of the stator and rotor raises questions about stiction.

iii) Microbearing Reliability Concerns

The biggest reliability concern for micromotors is the motor's connection to the substrate. Since the rotors must be supported on bearings, there is concern about the long term reliability of these bearings. It has been shown that, over time, there will be wear on the bearings caused by the frictional forces from the substrate. The wear on the bearings will increase the frictional force on the bearing, requiring higher driving voltages, which will further increase wear. This positive feedback loop will quickly lead to total device degradation. The only effective method to mitigate wear on bearings is to select wear- resistant materials.

In most macroscopic devices, liquid lubricants are used to prevent direct metallic contact. However, in MEMS, it is felt that liquid lubricants will not be in general use due to the fact that viscous friction forces are large compared to other frictional forces on micrometer scales.[19] While recent research has raised the possibility of using gas phase lubricants to reduce wear, these solutions involve extremely high temperature operations and are unlikely to be practical.[151] Instead, bearings are usually operated dry at ambient temperature, with direct contact made between structures. There have been studies conducted on these conditions and it has been found that different materials respond, as would be expected, in distinct ways to wear.

Several studies[19,153] indicate that single crystal silicon is moderately well suited as a bearing material. During initial burn-in, the rough points in a bearing will fracture off, leaving a smoothed surface that shows little wear over time. As a result, the wear on silicon decreases with time. Polysilicon shows moderate wear properties and is a suitable, although not ideal, bearing material. As would be expected, Si_3N_4 and SiO_2 exhibit poor bearing characteristics. They show linear wear that leads to total failure. Diamond-like carbon is a material that has shown promise as a bearing material and may eventually be used as a coating on many SCS and polysilicon structures that have large contact stresses. While the exact characteristics of bearing wear are dependent upon the materials involved and the environment in which they slide, a good rule of thumb is that wear is minimized by using dissimilar hard materials

Another problem associated with wear on microbearings is that, for electrostatically driven structures, forces on the device will be a function of the device height, and thus bearing height. Many devices place rotors above stators in order to have a non planar component of force to partially levitate the rotor. As the bearings wear, the electrode distance would decrease, which would cause forces to increase quadratically. This increases wear and alters drive performance. This behavior accelerates failure and leads to total device collapse. Ultimately, the contact morphologies of microbearings are the limiting factor in micromotor performance and, as such, they need to be well understood for high-rel applications.

iv) Additional Reading

Long-Sheng Fan, Yu-Chong Tai, and Richard S. Muller, "IC-Processed Electrostatic Micromotors." *IEEE International Electronic Devices Meeting*, December 1988.

Yu-Chong Tai, Long-Sheng Fan, and Richard S. Muller, "IC-Processed Micromotors: Design, Technology, and Testing" *Proceedings of IEEE Microelectromechanical Systems*, February 1989.

U. Beerschwinger, D. Mathieson, R. L. Reuben, and S. J. Yang. "A study of Wear on MEMS Contact morphologies" *Journal of Micromechanics and Microengineering*, 7 September 1994.

S. C. Jacobsen, R. H. Price, J. E. Wood, T. H. Rytting, and M. Rafaelof, "The Wobble Motor: An Electrostatic, Planetary Armature, Microactuator" *Proceedings of IEEE Microelectromechanical Systems*, pp. 17-24, February 1989.

VII. Magnetic Actuators

Magnetic actuators are a class of devices that, as their name implies, utilize magnetic fields to provide force. While creating magnetic fields on semiconductor devices is intrinsically more difficult than creating electric fields, the potential benefits of magnetic actuators has spurred the development of these devices. Due to the physics of magnetics, magnetic devices are capable of producing greater forces than electrostatics. Combined with the ability to apply force through a conductive medium, such as electrolytic fluids, these factors make magnetic actuators a promising field within MEMS.[15]

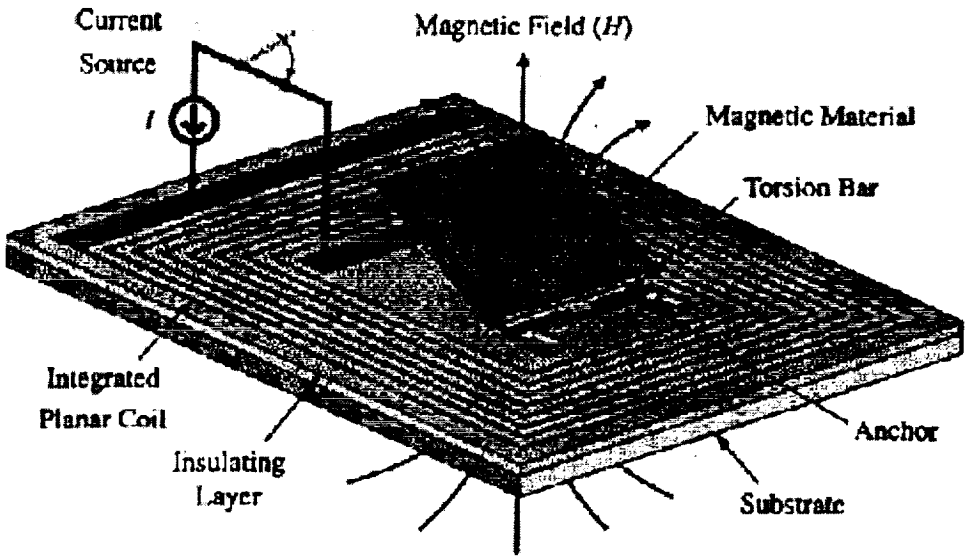

Figure 6-27: A magnetic actuator designed by Judy et al. (from [15])

There are several common methods employed in MEMS to make magnetic actuators. A magnetic field can be described from Maxwell's equations:

$$\nabla \times B = \left(\frac{4\pi}{c}\right) J + \left(\frac{1}{c}\right)\frac{\partial E}{\partial t} \tag{6-57a}$$

$$\nabla \cdot B = 0 \tag{6-57b}$$

where

B =magnetic field

c = the speed of light

E = electric field

J = current density

These equations show that a magnetic field can be produced either by a constant current or by a time varying electric field. While there are multiple methods to create one of these two effects, the simplest way to create an actuating magnetic field is through a loop of wire, as shown in Figure 6-20. For these actuating fields to create motion, the actuator requires a structure that is influenced by the magnetic field. The two most common structures that will be actuated in a magnetic field are those with current loops on their surfaces and those coated with magnetic films, such as ferromagnetic and diamagnetic materials. In either case, the interaction of the two magnetic fields creates an actuating force that then moves the structure.

As with many of the technologies within MEMS, magnetic actuators are being developed in a myriad of ways by different groups around the world. Since magnetic actuators have not become as standardized in MEMS as electrostatic actuators, it is difficult to discuss a typical magnetic actuator. For this discussion, a simple actuator developed by Judy et al. will be discussed to give an example of the forces at work within a magnetic device. This device, which is shown in Figure 6-27, uses a ferromagnetic plate influenced by a loop of wire integrated into the substrate.

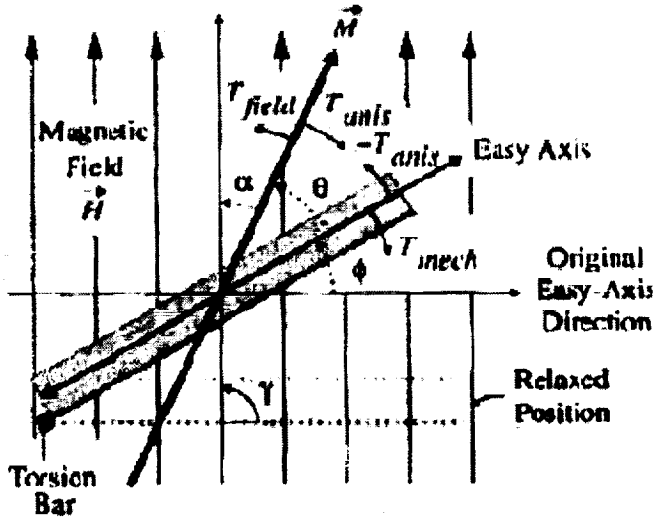

Figure 6-28: Diagram of forces acting on soft magnetic plate. (from [15])

A. Mechanical and Electrical Analysis

For this non-planar magnetic microactuator, the rotational deflection is a function of the magnetic field, H, and the stiffness of the torsion bar, k_ϕ. Assuming that the magnetic field remains perpendicular to the original orientation of the plate, the torque produced by the magnetic field, T_{field} is defined by:

$$T_{field} = V_{mag} M (H_{dc} + H_{ac} \sin(2\pi ft) \cos\phi) \tag{6-58}$$

where

M = net magnetization vector

V_{mag} = magnetic volume

H_{dc}, H_{ac} = magnetic field from respective dc and ac sources

f = ac current frequency

ϕ = angle plate rotates from rest.

To determine the actual mechanical response of the plate, it is necessary to use the dynamic torsional model of

$$J\ddot{\phi} + C_\phi \dot{\phi} + k_\phi \phi = T_{field} \tag{6-59}$$

where

Cϕ = dampening coefficient = $\sqrt{\frac{Jk_\phi}{Q}}$

J = polar moment of inertia of the magnetic plate

Q = quality factor

To determine ϕ as a function of time, Equation 6-59 must be solved. This can be done either analytically or numerically, although the analytic solutions might be difficult to obtain. In order to do either, M must be defined, which is done below:

$$M = \frac{\mu_0 (\pm H_c + H_a)}{N_M} \tag{6-60}$$

where

H_c = coercive field of the magnetic material under torque

H_a = applied field ~ H*cos(90-ϕ)

N_M = shape-anisotropy coefficient of the plate

μ_0 = permeability of free space ($4\pi*10^{-9}$ H/m)

The net result of the forces is that the plate will oscillate in the time varying magnetic field. While these equations give a basic description of the motion of a ferromagnetic plate in a magnetic field, other magnetic materials will have different responses to similar fields. Due to the fact that the exact internal effects of magnetic devices extend beyond the scope of this guideline, an interested reader should examine the references listed at the end of the section to gain a more detailed description of the physics of these devices.

B. Reliability Concerns

There are some basic problems with using magnetic forces in MEMS that need to be understood. An inherent drawback to magnetic devices is that they scale poorly into the micro domain. In order to scale a device effectively, certain quantities must be held constant while the physical dimensions of a device shrink. If three basic quantities of current density, heat flux, and temperature rise are considered to be held constant during scaling, it becomes apparent that there are serious limitations to micro-magnetic actuators.

If current density is held constant while scaling a device, then a wire with an order of magnitude drop in the cross sectional area will have an order of magnitude drop in current. While this results in a constant heat generation per unit volume, it will, for a wire- generated field operating on a permanent magnet, result in a drop in force of three orders of magnitude. While this loss can be slightly offset by the fact that smaller systems are better at conducting heat away, clearly this method of scaling severely limits the effectiveness of micro-magnetic actuators. If instead the heat flux per unit of surface area for a wire is constant during scaling, current density scales according to the inverse square root of the change in heat flux, so that, for an order of magnitude drop in cross sectional area, there will be an increase in force on the order of 2.5 orders of magnitude. This scaling is limited by the maximum allowable temperature on a device and is also not a desirable method to increase force as dimensions decrease. If the system is scaled to limit the temperature difference, it is possible to have a two order of magnitude increase in force. However, this comes at the expense of an increase in current density, which makes the device much less efficient, which may not be acceptable for many applications. Thus, magnetic devices cannot scale into the micro domain without sacrificing either force, operating temperature, or efficiency, which is a serious limitation.[55] As a result, any magnetic actuator design must be verified to insure that it meets the design requirements without unacceptable temperature dissipation or power losses.

Another issue to consider in using magnetic actuators aboard spacecraft is the presence of spurious magnetic fields. Since modern spacecraft employ an array of electronic devices that create magnetic fields, these devices can be unintentionally actuated by nearby devices. A good model of the magnetic fields in a spacecraft, which is usually developed by the systems engineers, will determine the risk level for parasitic actuation.

C. Additional Reading

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J. W. Judy and R. S. Muller, "Magnetic Microactuation of Torsional Polysilicon Structures," *Sensors and Actuators A, Physical*, Vol. A53, Nos. 1-3, pp. 392-397, 1996.

J. W. Judy and R. S. Muller, "Magnetically Actuated, Addressable Microstructures", *Journal of Microelectromechanical Systems*, Vol. 6, No. 3, September 1997.

VIII. Thermal Actuators

Thermal actuators are a class of devices that utilize heating to produce forces and deflections. These devices operate through the use of heat transport to rapidly change a device's temperature. Since MEMS devices operate on such small scales, it is possible to create devices with quick response times, as heat transport occurs in scales often measured in microseconds. While some objections may be raised to the power dissipation implicit with these devices, they offer a simpler alternative to many electrostatically and magnetically driven devices.

A. Bimetallic Strips

The most prevalent thermally actuated devices in MEMS are structures constructed out of layered materials. These thermal actuators utilize the bimetallic effect found in common household thermometers. There have been a number of arguments made for the advantages of bimetallic actuators. Since there is a direct coupling between dissipated power and beam deflection, the actuators can operate at low voltage levels. Combined with the ability to produce a force that is independent of displacement, thermal actuators have piqued serious interest and have been developed independently by a number of researchers.[150]

B. Mechanical Analysis

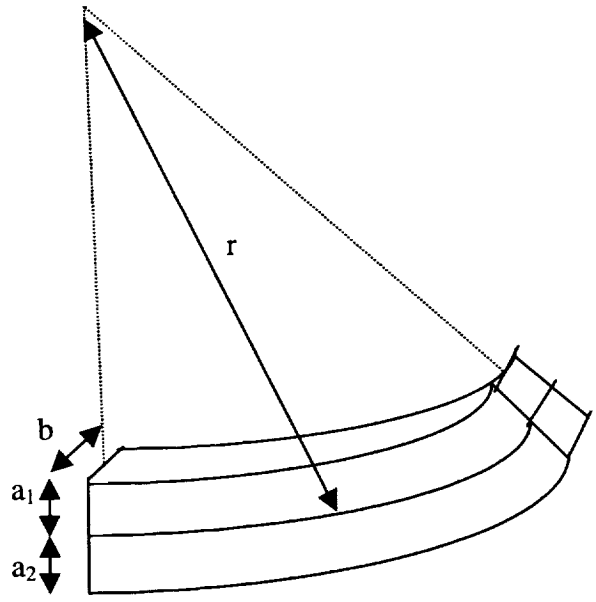

Figure 6-29: Side view of two metallic strips a and b bending due to temperature stress.

In these devices, two materials, often Si-SiO_2 or Si-Si_3N_4 are sandwiched together. As the device heats up, the differing changes in length caused by mismatched thermal expansion coefficient create stresses at the metallurgical junction, which bends the device. Figure 6-29 illustrates a bimetallic strip made of two cantilevered beams of lengths l that are exposed to a temperature change, ΔT.

The conversion factor γ, relates a temperature change, ΔT, with a deflection at the end of the cantilever, d, by:

$$d = \gamma \Delta T \tag{6-61}$$

If a uniform heat distribution is assumed with the beams, then the conversion factor can be approximated for l << r as

$$\gamma = \frac{l^2}{2r\Delta T} \tag{6-62}$$

where r is the radius of curvature of the beam:

$$r = \frac{2}{3}\frac{\frac{7}{4}(a_1 + a_2)^2 - 2t_1t_2 + \frac{E_1b_1a_1^3}{E_2b_2a_2} + \frac{E_2b_2a_2^3}{E_1b_1a_1}}{(\alpha_1 - \alpha_2)\Delta T(a_1 + a_2)} \tag{6-63}$$

where α is the linear coefficient of thermal expansion.

A closer mathematical analysis of this equation will show that it is minimized when the cantilever beams have identical values of b and a. For these beams, the deflection is given by:

$$r = \frac{a}{3(\alpha_1 - \alpha_2)\Delta T}\left(5 + \frac{1+\chi^2}{\chi}\right) \tag{6-64}$$

where χ is the ratio $\frac{E_1}{E_2}$.

Since the absolute width of a structure does not influence bending, the smallest radius of curvature, and thus the greatest deflection, will occur if (α_1-α_2) and l are maximized, while a is minimized. The simplest method to accomplish this comes through altering l and a, as there are only a few materials, and accompanying thermal expansion coefficients, to choose from in the semiconductor industry.[149]

As this derivation shows, the displacement of the strip is directly related to a change in temperature. There are several ways to induce temperature changes. One

common method is to apply an electric current through the beam. The power dissipated by the current flowing through a resistor will produce a ΔT. The amount of energy needed to raise temperature is determined by the heat capacity of the cantilever beams. In static operation, it is desirable to reduce all the dimensions of the actuator so that there is less thermal loss. In dynamic operation, as is the case for a high frequency switch, it is more useful to have larger surface areas with a greater heat exchange and a corollary increase in switching rate.[52]

C. Shape Memory Alloys

Shape memory alloy, or SMA, actuators are variants upon thermal actuators that use the shape memory alloy effect, which was first discovered in 1938 by Alden Greninger and V.G. Mooradian.[56] Materials that experience the SMA effect undergo reversible phase transformations. Below some critical temperature, the material is in the martensite phase and will easily deform. Above this temperature, the material changes to the austenite phase and begins to exert strong forces trying to restore to its original shape.

In the early 1960s, two researchers at the Naval Ordnance Laboratory discovered that the alloy NiTi can have a phase transition that is a function of alloying content and varies anywhere from –50 to 166°C. Since this material, nicknamed nitinol, for Nickel Titanium Naval Ordnance Laboratory, has superior mechanical properties, it is the material of choice in modern SMA research. While there are a number of applications of SMA materials, they all share some basic commonalities.[145]

A typical SMA uses a nitinol wire connected to a heater which, as previously discussed, can easily be a current flowing through a resistor. The materials properties of nitinol have been investigated and show the expected temperature dependence.

Properties	NiTi at 23 °C	NiTi at 110 °C
Young's Modulus	33.4 GPa	34.9 GPa
Linear Strain (at 10N)	1.6%	1.56%
Ductile Yield	20-30%	19-30%
Tensile strength	1.05 GPa	.962-.1.7 GPa
Resistivity	4400Ω/cm	4400Ω/cm
Linear coefficient of expansion	1.5×10^{-3} °C^{-1}	$.34\times10^{-3}$ °C^{-1}

Table 6-3: Properties of nitinol at different temperatures.[57]

The actual design of shape memory alloys varies wildly with applications. Studies have shown that nitinol springs can develop stresses in excess of 200 MPa. While these forces are impressive, SMA are not common MEMS devices and due to concerns discussed in Section C, may not see integration into space environments.

D. Reliability Issues for Thermal Actuators

One problem with making bimetallic thermal actuators is that they induce large stresses in the devices. These stresses can cause serious problems for long term reliability. It is not entirely clear how the interfaces that silicon forms with other materials will behave under repeated stressing and unstressing. Since these thermal actuators operate by stresses materials interfaces, there is an increased chance of fracture at this interface, which can lead to delamination. There is also an issue of long term thermal fatigue. Some of these devices are heated to above 800 °C and cooled to ambient temperature within the span of several tens of microseconds,[137] which could cause significant fatigue. The long term effects of this cycling is an issue that needs to be addressed in high-rel thermal actuators.

Thermal actuators are also frequency limited. The response of the actuator is governed by the time it takes for heat to convect and radiate away from a device. If the quantity 1/f is less than the time it takes a device to dissipate heat, oscillatory behavior will effectively stop, as illustrated in Figure 6-30. This causes some interesting concerns for the space environment, as there is no convective heat transfer in a vacuum. Thus the time required to dissipate heat should be significantly slower than it is in terrestrial applications.

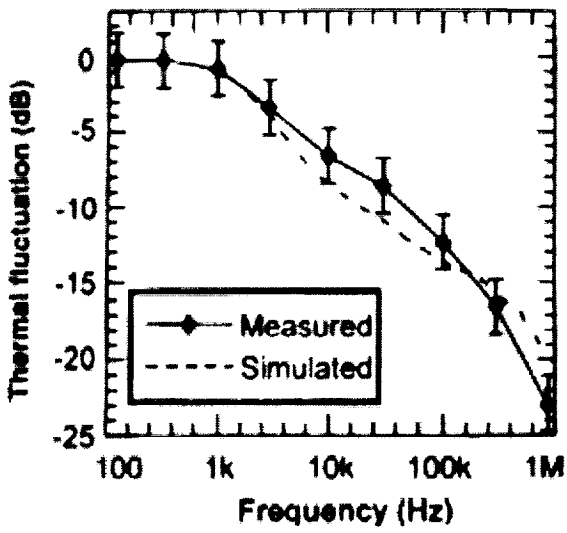

Figure 6-30: Mechanical response as a function of frequency for a thermal actuator. (from [117])

The time, t, required for a body to cool can be modeled by summing the sources of heat energy and equating them to the sinks. For a body radiating heat and having no convective transfer, this results in the equation:[156]

$$mc\frac{dT}{dt} = \sigma_b \varepsilon_m A\left(T^4 - T_0^4\right) \tag{6-65}$$

σ_b = Stefan-Boltzmann constant (5.67×10-8 W/m^2-K^4)

ε_m = emissivity of the material

A = the surface area of the material

T_0 = initial temperature

By solving this equation, it is possible to get a limit on the time it takes for a radiative mass to cool, which indicates the frequency limit of a thermal actuator operating in the vacuum of space.

Shape memory alloys have problems unique to their structures. Since these alloys are usually made of ductile materials, they experience wear and fatigue at much faster rates than brittle materials. While they can withstand stress in the range of a 1 GPa, the lifetime and reliability of these devices at these stresses is unsuitable for long-term operation. If high reliability and millions of temperature cycles are desired, then nitinol should be stretched from its memory state only a few percent and should not exceed a couple hundred MPa of stress.

Another concern with these devices in space applications is inadvertent heating. Since most spacecraft experience wide temperature swings from periods of full solar exposure to eclipse, these devices will either have to have active on-chip thermal control or be in a well thermally regulated part of the spacecraft. Otherwise there could be disastrous implications in using thermal actuators in the space environment.

E. Additional Reading

W. Riethmüller and W Benecke, "Thermally Excited Silicon Microactuators" *IEEE Transactions on Electron Devices*, Vol. 35, No. 6, June 1988.

P. A. Neukomm, H. P. Bornhauser, T. Hochuli, R. Paravicini, and G. Schwarz, "Characteristics of Thin-wire Shape Memory Actuators" *Transducers '89, Proceedings of the 5th International Conference on Solid-State Sensors and Actuators*, Vol. 2, pp. 247-252, June 1990.

IX. Piezoelectric Actuators

Piezoelectric materials exhibit motion under an applied electric field. The piezoelectric effect has been well researched and understood for many years and the MEMS community has used piezoelectrics to build devices that produce strong forces with small actuation distances.

A. The Piezoelectric Effect

Piezoelectricity determines the distribution of the electric polarization and demonstrates how a piezoelectric field reacts to an electric stress by emitting depolarization waves.[6] This polarization field is linearly related to mechanical strain in certain types of crystals, such as quartz and GaAs. When the crystal is in equilibrium, strain is balanced by internal polarization force. However, when equilibrium is offset by external mechanical stress or by an external electric field, the emitting depolarization field will create a force to restore internal equilibrium. As a result, an externally produced electric field will cause a displacement and an externally produced mechanical stress will create an electric field.

Since the piezoelectric effect couples mechanical and electrical fields effectively, it has been researched in a multitude of materials. In 1910, Voigt showed that there were 32 classes of crystals that exhibited piezoelectric properties, and he measured coupling coefficients for these. In MEMS, the most common materials used are crystalline SiO_2 (Quartz), ZnO, AlN, and PZT.

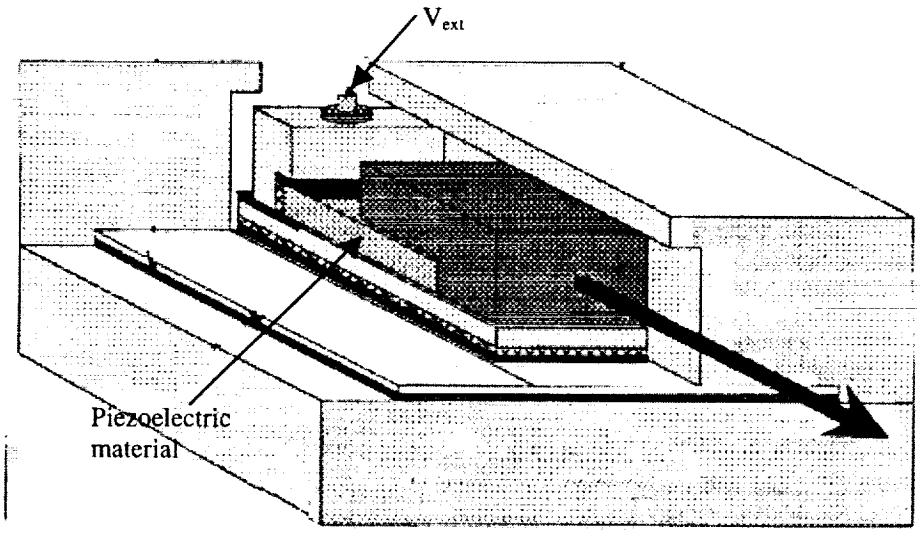

Figure 6-31: Diagram of a piezoelectric transducer (after [106]). An applied voltage causes the piezoelectric material to expand, which drives the structure.

B. Piezoelectric Devices

Piezoelectric devices can be constructed out of a number of different structures. A common implementation of piezoelectrics is to produce a piezoelectric mass and connect electrical leads to it, as shown in Figure 6-25. The extension and contraction of the piezoelectric bar is governed by the equation:

$$D = e_{\varepsilon} E + e\varepsilon \tag{6-66a}$$

$$T = c_E \varepsilon + eE \tag{6-66b}$$

where

E = the electric field

D = electric displacement at equilibrium

e_ε = dielectric constant at zero strain

e = is the piezoelectric stress constant

ε = mechanical strain

T =externally applied stress

c_E = elastic stiffness at equilibrium

So, clearly, the mechanical displacement in this structure is coupled to the applied electric field. One limitation of piezoelectric devices is that the actuation distance is usually small. Since piezoelectric devices operate by inducing a strain in a crystal, it would be extremely unusual to displace a piezoelectric device more than a few percent of its total length.

Piezoelectric devices are also commonly used as sensors. Since piezoelectric materials are electromechanically coupled, these devices can be used in much the same manner as piezoresistive elements, with strain being converted into a change in current instead of a change in resistivity.

C. Reliability Issues

Piezoelectric devices operate by inducing stress in a material. As such, they should be treated as structural devices and be analyzed for stress distributions to prevent fracture. The difficulty with structural analysis in piezoelectric devices stems from the fact that piezoelectric materials have unusual crystal structures. Quartz, for example, is a rhombohedral structure with nine individual elastic constants. For these materials

Young's modulus and Poisson's ratio will exhibit less symmetry than cubic crystals. While the analyses for these materials is not intractable, it is not as straightforward as it is for cubic crystals.

Piezoelectric devices also generate a considerable heat. Since these devices are subjected to mechanical stresses and have significant electrical losses, there is heat transfer across a device. For a rectangular piezoelectric actuator driven at a frequency f, there will be a change in temperature, ΔT, determined by:[116]

$$\Delta T = \frac{ufv_e}{k(T)A} \tag{6-67}$$

where

$$k(T) = \sigma_b \varepsilon_m \left(T^2 + T_0^2\right)\left(T + T_0\right) + \bar{h}_c$$

$\bar{h}_c$ = the average convective heat transfer coefficient (6-30 W/m^2-K in air)

u = loss of the material per cycle

A = surface area of the piezoelectric actuator

v_e = effective volume of the piezoelectric actuator (volume of the material not at equilibrium)

This heat production will stress a material and will also limit the performance of a device. Piezoelectricity is also, like piezoresistivity, temperature sensitive. As such, the heat generation must be considered in determining the reliability characteristics of a piezoelectric device.[116]

D. Additional Reading

J. W. Judy, D. L. Polla, and W. P. Robbins, "Experimental Model and IC-Process Design of a Nanometer Linear Piezoelectric Stepper Motor" *Microstructures, Sensors and Actuators*, DSC-Vol. 19, pp. 11-17, November, 1990.

K. Ikuta, S. Aritomi, T. Kabashima, "Tiny Silent Linear Cybernetic Actuator Driven by Piezoelectric Device with Electromagnetic Clamp", *IEEE Proceedings Microelectro-mechanical Systems*, pp. 232-237, February 1992.

Chapter 7: Finite Element Analysis and Applications to MEMS

J. Newell , K. Man, and B. Stark

The design and development of MEMS is a challenging task, requiring substantial investment in capital equipment and plant facilities. For such investments to be fruitful, MEMS engineers must have the capability to fully characterize the inner workings of these devices, in order to predict temperatures, stresses, dynamic response characteristics, and possible failure mechanisms. Relatively simple hand calculations can often be performed for such analyses, particularly when considering planar or beam-type geometries subject to the influence of temperature, applied force, or pressure loads. These analyses were presented in the preceding chapter for individual devices. The finite element method provides a convenient tool for conducting more complex analyses, and will be discussed in some detail.

In finite element analysis, the structure to be analyzed is discretized into small elements, each having an associated stiffness matrix. Several finite elements have been developed to represent common structures, including quadrilateral plates, triangular plates, solid brick elements, and beam elements. For each such element, the stiffness matrix is stored mathematically in a lookup table, in the form of fundamental equations. When problem-specific parameters such as dimensional coordinates, the material elastic modulus, Poisson's ratio and density are put in these equations, the local stiffness, as represented by one element, is uniquely known. When a structure is fully discretized, or meshed, into many such elements, its global stiffness can be assembled, again in the form of a matrix, from the combined stiffnesses of all the interacting elements. If a force or set of forces is subsequently applied to the structure, the static displacement response can then be calculated by inverting the global stiffness matrix, as follows:

$$\{F\} = \{k\}\{x\} \Rightarrow \{x\} = \{F\}\{k\}^{-1} \tag{7-1}$$

where $\{F\}$ = applied force vector

$\{k\}$ = stiffness matrix

$\{x\}$ = displacement vector.

This basic concept can be used in the solution of many problems involving a variety of applied loading conditions, including externally applied static forces, pressures and temperatures. Several example cases of such analyses are provided below.

I. Heat Transfer Analysis

Finite element models are often used to study the heat transfer characteristics of a device, to understand where and how heat is rejected as well as the transient and steady-state temperature distributions. Figure 7-1 shows such a finite element model of an advanced hybrid, where unpackaged die are bonded to a chip carrier substrate.

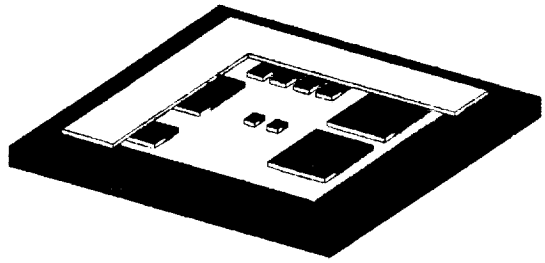

Figure 7-1: Hybrid device with cover removed.

When the device is powered, the die reject a known amount of power. The temperature increase through the stack of materials from the top of the chip to the bottom of the package is evaluated, along with the temperature distribution within the various layers. This identifies any potential limitations due to adhesive or dielectric material selection.

Another example of a heat transfer analysis is illustrated in Figure 7-2, which shows a solid model of a substrate-mounted die. In this model, the die is bonded to a substrate with an adhesive, and the substrate is in turn bonded to a steel header. When the die-generated heat flux is applied to the model, the steady state temperature distribution, shown in the figure, occurs.

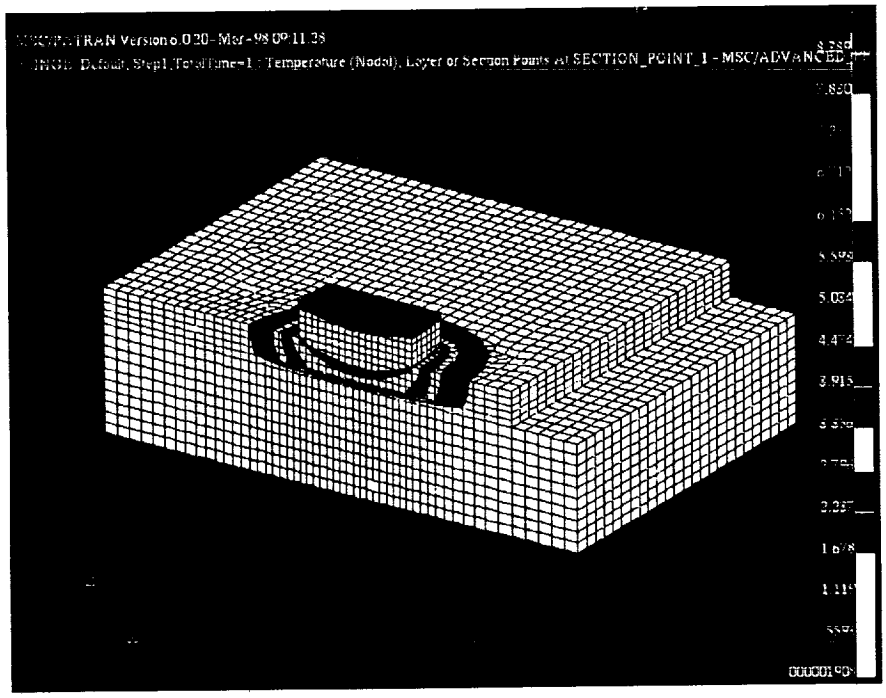

Figure 7-2: Substrate mounted die.

This modeling can be applied to aid in MEMS design. One example of this was done in the development of a microisolation valve for future spacecraft propulsion systems. To do this, a model was created to study temperature distributions in a channel barrier upon application of device power. The geometry of Figure 7-3 was used to create the model of heat distribution, which was analytically loaded with a known power input. The finite element analysis resulted in Figure 7-4, which shows temperature distribution at discrete locations on the valve.

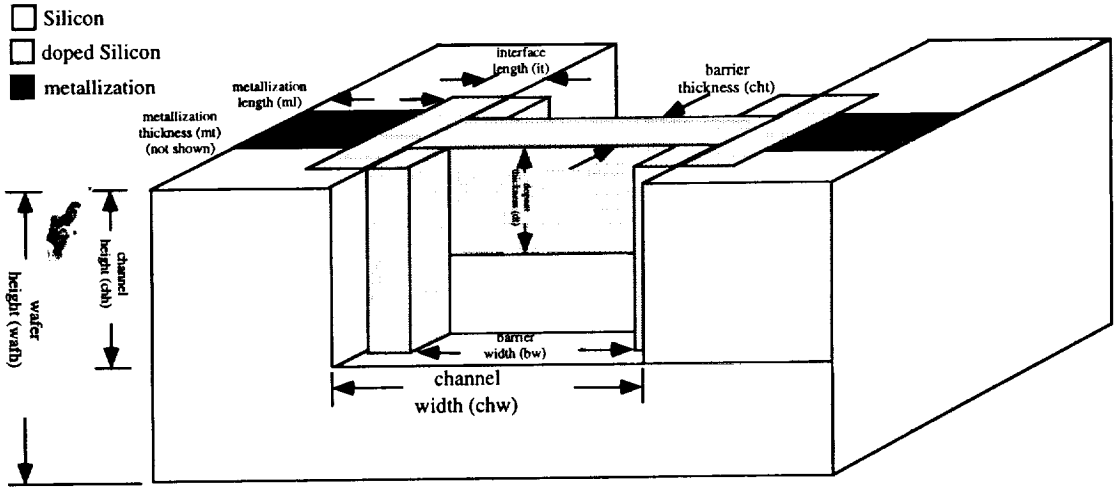

Figure 7-3: Channel barrier schematic.

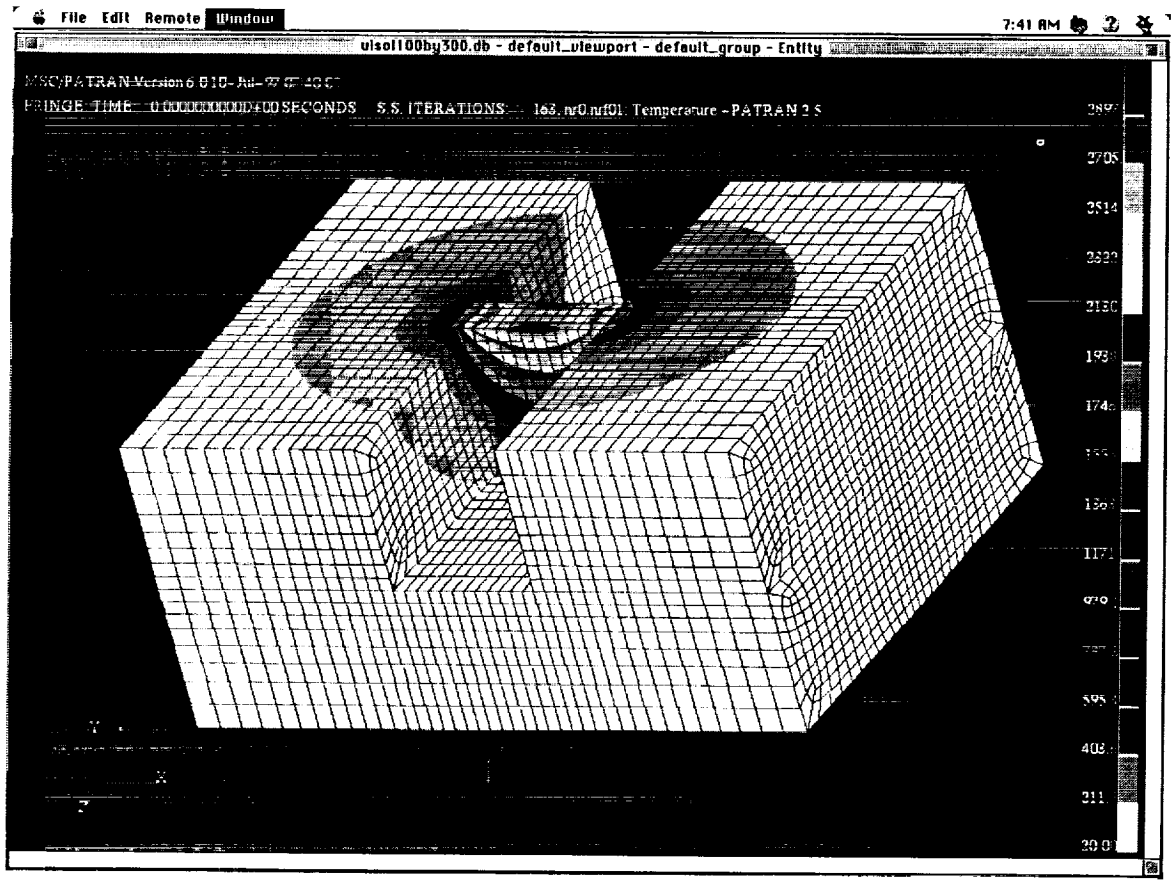

Figure 7-4: Temperature distribution in channel barrier.

II. Thermal Stress Analysis

Finite element modeling can also be used to model thermal stress. Figure 7-4 shows an etched recess in silicon, part of another micropropulsion system, which is used to reduce heat loss into the structure by creating a thermal choke near the edge of the heater strips. The thermal and structural finite element models used to assess the heat loss associated with the geometry of the structure are shown on the right. They show a dramatic reduction in heat loss by decreasing the cross sectional area through which heat flux occurs and by increasing the heat conductive path. However, there is a limit to which the bridge thickness can be reduced without compromising its structural integrity. Through these applications of finite element analyses, it is possible to obtain a nearly optimum design.

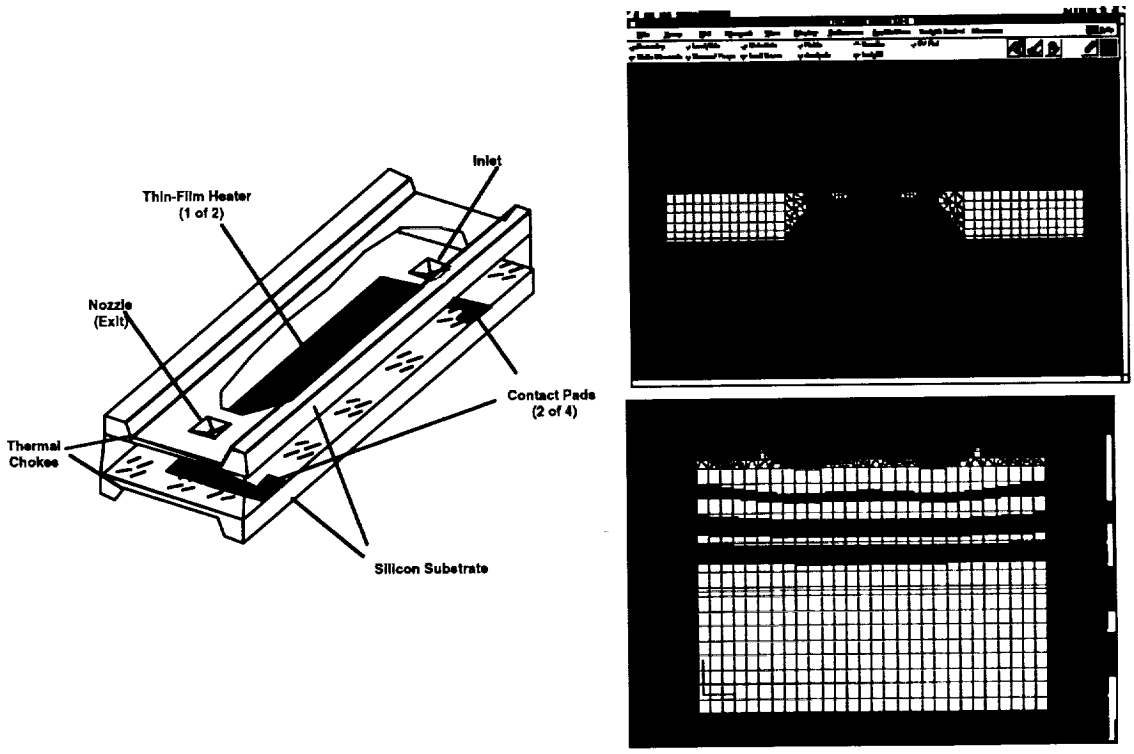

Figure 7-5: Finite element model of a vaporizing liquid microthruster.

III. Thermal Fatigue Stress Analysis

Another application of finite element analysis is examining the effects of thermal fatigue. When structural members are subjected to repeated loading, failure can occur at stresses significantly lower than the ultimate tensile strength of the material, as discussed in Chapter 3. In a fatigue situation, the designer or engineer would generally like to predict the number of cycles a member can endure prior to failure. A widely used technique for such predictions is the Coffin-Manson relation:[60]

$$\frac{\Delta\varepsilon}{2} = \frac{\sigma_f'}{E}(2N_f)^b + \varepsilon_f'(2N_f)^c \tag{7-2}$$

where

$\Delta\varepsilon$ is the total cyclic strain excursion,

σ_f' is the fatigue strength coefficient,

$2N_f$ is the number of load reversals to failure,

b is the fatigue strength exponent,

ε_f is the fatigue ductility coefficient,

c is the fatigue ductility exponent.

The four fatigue parameters σ_f', ε_f', b and c must be determined from experimental cycle test data, and are documented in the literature for many materials. The usefulness of this equation comes from the fact that, when the cyclic strain excursion, elastic modulus and four fatigue parameters are known, the number of load reversals to failure $2N_f$ can be calculated.

This analysis can be facilitated through finite element modeling, and an example of the thermal stresses occurring in microelectronic device vias is offered. The via is an aluminum trace embedded in a parent silicon substrate, which serves as a conductive path to facilitate signal flow from one location to another within the device. When the chip is powered, internally dissipated heat elevates the device temperature, inducing thermal stresses in regions of dissimilar material. These stresses, produced by mismatches in the local coefficient of thermal expansion, are important parameters to understand, as they directly affect the life of the device.

Figure 7-6 shows a 3-dimensional electron microscope image of the structure under study. If a cross-section is taken through the Figure 7-6 via, the geometry illustrated in Figure 7-7 is found. The typical via has a slope of 26 degrees, with sharp intersecting corners at signal plane transitions.

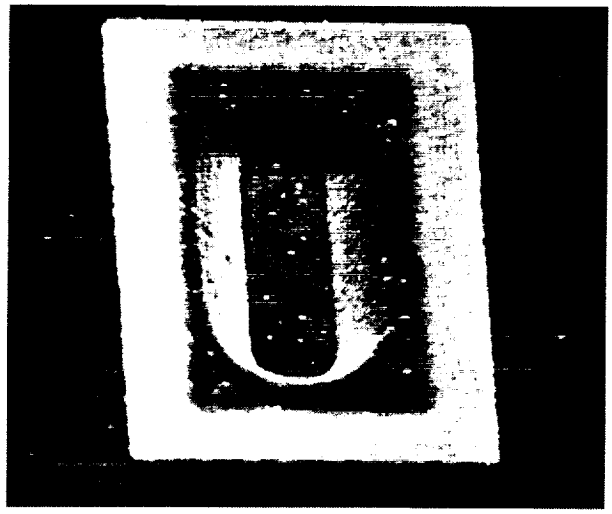

Figure 7-6: Electron micrograph of 3-D intermetallic via.

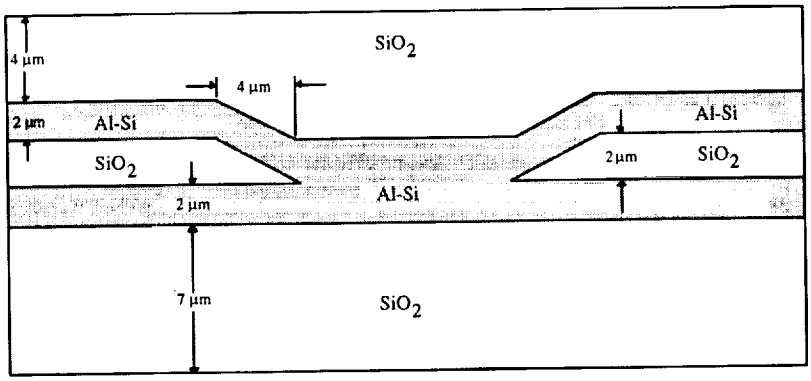

Figure 7-7: Inter-metallization via geometry.

The device must operate in a severe environment, with temperatures ranging from -65 °C to 150 °C. Such a large temperature excursion causes significant stress in the materials, due primarily to the difference in coefficients of thermal expansion between the metal layers and the SiO_2 dielectric. The stress problem is made even worse through duty cycling, in which the unit is powered on and off repeatedly, forcing the via to undergo cyclic stress-strain excursions.

To effect a calculation of the total cyclic strain range, the device cross-section was used in the construction of a 2-dimensional, plane strain finite element model. As illustrated in Figure 7-8, the finalized FEM incorporated 702 two-dimensional elements, connecting a total of 758 space coordinates. A vertical constraint boundary condition was placed on nodes of the base silicon dioxide layer, while a symmetry argument was invoked on the two sides. The top of the passivation layer was allowed to expand without restraint.

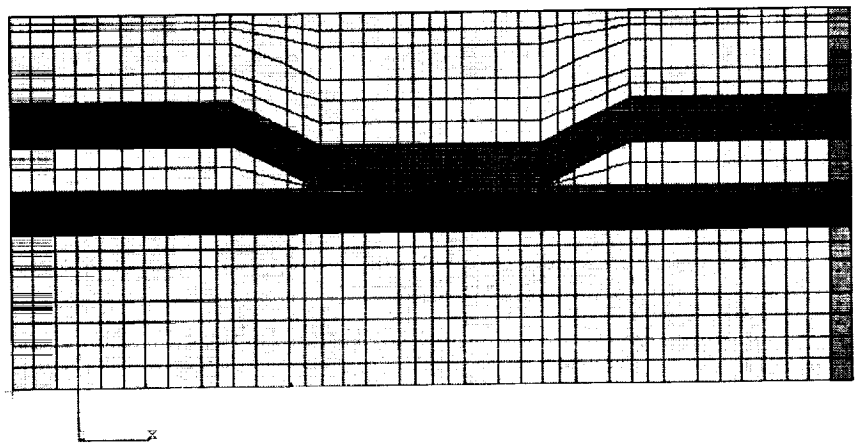

Figure 7-8: Finite element model of intermetallic via.

To obtain the cyclic stress-strain response, a temperature field was applied to the model to simulate repeated heat-up and cool-down cycling between temperatures of -65 °C and 150 °C. The resulting non-linear, elasto-plastic stress-strain response was obtained, assuming a von Mises yield criterion.

Figure 7-9 shows a plot of maximum von Mises equivalent stress versus equivalent strain from the finite element model. The output was requested at a single space coordinate, whose stress-strain response was larger than at any other model location.

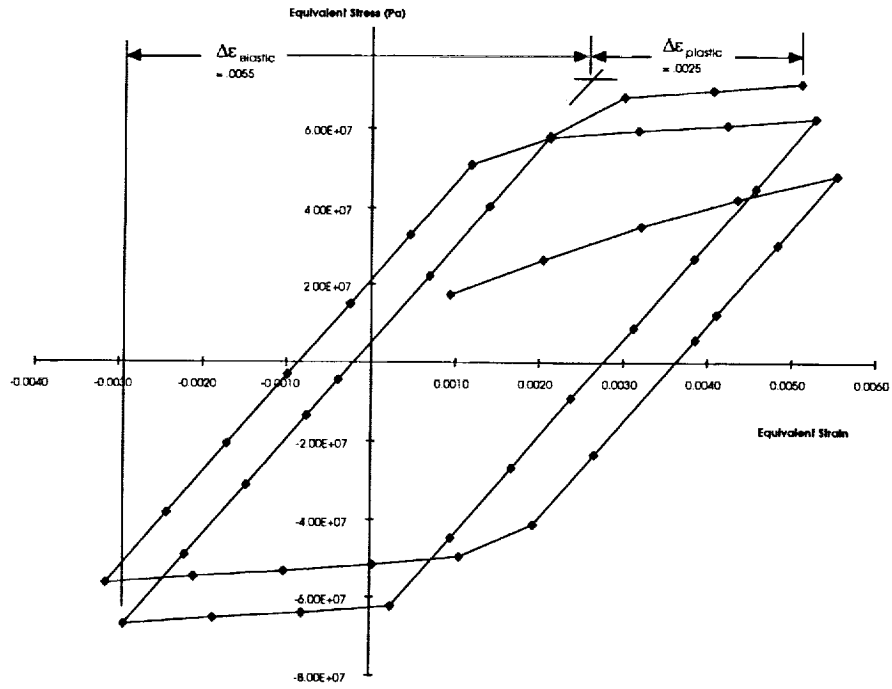

Figure 7-9: Stress-strain hysteresis loop from finite element analysis.

The plot shows a total of 5 temperature cycles, and illustrates a number of interesting facts. Nonlinearity of the via material is evident, with yielding seen to occur at the outset of the initial temperature rise, and subsequently at various points in hot/cold cycling. The material also undergoes strain hardening during each cycle such that, with each subsequent temperature loop, a slightly higher stress is required to develop the same strain. The material response tends to stabilize with each successive load reversal, until a relatively stable hysteresis loop is achieved.

By examining the last, ostensibly stable hysteresis loop, the total cyclic strain range is seen to equal approximately 0.008, with elastic and plastic components as indicated in Figure 7-10. With the cyclic strain range determined, device life can be

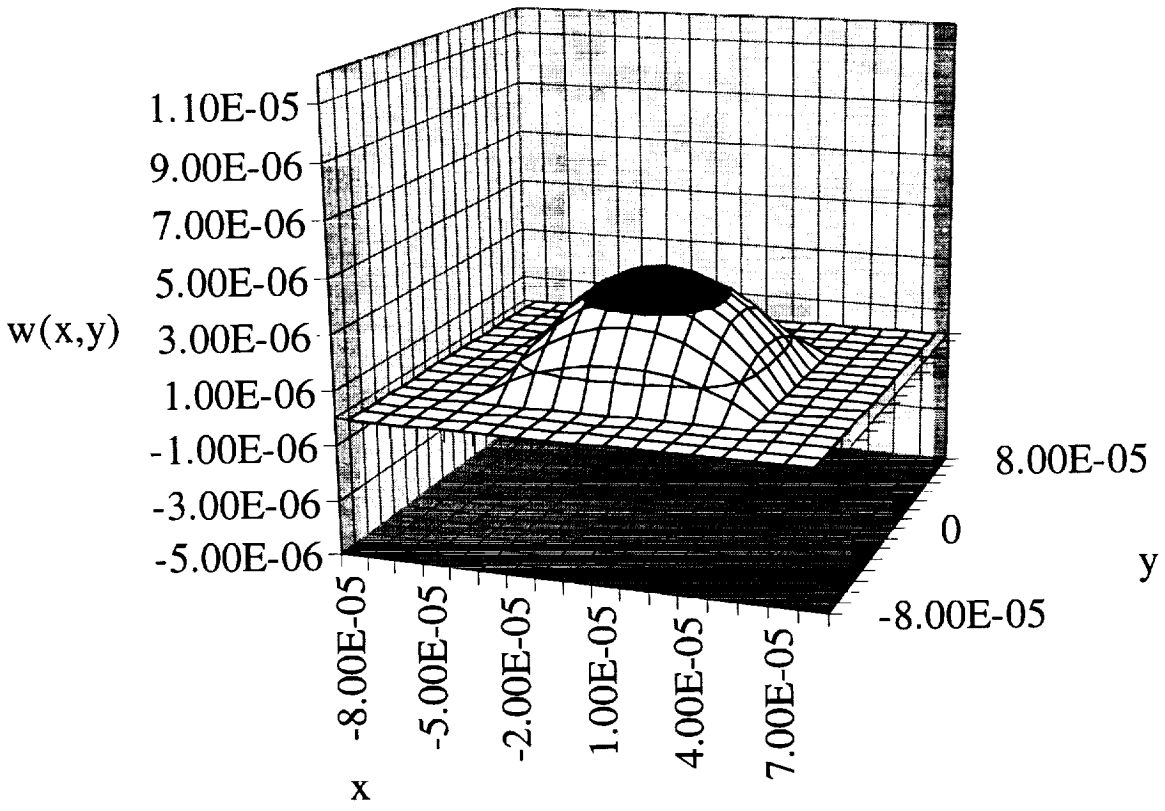

Figure 7-10: Static deflection of a 3 μm thick Si membrane subjected to a 1 MPa pressure.

calculated from Equation 7-2. For additional information regarding these techniques, the reader is referred to References [60] and [62].

IV. Static Analysis

One of the more common uses of finite element modeling is to look at the static motion of mechanical objects. As presented in Chapter 6, motion becomes very difficult to analytically determine as structures become arbitrarily complex. For this reason, finite element modeling can be used to determine the mechanical response of structures to external forces.

One common application of static analysis is in the deflection of thin plates. Application of finite element modeling yields the result for a square plate of width a, with fixed boundary conditions, that the deflection of the center of the plate, w_0, is approximated by:

$$w_0 = \frac{qa^4}{256D} \tag{7-3}$$

where

q = uniformly distributed load

D = flexural rigidity of the membrane

If this method is applied to the entire plate, it will yield a deflection shown in Figure 7-10.

V. Modal Analysis

Another application of finite element modeling to MEMS is the analysis of resonant modes. Modal information is useful because a) it shows displacement maxima in a vibration event, b) it reveals the frequencies of natural vibration, and it can be used to predict the stochastic response of the device when it is excited by random vibration, as occurs during a spacecraft launch. Figures 7-12 and 7-13 show the resulting shapes of two such modes in the device shown in Figure 6-8. It should be noted that these are naturally occurring resonant excitation states of the device, and will be excited if a harmonic forcing function is applied to the unit.

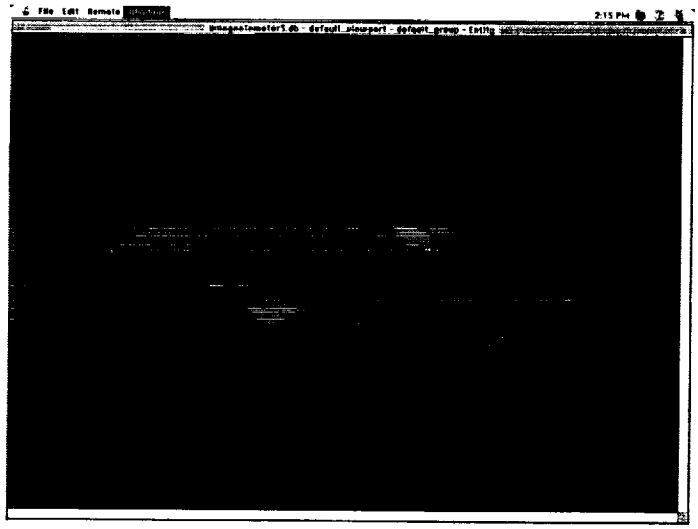

Figure 7-11: Finite element model of a micromagnetometer.

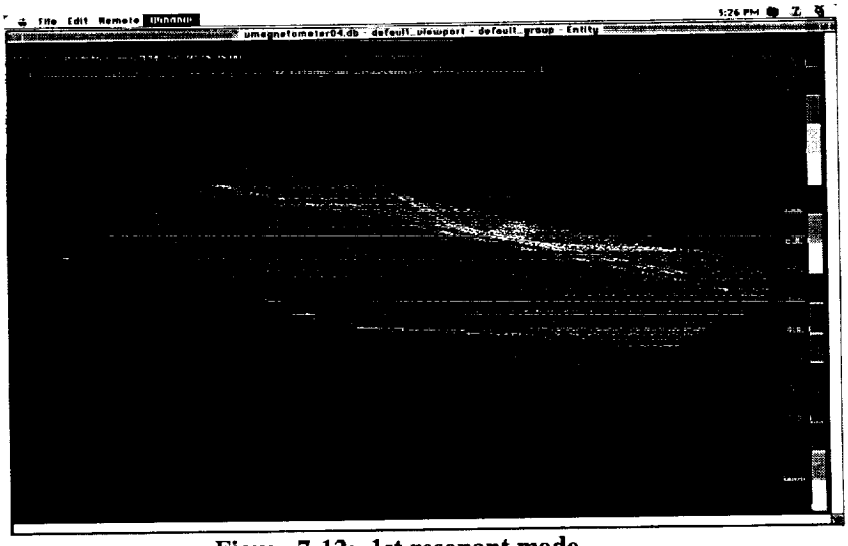

Figure 7-12: 1st resonant mode.

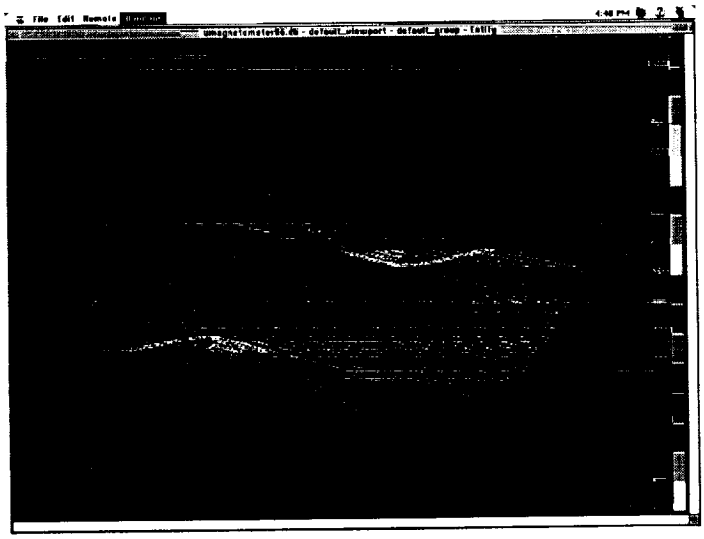

Figure 7-13: 2nd resonant mode.

VI. Software Tools

Many software tools are available for general finite element analysis, and information regarding a number of these is included in the table below. Note that virtually all such packages provide linear static, dynamic and normal modes analysis capabilities. PATRAN and I-DEAS both have highly evolved user interfaces, and are most suitable for pre- and post-processing of finite element models, regardless of the FE solver utilized. ABAQUS and ANSYS are known for their strong capabilities in highly non-linear analysis. Both COSMOS and FEMAP are PC-based codes, designed for optimum performance on Windows-based personal computers. Cosmic NASTRAN is a

public-domain code developed by NASA in the 1960s. As such, it comes with few features, but is available at very low cost.

Software Package	Capabilities	Vendor
Cosmic NASTRAN	Linear statics, dynamics, normal modes	University of Georgia Computer Software Mgmt Info Center 382 East Broad Street Athens, GA 30602-4272 Phone: (706) 542-3265 Web: http://www.cosmic.uga.edu
MSC/PATRAN MSC/NASTRAN MSC/ABAQUS	General pre- and post-processing package Linear statics, dynamics, normal modes, heat transfer Non-linear statics & dynamics	MacNeal Schwindler Corp. 815 Colorado Blvd. Los Angeles, CA 90041-1777 Phone: (800) 336-4858 Web: http://www.macsch.com
ANSYS	Linear statics, dynamics, normal modes, heat transfer Highly non-linear statics & dynamics capability	ANSYS, Inc. Southpointe 275 Technology Drive Canonsburg, PA 15317 Phone: (724) 746-3304 Web: http://www.ansys.com
I-DEAS	General pre- and post-processing package Linear statics, dynamics, normal modes, heat transfer	Structural Dynamics Research Corp. 2000 Eastman Drive Milford, Ohio 45150-2789 Phone: (513) 576-2400 Web: http://www.sdrc.com
FEMAP	General pre- and post-processing package Linear statics, dynamics, normal modes, heat transfer	Enterprise Software Products, Inc. 415 Eagleview Blvd., Suite 105 Exton, PA 19341 Phone: (610) 458-3660 Web: http://www.entsoft.com
COSMOS	Linear statics, dynamics, normal modes, heat transfer	Structural Research & Analysis Corp. 12121 Wilshire Boulevard, 7th Floor Los Angeles, CA 90025 Phone: (310) 207-2800 Web: http://www.cosmosm.com

Table 7-1: Finite element modeling software packages.

VII. Additional Reading

Timoshenko, S. and Woinowsky-Krieger, Theory of Plates and Shells, 2nd edition, New York: McGraw-Hill, 1959

Roark, R. and Young, W., Roark's Formulas for Stress and Strain, 6th edition, New York: McGraw-Hill, 1989.

Shigley, J., and Mischke, C., Mechanical Engineering Design, 5th edition, New York: McGraw-Hill, 1989.

Blevins, R., Formulas for Natural Frequency and Mode Shape, New York: Van Nostrand Reinhold, 1979.

Newell, J., Larson, T. and Cornford S., "A Thermo-mechanical Stress Analysis of an MCM-D Interconnect," Proceedings of the Pan Pacific Microelectronics Symposium, Honolulu, Hawaii, February 1996.

Chapter 8: MEMS Packaging

R. D. Gerke

I. Introduction

MEMS is a relatively new field which is tied so closely with silicon processing that most of the early packaging technologies will most likely use "off-the-shelf" packaging "borrowed" from the semiconductor microelectronics field. Packaging of microelectronics circuits is the science and art of establishing interconnections and an appropriate operating environment for predominantly electrical (and in the case of MEMS, electromechanical) circuits to process and/or store information.

Packaging manifests itself in novel and unique creations that ingeniously reconcile and satisfy what seem to be mutually exclusive application requirements and constraints posed by the laws of nature and the properties of materials and processes. All applications can be summed up in three terms: cost, performance and reliability.

Packaging can span from the consumer to midrange systems to the high performance/reliability applications. It must be noted that no sharp boundaries exist between the classes, only a gradual shift from optimization for parameters which control performance and cause the cost to increase. All along, the reliability must also be considered. The packaging chapter that follows will summarize the primary package types that will likely apply to MEMS technology and the concerns that traditionally have concerned the microelectronics field.

Webster's dictionary defines **package** as a group or a number of things, boxed and offered as a unit. MEMS packages can contain many electrical and mechanical components. To be useful to the outside world these components need interconnections. Alone, a MEM die sawed from a wafer is extremely fragile and must be protected from mechanical damage and hostile environments. To function, electrical circuits need to be supplied with electrical energy, which is consumed and transformed into mechanical and thermal (heat) energy. Because the system operates best within a limited temperature range, packaging must offer an adequate means for removal of heat.

II. Functions of MEMS Packages

The package serves to integrate all of the components required for a system application in a manner that minimizes size, cost, mass and complexity. The package provides the interface between the components and the overall system. The following subsections present the three main functions of the MEMS package: mechanical support, protection from the environment, and electrical connection to other system components.

A. Mechanical Support

Due to the very nature of MEMS being mechanical, the requirement to support and protect the device from thermal and mechanical shock, vibration, high acceleration, particles, and other physical damage (possibly radiation) during storage and operation of the part becomes critical. The mechanical stress endured depends on the mission or application. For example, landing a spacecraft on a planet's surface creates greater mechanical shock than experienced by a communication satellite. There is also a difference between space and terrestrial applications.

The coefficient of thermal expansion (CTE) of the package should be equal to or slightly greater than the CTE of silicon for reliability, since thermal shock or thermal cycling may cause die cracking and delamination if the materials are unmatched or if the silicon is subject to tensile stress. Other important parameters are thermal resistance of the carrier, the material's electrical properties, and its chemical properties, or resistance to corrosion.

Once the MEMS device is supported on a (chip) carrier, the wire bonds or other electrical connections are made, the assembly must be protected from scratches, particulates, and other physical damage. This is accomplished either by adding walls and a cover to the base or by encapsulating the assembly in plastic or other material. Since the electrical connections to the package are usually made through the walls, the walls are typically made from glass or ceramic. The glass or ceramic can also be used to provide electrical insulation of the leads as they exit through a conducting package wall (metal or composite materials). Although the CTE of the package walls and lid do not have to match the CTE of silicon based MEMS as they are not in intimate contact (unless an encapsulating material is used), it should match the CTE of the carrier or base to which they are connected.

B. Protection From Environment

a) The Simple – Mechanical only

Many MEMS devices are designed to measure something in the immediate surrounding environment. These devices range from biological 'sniffers' to chemical MEMS that measure concentrations of certain types of liquids. So the traditional 'hermeticity' that is generally thought of for protecting microelectronic devices may not apply to all MEMS devices. These devices might be directly mounted to a printed circuit board (PCB) or a hybrid–like ceramic substrate and have nothing but a 'housing' to protect it from mechanical damage such as dropping or something as simple as damage from the operator's thumb.

b) The Traditional – Hermetic and non-Hermetic

Many elements in the environment can cause corrosion or physical damage to the metal lines of the MEMS as well as other components in the package. Although there is no moisture in space, moisture remains a concern for MEMS in space applications since it may be introduced into the package during fabrication and before sealing. The susceptibility of the MEMS to moisture damage is dependent on the materials used in its manufacture. For example, Al lines can corrode quickly in the presence of moisture, whereas Au lines degrade slowly, if at all, in moisture. Also, junctions of dissimilar metals can corrode in the presence of moisture. Moisture is readily absorbed by some materials used in the MEMS fabrication, die attachment, or within the package; this absorption causes swelling, stress, and possibly delamination.

To minimize these failure mechanisms, MEMS packages for high reliability applications may need to be hermetic with the base, sidewalls, and lid constructed from materials that are good barriers to liquids and gases and do not trap gasses that are later released.

C. Electrical Connection to Other System Components

Because the package is the primary interface between the MEMS and the system, it must be capable of transferring DC power and in some designs, RF signals. In addition, the package may be required to distribute the DC and RF power to other components inside the package. The drive to reduce costs and system size by integrating more MEMS and other components into a single package increases the electrical distribution problems as the number of interconnects within the package increases.

When designs also require high frequency RF signals, the signals can be introduced into the package along metal lines passing through the package walls, or they may be electromagnetically coupled into the package through apertures in the package walls. Ideally, RF energy is coupled between the system and the MEMS without any loss in power, but in practice, this is not possible since perfect conductors and insulators are not available. In addition, power may be lost to radiation, by reflection from components that are not impedance matched, or from discontinuities in the transmission lines. The final connection between the MEMS and the DC and RF lines is usually made with wire bonds, although flip-chip die attachment and multilayer interconnects using thin dielectric may also be possible.

D. Thermal Considerations

For small signal circuits, the temperature of the device junction does not increase substantially during operation, and thermal dissipation from the MEMS is not a problem. However, with the push to increase the integration of MEMS with power from other circuits such as amplifiers perhaps even within a single package, the temperature rise in

the device junctions can be substantial and cause the circuits to operate in an unsafe region. Therefore, thermal dissipation requirements for power amplifiers, other large signal circuits, and highly integrated packages can place severe design constraints on the package design.

The junction temperature of an isolated device can be determined by

$$Tj = Q * R, + T_{case}$$

where

Q is the heat generated by the junction and is dependent on the output power of the device and its efficiency,

R is the thermal resistance between the junction and the case, and

T is the temperature of the case.

Normally, the package designer has no control over Q and the case temperature, and therefore, it is the thermal resistance of the package that must be minimized. Figure 8-1 is a schematic representation of the thermal circuit for a typical package, where it is assumed that the package base is in contact with a heat sink or case.

It is seen that there are three thermal resistances that must be minimized: the resistance through the package substrate, the resistance through the die-attach material, and the resistance through the carrier or package base. Furthermore, the thermal resistance of each is dependent on the thermal resistivity and the thickness of the material. A package base made of metal or metal composites has very low thermal resistance and therefore does not add substantially to the total resistance. When electrically insulating materials are used for bases metal-filled via holes are routinely used, under the MEMS, to provide a thermal path to the heat sink. Although thermal resistance is a consideration in the choice of the die attach material, adhesion and bond strength are even more important. To minimize the thermal resistance through the die-attach material, the material must be thin, there can be no voids, and the two surfaces to be bonded should be smooth.

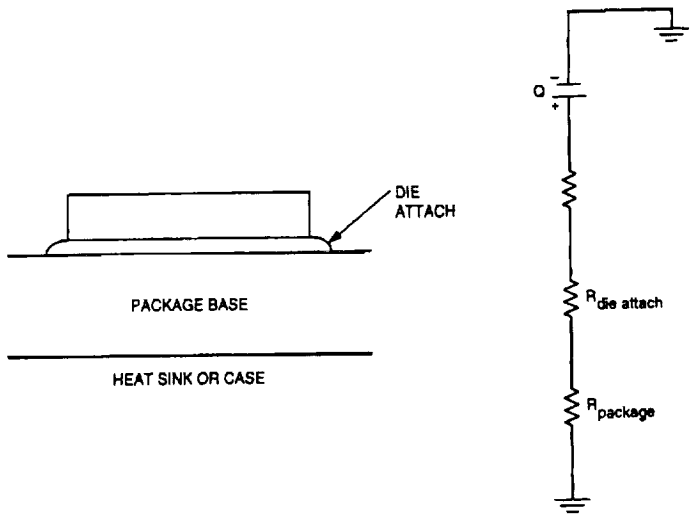

Figure 8-1: Cross section of MMIC attached to a package and its equivalent thermal circuit.

III. Types of MEMS Packages

Each MEMS application usually requires a new package design to optimize its performance or to meet the needs of the system. It is possible to loosely group packages into several categories. Four of these categories: 1) all metal packages, 2) ceramic, 3) plastic packages, and 4) thin-film multilayer packages are presented below.

A. Metal Packages

Metal packages are often used for microwave multichip modules and hybrid circuits because they provide excellent thermal dissipation and excellent electromagnetic shielding. They can have a large internal volume while still maintaining mechanical reliability. The package can use either an integrated base and sidewalls with a lid or it can have a separate base, sidewalls, and lid. Inside the package, ceramic substrates or chip carriers are required for use with the feedthroughs.

The selection of the proper metal can be critical. CuW (10/90), Silvar™ (a Ni-Fe alloy), CuMo (15/85), and CuW (15/85) all have good thermal conductivity and a higher CTE than silicon, which makes them good choices. Kovar™, a Fe-Ni-Co alloy commonly. All of the above materials, in addition to Alloy-46, may be used for the sidewalls and lid. Cu, Ag, or Au plating of the packages is commonly done.

Before final assembly, a bake is usually performed to drive out any trapped gas or moisture. This reduces the onset of corrosion-related failures. During assembly, the highest temperature curing epoxies or solders should be used first and subsequent processing temperatures should decrease until the final lid seal is done at the lowest temperature to avoid later steps damaging earlier steps. Au-Sn is a commonly used solder

that works well when the two materials to be bonded have similar CTEs. Au-Sn solder joints of materials with a large CTE mismatch are susceptible to fatigue failures after temperature cycling. The AuSn intermetallics that form tend to be brittle and can accommodate only low amounts of stress.

Welding (using lasers to locally heat the joint between the two parts without raising the temperature of the entire part) is a commonly used alternative to solders. Regardless of the seal technology, no voids or misalignments can be tolerated since they can compromise the package hermeticity. Hermeticity can also be affected by the feedthroughs that are required in metal packages. These feedthroughs are generally made of glass or ceramic and each method (glass seal or aluminum feedthrough) has its weakness. Glass can crack during handling and thermal cycling. The conductor exiting through the ceramic feedthrough may not seal properly due to metallurgical reasons. Generally, these failures are due to processing problems as the ceramic must be metallized so that the conductor (generally metal) may be soldered (or brazed) to it. The metallization process must allow for complete wetting of the conducting pin to the ceramic. Incomplete wetting can show up as a failure during thermal cycle testing.

B. Ceramic Packages

Ceramic packages have several features that make them especially useful for microelectronics as well as MEMS. They provide low mass, are easily mass produced, and can be low in cost. They can be made hermetic, and can more easily integrate signal distribution lines and feedthroughs. They can be machined to perform many different functions. By incorporating multiple layers of ceramics and interconnect lines, electrical performance of the package can be tailored to meet design requirements. These types of packages are generally referred to as co-fired multilayer ceramic packages. Details of the co-fired process are outlined below. Multilayer ceramic packages also allow reduced size and cost of the total system by integrating multiple MEMS and/or other components into a single, hermetic package. These multilayer packages offer significant size and mass reduction over metal-walled packages. Most of that advantage is derived by the use of three dimensions instead of two for interconnect lines.

Co-fired ceramic packages are constructed from individual pieces of ceramic in the "green" or unfired state. These materials are thin, pliable films. During a typical process, the films are stretched across a frame in a way similar to that used by an artist to stretch a canvas across a frame. On each layer, metal lines are deposited using thick-film processing (usually screen printing), and via holes for interlayer interconnects are drilled or punched. After all of the layers have been fabricated, the unfired pieces are stacked and aligned using registration holes and laminated together. Finally, the part is fired at a high temperature. The MEMS and possibly other components are then attached into place (usually organically (epoxy) or metallurgically (solders), and wire bonds are made the same as those used for metal packages.

Several problems can affect the reliability of this package type. First, the green-state ceramic shrinks during the firing step. The amount of shrinkage is dependent on the number and position of via holes and wells cut into each layer. Therefore, different layers may shrink more than others creating stress in the final package. Second, because ceramic-to-metal adhesion is not as strong as ceramic-to-ceramic adhesion, sufficient ceramic surface area must be available to assure a good bond between layers. This eliminates the possibility of continuous ground planes for power distribution and shielding. Instead, metal grids are used for these purposes. Third, the processing temperature and ceramic properties limit the choice of metal lines. To eliminate warping, the shrinkage rate of the metal and ceramic must be matched. Also, the metal must not react chemically with the ceramic during the firing process. The metals most frequently used are W and Mo. There is a class of Low Temperature Co-fired Ceramic (LTCC) packages. The conductors that are generally used are Ag, AgPd, Au, and AuPt. Ag migration has been reported to occur at high temperatures, high humidity, and along faults in the ceramic of LTCC.

C. Thin-Film Multilayer Packages

Within the broad subject of thin-film multilayer packages, two general technologies are used. One uses sheets of polyimide laminated together in a way similar to that used for the LTCC packages described above, except a final firing is not required. Each individual sheet is typically 25 μm and is processed separately using thin-film metal processing. The second technique also uses polyimide, but each layer is spun onto and baked on the carrier or substrate to form 1- to 20 μm-thick layers. In this method, via holes are either wet etched or reactive ion etched (RIE). The polyimide for both methods has a relative permittivity of 2.8 to 3.2. Since the permittivity is low and the layers are thin, the same characteristic impedance lines can be fabricated with less line-to-line coupling; therefore, closer spacing of lines is possible. In addition, the low permittivity results in low line capacitance and therefore faster circuits.

D. Plastic Packages

Plastic packages have been widely used by the electronics industry for many years and for almost every application because of their low manufacturing cost. High reliability applications are an exception because serious reliability questions have been raised. Plastic packages are not hermetic, and hermetic seals are generally required for high reliability applications. The packages are also susceptible to cracking in humid environments during temperature cycling of the surface mount assembly of the package to the mother-board. Plastic packaging for space applications may gain acceptability as time goes on. The reliability of plastic packages is presented in Section 8-V.

IV. Package-to-MEMS Attachment

The method used to attach a MEMS device to a package is a general technology applicable to most Integrated Circuit (IC) devices. Generally referred to as *die attach*, the function serves several critical functions. The main function is to provide good mechanical attachment of the MEMS structure to the package base. This ensures that the MEMS chip (or die) does not move relative to the package base. It must survive hot and cold temperatures, moisture, shock and vibration. The attachment may also be required to provide a good thermal path between the MEMS structure and the package base. Should heat be generated by the MEMS structure or by the support circuitry, the attachment material should be able to conduct the heat from the chip to the package base. The heat can be conducted away from the chip and 'spread' to the package base which is larger in size and has more thermal mass. This spreading can keep the device operating in the desired temperature range. If the support circuitry requires good electrical contact from the silicon to the package base, the attachment material should be able to accommodate the task.

The stability and reliability of the attach material is largely dictated by the ability of the material to withstand thermomechanical stresses created by the differences in the coefficient of thermal expansion (CTE) between the MEMS silicon and the package base material. These stresses are concentrated at the interface between the MEMS silicon backside and the attach material and the interface between the die attach material and the package base. Silicon has a CTE between 2 and 3 ppm/°C while most package bases have higher CTE (6 to 20 ppm/°C). An expression which relates the number of thermal cycles that a die attach can withstand before failure is based on the Coffin-Manson relationship for strain. The equation below defines the case for die attach,

$$N(f) \propto \gamma^{m}\left(\frac{2*t}{L*\Delta CTE*\Delta T}\right)$$

where

γ = shear strain

m = material constant

L = diagonal length of the die

T = die-attach material thickness

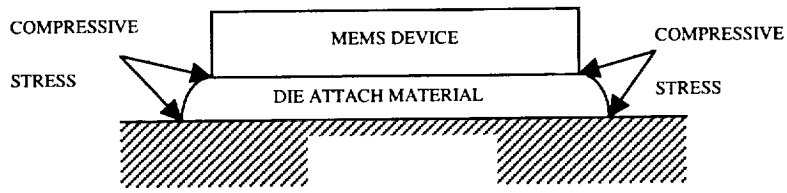

Figure 8-2: MEMS device in compression.

Voids in the die attach material cause areas of localized stress concentration that can lead to premature delamination. Presently, MEMS packages use solders, adhesives or epoxies for die attach. Each method has advantages and disadvantages that affect the overall MEMS reliability. Generally, when a solder is used, the silicon die would have a gold backing. Au-Sn (80-20) solder generally is used and forms an Au-Sn eutectic when the assembly is heated to approximately 250°C in the presence of a forming gas. When this method is applied, a single rigid assembled part with low thermal and electrical resistances between the MEMS device and the package. One problem with this attachment method is that the solder attach is rigid (and brittle) which means it is critical for the MEMS device and the package CTEs match since the solder cannot absorb the stresses.

Adhesives and epoxies are comprised of a bonding material filled with metal flakes as shown in the figure. Typically, Ag flakes are used as the metal filler since it has good electrical conductivity and has been shown not to migrate through the die attach material.[1,2] These die attach materials have the advantage of lower process temperatures. Generally between 100 and 200 °C are required to cure the material. They also have a lower built-in stress from the assembly process as compared to solder attachment. Furthermore, since the die attach does not create a rigid assembly, shear stresses caused by thermal cycling and mechanical forces are relieved to some extent.[3,4] One particular disadvantage of the soft die attach materials are that they have a significantly higher electrical resistivity which is 10 to 50 times greater than solder and a thermal resistivity which is 5 to 10 times greater than solder. Lastly, humidity has been shown to increase the aging process of the die-attach material.[2]

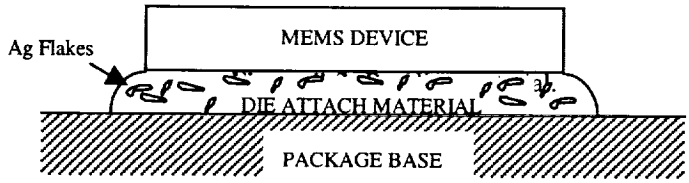

Figure 8-3: Schematic representation of silver filled epoxy resin.

V. Chip Scale Packaging

A. Flip Chip

Controlled Collapse Chip Connection (C4) is an interconnect technology developed by IBM during the 1960s as an alternative to manual wire bonding.

Often called "flip-chip," C4 attaches a chip with the circuitry facing the substrate. C4 uses solder bumps (C4 Bumps) deposited through a Bump Mask onto wettable chip pads that connect to matching wettable substrate pads (Figure 8-4). MEMS technology initially may not use flip chip packaging but the drive toward miniaturization may necessitate its incorporation into future designs.

"Flipped" chips align to corresponding substrate metal patterns. Electrical and mechanical interconnects are formed simultaneously by reflowing the C4 Bumps (Figure 8-5). The C4 joining process is self-aligning, i.e., the wetting action of the solder will align the chip's bump pattern to the corresponding substrate pads. This action compensates for slight chip-to-substrate misalignment (up to several mils) incurred during chip placement.

An added feature of C4 is the ability to rework. Several techniques exist that allow for removal and replacement of C4 chips without scrapping the chip or substrate. In fact, rework can be performed numerous times without degrading quality or reliability.

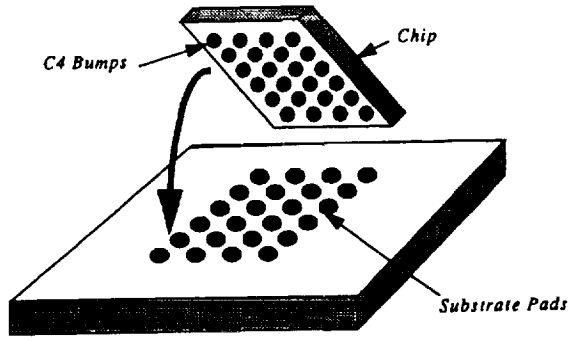

Figure 8-4: C4 (Controlled Collapse Chip Connection) flip chip.

For improved reliability, chip underfill may be injected between the joined chip and substrate as illustrated in Figure 8-5. It should be noted that any rework must be performed prior to application of chip underfill.

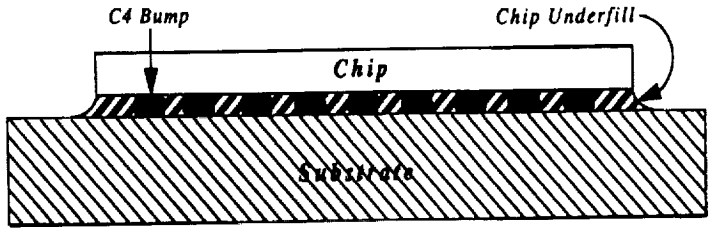

Figure 8-5: Mechanical and electrical connections.

It is important to recognize certain C4 characteristics when deciding on an interconnect technology. While application, size, performance, reliability and cost all must be factored in the selection process. However, these factors cannot be applied to the chip or product only. The overall impact at the system level must be considered for an equivalent comparison.

The primary advantage of C4 is its enabling characteristics. Specific advantages include:

- Size and weight reduction
- Applicability for existing chip designs
- Increased I/0 capability
- Performance enhancement
- Increased production capability
- Rework/chip replacement

Key considerations include:

- Additional wafer processing vs. wire bond
- Supplemental design groundrules
- Wafer probe complexity for array bump patterns
- Unique thermal considerations

Most importantly, C4 provides performance, size and I/O density improvements. With C4, nearly the entire chip surface can be utilized for interconnect pad locations. In fact, it has been demonstrated that one can have over 2500 C4 Bumps on a chip, and chips with over 1500 C4 Bumps are in production.

C4 enables increased interconnect density. Signal, clock and power connections can be placed almost anywhere on the chip and redundancy means distributions can be optimized for minimum noise and skew, current density and line length. Additionally, on-chip wiring can be reduced since z-axis escapes are available where needed.

Figure 8-6 compares single row wirebond and C4 chips. Each chip is 8 mm (200 mil) square. Wirebond pitch is 76 μm (3 mil) pads on 100 μm (4 mil) centers. C4 pitch is 100 μm (4 mil) bumps on 230 μm (9 mil) centers. In this example, interconnect density is increased over 140% using C4.

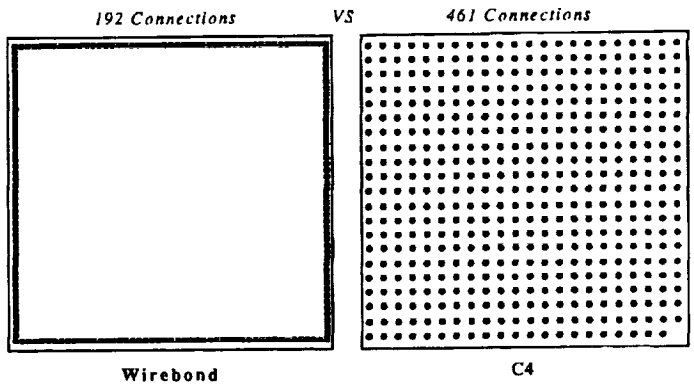

Figure 8-6: Interconnect density (wire bond vs. C4).

The reliability of flip-chip contacts is determined by the difference in the CTE between the chip and the ceramic substrate or the organic printed circuit board (PCB). For example, the CTE for silicon is ~2 – 3 ppm/°K, for 96% alumina it is 6.4 ppm/°K, and for PCB it is typically 20 to 25 ppm/°K. The CTE mismatch between the chip and the carrier induces high thermal and mechanical stresses and strain at the contact bumps. The highest strain occurs at the corner joints, whose distance is the largest from the distance neutral point (DNP) on the chip. For example, the DNP for a 2.5- x 2.5-mm chip is 1.7 mm. The thermomechanical stress and strain cause the joints to crack. When these cracks become large, the contact resistance increases, and the flow of current is inhibited. This ultimately leads to chip electrical failure. The typical reliability defined failure criterion is an increase in resistance in excess of 30 mΩ over the zero time value.[5] The tradeoff in selecting the bump height is that large bumps introduce a series inductance that degrades high-frequency performance and increases the thermal resistance from the device to the carrier, if that is the primary heat path.

The reliability of the bump joints is improved if, after reflow, a bead of encapsulating epoxy resin is dispensed near the chip and drawn by capillary action into the space between the chip and the carrier. The epoxy is then cured to provide the final flip-chip assembly. Figure 8-5 shows a typical flip-chip package. The epoxy-resin underfill mechanically couples the chip and the carrier and locally constrains the CTE mismatch, thus improving the reliability of the joints. The most essential characteristic of the encapsulant is a good CTE match with the z-expansion of the solder or the bump

material. For example, if one uses 95 Pb/5 Sn solder having a CTE of 28 ppm/°K, an encapsulant with a CTE of about 25 ppm/°K is recommended. Underfilling also allows packaging of larger chips by increasing the allowable DNP. In some cases, the encapsulant acts as a protective layer on the active surface of the chip

Good adhesion among the underfill material, the carrier, and the chip surface is needed for stress compensation. The adhesion between the surfaces can be lost and delamination can take place if contaminants, such as post-reflow flux residue, are present. For this reason, a fluxless process for flip-chip assembly is desirable.[5] Unfortunately, flip-chip bonding on PCB requires the use of flux.[6] However, on ceramic carriers with gold, silver, and palladium-silver thick-film patterns and via metallizations, fluxless flipchip thermocompression bonding with gold-tin bumps has demonstrated high reliability.[5] The results of reliability testing[5] are summarized in Table 8-1 and may serve as a guideline for future work.

Parameter	Value
Bump height	30 to 70 μm
Chip size	A few mm
Chip carrier	Ceramic
Carrier camber	5 μm per cm
Camber compensation	By bump deformation
Underfill	Yes
Thermal cycling	After 6500 cycles (-55°C to +125°C), no contact failure and no change in contact resistance
High-temperature storage	After 1000 h, no increase in contact resistance
Temperature and humidity	After 1000 h (85'C and 85% RH), no change in contact resistance
Pressure-cooker test	After 1000 h (121°C and 29.7 psi), contact resistance increased slightly from 3 mW to 4 mW

Table 8-1: Summary of reliability test conditions and results for fluxless flip-chip thermocompression-bonded bump contacts.

Finally, care should be taken that the encapsulant or underfill covers the entire underside without air pockets or voids, and forms complete edge fillets around all four sides of the chip. Voids create high-stress concentrations and may lead to early delamination of the encapsulant. After assembly, a scanning acoustic microscope can be used to locate voids in the encapsulant. The encapsulant should also be checked for microcracks or surface flaws, which have a tendency to propagate with thermal cycling and environmental attacks, eventually leading to chip failure.[7]

B. Ball-Grid-Array (BGA)

Ball Grid Array is a surface mount chip package that uses a grid of solder balls as its connectors. It is noted for its compact size, high lead count and low inductance, which allows lower voltages to be used. BGAs come in plastic and ceramic varieties. It essentially has evolved from the C4 technology whereas more I/Os can be utilized in the same area as in a peripherally leaded package (or chip). The CBGA and PBGA are not truly Chip Scale Packaging but the evolution to the μBGA has come out of the experience the industry has gained from the CBGA and PBGA packages.

i) Ceramic Ball-Grid-Array (CBGA)

Originally designed by IBM, the CBGA was developed to complement their C4 (flip-chip) technology. The package is comprised of a ceramic (alumina) substrate and a C4 chip and an aluminum lid as depicted in Figure 8-7. The ball-grid spacing is on 50 mil centers with solder balls composed of high melt solder (90/10 Pb/Sn) attached by eutectic solder (63/37 Sn/Pb). Recent designs have concentrated on miniaturization and have reduced the package size and utilized 40 mil on center solder balls.

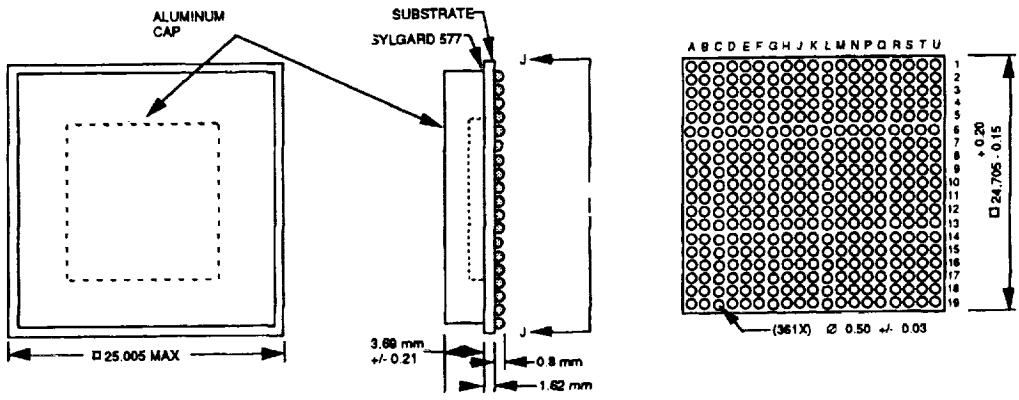

Figure 8-7: Ceramic Ball-Grid-Array Package shown with connections on 50 mil centers with a) top view, b) side view and c) bottom view illustrating the high number of connections.

Aluminum covers that have typically been used with the C4 technology have been bonded with a silicone adhesive (Sylgard 577) to provide a non-hermetic seal. With the flip-chip technology this is usually adequate for most applications. A hermetic seal can be accomplished by designing a seal ring into the ceramic and using a Ni/Fe cover plate for soldering.

The package as described above has a cavity which would allow for typical chip-and-wire technology to be utilized. A MEMS device could be utilized in the wire bond package configuration first and migrate to use as a flip-chip in later designs.

ii) Plastic Ball-Grid-Array (PBGA)

The Plastic Ball-Grid-Array (PBGA) is very similar to the plastic packaging technology described in Section 8-V. It is based on the same chip-and-wire technology and has moisture sensitivity (i.e., susceptible to 'popcorn' cracking during solder reflow) issues just like plastic packaging. It is different in that it is built on a printed circuit board substrate rather than a leadframe (metal) material (Figure 8-8). The attach method (to the motherboard) is accomplished by soldering solder balls or bumps rather than leads.

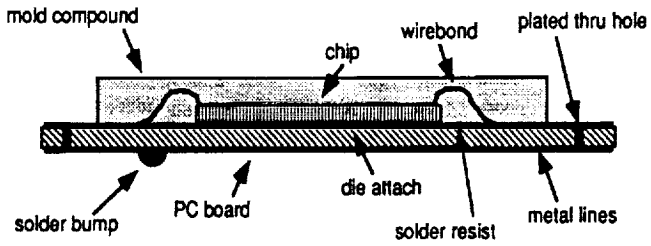

Figure 8-8: A schematic representaion of a Plastic Ball-Grid-Array Package.

One advantage this technology has over conventional plastic packaging is that the PC board material (which can vary from FR4 to polyimide to BT resin to name a few materials) can be a simple 2 layer board or be made of multiple layers. Additional layers allow for power and ground planes.

iii) Micro-Ball-Grid-Array (μBGA)

μBGA is a true "Chip Scale Package" (CSP) solution, only slightly larger than the die itself (die + 0.5mm). It is the ideal package for all memory devices such as Flash, DRAM and SRAM. uBGA packages enable broad real-estate reductions of typically 50-80 percent over existing packages. End use applications include cell phones, sub-notebooks, PDAs, camcorders, disk drives, and other space-sensitive applications. This package is also an excellent solution for applications that require a smaller, thinner, lighter or electrically enhanced package. It therefore lends itself nicely to space flight applications.

The uBGA package is constructed utilizing a thin, flexible circuit tape for its substrate and low stress elastomer for die attachment. The die is mounted face down and

its electrical pads are connected to the substrate in a method similar to TAB bonding. After bonding these leads to the die, the leads are encapsulated with an epoxy material for protection. Solder balls are attached to pads on the bottom of the substrate, in a rectangular matrix similar to other BGA packages. The backside of the die is exposed allowing heat sinking if required for thermal applications. Ball pitches available today are 0.50, 0.75, 0.80, and 1.0 mm. Other features and benefits include: 0.9 mm mounted height, excellent electrical and moisture performance, 63/37 Sn/Pb solder balls, and full in-house design services.

VI. Multichip Packaging

A. MCM/HDI

Multichip packaging of MEMS can be a viable means of integrating MEMS with other microelectronic technologies such as CMOS. One of the primary advantages of using multichip packaging as a vehicle for MEMS and microelectronics is the ability to efficiently host die from different or incompatible fabrication processes into a common substrate. High performance multichip module (MCM) technology has progressed rapidly in the past decade, which makes it attractive for use with MEMS.

The Chip-on-Flex (COF) process has been adapted for the packaging of MEMS.[8] One of the primary areas of the work was reducing the potential for heat damage to the MEMS devices during laser ablation. Additional processing has also been added to minimize the impact of incidental residue on the die.[9]

i) COF/HDI Technology

COF is an extension of the HDI technology developed in the late 1980's. The standard HDI "chips first" process consists of embedding bare die in cavities milled into a ceramic substrate and then fabricating a layered thin-film interconnect structure on top of the components. Each layer in the HDI interconnect overlay is constructed by bonding a dielectric film on the substrate and forming via holes through laser ablation. The metallization is created through sputtering and photolithography.[10]

COF processing retains the interconnect overlay used in HDI, but molded plastic is used in place of the ceramic substrate. Figure 8-9 shows the COF process flow. Unlike HDI, the interconnect overlay is prefabricated before chip attachment. After the chip(s) have been bonded to the overlay, a substrate is formed around the components using a plastic mold forming process such as transfer, compression, or injection molding. Vias are then laser drilled to the component bond pads and the metallization is sputtered and patterned to form the low impedance interconnects.[11]

For MEMS packaging, the COF process is augmented by adding a processing step for laser ablating large windows in the interconnect overlay to allow physical access to

the MEMS devices. Figure 8-10 depicts the additional laser ablation step for MEMS packaging. Additional plasma etching is also included after the via and large area laser ablations to minimize adhesive and polyimide residue which accumulates in the exposed windows.

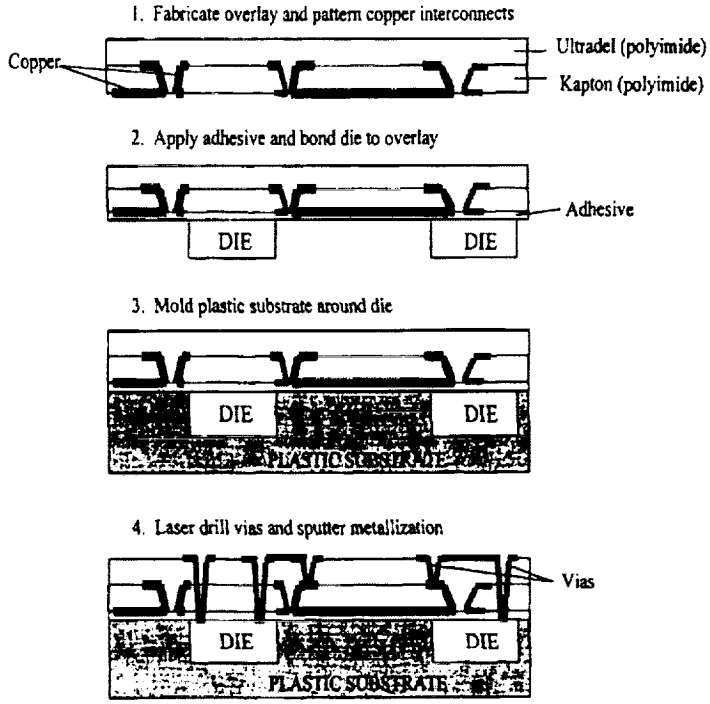

Figure 8-9: Chip-on-Flex (COF) process flow.[1]

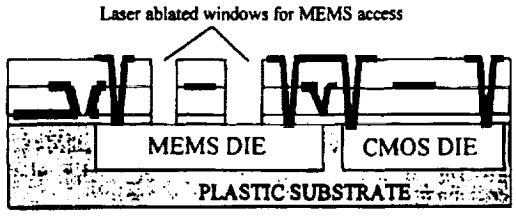

Figure 8-10: Large area ablation for MEMS access in COF package.

ii) MEMS Test Chip

MEMS test die can be used in research to assess the impact of various packaging technologies on MEMS. Test die typically contain devices and structures designed to facilitate a structured method of monitoring the health of MEMS devices after packaging.

Surface micromachined test die have been available through the Multi-User MEMS Processes (MUMPs). The MUMPs process has three structural layers of polysilicon which are separated by sacrificial layers of silicon oxide. The substrate is electrically isolated from the polysilicon layers by a silicon nitride barrier. The top layer of the process is gold and is provided to facilitate low-impedance wiring of the MEMS devices but can also be used as a reflective surface for optical devices. Table 8-2 lists nominal thicknesses of the various layers, and Figure 8-11 shows a cross-sectional view of a notional MUMPs layout.

Layer	Thickness (μm)
Gold	0.5
Poly 2	1.5
2^{nd} Oxide	0.75
Poly 1	2.0
1^{st} Oxide	2.0
Poly 0	0.5
Nitride	0.6

Table 8-2: MUMPs layer thickness.[10]

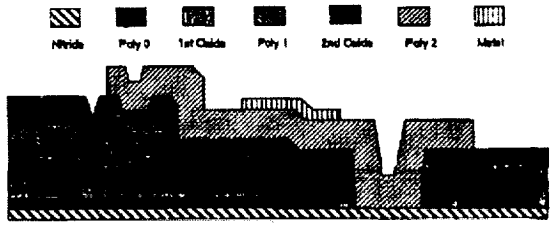

Figure 8-11: Cross-section of MUMPs layout.[10]

Among the test structures on the test die are breakage detectors to monitor excess force and polysilicon resistors to monitor excess heating. Other devices on the die are representative of MEMS structures which might be used in an actual application. Table 8-3 lists general categories of devices on the surface micromachining test die.

Device Category
Breakage Detectors
Polysilicon Resistors
Variable Capacitors
Flip-up and Rotating Devices
Thermal Actuators
Electrostatic Piston Mirrors
Electrostatic Comb Drives

Table 8-3: MEMS device categories included on surface micromachining test die.

The bulk micromachining test die was fabricated through MOSIS using the Orbit CMOS MEMS process. The CMOS MEMS process is based on the standard 2 μm CMOS technology. The CMOS process has two metal and two polysilicon layers. Additional processing is added to allow MEMS fabrication. Provisions are made to specify cuts in the overglass to expose the silicon substrate for bulk micromachining. In addition, regions of boron doping can be specified to form etch steps for anisotropic silicon etchants such as ethylene diamine Pyrocatechol (EDP) and potassium hydroxide (KOH). These tools allow for bulk micromachining to be accomplished in the standard CMOS process.[12] Table 8-4 lists some of the device categories represented on our bulk micromachining test die. A sampling of integrated circuits such as ring oscillators for testing package interconnects was also included on the test die.

Device Category
Breakage Detectors
Polysilicon Resistors
Cantilevers
Suspended Structures
Thermal Bimorphs

Table 8-4: MEMS device categories included on bulk micromachining test die.

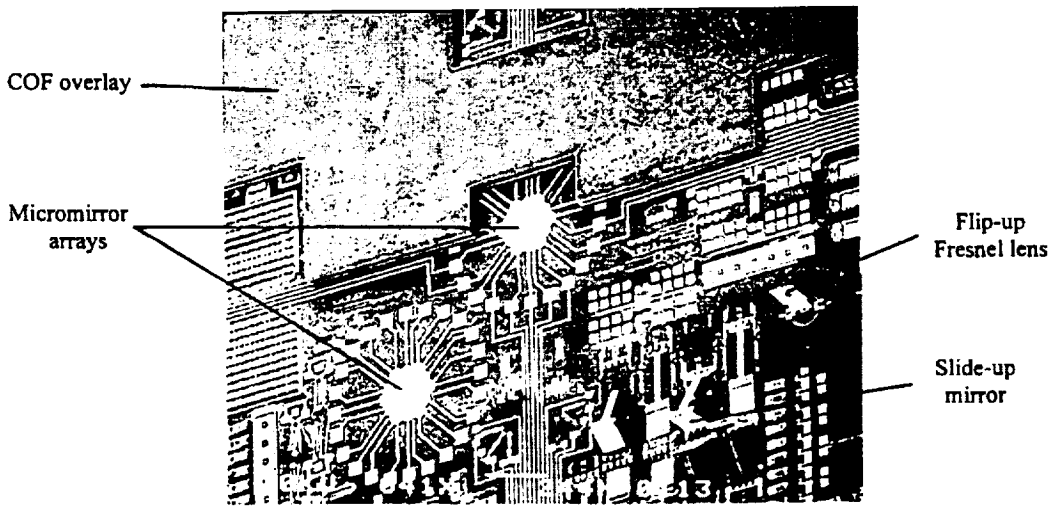

Figure 8-12: Windows laser ablated in COF overly for MEMS access.[9]

B. System on a Chip (SOAC)

System on a chip may not necessarily be classified as a packaging technology. It is derived from the wafer fabrication process where numerous individual functions are processed on a single piece of silicon. These processes, generally CMOS technology, are compatible with the MEMS processing technology. Most SOAC chips are designed with a microprocessor of some type, some memory, some signal processing and others. It is very conceivable that a MEMS device could one day be incorporated on a SOAC. Initially, it may be incorporated by some other packaging technology such as flip chip or μBGA.

VII. Plastic Packaging (PEMs)

Most MEMS designs either have moving parts or do not allow for intimate contact of an encapsulating material such as in a traditional plastic package. Furthermore, plastic packages have not gained wide acceptance in the field of space applications. However, there are many semiconductor designs that are beginning to be flown in space applications. Programs such as Commercial of the Shelf (COTS) which include Plastic Encapsulated Microelectronics (PEMs) are gaining wide acceptance. It is therefore important to outline the basic issues in PEMs for MEMS applications.

Studies have shown that during the high-temperature soldering process encountered while mounting packaged semiconductor devices on circuit boards, moisture present in a plastic package can vaporize and exert stress on the package. This stress causes the package to crack and also causes delamination between the mold compound and the lead frame or die. This phenomenon is often referred to as 'popcorn' cracking. These effects are most pronounced if the package has greater than 0.23% absorbed moisture before solder reflow.[13] Figure 8-13 shows a typical example of a package

crack. The mismatch in thermal expansion coefficients of the package's components also induces stresses. If these combined stresses are greater than the fracture strength of the plastic, cracks will develop. The cracks can provide a path for ionic contaminants to reach the die surface, and/or die delamination can cause wire-bond failure. Hence, these are reliability concerns.

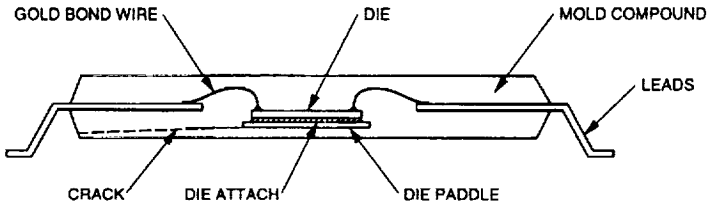

Figure 8-13: Typical plastic package showing the onset of a crack.

JEDEC defines five classes for moisture resistance of plastic packages and sensitivity to 'popcorning'. Class 1 is defined as unlimited exposure to moisture and the package will still not exhibit delamination during the surface mount operation. Class 5 can tolerate minimal exposure to moisture before it needs to be dried (by baking in an oven set at ~125°C for a duration of 8 to 24 hours depending on the package). Classes 2 through 4 are defined as somewhere in between the extremes. Most commercial packages are classified as class 3 moisture resistant.

To overcome the delamination problem, results derived from numerical simulation and experimental data can serve as a guide in the selection of suitable molding compound properties.[14] The properties considered are the adhesion strength, S, and the coefficient of thermal expansion, α. These results are summarized in Figure 8-14.

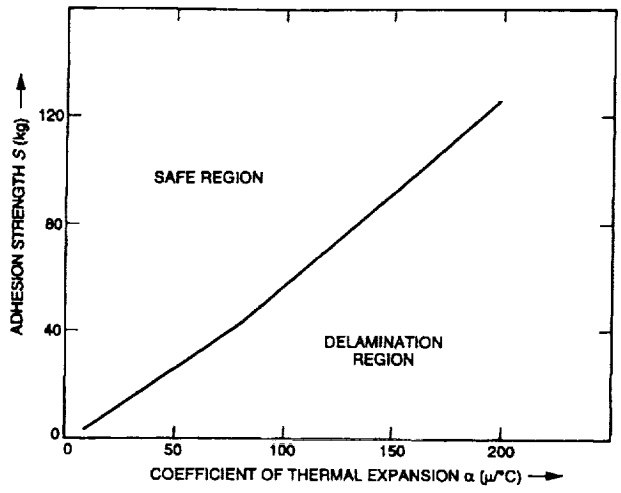

Figure 8-14: Mold compound properties.

The amount of moisture a particular package design can take up prior to delamination and catastrophic popcorning can be empirically determined as shown in Figure 8-15. As can be seen, a high moisture environment (as well as high temperature) greatly reduces the amount of time on a production floor prior to the surface mount operation.

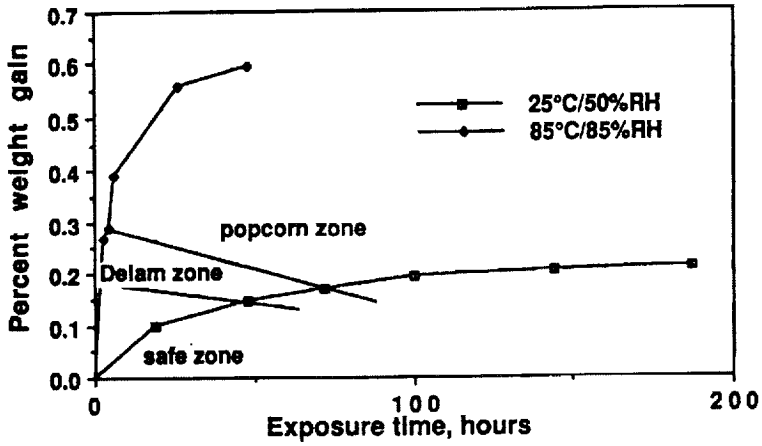

Figure 8-15: Moisture weight gain of a plastic package exposed to two different moisture conditions.

Also, it has been shown that polyimide die overcoat, or PIX, can reduce the percent of die or pad delamination by up to 30% on parts subjected to temperature cycling.[13,15] This PIX coating can mechanically support air bridges during plastic encapsulation, provide a more uniform electrical environment for the die, and provide protection to the surface of the die. Figure 8-16 shows cross sections of three PIX-treated dies. It has been reported that the PIX shown in Figure 8-16(a) yields the best improvement in reliability.[13] The PIXs shown in 8-16(b) and (c) are not as desirable, because, respectively, they cause wirebond stress and do not protect the die surface.

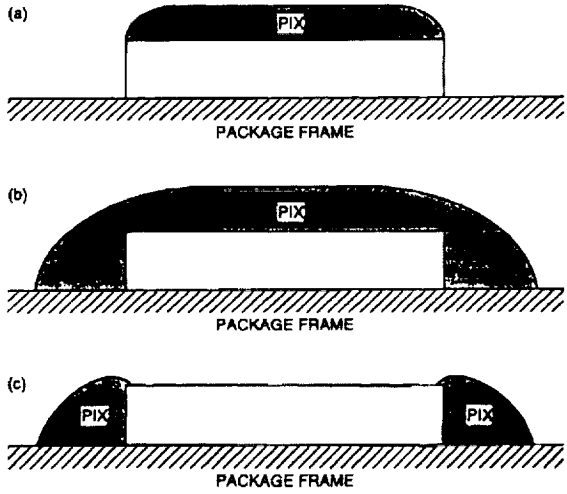

Figure 8-16: Polyimide die overcoat (PIX) on MEMS die: (a) PIX on MEMS top surface only, (b) PIX on MEMS and package frame, and (c) PIX on package frame and sides of MEMS only.

The last mechanisms by which a chip can fail in a plastic package are caused by bond-wire sweep and lift-off, which in turn are caused by the viscous flow of the molten plastic mold compound. The viscosity of the molten plastic is a function of the filler particle size and concentration. Figure 8-17 shows the typical geometries of wire bonds with different die settings. Studies[16] show that of the three wire bonds, the one with the raised die experiences the largest maximum displacement. Further, the raised die and the downset die experience maximum stress at the ball bonds. In these cases, plastic deformation of the ball bonds is a major cause of failure. In contrast, the wire bond for the double-downset die suffers only elastic deformation. Thus, the double downset is the recommended device layout to minimize bond wire sweep.

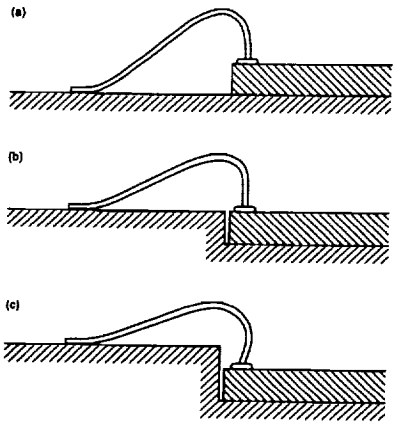

Figure 8-17: Typical geometry of wire bond with different die settings: (a) raised, (b) downset, (c) double downset.

VIII. Additional Reading

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Chapter 9: Test Structures

B. Stark

As previously mentioned, there is a serious debate within the MEMS community about the materials properties of thin films. Accurate knowledge of these properties is critical for assessing the long-term reliability of MEMS devices. In order to measure thin film properties and make these basic assessments, test structures are needed. Test structures are, in their simplest sense, sensors. Instead of sensing external forces they sense the environment they are exposed to. Most fabrication facilities utilize test structures on their production line to assess the quality of their process.

In order to ensure reliable operation, test structures that characterize both the process and materials used to manufacture devices must be made concurrently. It is the analysis of these test structures that will enable systems engineers to incorporate MEMS into their designs with a high degree of confidence in their reliability. This chapter describes some of the basic test structures used and their implications.

I. Technology Characterization Vehicle

A technology characterization vehicle, or TCV, is a structure that is used to evaluate the effects of specific failure mechanisms on a technology. Typically the devices used in TCVs will be derived from a standard library of device elements. This library might include cantilever beams, membranes, and other structures that are used commonly in MEMS technology.

Technology characterization vehicles will be subjected to a given test in order to predict failure from particular failure mechanisms. These structures should be used to determine an estimate of the mean-time-to-failure and failure probability models. The use of these devices is a critical part of the qualification process, as they provide a wealth of knowledge about the reliability of structures. TCVs should be packaged and handled exactly the same as other MEMS so that the information that they provide is as accurate as possible.

II. Standard Evaluation Devices

A standard evaluation device, or SED, is similar to a TCV except that an SED is not constructed out of typical design elements, but is instead constructed out of actual sensor and actuator structures. Usually the SED is a less complicated version of a completed device and provides reliability information about the performance of devices instead of structures. In a good quality control process, the parameters measured in different SEDs will be compared across wafers and lots to determine reliability

characteristics of production runs. As in TCVs, SEDs should be treated in the same fashion as a fully functional device.

III. Parametric Monitors

Parametric Monitors, or PMs, are used as a method to measure the properties of the materials used in MEMS devices. Unlike TCVs and SEDs, a PM is designed solely as a test structure and is not just a part of a pre-existing design. While PMs have long been used in the electronics industry, their use for the measurement of the mechanical properties of materials is relatively new. For this reason, several basic structures will be described in the following section to illustrate the recent developments in this field.

As with other test structures, the data collected from PMs will be compared across production runs to examine the effects of processing conditions on material properties.

A. Beam Stubs

Many processes include the dimensions of thin film layers in their design specifications. A typical surface micromachining process might state that the poly 2 layer is 3 microns thick and that the oxide layers are all 2 microns thick. In order to verify the actual dimensions of the process run, beam stubs are employed. Beam stubs are simply short cantilever beams with open cross sections. Usually an engineer will examine these beams to guarantee that the internal composition of each process is what it was supposed to be. This is a simple procedure performed with a scanning electron microscope. Measuring the internal composition of beams stubs allows the determination of the moment of inertia and mass of structural beams.

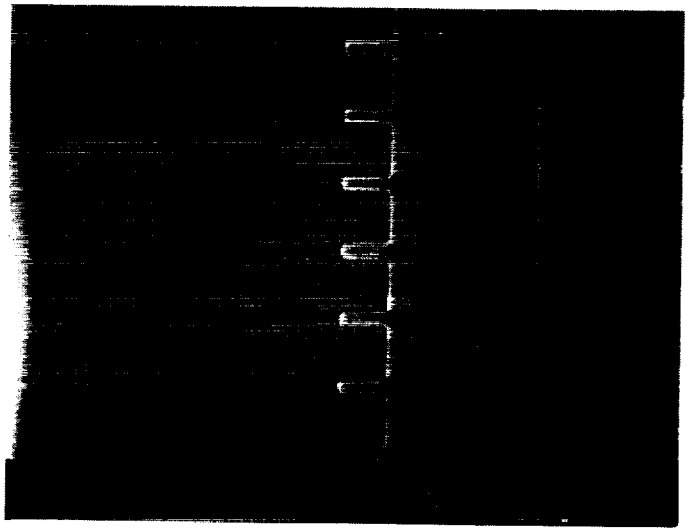

Figure 9-1: A row of beam stubs. (from JPL)

B. Elastic Measurements

In order to optimize MEMS designs, the elastic properties of materials must be known. To make these measurements, several established techniques are used.

i) Bending Beam Method

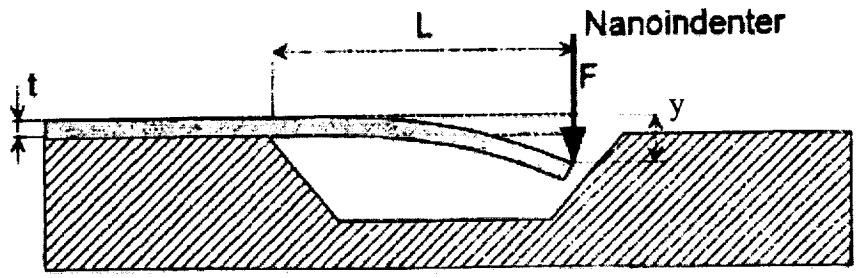

Figure 9-2: Bending beam method. (from [126])

One method of measuring Young's modulus employs static loading of a cantilever beam. A nanoindenter is applied to one end of a beam and the force-displacement curve is measured. For a small deflection, Young's modulus can be obtained as[1]:

$$E = \frac{FL^3}{3yI} \tag{9-1}$$

where the dimensions are labeled in Figure 9-2. This method can also be used to measure the modulus of thin films on multilayered beams that have residual stress. The modulus of a thin film, E_f, can be related to the modulus of a structural material, E_s, for $t_f << t_s$:

$$E_f = \frac{1}{3}\left(\frac{t_s}{t_f}\right)\left(\frac{\Delta F}{F_0}\right)E_s \tag{9-2}$$

where:

F_0 = the force required to displace an uncoated beam d_0

ΔF = (the force required to displace a coated beam d_0) – F_0

[1] A common alternative to this equation attempts to linearize the nonlinear factors in Equations (9-1) and (9-2). This method defines $E'=E/1-\nu^2$.[40]

This method is only effective for films with little to no residual stress. Furthermore, this technique, due to the cubic powers in Equation 9-1, is critically limited by the ability to accurately measure the dimensions of the beam.[126]

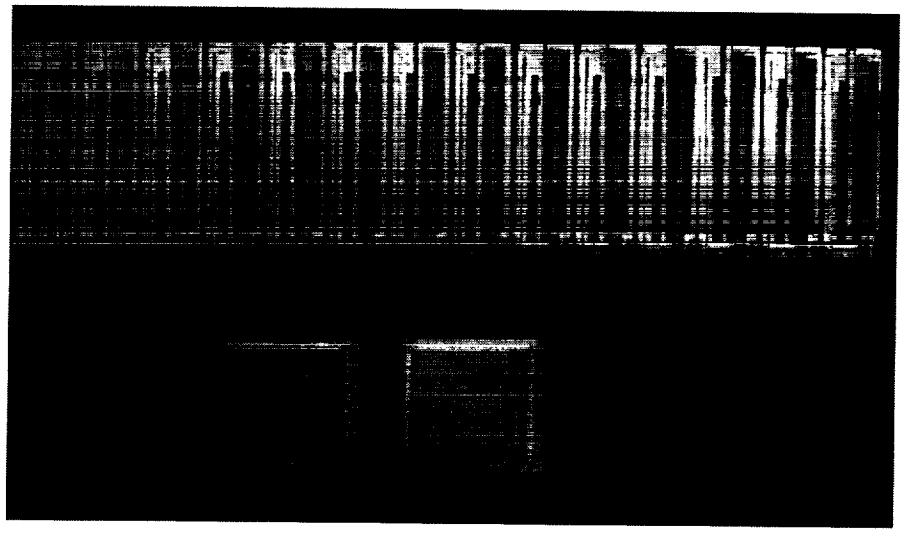

Figure 9-3: Resonant beam array.

ii) Resonant Beam Structures

Resonant beams are structures designed to measure the stiffness of beams. Equation 6-8 described the resonant frequency of beams as:

$$\omega_0 = \sqrt{\frac{k}{m_{eff}}} \tag{6-8}$$

This equation shows that measuring ω_o and m_{eff} will give k. The dimensions of a beam can be measured using beam stubs. Multiplying these dimensions by published densities will determine the mass of these beams. The resonant frequency is usually measured either internally through parallel plate capacitors or externally by a laser vibrometer. Once these values have been measured, it is fairly simple to extract Young's modulus from the equations in Section 6-I. For a cantilever beam, Young's modulus is:

$$E = \frac{.92\omega_o^2 ml^3}{a^3 b} \tag{9-3}$$

Another structure used to measure Young's modulus is a lateral comb drive resonator. This structure is useful for measuring the properties of LPCVD deposited polysilicon and has the desirable property that dampening at atmospheric pressure is extremely low.

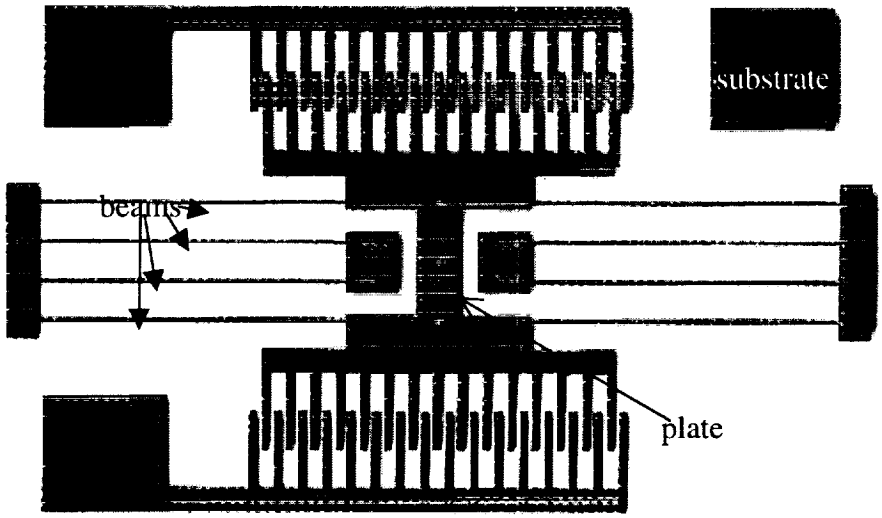

Figure 9-4: Layout of comb-drive resonator.

For these structures, the resonant frequency is related to Young's modulus by: [24]

$$\omega_0 = \sqrt{\frac{2Eba^3}{L^3\left(M_p + .03714M\right)}} \tag{9-4}$$

where Mp and M are the respective masses of the plate and the beams.

Typically resonant beams are used to measure Young's modulus and to compare it against published values. Since the values of Young's modulus differ across process lines, it is useful to have made measurements on the same wafer as actual devices. One drawback of this device is that plate mass is difficult to measure accurately.

C. Stress/Strain Gauges

With residual stress having been established as a serious reliability concern, there has been a serious push for devices capable of measuring residual stress in MEMS. There are a number of methods to measure internal stress, all of which have varying degrees of usefulness and precision. This section will examine some of the more common methods for measuring stress.

i) Bent Beam Strain Sensors

Bent beam strain sensors are common devices used in measuring internal strain in a device. Initially described by Gianchandani and Najafi in 1996, these devices are popular strain gages due to the fact that they can measure both compressive and tensile

stresses. Shown in Figure 9-5, these structures are constructed of two built-in beams connected to cantilever beams.

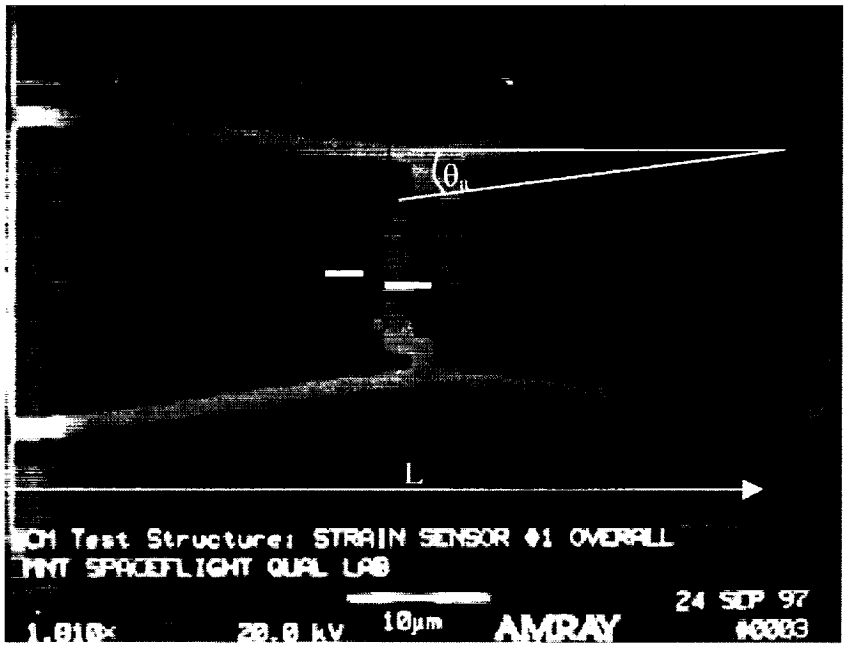

Figure 9-5: Stress/strain gauge. The two marked stubs were aligned prior to release.

The cantilevers are covered with a vernier scale. Upon release from the substrate, these structures will shift position due to internal stresses. By measuring the deflection of the teeth of the vernier, it is possible to extract stress measurements. This can be done with a computer through finite element analysis, but an excellent analytical approximation of this model is given by:[30]

$$\sigma_{int} = \frac{E}{L}\left(\Delta L' + \frac{FL}{Eab}\right) \tag{9-5}$$

where

F = load applied to beam by internal stress

L = distance indicated in Figure 9-5

L' = the difference between the actual length of the beam and L, which is equal to

$$\frac{L'}{2} = -\frac{1}{2}\int_0^{L/2}\left(\frac{\partial y}{\partial x}\right)^2 dx \tag{9-6a}$$

When solved, L' becomes:

$$L' = \frac{(\tan(\theta_a))^2}{4k}\left[2H + kL - kLH^2 + \sinh(kL) - 2H\cosh(kL) + H^2\cosh(kL)\right] \text{in} \qquad (9\text{-}6b)$$

tension and

$$L' = \frac{(\tan(\theta_a))^2}{4k}\left[2G + kL + kLG^2 + \sin(kL) - 2G\cos(kL) - G^2\sin(kL)\right] \qquad (9\text{-}6c)$$

in compression

where

G = tan(kL/4)

H = tanh(kL/4)

$$k = \sqrt{\frac{F}{EI}}$$

The displacement y is related to k, and thus L' by the relationship

$$y_{Tension} = 2\frac{\tan(\theta_a)}{k}\tanh\left(\frac{kL}{4}\right) \qquad (9\text{-}7)$$

$$y_{Compression} = 2\frac{\tan(\theta_a)}{k}\tan\left(\frac{kL}{4}\right) \qquad (9\text{-}8)$$

These structures are limited in resolution by the minimum feature size of a technology. While these limitations are usually small, they could be a serious problem on some larger technologies, such as LIGA. Out-of-plane displacements caused by stress gradients and non-uniform beam thickness can inhibit device sensitivity. Ultimately these devices will have difficulty being accurate below 10 MPa.[30]

ii) Cantilever Beams

Cantilever beams are commonly used as a simple way to measure internal stress. Since most technologies utilize cantilever beams, it is a relatively simple step to place extra cantilever beams onto a device for stress measurement. One method uses cantilever beam deflection to measure stress. Since most stresses on these devices causes non-planar displacement, a system that can measure z-axis deflection can measure stress. With a multitude of laser interferometery systems now available to measure surface topology, these measurements are easy to make both quickly and accurately.

Since internal stress is rarely uniform, but is instead a function of material thickness, many researchers are interested in the stress gradient within a material. The stress gradient is calculated by looking at the change in stress over the change over film thickness. For a cantilever beam, the stress gradient can be analytically approximated by:

$$\frac{d\sigma}{dt} = \frac{2yE}{(1-\nu)l^2} \tag{9-9}$$

where

y = non-planar deflection of the cantilever tip

t = thickness of the film

l = length of the cantilever

While this equation assumes a linearly varying stress field, this is not an unrealistic assumption. Although this equation does not take into account many of the irregularities considered in a finite element analysis, it does offer a good order of magnitude calculation for the stress field within thin films.

iii) Buckling Beam Structures

Many test structures take advantage of buckling behavior in beams to measure stresses. The stress needed to buckle a doubly clamped beam is defined as:

$$\sigma_b = -\frac{\pi^2 h^2 E}{3L^2} \tag{9-10}$$

where

h = beam thickness

L = beam length

As such, for structural beams, buckling is a function of stress levels. Designers have used this fact in creating arrays of these beams. Each beam in the array has different dimensions, with a corresponding buckling stress. By examining the beams after release it is possible to measure stress by observing the beam with the largest σ_b that buckled. This technique is a very accurate way of measuring compressive stresses in beams. With longer beams having a σ_b<1 MPa, these arrays can be quite sensitive.

For tensile stresses, another set of test structures called Guckel Rings, has been developed to utilize buckling in measuring stresses. Guckel Rings are also used in arrays and the critical buckling load is defined by:[130,138]

$$\sigma_b = \frac{\pi^2 h^2 E}{12 g(R) R^2} \tag{9-11}$$

where

R = ring radius

g(R) = a function of inner and outer ring radius ≤ 0.918

iv) Substrate Analysis

One method to measure stress in thin films does not use actual test structures as they are commonly known. Instead this technique uses substrate deformation to measure stress. This is done by measuring the radius of curvature of the substrate before and after deposition of a thin film. Then the Stoney equation can relate these measurements to the residual stress:[139, 140]

$$\sigma_r = \frac{E t_s^2}{6(1-\nu)t}\left(\frac{1}{R_o} - \frac{1}{R_f}\right) \tag{9-12}$$

where

R_o, R_f = initial and final radii

t = thin film thickness

t_s = wafer thickness

This method provides good residual stress measurements down to about 10 MPa. Below this level, boundary conditions and gravity affect measurement accuracy. The major limitation of this method is that it does not provide direct measurement of stresses in finished devices.

D. Undercut Squares

Another area of concern in MEMS is the width of an isotropic undercut etch. These etches are critical to releasing structures, and many researchers are interested in determining how thick of a structure can be undercut. The simplest way to make a test structure to measure this is to create an array of squares. The squares vary in size from a dimension that clearly can be undercut to a dimension that clearly cannot be undercut. After release, the structures that have been fully undercut will be separated from the substrate, while the structures that have not will still be intact.

IV. Fracture Specimens

The most common method used to measure fracture strength is to place a static load on a cantilever beam. This technique is similar to static elastic property measurements, with larger loads and deflections.

Another method reported by Tsuchiya et al.[127] involves a tensile tester for thin films that holds samples electrostatically. This method requires that the tester is placed into a SEM to measure displacement, as shown in Figure 9-6.

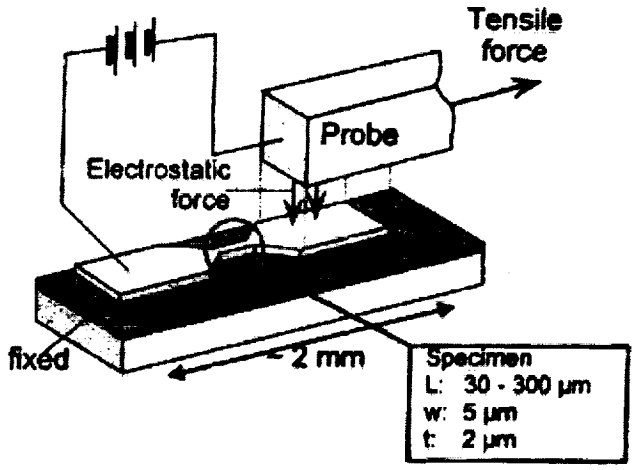

Figure 9-6: Tensile tester reported by Tsuchiya et al. (from [127])

A less complicated method described by Greek et al. is to use a probe tip connected to a thin beam. By applying a force to the probe, it is possible to measure fracture stress.[128,129]

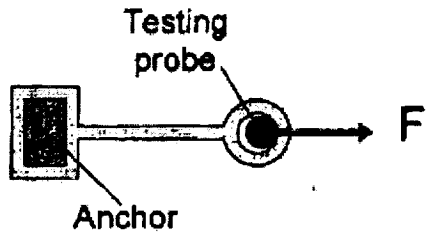

Figure 9-7: Tensile tester reported by Greek et al. (from [128])

A. Thermal Properties Measurements

The thermal properties of MEMS are important for a number of applications. It is important to accurately know the linear expansion coefficient and the thermal conductivity for certain devices. There are several methods to do this.

i) Cantilever Beam Method

A cantilever beam can be used to measure the linear coefficient of expansion. By measuring the change in curvature, $\Delta(dy/dx)$, for a given change in temperature, it is possible to determine the linear coefficient of expansion of a thin film material, α_f:[131]

$$\Delta\frac{dy}{dx}(\Delta T)=\frac{(\alpha_f-\alpha_s)}{C}\Delta T \tag{9-13}$$

where

α_s = the coefficient of expansion of the substrate (a well-known value)

$$C=\frac{E_s t_s^2}{6E_f t_f}\left(1+\frac{t_f}{t_s}+4\frac{E_f t_f}{E_s t_s}\right)$$

ii) Thin Film Heater

One popular method for measuring the thermal conductivity of a film employs a thin film heater attached to the free end of a cantilever beam. The temperature gradient between the heater and the fixed end of the cantilever can be determined via a row of thermocouples, as shown in Figure 9-8.[129,132,133]

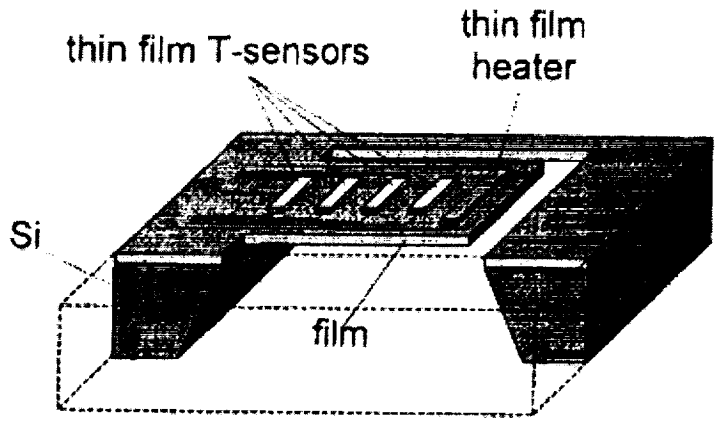

Figure 9-8: Layout of thin film heater with thermocouples. (from [129])

The thermal conductivity for one of these devices is calculated as:

$$k = \frac{P}{A\left(\frac{dT}{dx}\right)} \tag{9-14}$$

where

P = applied thermal power

A = the area normal to the heat flow

iii) Microbridge

Another method to measure thermal conductivity involves a microbridge. The bridge is doped less in the center so that it has a greater resistance. Then a current heats up the bridge and the I-V curve is measured to determine the thermal conductivity:[129, 134]

$$k(T_c) = \frac{I}{wt}\frac{dP}{dT_c} \tag{9-15}$$

where w, t, and T_c are defined in Figure 9-9.

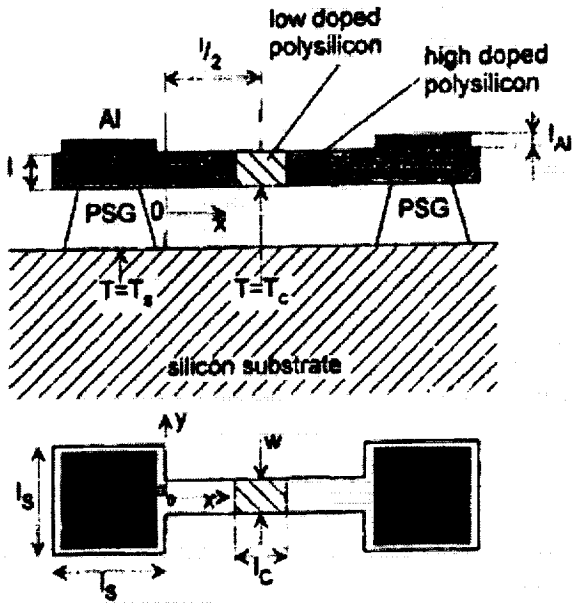

Figure 9-9: Layout of a microbridge. (from [129])

V. Additional Reading

E. Obermeier, "Mechanical and Thermophysical Properties of Thin Film Materials for MEMS: Techniques and Devices" *Materials Research Society Symposium Proceedings*, Vol. 444.

Chapter 10: Qualification Testing Protocols for MEMS

B. Stark and S. Kayali

This guideline has offered detailed physical analysis of the distinct parts and materials used to manufacture a MEMS device. In this chapter, all the information presented will be tied together through the common thread of space qualification. It must be primarily understood that this guideline is not, and was never intended to be, a rigid set of specifications. It is instead a recommendation of qualification methods. Clearly with the vast array of devices used in the industry, it would be difficult to qualify the individual tests needed on a given device.

The proper use of this guide requires referencing to all the chapters. The specifics of qualifying a device depend upon the specifics of the process, materials, and structures in a device. The reason that specific standards were not set for MEMS in space is that many people within the electronics community have complained that these standards limit their device development and do not recognize that some tests on some devices are unnecessary. A further problem with standards is that they often do not take into account mission requirements. It is the ultimate job of the mission designers to determine the thermal ranges and radiation levels expected during the mission. To set these ahead of time, without this foreknowledge, can require expensive overdesigning of parts on short term missions and be too lenient on parts used on longer missions.

In order to improve reliability, qualification should begin as early as possible. History has shown that the reliability of a device will fluctuate over its development cycle as shown in Figure 10-1.

The initial low reliability of prototypes can be attributed to a myriad of causes from design flaws to manufacturing process problems, with a number of other environmental and handling issues having an impact. After this initial period, reliability improves from refinements in device manufacture and from the identification and eradication of predominant failure modes. Once a device is placed into production, there is a regression of reliability stemming from the compromises made to transfer a device from research production to a full scale manufacturing line. With eventual improvements in production processing, reliability should approach the potential device reliability.

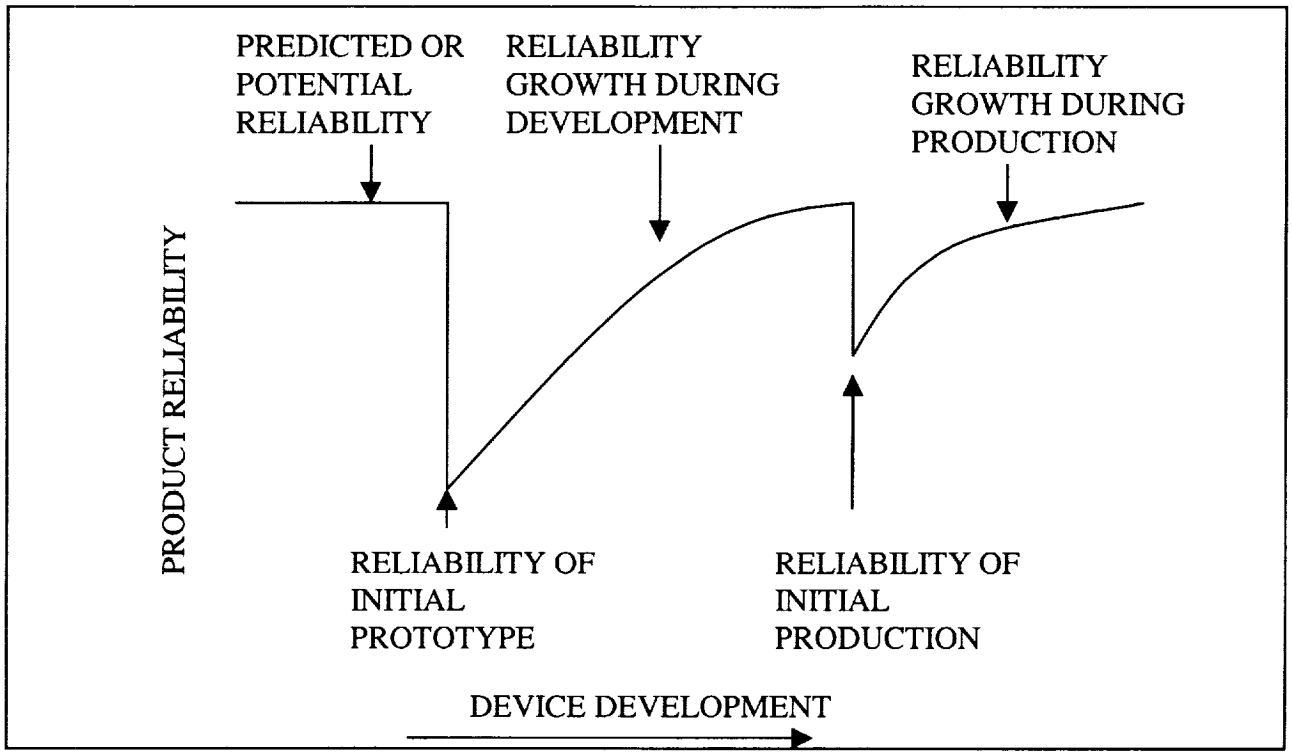

Figure 10-1: Reliability over the development cycle.

These reliability fluctuations from design to production can be minimized by incorporating statistical process control methodologies into device fabrication and by performing life-testing. This step will force reliability improvements to coincide with device production and will ultimately lead to a more reliable device that can be brought to market much quicker than would be otherwise expected. As such, this chapter provides the methods necessary to both limit this reliability swing during device development and to improve long term device reliability.

There is a four-step procedure followed by most satellite manufacturers which includes some practices recommended by Qualified Manufacturers Listing, or QML, programs. These steps of Process Qualification, Product Qualification, Product

Acceptance, and Company Certification, are summarized in Figure 10-2. Process Qualification concerns a procedure the manufacturers should follow to assure the quality, uniformity, and reproducibility of MEMS from a specific fabrication process. Product Qualification encompasses a set of simulations and measurements to establish the mechanical, electrical, thermal, and reliability characteristics of a particular device. Product Acceptance is a series of tests performed on the deliverable device that are designed to ensure that a part meets the program requirements and to provide specific reliability information pertinent to that product. Company Certification focuses on the procedures and management controls that a manufacturer should have in place to assure the quality of their MEMS devices.

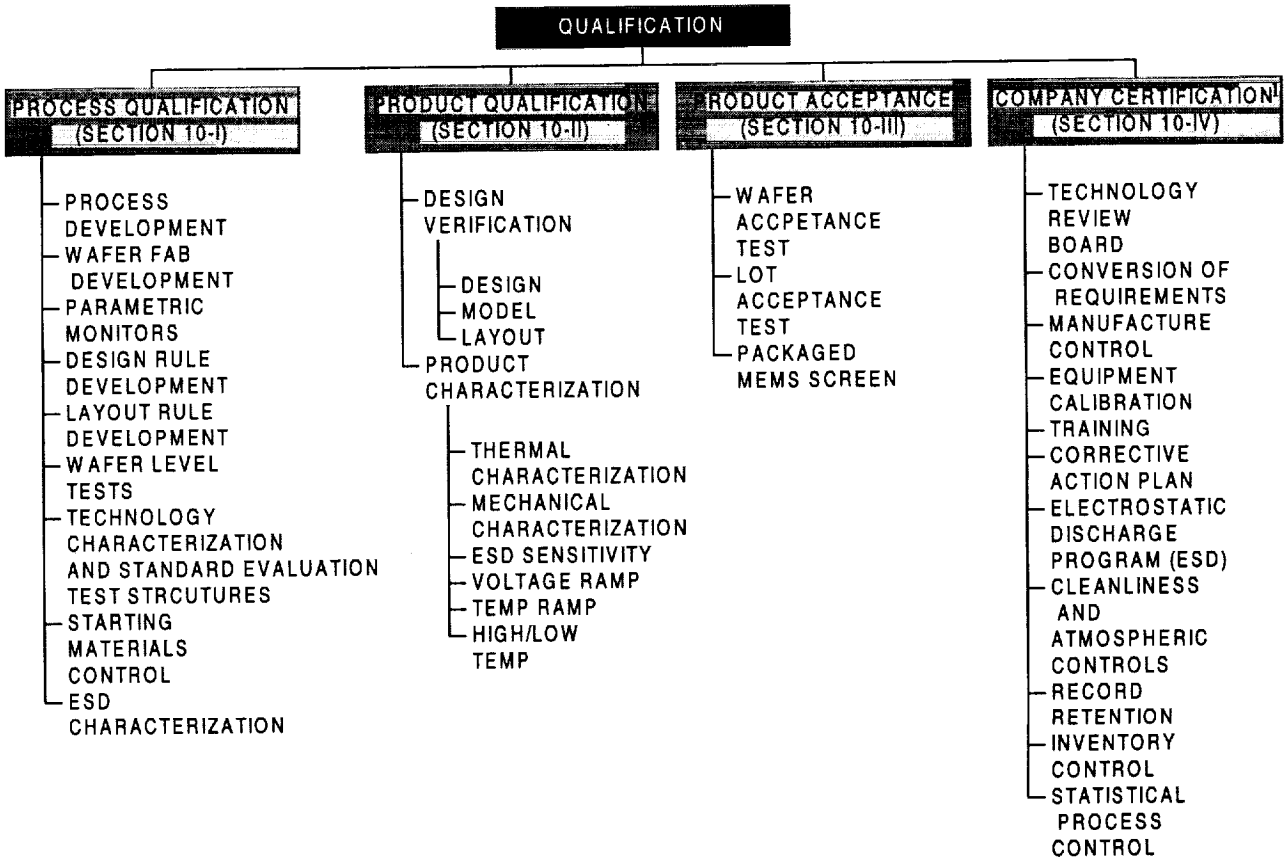

Figure 10-2: Recommended qualification methodology.

Before these four steps are presented in any detail, one important aspect of MEMS qualification must be addressed. Although the manufacturer is ultimately responsible for delivering a reliable MEMS, the overall system reliability is the domain of the MEMS

[1] Company Certification is a process that may only be possible in mature industries. Given the paucity of MEMS foundries, it is uncertain if Company Certification is realizable. For this reason it is suggested, but certainly not required that Company Certification be performed.

user. For this reason, it is in the interest of both parties to understand the expected performance requirements of both the MEMS and the system into which it will be inserted.

I. Process Qualification

Manufacturers who have standardized their production to a single technology will often try to qualify their entire production line. Through this process, the manufacturer attempts to show that its entire production line is under control and operating efficiently. Furthermore, this process enables the manufacturer to establish an electromechanical baseline to use in measuring performance and reliability for all products coming off the line. The benefits of this process are twofold. The manufacturer saves costs and time in the development of future devices, since the reliability and performance characteristics of the constituent parts of a device will have already been established. The user gains both the comfort of procuring parts from an established line with a history of producing qualified parts and the cost savings inherent to a reduced qualification time.

The procedure of qualifying a production line is called process qualification. This is generally defined as the set of procedures that a manufacturer follows to demonstrate that they have control of the entire process of designing and fabricating a MEMS device using a specific process, which will usually be one of the processes listed in Chapter 5. This act addresses all aspects of production, including the acceptance of starting materials, documentation of procedures, implementation of handling procedures, and the establishment of lifetime and failure data for devices fabricated with the process. Since the goal of process qualification is to provide assurance that a particular process is under control and known to produce reliable parts, it needs to be performed only once, although a routine monitoring of the production line is standard. It is important to understand that only the process and basic structures are being qualified and that no reliability information is obtained for a particular MEMS design.

Although process qualification is intended to qualify a defined fabrication procedure and device family, it must be recognized that MEMS technology is evolving at an astounding rate, which requires the continual updating of fabrication procedures. Furthermore, minor changes in the fabrication process to account for environmental variations, incoming material variations, continuous process improvement, or minor design modifications may be required. All of these changes are permitted and frequently occur under the direction of the TRB. Thus, maintaining the status quo does not guarantee maintaining qualification.

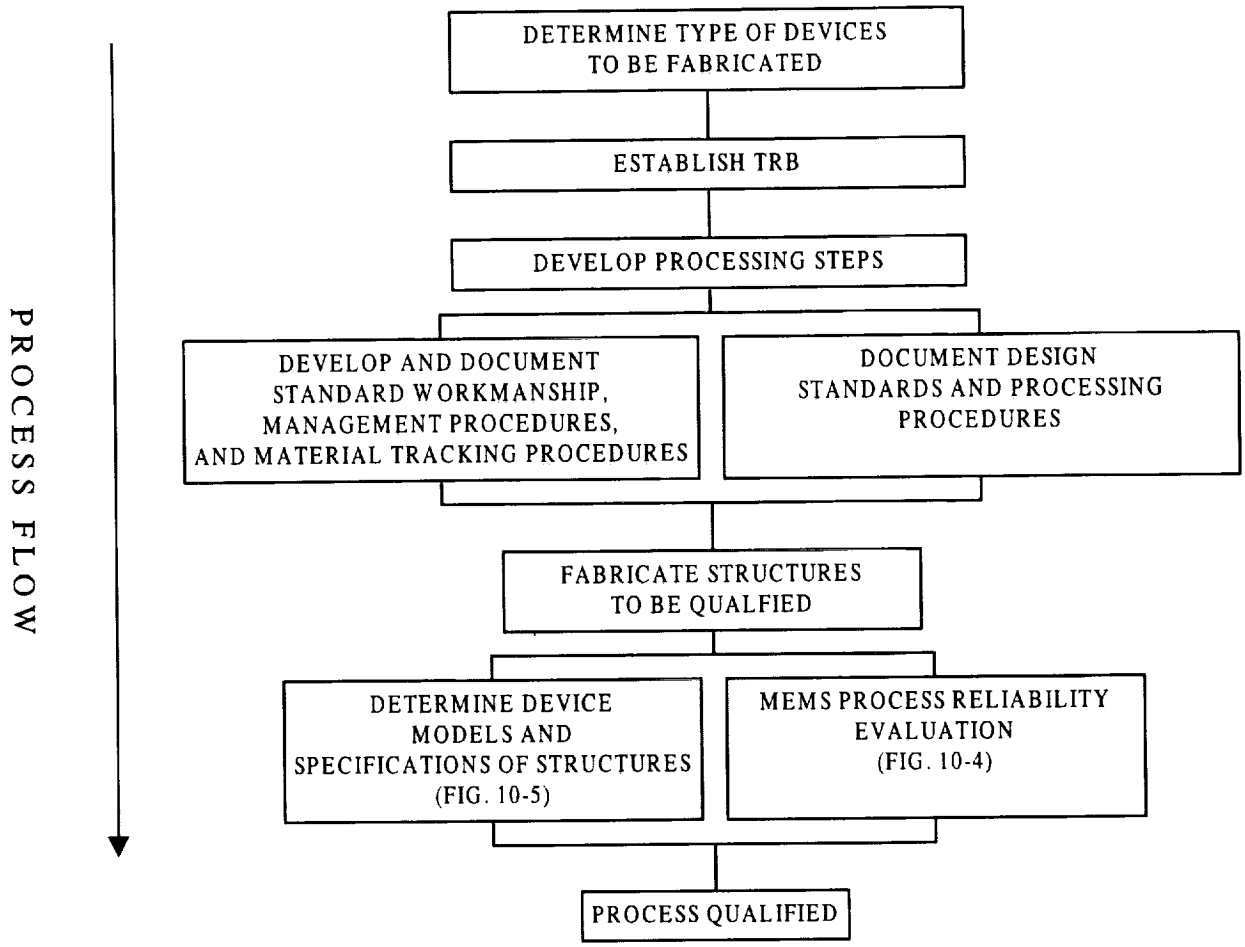

Figure 10-3: MEMS process qualification steps.

The internal documents and procedures used by most manufacturers are summarized in Figure 10-3. In addition to this, the QML program provides guidelines for process qualification. The first step in this procedure is to determine the family of devices to be fabricated and the technology that will be used in the fabrication. After this, the manufacturer will establish a TRB to control the process qualification procedure. After the processing steps have been defined and documented, the workmanship, management procedures, material tracking procedures, and design procedures should be documented. The information contained in the documentation described the process domain that is being qualified.

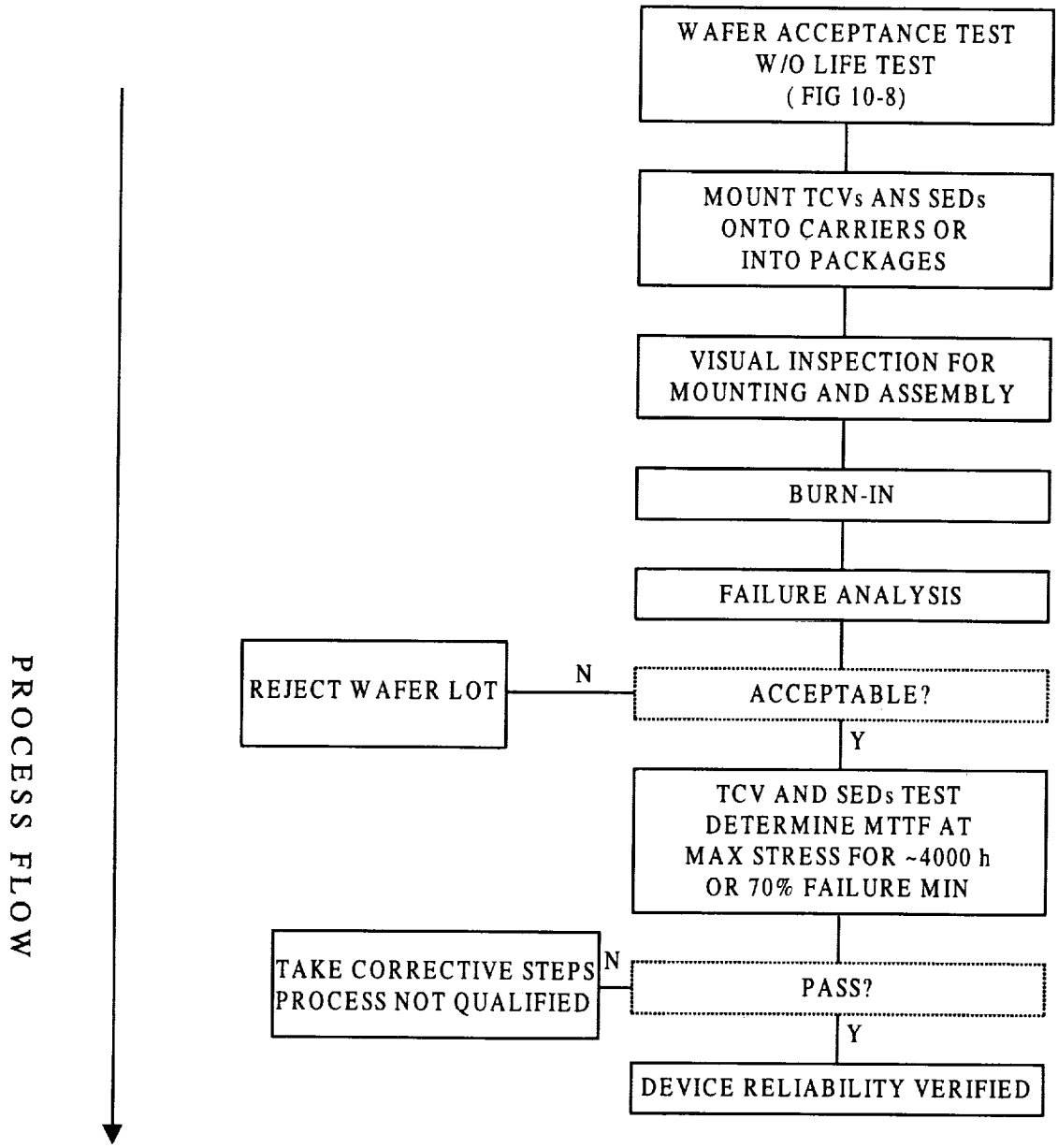

Figure 10-4: MEMS process reliability evaluation.

The qualification process also involves a series of tests designed to characterize the technology being qualified. This includes the properties and the reliability characteristics of components being fabricated on the line. Some of these tests are performed at wafer level, while other tests require the mounting of structures onto carriers. All of these tests and the applicable procedures are an integral part of the qualification program and provide valuable reliability and performance data at various stages of the manufacturing process. Figure 10-4 outlines a recommended series of tests for MEMS process reliability evaluation. The number of devices subjected to each test will normally be determined by the TRB and the rationale for their decision will become

part of the process qualification documentation. Clearly a higher level of confidence exists if more structures are tested, but this must be balanced by the understanding that, after a certain point, the incremental gain in confidence is more than offset by the increase in cost related to the testing. Since the stability of the process is being determined as part of the process qualification, the manufacturer will typically fabricate and test components from several wafer lots. Figure 10-5 provides a series of tests that are recommended to characterize the electromechanical limitations of devices. The performance limitations obtained from these tests often become the basis for limits incorporated into the design and layout rules.

One of the aspects of the processes qualification procedure to note is that the procedure is QML-like and therefore addresses topics similar to those of company certification. The major difference between the two is that company certification is performed by the customer, whereas process qualification is self-imposed by the manufacturer, often before customers are identified. Items particular to process qualifications are described below.

A. Process Step Development

Although the Company Certification process is also fundamental to the process qualification procedure, the actual task of turning a bare wafer into a processed device is often the only task associated with process qualification. While process qualification is actually more involved, processing is the most critical step in process qualification and requires the most time and resources to develop, In addition to this, it is important to recognize that the fabrication procedures and devices processed on the line are the factors that separate one process from another. The first step towards process qualification is the documentation of all the steps necessary to produce a MEMS device. Although all of the steps in the fabrication process should be documented, the details are typically considered proprietary by the manufacturer. Therefore the MEMS customer can expect to see a generalized process flow, but not a detailed account of each step necessary to reproduce a given product on another line.

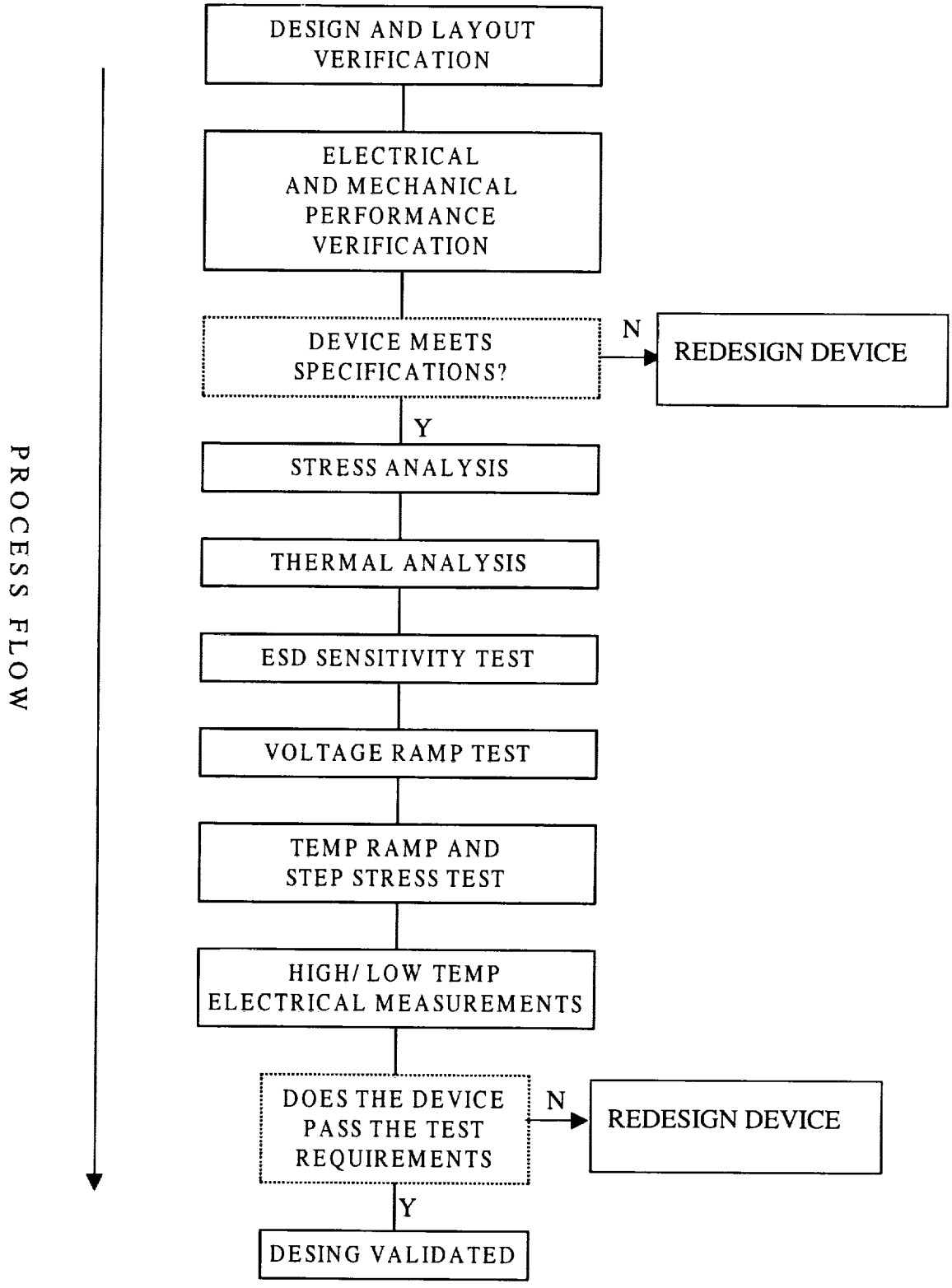

Figure 10-5: Device design validation.

B. Wafer Fabrication Documentation

Once a process is qualified, reliability concerns may still arise from minor variations in the process flow, environment, or starting materials. For this reason, all wafer fabrication steps and conditions should be recorded by the manufacturer to maintain the repeatability of the product. Documentation of these steps and fabrication conditions should be maintained to trace any future quality or reliability concerns to a specific step. Although process travelers can be used to document the fabrication and manufacturing steps, they usually lack the detail necessary to trace quality or reliability problems to specific fabrication steps. The wafer fabrication steps themselves and the documentation describing them are usually considered proprietary by the manufacturer.

C. Parametric Monitors

Parametric monitors are essential for monitoring a production line's quality or continuous improvement. PMs were fully described in Chapter 8; they are mentioned here only to emphasize the fact that the choice of the test structures is dependent on the process and technology being monitored. Therefore, this choice is a critical element in the process qualification procedure. The complete list of parametric monitors is usually combined into a single list that is included on all wafers. The data obtained from the test structures will be normally stored in a database that permits the quick comparison of each wafer fabricated on the line to all of the other wafers. This permits determination of the process stability.

D. Design-Rule and Model Development

The reliability of MEMS fabricated on a qualified process will greatly depend on whether or not they are fabricated from qualified structures according to prescribed rules. In addition to this, the standardization of the structures brings a certain degree of cost reduction. For this reason, part of the process qualification procedure is to determine and document design rules that are specific to the process. Typical information included will be the minimum feature size, maximum etch hole separation, thickness of thin film materials, required overlap in layers, depth of dry etching. While individual processes will compile their own design rules, the list must contain all information necessary to produce a working device. In addition to this information, manufacturers should compile information on the properties of all the materials in the process. Information such as Young's modulus, fracture strength, intrinsic resistivity, stray stress, and thermal characteristics, should be maintained by the manufacturer.

To use standard components in MEMS designs, models must be developed. Although some commercial packages may include models, they need to be altered to fit measured characteristics. Once standardized models are constructed, the chances of design success are greatly increased.

E. Wafer Level Tests

The semiconductor industry strives to reduce production costs by shifting as much testing as possible to the earliest possible point in the production cycle in order to weed out bad wafer lots before more time, and thus money, has been spent on them. The best strategy performs wafer level tests that includes electromechanical characterization, test structure characterization, and environmental performance. Limitations may exist in the level of test detail depending upon the device design and the manufacturer's test capabilities. In general, wafer-level tests are performed, but they must be supplemented with other verifications, such as test fixture or in-package tests. Once agreement between the wafer-level and the package-level tests has been established, the manufacturer may rely on the wafer-level tests for production monitoring.

F. TCV and SED Tests

One of the most important steps in the process-qualification procedure is to determine the electromechanical, environmental, and reliability characteristics of devices fabricated within the domain of the process. This data is obtained through the characterization of TCV and SEDs, as shown in Figures 10-5 and 10-6. All data gathered from these tests should be stored by the TRB. In most cases, the success of a manufacturer in the qualifying process will depend on the data from these tests.

G. Starting Materials Control

The manufacturer should have a mechanism to assure the quality and characteristics of every starting material, from the wafers and chemicals used in the processing steps to the shipping containers used for die/wafer transportation and storage, since they all have a direct impact on the quality and reliability of the final product. Analyses of the chemicals and gases used in processing devices is normally performed by the device manufacturer or the supplier of the chemicals. Traceability and documentation of the characterization results to the individual wafer process lot is essential in resolving any process variation or concerns. The facility audit program can be the vehicle used to determine the manufacturer's level of control.

Most device manufacturers procure wafers from outside suppliers. Procurement requirements imposed by the device manufacturer identify the dislocation density, type of starting material, resistivity, crystalline orientation, and other characteristics that are important to the user. This information can help determine the suitability of the starting material to the process and the material's capabilities. The traceability and documentation of the procurement requirements and wafer characterization can be used to resolve any process variation concerns. Wafer preparation steps, such as initial surface cleaning, can also alter device characteristics and are an important aspect of process control.

Integral to the complete process flow is the mask preparation and the method of identifying changes to the mask sets. The repeatability and quality of the masks should be assessed and documented prior to initiation of the fabrication process.

H. Electrostatic Discharge Characterization and Sensitivity

If not handled properly, several elements used in MEMS can be damaged by ESD. Therefore, every process and design should be characterized to determine ESD sensitivity. Regardless of these results, all MEMS devices should be treated as sensitive to ESD damage. An ESD handling and training program is essential to maintain a low level of ESD-attributed failures.

Inspection, test, and packaging of MEMS should be carried out in a static-free environment to assure that delivered products are free of damage. Devices should be packaged in conductive carriers and delivered in static-free bags. All handling and inspection should be performed in areas meeting "Class 1" handling requirements. Both the manufacturer and the user share the responsibility of assuring that an adequate procedure is in place for protection against ESD.

In general, the following steps can help reduce or eliminate ESD problems in device manufacturing and test areas:

- Ensure that all workstations are static free.
- Handle devices only at static free workstations.
- Implement ESD training for all operators.
- Control relative humidity to within 40 to 60%.
- Transport all devices in static-free containers.
- Ground yourself before handling devices.

II. Product Qualification

Product qualification is the process by which a manufacturer proves that a given device performs its specified task as required by the consumer. To do this, a manufacturer must test a device under a wide range of conditions and collect data proving that the device performed adequately. Every MEMS device, before it is introduced into the market, needs to pass product qualification. Since the process is device specific, even products developed on qualified lines need to go through product qualification. Figure 10-6 shows a product qualification procedure that addresses issues critical to MEMS. Although the exact sequence of tests is not critical, it is recommended that the first two tests, design and performance verification, are conducted first, since unacceptable performance at this stage will require redesign. Ultimately the exact tests conducted will depend upon the device being tested, which makes it the job of the manufacturer and end-

user to determine what tests are necessary. However, the next several sections describe recommended steps that will be common to most MEMS qualification efforts.

A. MEMS Design and Layout Verification

One of the best ways to reduce MEMS engineering cost and improve reliability is to verify the design and layout of the device before fabrication. This is usually done by design reviews conducted both internally and externally by the customer. Commonly this involves structural analysis of all the mechanical subcomponents of the device. With Chapter 6 offering a solid introduction to the mechanical limits of specific structures, it should be evident that the entire device needs to be analyzed to insure that there are no parts experiencing stress over the fracture limits and that there are no unstable device configurations. This analysis should also lead to the development of a structural safety factor, f_s:

$$f_s = \frac{\text{actual stress}}{\text{maximum allowable stress}} \tag{10-1}$$

This analysis will determine a confidence level for a device based upon its design. Clearly, the higher the factor of safety, the better a part is suited for high-rel applications. However, a high factor of safety often impedes both device cost and performance. Ultimately it is up to the user to determine what safety margins are acceptable. Typically the verification process involves representatives from different departments working together to make sure that both the theoretical design and the actual on-chip implementation are sound. These reviews should be conducted after design, after layout, but before mask making, and after final MEMS characterization.

B. Electromechanical Performance Verification

After a device has been fabricated, but before any of the expensive qualification tests have been conducted, it is recommended that a basic performance evaluation is conducted. This involves taking a device and subjecting it to normal operating conditions. The output should be measured and compared with expected values. If the device cannot operate as expected, then there is no need for further evaluation of it. Upon passing these basic tests, more extensive tests can be conducted.

C. Thermal Analysis

Thermal analysis is an important part of determining the expected lifetime of any ASIC sub-components of a MEMS device. Since electronic components' expected lifetime is exponentially related to temperature, it is important to look for any hot spots on a device that could significantly impinge device lifetime. This can be done analytically through the equations of thermodynamics, but it is more often done through external examination. This test needs to be conducted over the operating range of the device. For

structural components, this test can reveal areas of high stress, as there is a mechanical dissipation of stress through heat. It is also important to perform this test in thermally activated devices.

D. ESD Sensitivity Tests

It is quite conceivable that some MEMS devices will be sensitive to ESD damage, and therefore the ESD characterization given in reference [38] should be conducted to determine the sensitivity of the design. While literature on ESD and MEMS is essentially nonexistent, certain electrostatic components of MEMS would appear to be susceptible to ESD. Until more tests are conducted on the ESD sensitivity of MEMS, these devices should be treated as "Class 1" devices.

E. Voltage Ramp

The sensitivity of a MEMS device to voltage overstress and the absolute maximum voltage ratings are determined during the voltage ramp test. Testing is normally done by ramping the power supply until a catastrophic failure occurs. Ramp rates and step duration are a function of the design limitations, but the test should allow the device to stabilize at each step. After the test, an analysis is recommended to determine the exact failure site. Failure-point definition should be in conservative agreement with the device data sheet and design limits

F. Temperature Ramp

A temperature ramp is a useful test to run on a device slated for space insertion. This involves ramping temperature up and down from ambient until failure or severe output degradation occurs. The duration of the individual steps may vary, but they should be long enough to insure that the device reaches thermal equilibrium. This will allow a determination of the allowable operating limits of the device, keeping in mind that high temperature operation can significantly weaken the lifetime of electrical subsystems and is not recommended, even if it is possible. As with voltage ramping, failure analysis is recommended after the test and failure points should be in conservative agreement with the device data sheet and design limits.

III. Product Acceptance

MEMS that are designed by qualified engineers, fabricated on process qualified lines, and verified to meet design goals may still exhibit poor reliability characteristics. This can be due to a myriad of reasons including variations in the fabrication process, undetected materials flaws, and packaging induced stress. No matter what the actual cause, these devices must be screened out before they are integrated into high-rel systems. For this reason, manufacturers of all high-rel systems require devices to pass a series of product acceptance tests, in order to increase the confidence in device reliability. It is this

step in the qualification process that is significantly different for space qualified MEMS as opposed to commercial grade devices.

The level of testing performed during product acceptance is a function of the form of the deliverable. For example, the first level of acceptance testing, called "wafer acceptance test" is performed at the wafer level to assure the uniformity and reliability of the fabrication process through a wafer to wafer comparison. The lot acceptance test for die is a second level test that provides further reliability information, but only on a sample of MEMS, due to the difficulty in performing full characterization on unpackaged devices. It is used if the MEMS user has requested the MEMS to be delivered in die form for integration into a larger module. This sample testing will provide the user with only an estimate of device reliability, with no knowledge of the impact packaging will have upon final device reliability. If packaged parts are requested instead, a full screening can be performed and the user should have the assurance that the delivered parts are reliable. The acceptance testing procedure is summarized in Figure 10-6.

The recommended product acceptance test for die deliverable is shown in Figure 10-7. Note that there are three levels of testing within the procedure and each starts with the wafer acceptance test shown in Figure 10-8. The lowest level of testing is required for MEMS that have already been product qualified and have been manufactured on a qualified process line, whereas the highest level of testing is required for a new circuit design that is processed on an unqualified line. Whichever level of testing is required, the same level of reliability assurance should be granted to the MEMS device upon completion of the lot acceptance test. The cost and time advantage of buying MEMS from manufacturers with qualified processes and validated circuit design should be both self evident and substantial.

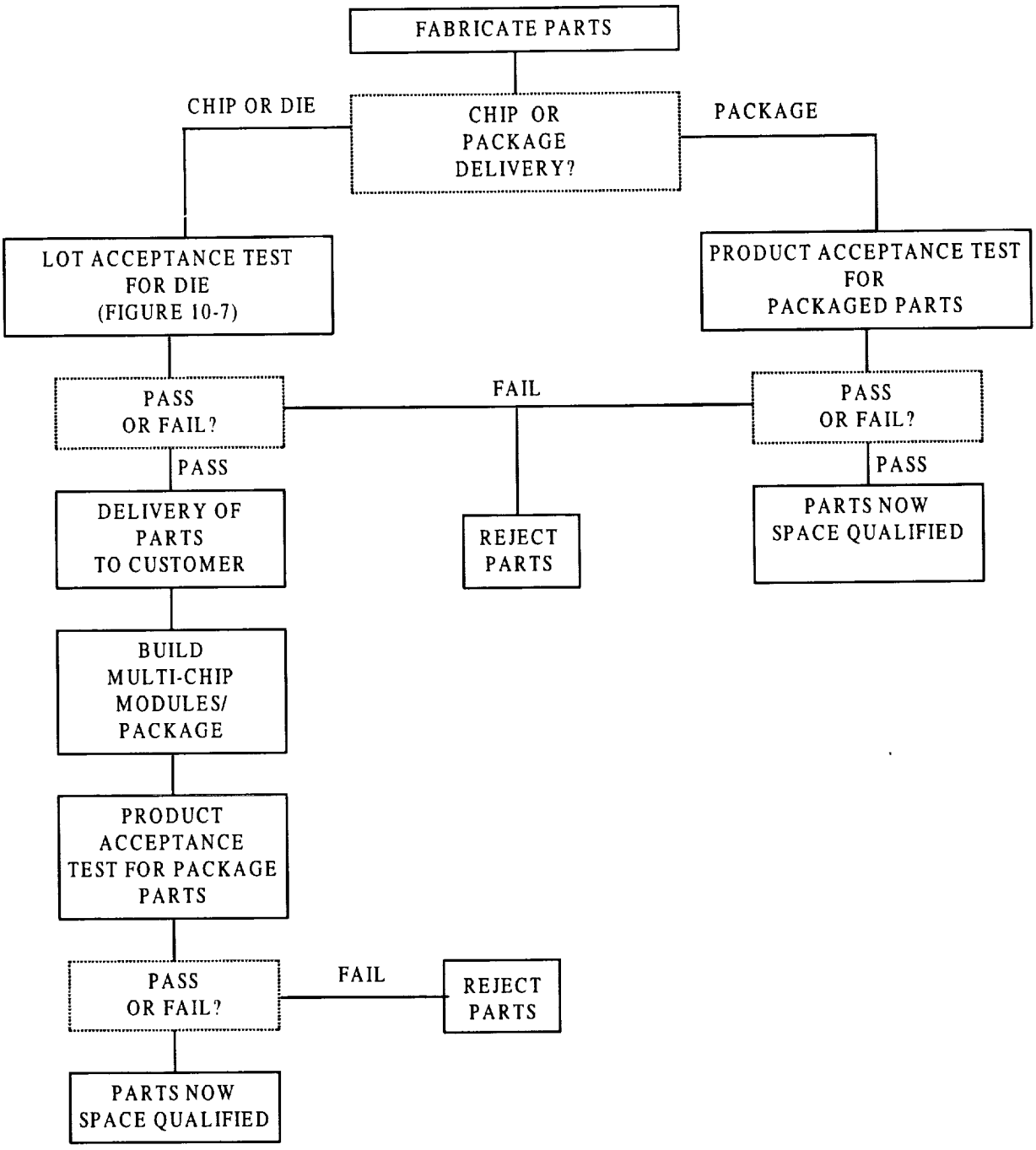

Figure 10-6: MEMS part qualification overview.

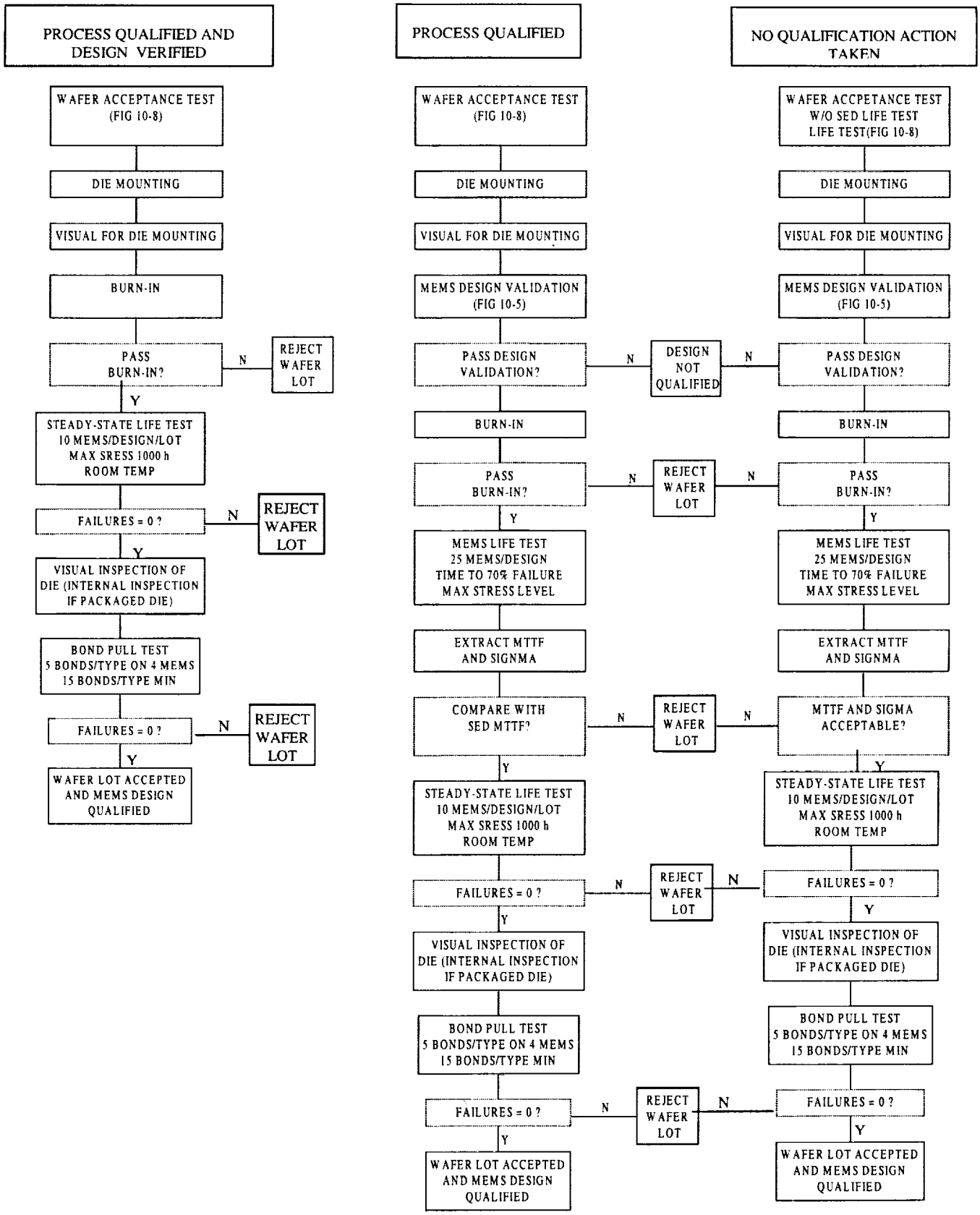

Figure 10-7: Lot acceptance test for die.

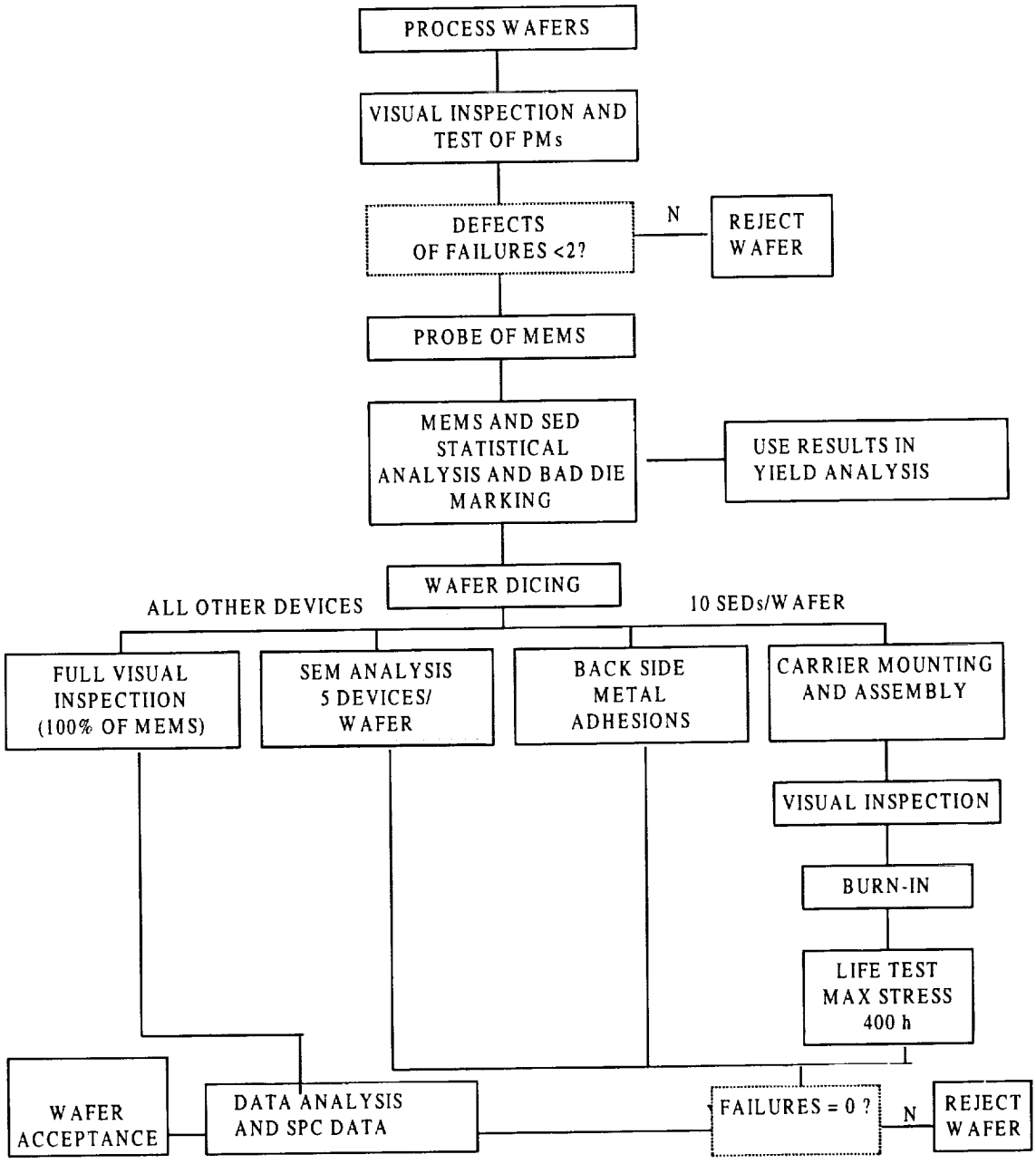

Figure 10-8: Wafer acceptance test.

It is assumed either that a product acceptance of die deliverables is performed on the devices before they are inserted into the packaging process or that a subgroup of the parts can be removed from the packaged parts and life testing performed on them in a way similar to that recommended for the die deliverables. Thus, this screen adds further reliability information to the data obtained from the wafer and lot acceptance tests. 100% of the packaged MEMS devices are recommended to be screened using the packaged

parts screen. It must be understood that this is only a recommended screen and not all tests will be necessary for all devices.

Table 10-1 shows the recommended screening tests that can be used for MEMS packaged devices and the reference for the screen. This information is modified from MIL-PRF-38534 Class K requirements and should be applied after careful consideration of the applicability and mission requirements. It should be kept in mind that these tests are designed for microelectronic circuits and may need to be modified for specific applications of MEMS.

Test	Reference
Nondestructive bond pull	MIL-STD-883, Method 2023
Internal visual inspection	MIL-STD-883, Method 2017
IR-scan (prior to seal)[1]	JEDEC Document JES2 [39]
Mechanical Shock	MIL-STD-883, Method 2002
Constant Acceleration	MIL-STD-883, Method 2001
Temperature cycling	MIL-STD-883, Method 1010
Thermal shock	MIL-STD-883, Method 1011
Particle impact noise detection	MIL-STD-883, Method 2020
Electrical	Customer's specifications
Burn-in	MIL-STD-883, Method 1015
Electrical (high/low) temp	Customer's specifications
Fine leak Gross leak	MIL-STD-883, Method 1014 MIL-STD-883, Method 1014
Radiographic	MIL-STD-883, Method 2012
External visual	MIL-STD-883, Method 2009

Table 10-1: Typical packaged device screening.

Throughout the rest of this chapter, a brief description of, and the rationale for, each product acceptance test or screen will be given.

A. SEM Analysis

Scanning Electron Microscopy analysis can provide valuable information regarding the step coverage and quality of the metallization and passivation on device. Thus, this tool is required as part of the wafer acceptance tests. Some accept/reject criteria are provided in MIL-STD-883, but they may need some modification to cover different MEMS technologies.

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[1] This test may only be necessary if a MEMS device has on-chip electronics.

B. Nondestructive Bond Pull Test

The integrity of wire bonds cannot always be judged through visual and electrical tests. Therefore, some qualification procedures recommend the implementation of a nondestructive bond pull test of each bond. The pull force selected for this test is generally dependent on the material and wire diameter in question. MIL-STD-883, Method 2023, is normally used for this application. Obviously selecting the required pull force is critical and must be decided by the manufacturer and the user.

Mechanical damage to good bonds as a result of the test is possible. Due to this problem, some manufacturers have removed this step from their qualification and screen procedures and resorted to in-process controls and testing to provide the necessary information. The decision to require this test must be made by the MEMS user after careful consideration of the system application and workmanship of the manufacturer.

C. Visual Inspection

Many defects in MEMS, such as substrate cracks, poor wire bonds, and foreign materials, reduce device reliability. Cracks can separate devices that are designed to be mechanically coupled, thus changing the mechanical characteristics of the device. Poor wire bonds increase the resistivity of the device, which can change the anticipated electrical output. Conductive particulates can short out devices, causing huge current flow through tiny fingers of comb drives. To prevent these and any other obvious flaws from impinging upon device performance, a visual screen of a device is performed during wafer acceptance tests for defects of the die and during the packaged device screens for packaging and bonding defects.

D. Laser Profile

Since some MEMS will have unacceptably high residual stresses, it is useful to measure the warping in a device caused by these stresses. One method of doing this is to use a laser profiling system to examine surface contour. These systems record non-planar displacements through the use of laser interferometry and have proven useful in the analysis of MEMS. One limitation to these systems is that they do not distinguish between surface contour and internal stress. The only tactic that has proven effective for differentiating between these two effects is to use differential measuring of surface profiles on devices that are etched on both sides. For devices suspended above the substrate, there is no method available for directly measuring internal stress.

E. IR Scan

Some defects, such as substrate cracks and die-attach voids, must be detected, whether or not they are visible. Since these types of defects have a different thermal conductivity than the surrounding defect free region, they may be detected through

thermal mapping. The baseline for comparison is the thermal profile of the MEMS device that was made as part of the product or design verification step. Typically a 5 °C variation in thermal output is enough for a device to be considered a reject. However, this step may not prove that informative if the temperature of the MEMS device does not vary much from the ambient temperature. Thus the applicability of this test will be design dependent and will likely require enough on-chip electronics to noticeably heat the device.

Although infrared microscopes are expensive, require calibration, and have a minimum resolution of approximately 15 μm, they are the best method of mapping a device's thermal characteristics, since they do not damage the device. While this screening step is not typically imposed as a requirement following MIL-PRF-38534, it is a good idea for any high power applications or application, such as those involving thermal actuators, that require good thermal stability. This step should be performed after die attach and before attachment of the package lid.

F. Mechanical Shock Screen

This screen is intended to detect weak parts that are required to undergo severe shocks during transportation, handling, satellite launch, or other operations. The test subjects the packaged MEMS to a number of short shock pulses with a defined peak. Failures are detected during final visual and electrical screens.

G. Constant Acceleration

This screen is intended to detect failures due to mechanical weaknesses by subjecting the packaged MEMS to a constant acceleration. Typical failures occur in the bonds and die attach, and these are detected during the final visual and electrical screens. This screen is an effective tool to detect poor workmanship. The appendix to this section describes methods for producing mission specific dynamic tests for MEMS and can be used either as a supplement or a replacement for the military standards.

H. Temperature Cycling and Shock Screen

Failure in mechanical devices can be accelerated by applying thermal stress. These tests detect structural defects or weak points in packaging that would normally result in early failures. Temperature cycling consists of cycling a packaged MEMS between extreme temperatures many times. Typically the temperatures used are –65 to 200 °C and the number of cycles is 15. The temperature shock screen is similar to the temperature cycle screen in that the test involves subjecting the packaged MEMS to extreme low and high temperature, usually -65 to 150 °C, over many cycles. The difference is that the rate of change in temperature with respect to time is much greater. Temperature shock screens are typically done between baths of hot and cold materials, while cycling screens use conductive air cooling to change temperature. Failure detection

for both screens is done in a final electrical and visual inspection. These tests are also discussed in great detail in MIL-STD-883, Methods 1010 and 1011.

I. Particle Impact Noise Detection

During encapsulation, thermal stress screens, and mechanical tests, particles may break off from either the MEMS device or the package. These loose particles may mechanically damage the MEMS or short out part of the circuit. That particle impact noise detection screen, or PIND, is a nondestructive test used to find parts that have this defect. During the test, the part is vibrated and a sensor is used to detect anomalous noise. Failure criteria are given in MIL-STD-883, Method 2020.

J. Burn-In

In an ideal world, devices that were substandard would be eliminated by a well controlled process line before they ever reach the customer. However, it is unrealistic to assume that a manufacturer can detect or predict which devices will fail with 100% accuracy. Therefore, to eliminate the device discussed in Chapter 2 as being part of the infant mortality group in a given production population, the burn-in screen must be performed.

The burn-in screen stresses devices above their normal operating conditions to accelerate any early failure that would occur from latent defects. For electronic circuits, burn-in is typically done at elevated temperatures to accelerate early failure mechanisms. For MEMS, the import of elevated temperatures will be device dependent. Far more likely to be of use is the practice of supplying a voltage that is above the normal operating regime for a device.

The difficulty in the burn-in test is to select a level of testing that will weed out weak devices while not damaging good ones. An implicit trade off in burn-in is that the confidence that a device will not suffer infant mortality comes at the expense of its long-term life expectancy. Thus, running the test for too long can be as problematic as running it in an abbreviated manner. The exact details of the burn-in will be up to the manufacturer and customer to decide in trying to balance the two conflicting goals of confidence and lifetime with the mission requirements. Devices that fail burn-in, which is usually defined as a pre-determined shift in output characteristics, should be discarded, rather than have any attempts made to salvage them.

K. Leak Test

There was a fair amount of information devoted to the subject of contamination and induced failure mechanisms in Chapter 3. To eliminate many of these problems, many MEMS devices are hermetically sealed in their packages and for these devices, their reliability is dependent upon the integrity of these seals. The thermal and mechanical

tests were intended to detect defects in packaging but often a leak test is required to find failed devices.

Fine leak tests consist of placing the packaged device in a chamber pressurized with a known gas, which will enter the package through any cracks that have developed. Usually helium or nitrogen gas with a small concentration of a radioactive isotope is used, since these gases can be detected in small concentrations using commercially available equipment. After a time, the chamber is cleansed by circulating air and the packages are tested to determine if gas leaks from them. Although the use of radioactive isotopes sounds somewhat extreme, it is the preferred method in high-volume production lines due to the fact that it is easier to detect for a longer period of time. The disadvantage of this method is that the gas will escape from a gross leak before it has time to be detected. Therefore, a gross leak test is used that is similar to the fine leak test except that it is conducted with a pressurized liquid bath instead of the gas.

L. Radiographic

The final screen is usually a radiographic picture of the inside of the sealed package taken with an x-ray machine. This nondestructive test uses radiation to penetrate the package walls and produce a shadow image on a photographic plate. It is useful for checking the location and position of wire bonds and for detecting loose particles that may have moved or broken off during the screening process. In some cases, this screen can also be useful in determining the presence of die-attach voids.

IV. Company Certification

Procurement of MEMS will often be the result of long-term partnerships between the customer and manufacturer in which both parties collaborate in order to assure the reliability and performance specifications of the flight ready device. This close relationship between the two parties evolves through mutual trust. In a new partnership, the best way for a manufacturer to establish trust is to show that it has good control over the facilities, processes, and personnel used to make these devices. Typically these controls, which include documentation, procedures, and management practices, are part of a Quality Management Program. This step of proving that the company has these processes in place is referred to as "company certification" and is usually verified by the MEMS user through a written or facility audit. It is recommended that the audit and company certification be completed before the contract for a deliverable MEMS device is signed. In some cases, the MEMS user may make this requirement a paramount consideration in selecting a company from which to buy parts. A company that does not have tight quality controls installed should not be allowed to supply MEMS for high-rel applications.

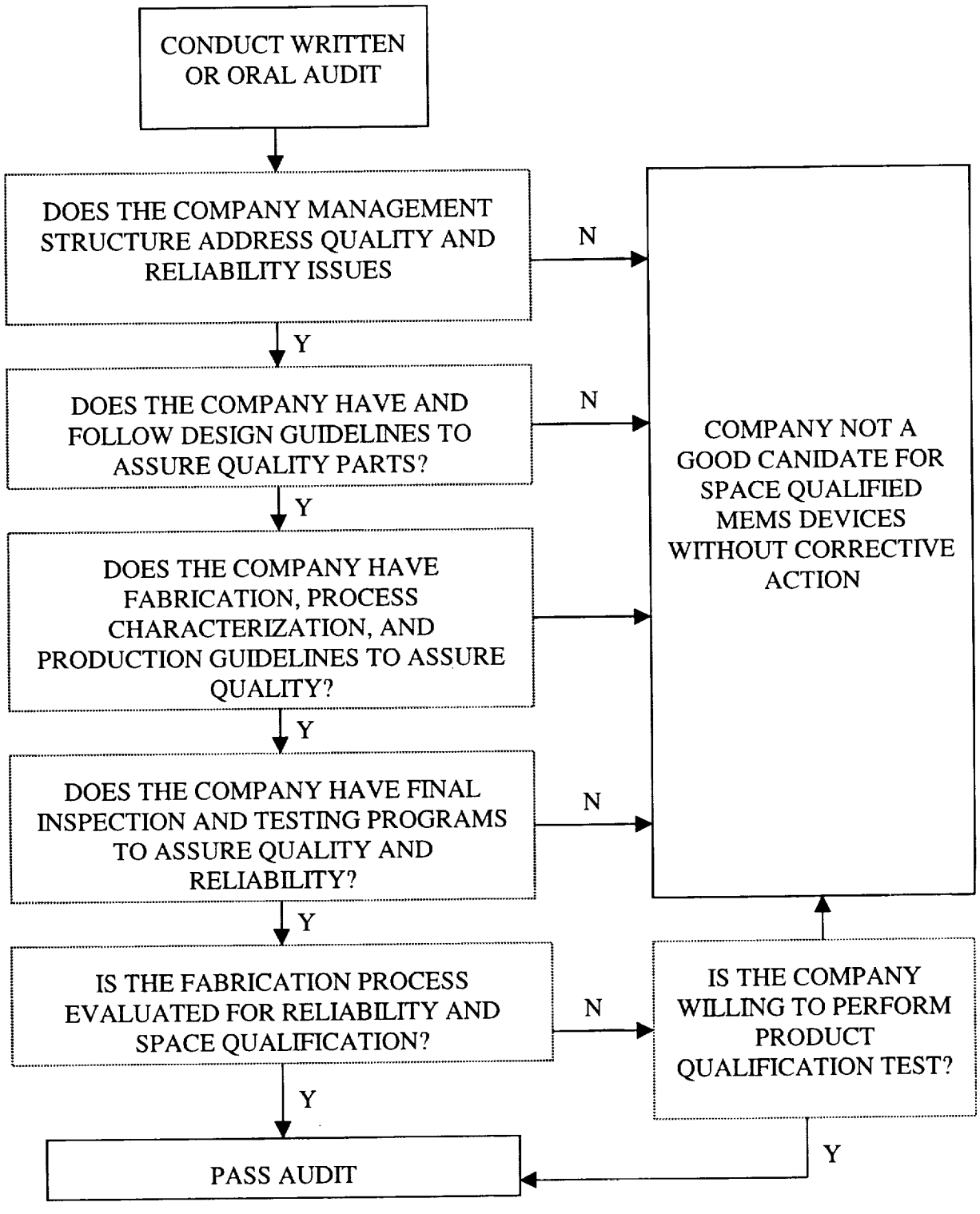

Figure 10-9: Reliability audit.

Since most of the information sought during company certification is based upon established quality control programs and standard industry methodologies,[1] the audit should be easy and inexpensive for both the user and manufacturer. Manufacturers should keep this information available and ready for distribution at all times. This whole process may be facilitated if the manufacturer has passed previous qualification audits, in which case this step may only require an update from previous audits.

A simplified version of the audit is shown in Figure 10-9. The audit for a specific MEMS must be developed on a case-by-case basis. The major items in the Quality Management Program are presented in the rest of this section, but it must be remembered that this is only a partial list. As stated before, the end goal of a reliable MEMS device is ultimately in the hands of the user. Any additional device specific tests must be specified by the user as needed.

A. Technology Review Board

In order to assure the quality and reliability of MEMS, manufacturers will usually have a permanent committee in place with authoritative knowledge of the entire fabrication process. If the quality of the process is not maintained, this committee, called the Technology Review Board, or TRB for short, will have power to change the process to improve quality. The TRB is responsible for the following measures:

- The development, implementation, and documentation of the manufacturer's Quality Management Program and Quality Management Plan.
- The development, implementation, and documentation of the manufacturer's Process Qualification, Product Qualification, and Product Acceptance Plans.
- Compiling and maintaining all records of the fabrication process, statistical process control (SPC) procedures, SPC data, certification and qualification processes, reliability data analysis, and corrective actions taken to remedy reliability problems.
- Examining test structures and MEMS reliability data and establishing and implementing corrective actions when the reliability of the devices decreases.
- Notifying customers when the reliability of a wafer lot is questioned and supplying the customers an evaluation of the problem and any corrective action required.
- Supplying reliability data to customers.

Because of these great responsibilities that cover such a broad area of knowledge, the members of the TRB should have good hands-on knowledge of device design, technology development, wafer fabrication, assembly, testing, and quality assurance procedures. While the members of the TRB board are usually from the manufacturing company, it is not unusual for a customer to request a seat on the board for their products.

B. Conversion of Customer Requirements

Not all customers express their specifications in the same way, and not all MEMS manufacturers publish their performance specifications and operating guidelines in the same way. Normally a user will ask for a device with specific characteristics, such as an accelerometer with a dynamic range of +/- 50g and a resolution of .1g instead of saying that they want a bulk micromachined device with a cantilever beam accelerometer. It is the job of the manufacturer to use the requirements of the user to determine the device design. It is through the conversion of the customer's specifications to the manufacturer's designs that the manufacturer can determine the cost and reliability concerns of the device. It is recommended that the procedure by which a customer's requirements are converted to the manufacturer's working instructions be documented. A typical document will describe the procedure a company performs, the order in which they are performed, and the typical schedule. Some of the items typically included in this conversion are:

- Relating customer device requirements to manufacturer device requirements.
- Converting the device requirements to a device design, using controlled design procedures and tools (i.e. established electric, geometric, mechanical, and reliability design rules).
- Establishing a design review team.
- Selection of test structures.
- Mask generation procedure within the controlled design procedure.
- Wafer-fabrication-capabilities baseline.
- Circuit fabrication procedure in accordance with approved design, mask, fabrication, assembly, and test flows.
- Incoming inspection and supplier procurement document covering design, mask, fabrication, and assembly.
- Establishment of screening and traveler documents.
- Technology Conformance Inspection, or TCI, procedures.
- Marking requirements.
- Rework procedures.

C. Manufacturing Control Procedures

MEMS manufacture is a complicated process that involves multiple materials and steps, each of which are critical to final device performance and reliability. Only a properly controlled manufacturing line can be expected to routinely produce quality MEMS devices. For this reason, the customer needs to be assured that the manufacturer is using only certified processes and qualified technologies at every step of the manufacturing process. To obtain that level of assurance, the company certification audit should review the manufacturer's procedure for:

- Traceability of all materials and products to the wafer lot.
- Incoming inspection to assure conformance to the material specification.
- Electrostatic discharge, or ESD, control in handling the material in all stages of manufacturing.
- Conformance with design requirements at:
  1. Device procurement specification
  2. Layout verification
  3. Testability and fault coverage verification
  4. Electrical and mechanical parameter performance extraction
  5. Archived data
- Conformance with fabrication requirements at:
  1. Mask fabrication
  2. Mask inspection
  3. Wafer fabrication
- Assembly and package requirements.
- Electrical and mechanical testing.

Most of this information can be obtained by examining the manufacturer's process flow.

D. Equipment Calibration and Maintenance

In order to maintain device quality, the processing equipment must be maintained. For this reason, all equipment used in the manufacturing process must be kept to the equipment manufacturer's specifications. In addition to routine maintenance, the equipment must also be calibrated on a regular basis. Documentation showing the

maintenance and calibration schedule, departures from this schedule, and corrective action taken due to these departures should be kept by the manufacturers. This documentation will also highlight any major discrepancies found in the calibration and maintenance of a piece of equipment, since it could affect the reliability of the MEMS. The TRB will review this documentation to determine if any corrective action is required. Further information on equipment calibration can be found in Reference [31].

E. Training Programs

Even well maintained and calibrated equipment cannot produce quality devices without skilled operators. To assure the skills of the personnel employed in the design, fabrication, and testing of devices, each engineer, scientist, and technician should have formal training relative to their tasks. Furthermore, retesting and retraining should be provided regularly to maintain the worker's proficiency, especially if new equipment or procedures are introduced into the manufacturing process. It is therefore recommended that the work training and testing practices employed to establish, evaluate, and maintain the skills of personnel engaged in reliability-critical work be documented with respect to form, content, and frequency.

F. Corrective Action Program

One of the best ways to continuously improve the reliability of manufactured parts is to test and analyze failed parts from all stages of manufacturing and, based on these findings, make corrective actions to the manufacturing process or to the education of the end users. The plan that describes these corrective actions is normally documented and should detail the specific steps followed by the manufacturer to correct any process that is found to be defective. The documentation should also include the mechanisms and time frames involved in informing customers of potential reliability problems.

G. Self-Audit Program

To promote continual quality improvement, manufacturers regularly review their manufacturing procedures through an independent internal self-audit program under the direction of the TRB. The self-audit program should identify the critical review areas, their frequency of audit, and the corrective action system to be employed when deviations from requirements are found. Typical areas included in a self-audit are:

- Calibration and preventive maintenance,
- Fabrication procedures,
- Training programs,
- Electrical and mechanical tests,
- Failure analysis programs,

- Test methods,
- Environmental control,
- Incoming inspection,
- Inventory control and traceability,
- Statistical Process Control and
- Record Retention.

The self-audit checklist, the date of the previous audits, and all the findings from the audits are typically maintained by the TRB, which will use these findings to recommend corrective actions and prepare a self-audit follow-up.

H. Electrostatic Discharge Handling Program

Because of the catastrophic failure caused by ESD, all personnel that work with MEMS should be trained in the proper procedures for handling the devices. Furthermore, these procedures should be documented and available for reference. Typically, the procedures include the methods, equipment, and materials used in the handling, packaging and testing of MEMS. Further guidance for device handling is available in the Electronics Industry Association JEDEC Publication EIA 625 [33] and MIL-STD-1686.[34]

I. Cleanliness and Atmospheric Controls

The quality of MEMS and the yield of the fabrication line is directly linked to the manufacturer's control over the cleanliness of the environment in which the parts are fabricated. Therefore, manufacturers often spend a large amount of their resources to guarantee that devices are fabricated in ultraclean rooms where the atmosphere is tightly controlled. Since the yield of the fabrication process is so strongly dependent on the success of maintaining those conditions, regular measurements are taken to assure the temperature, humidity, and cleanliness of the fabrication areas. In addition, during transit and storage prior to seal, the die/wafer should be protected from human contact, machine overspray, or other sources of contamination. All of these procedures and measurements are recorded and compiled into a single document by the clean-room manager for future reference.

J. Record Retention

Documentation is the only method available to gauge the reliability of MEMS as a function of time, which is critical to spotting faults in the process line. Although many sections in this guide recommend the documentation of certain data or procedures, it is helpful if a list of documents and the period of retention for each document is made.

Furthermore, the list should contain a record of when each document was last changed, who is responsible for maintaining the document, and where the document is stored. The typical documents to be retained are those that relate to

- Inspection operations,
- Failure and defect report and analysis,
- Initial documentation and subsequent changes in design, materials, or processing,
- Equipment calibration,
- Process, utility, and material controls,
- Product lot identification,
- Product traceability,
- Self-audit report,
- Personnel training and testing and
- TRB meeting minutes.

K. Inventory Control

The proper inventory of all incoming materials and outgoing parts is not only required for the management of a profitable company but also for the manufacture of reliable MEMS devices. Many materials and chemicals used in the fabrication of MEMS have shelf lives that must be tracked if process yield and reliability are to be maintained. The tracking of in-process and completed MEMS is essential for the establishment of MEMS history, which is critical in failure analysis. Therefore, the methods and procedures used to control the inventory of all materials related to MEMS manufacturing should be documented. This documentation typically includes:

- Incoming inspection requirements and reports.
- Identification and segregation of non-conforming materials.
- Identification and control of limited-life materials.
- Control of raw materials.
- Data retention for required receiving reports, test reports, certification, etc.
- Supplier certification plan.

L. Statistical Process Control

The establishment of a statistical baseline for judging the continuous improvement of a manufacturer's process is an important task. To establish that baseline, the manufacturer should develop an SPC program using in-process monitoring techniques to control the key processing steps that affect device yield and reliability. As part of the SPC process, every wafer lot typically has built-in control monitors from which data are gathered, which should then be analyzed by appropriated SPC methods to determine the effectiveness of the company's continuous improvement plans. Additional information on SPC analysis can be found in the Electronics Industry Association JEDEC EIA 556A [35] and in MIL-I-38535.[36]

V. Additional Reading

Microelectronics Failure Analysis Techniques, A Procedural Guide, E. Doyle, Jr., and B. Morris, Editors, report written for Air Force Systems Command, Rome Air Development Center under contracts F30602-78-C-0339 and F30602-78-C-0281

MIL-STD-1540C, *Test Requirements for Launch, Upper-Stage and Space Vehicles,* United States Air Force Military Standard, 1994.

Thomson, W. T., "Theory of Vibration with Applications," 2nd ed., Prentice-Hall, Inc., Engelwood Cliffs, New Jersey, 1981.

Kinsler, L. E. and A. R. Frey, "Fundamentals of Acoustics," 2nd ed., John Wiley & Sons, Inc., New York, 1962.

Markstein, H. W., "Designing Electronics for High Vibration and Shock," *Electronic Packaging & Production,* April 1987, pp. 40-43.

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Appendix: Mission Specific Environmental Testing

J. Newell and K. Man

One of the challenges in space qualification is to define the operational environment of a part such that it is tested to the limits of a mission without requiring expensive overdesign. To aid this, this section defines, discusses and recommends environmental design and verification requirements for space microelectromechanical systems. Typical environmental program policies are presented, along with environmental design and test configuration requirements. Sample specifications are provided for a variety of environments, ranging from launch vehicle dynamics to ground handling conditions. Through judicious implementation of the analysis, test and verification techniques outlined herein, robust and reliable MEMS devices can be developed for long term survival in the unforgiving space environment.

A. Test Procedures

The fundamental purposes of an environmental test program are to simulate the launch environment, to qualify designs for launch and in-service conditions, and to screen flight hardware for manufacturing workmanship. Such a program should effectively demonstrate the quality and reliability of a design, as well as its suitability for the intended purpose or mission.

Environmental Compatibility Analyses are often conducted to verify hardware design compliance with mission environments that are impractical to verify by test. Design margins for these analyses must normally be higher than margins demonstrated by environmental test.

Such analyses are often conducted for the ground handling environment, including vibration and shock, temperature and humidity. Analyses are also normally conducted to demonstrate compatibility with explosive atmosphere requirements, and to prove structural integrity under launch pressure decay and thermal shock conditions.

Environmental Testing is conducted at two levels: the assembly/subsystem level and the system level. Assembly/subsystem level testing is completed prior to delivery for higher level integration into a flight system, and is generally the responsibility of a cognizant hardware engineer. The majority of space micromechanisms fall into this category. Post delivery environmental testing at a higher level of system integration is then usually conducted under the auspices of an Assembly, Test and Launch Operations, or ATLO, Manager.

Environmental tests are categorized for the purpose of hardware quality and reliability verification as *Protoflight*, *Qualification* and *Acceptance*, which are defined as follows.

Protoflight tests are conducted on flight hardware to demonstrate its ability to meet mission requirements. Protoflight test levels are generally equal to qualification levels, although test duration is often reduced.

Qualification tests are performed to a level and/or duration sufficient to demonstrate ability of a hardware design to meet mission requirements, with adequate margin. Such testing is generally conducted on a dedicated unit.

Acceptance tests are performed to detect workmanship or other defects which may have been introduced in the fabrication process, and to demonstrate hardware acceptability for flight. Acceptance testing is performed on flight hardware and spares when an adequate protoflight or qualification heritage exists.

In addition, development environmental testing is also often conducted to gain insight into design compatibility or functionality in expected mission environments. As an example, a dynamics test model of a flight system is sometimes assembled for purposes of structural verification.

i) Test Sequencing

To accurately simulate the environment sequence, flight hardware testing should be performed as follows:

1. Sinusoidal or transient vibration, random vibration, pyroshock and acoustics, as required. The order among these dynamics tests may be interchanged.

2. Thermal-vacuum testing.

During the normal flight sequence, the launch environment is followed by vacuum and potential temperature extremes. In this flight sequence, hardware is exposed to acoustics and vibration followed by vacuum and temperature variations. Consequently, by performing dynamics tests prior to thermal-vacuum tests, the actual flight sequence will be simulated. If the flight sequence produces synergistic effects, the synergism will also be simulated.

Experience has shown that until the thermal-vacuum tests are performed, many failures induced during dynamics testing are not detected because of the short duration of the dynamics tests. In addition, the thermal-vacuum test on flight hardware at both the

assembly level and the system level provides a good screen for intermittent as well as incipient hardware failures.

Preserving the sequence of service environments in the environmental test program is a widely accepted practice. As a result, the effect of reversing the test sequence on spacecraft failure rates has not been quantified. However, evidence exists that many acoustic induced failures have not been detected until the spacecraft is exposed to the thermal-vacuum environment. These failures may not be detected during acoustics tests because of the short one-minute duration or a non-operating power condition. Typically, the identified failures that could be related to or caused by the dynamic acoustic environment were bad solder joints, intermittents, bad bearings, broken wires, poor welds, leaks, and foreign materials.

An example of a failure that might be induced by dynamic tests but not revealed until thermal vacuum, would be a broken wire or solder joint. This defect might be induced by acoustics but not be detected during the acoustic test due to the short duration of the test or to an unpowered or unmonitored state of the affected equipment. During post-acoustic functional testing, the wire or solder joint broken ends may be making adequate contact to show electrical continuity. In the subsequent thermal-vacuum test, the thermal distortions could cause loss of contact, allowing the failure to be detected. Reversing the test sequence could result in the defect not being induced until after thermal vacuum test and not detected until exposure to the flight thermal environment.

Even if all defects precipitated by the dynamics tests are revealed during the test or during post-test functional testing, performing dynamic tests first will nonetheless increase the probability of early defect detection, when correction of defects will have less impact on the flight program cost and schedule.

If the thermal-vacuum tests do not follow the dynamics tests, more intermittent or incipient discontinuity type failures may go undetected. If the defects are not detected during assembly level tests and are subsequently detected during the system level tests, redesign or rework at this late stage of the process could cause delays, increase costs, or make it necessary to accept additional risk that might have been avoided. If the defects are not detected at the system level, the defects may then cause hardware anomalies during the mission, and in the extreme could cause a mission failure.

B. Environmental Test Requirements

Appropriate in-situ environments must be determined and specified in order to effect a robust space microelectromechanical device design. These environmental design requirements depend upon factors ranging from the choice of launch vehicle to the type of spacecraft thermal control subsystem. Establishment of these requirements can be a time consuming task involving considerable research and analysis effort.

The requirements within this section encompass the basic launch environments, as well as those associated with ground operations and handling. They are offered here as generic baseline environmental levels, and should be used primarily as examples.

i) Launch Environment

The launch environment encompasses pre-launch operations, liftoff, and ascent. Typical requirements are provided here for both design and test of space micro-electromechanical devices, with environments including thermal conditions, deep space vacuum and insertion pressure decay, random and sinusoidal vibration, pyrotechnic shock and acoustic noise.

ii) Thermal

Spacecraft microelectromechanical systems should be designed to operate within specification over the temperature range of -55°C to +70°C, or flight allowable ±20°C, whichever is more extreme.

iii) Definitions

Terms used in thermal design and test of space microelectromechanical systems are defined as follows:

Operating Allowable Flight Temperatures: The temperature ranges of MEMS devices when powered-on in a worst case operational mode (hot or cold). In-spec operation is required.

Non-Operating Allowable Flight Temperatures: The temperature ranges of MEMS devices when powered-off in a worst case non-operational mode (hot or cold). MEMS devices must be capable of returning to in-spec operation as temperatures return to Operating Allowable Flight levels.

Design Temperature Limits: Temperature limits to which all MEMS devices should be designed to meet all functional and performance specifications.

Stabilization Temperature: In specification of test conditions, an assembly is defined to have attained a stabilization temperature when the rate of temperature change of its largest centrally located thermal mass is less than 2°C per hour.

Control Temperature - Conductive Heat Transfer Tests: The control temperature for a thermal/vacuum conductive heat transfer test is defined to be the temperature of the heat exchanger plate midway between input and output of heat exchange fluid.

Control Temperature - Radiative Heat Transfer Tests: The control temperature for a thermal/vacuum radiative heat transfer test is defined to be the temperature of the major temperature control surface of the assembly (e.g. radiator).

iv) Thermal Radiation

Assembly allowable flight temperatures should not be exceeded during the mission under exposure to the applicable worst case expected thermal radiation levels in the accompanying table.

Mission Phase	Direct Solar	Reflected Solar (Albedo)	Planetary IR (LW Radiation)
Earth Orbit:	0 to 1400 W/m^2 (5770K effective blackbody temperature)	0 to 0.32 0 to 450 W/m^2 (global annual mean) 0 to 0.70 W/m^2 (polar regions)	100 to 270 W/m^2 (206K to 262K effective blackbody temperature)
Deep Space Cruise: Near Earth	0 to 1400 W/m^2 (at earth perihelion)	Negligible beyond 4 earth radii	Negligible beyond 4 earth radii

Table A-1: Thermal radiation levels.

v) Vacuum Pressure Decay

The design pressure for a typical mission can be expected to decrease from 101325 N/m^2 (760 Torr) on Earth to 1.33 x 10^{-3} N/m^2 ($1x10^{-5}$ Torr) in deep space. A typical launch pressure decay rate, showing launch vehicle internal fairing pressure versus time, is provided in the figure below.

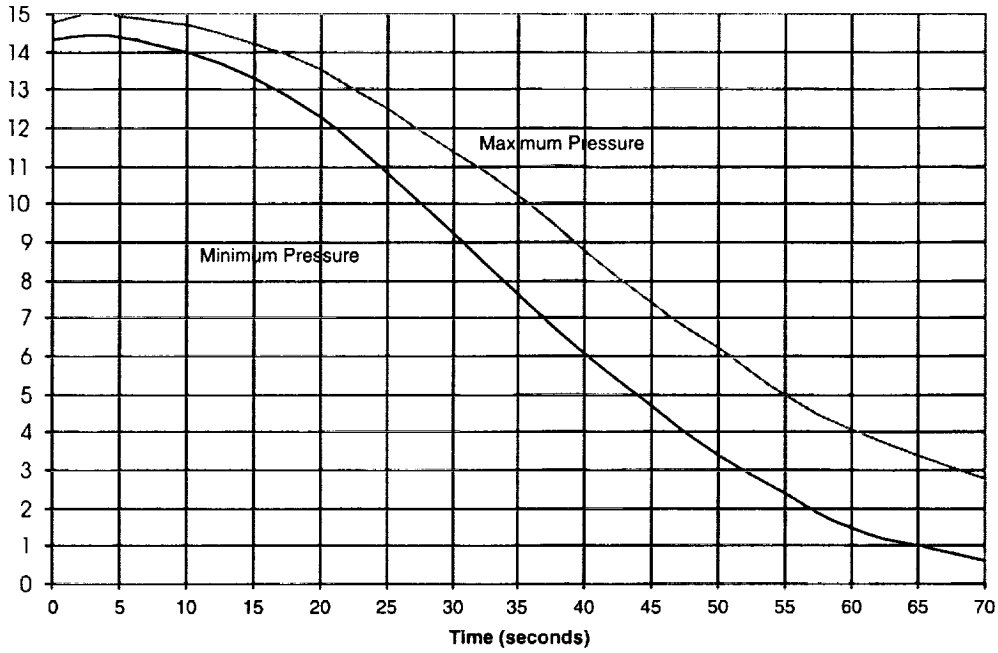

Figure A-1: Launch pressure decay rate.

Assemblies affected by launch pressure decay should be designed with a recommended structural design factor of 1.0 on yield and 1.4 on ultimate if tested, or 1.6 on yield and 2.0 on ultimate if not tested.

vi) Dynamics

Assembly-level vibration and shock tests, simulating launch vibroacoustics and upper-stage pyrotechnic separation events, represent the most severe dynamic environments for spacecraft hardware. Components of a spacecraft, at various levels of assembly, should generally be subjected to the following environments:

(1) Definitions

Sinusoidal vibration requirements are imposed to cover the various mid-frequency (5-100 Hz) launch vehicle-induced transient loading events.

Random vibration requirements are derived from launch vehicle induced acoustic excitations during liftoff, transonic and maximum dynamic pressure (e.g. "max q") events.

Acoustic requirements are based on maximum internal payload fairing sound pressure level spectra.

Pyroshock requirements are intended to represent the structurally transmitted transients from explosive separation devices, including pyrotechnic fasteners utilized to effect spacecraft separation from the upper stage.

Quasi-Static Accelerations are associated with quasi-steady flight events generated by rocket motor-induced forces and other external forces which change slowly with time and for which the elastic responses are relatively small. Typical assembly design requirements for quasi-static acceleration environments are specified in the table below.

Axis	Acceleration (g)
Thrust	+14 ± 0.7
Lateral	+3 ± 0.3

Table A-2: Quasi-static accelerations.

Qualification testing of microelectromechanical systems for the quasi-static acceleration environment can be performed in a centrifuge. However, a low frequency sine vibration test, conducted on an electrodynamic shaker, can often be substituted for the relatively expensive centrifuge trial. If a microelectromechanical system is subjected to sine testing at a frequency sufficiently below its fundamental resonance, it will not vibrate, but will instead move as a rigid body under the input sine acceleration. To ensure pure rigid body behavior of the assembly under test, the frequency of sine excitation should generally be less than the microelectromechanical system resonance by a factor of two. More detail on each of the other test environments is provided below.

(2) Dynamics Test Tolerances

Tolerances for dynamics testing are provided below. The indicated tolerances are derived from space vehicle hardware test experience, and may be facility-, equipment-, and personnel-dependent.

a. Time: ±5 percent

b. Vibration Frequency: ±5 percent or 1 Hz, whichever is greater.

c. Acoustic Spectral Shape: Match to spectral shape of the specified Sound Pressure Level (SPL) in 1/3 octave bands.

d. Acoustic Overall Level: ± 1 dB of the specified level.

e. Random Vibration Spectral Shape: The Acceleration Spectral Density (ASD) shall be within ±3 dB when measured in frequency bands no wider than 25 Hz.

f. Random Vibration Wideband RMS Acceleration: Within ±1.0 dB of that specified.

g. Pyro Shock : ± 3 dB 20 to 2000 Hz

h. Static Acceleration: ±5%

(3) Sinusoidal Vibration

Sinusoidal vibration is employed to simulate the effects of significant flight environment launch transients. These transients typically produce the dominant loading on primary and secondary structure and many of the larger subsystems and assemblies. Sinusoidal vibration is the only widespread current method of adequately exciting the lower frequency dynamic modes, particularly those below 40 Hz.

Sweeping at a log rate between 1 octave/minute and 6 octaves/minute should avoid application of excessive fatigue cycles. The higher rate is near the upper limit which most control systems can accommodate without experiencing some instability. The use of logarithmic sweep rates has the advantage in that a nearly equal time is spent at resonance for a given Q, independent of frequency. Sinusoidal vibration levels can be derived as illustrated in the following example:

Step 1. Create analytically derived transient waveforms from various flight events:

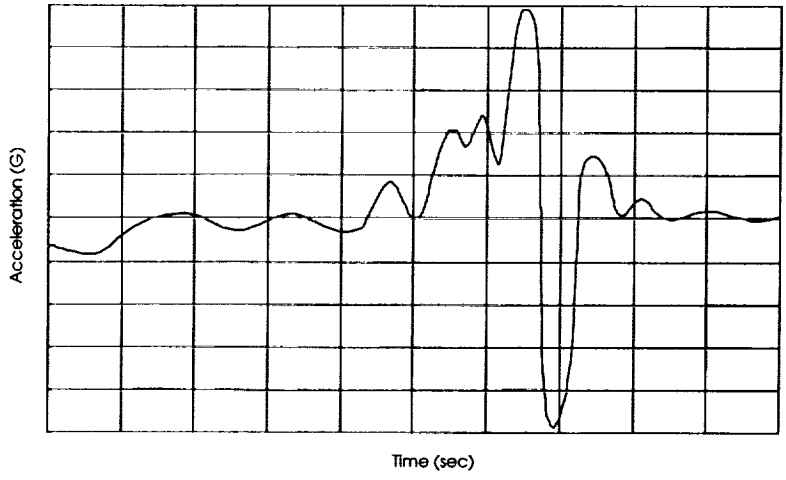

Figure A-2a: Creation of a sinusoidal vibration test profile (see 2b-e).

Step 2. Compute the shock spectra for each of the waveforms in Step 1:

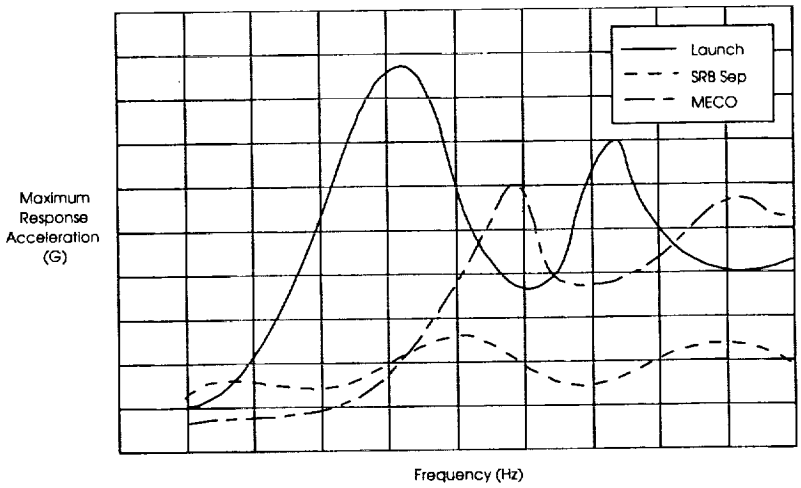

Figure A-2b

Step 3. Take data from previous flight measurements:

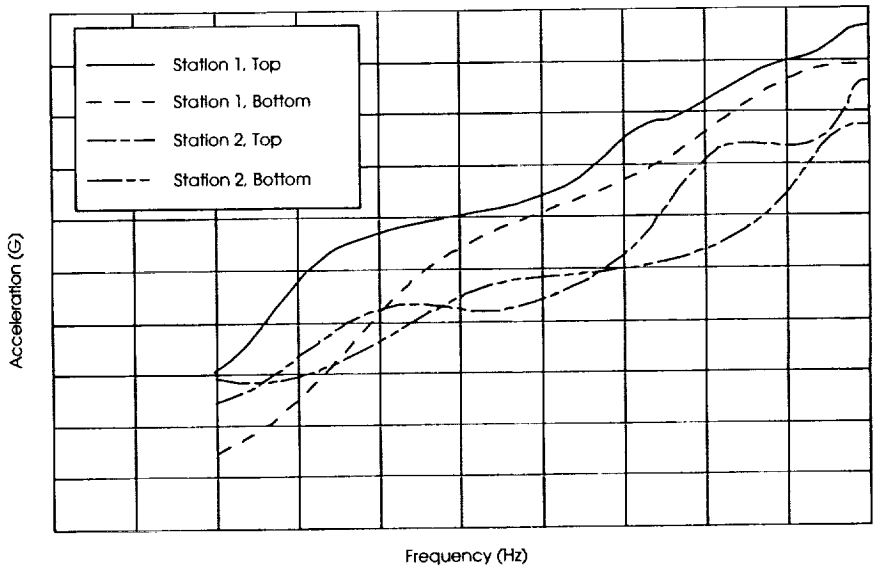

Figure A-2c

Step 4. Combine results from steps 2, and 3 and envelope:

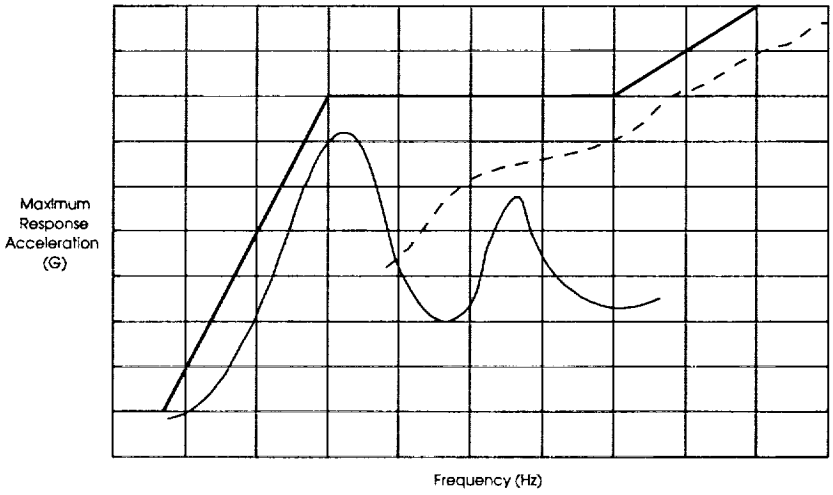

Figure A-2d

Step 5. Convert to a sine amplitude equivalent vs. frequency by dividing Shock Response Spectrum envelope in Step 4 by Q:

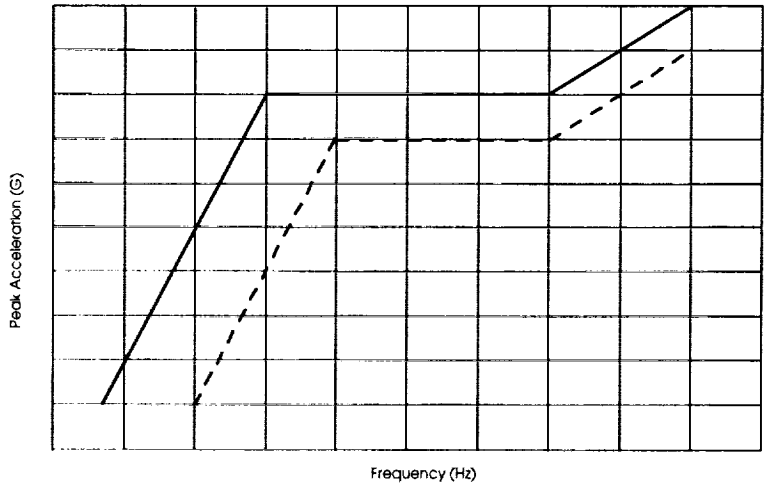

Figure A-2e

Alternatives to the use of swept sine vibration testing are currently under development which address several of the objections to this method. In particular, the problem of excessive resonance build-up in a sinusoidal vibration sweep relative to the flight transient environment may be alleviated by any of the following tests:

- Narrow band swept random.
- Discrete frequency sinusoidal pulses applied at regular frequency intervals.

- Complex waveform pulses representative of a composite of the various launch transient events.

Space microelectromechanical systems should be subjected to a set of swept sinusoidal vibration requirements similar to those specified in the table below. The sine vibration should be applied to the test item by sweeping over a frequency range beginning at 10 Hz (± one octave) up to 100 Hz (± one octave). The frequency range should be swept at a logarithmic rate, such that $\Delta f/f$ is constant. This testing may generally be performed with the same fixturing as a random test, and is often run concurrent with the random vibration trial.

For all tests, these conditions should be applied at interface or mounting surfaces. For structure-like assemblies such as antennas and some large microelectromechanical systems, the input forces may be limited or notches may be applied to the acceleration levels, such that forces at the interface do not exceed spacecraft structural design loads.

Spacecraft-Level		**Assembly-Level**	
Frequency (Hz)	**Level (Gs)**	**Frequency (Hz)**	**Level (Gs)**
5 - 10	1.0 cm DA[1]	5 - 20	1.9 cm DA
10 - 100	2.0 (0 - peak)	20 - 100	12.0 (0 - peak)
100 - 200	1.0 (0 - peak)	100 - 200	3.0 (0 - peak)

SWEEP RATE:
QUAL: 1 OCTAVE PER MINUTE, ONCE UP OR DOWN IN EACH OF THREE ORTHOGONAL AXES.
PF TEST: 2 OCTAVES PER MINUTE, ONCE UP OR DOWN IN EACH OF THREE ORTHOGONAL AXES.
ACCEPTANCE: SAME AS PF.

Table A-3: Sinusoidal vibration.

(4) Random Vibration

The random vibration environment consists of stochastic instantaneous accelerations which are input to a microelectromechanical system or other assembly, transmitted via spacecraft structure under launch dynamic excitation conditions. Random vibration input occurs over a broad frequency range, from about 10 Hz to 2000 Hz. In the space vehicle launch environment, random vibration is caused primarily by acoustic noise

[1] DA: Double Amplitude Displacement.

in the payload fairing, which is in turn induced by external aerodynamic forces due to dynamic pressure and reflection of rocket exhaust from the ground.

For microelectromechanical systems, random vibration can induce a number of failure modes, including fretting in gear trains and breakage of lead-wires in drive electronics. Brinnelling in recirculating bearings can also occur, as the random environment produces the equivalent of micro-shocks in these assemblies.

Random vibration criteria should be developed by the process described in the following four steps:

1. Determine the Power Spectral Density (PSD) of the random vibration directly transmitted into the flight article through its mounts from the launch vehicle sources such as engine firing, turbopumps, etc., as illustrated in the following figure. These vibration conditions at the launch vehicle-to-payload interface are typically available from the launch vehicle developer.

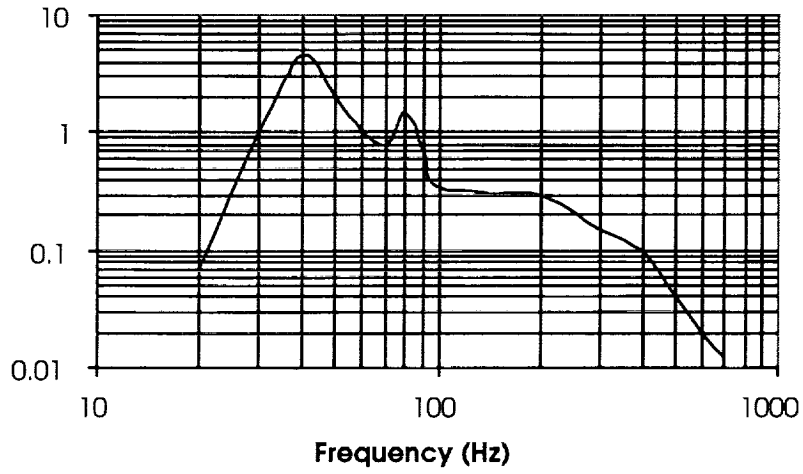

Figure A-3: Vibration levels transmitted to flight article through mounts.

2. Perform an analysis to predict the payload/flight article's vibration response to the launch vibroacoustic environment, as illustrated in the figure below. Statistical energy analysis (SEA) methods such as the VAPEPS (VibroAcoustic Payload Environment Prediction System) program are effective predictors in the higher frequencies. The VAPEPS program can also effectively extrapolate from a database using SEA techniques to provide predictions for a similar configuration. If random vibration predictions are needed for the lower frequencies, finite element analysis methods, such as NASTRAN,

are commonly used. The vibration is induced into the test article both directly and indirectly through its mounting.

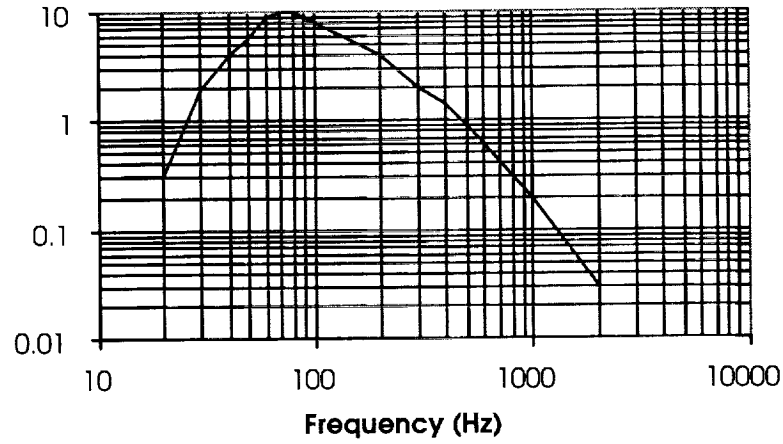

Figure A-4: Payload/flight article response to vibroacoustic environment.

3. Establish a minimum level of vibration which is necessary to ferret out existing workmanship defects and potential failures. The figure below provides such a workmanship vibe level, as specified in MIL-STD-1540.

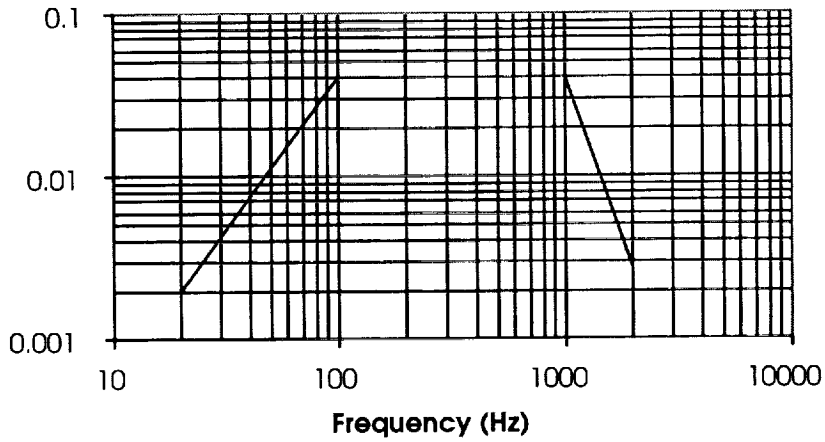

Figure A-5: Minimum vibration levels for workmanship defect detection

4. Envelope the curves from steps 1-3 to produce a composite random vibration specification for the test article, as illustrated below.

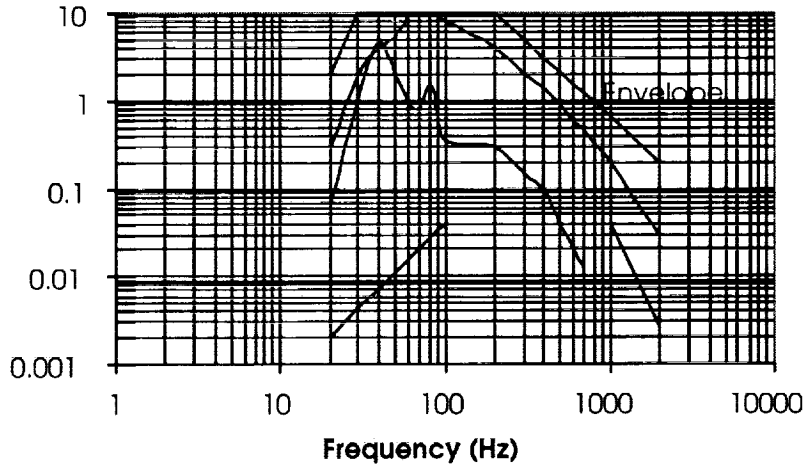

Figure A-6: Composite random vibration envelope.

This resultant random vibration specification, which is employed as the flight acceptance test level, covers the two primary sources of this vibration while also providing an effective process for uncovering workmanship defects. Qualification and Protoflight test levels are increased typically 3 to 6 dB above flight acceptance to verify that the design is not marginal.

Recommended random vibration environments for both spacecraft and assembly-level testing are specified in the accompanying table. Instantaneous accelerations are assumed to exhibit a gaussian distribution. For structure-like assemblies such as antennas and some large instruments, force limit criteria should be used in testing to mitigate the problem of impedance mismatch between the test article and rigid shaker fixture.

Typically, microelectromechanical systems and similar assemblies are mounted to spacecraft structure which is somewhat flexible. If, during a launch event, the MEMS is excited into a state of mechanical resonance, the relatively low stiffness spacecraft mount will serve to limit interface forces. On the other hand, if a microelectromechanical system resonates during a vibration test, the interface forces between shaker and test article can become artificially high, as the infinite impedance shaker continues to drive the resonating mechanical structure to the specification acceleration power spectral density level. To mitigate this problem, the input vibration specification can be notched at resonances or force limiting can be effected. Either way, the interface forces will be limited to more realistic levels, and an unnecessary overtest will be avoided.

Spacecraft-Level		Assembly-Level	
Frequency	**Level**	**Frequency**	**Level**
(Hz)		(Hz)	
20 - 45	+10 dB/octave	20 - 80	+6 dB/octave
45 - 600	0.06 g^2/Hz	80 - 1000	0.25 g^2/Hz
600 - 2000	6 dB/octave	1000 - 2000	-12 dB/octave
Overall	**7.7 grms**	**Overall**	**17.6 grms**

DURATION:
DESIGN: 3 MINUTES IN EACH OF 3 ORTHOGONAL AXES
PF TEST: 2 MINUTES IN EACH OF 3 ORTHOGONAL AXES
ACCEPTANCE SAME AS PF

Table A-4: Random vibration specifications.

Launch Random Vibration Tests are generally applied in each of three orthogonal axes, and have a gaussian distribution of the instantaneous acceleration. Both the Acceleration Spectral Density and wideband acceleration are test parameters and should be within specified tolerances. Each assembly or subsystem should be in its launch configuration. Powered-on vibration of MEMS support electronics, with attendant functional monitoring during testing, should be considered as an effective defect screening tool. All microelectromechanical systems or subsystems should be attached to vibration test fixtures at their normal flight structural interfaces.

Test Control accelerometers should be located at fixture-to-test article interfaces. When more than one control accelerometer is specified, the test should be controlled by averaging the accelerometer signals. Automatic, closed-loop servo control should always be implemented with an electrodynamic vibration exciter.

Vibration Instrumentation for microelectromechanical system testing should include appropriately located accelerometers and strain gages. The accelerometers, strain gages and data acquisition system should have flat frequency response characteristics within ± 1 dB from 5 Hz to 2 kHz. Visual data available on site during actual execution of the test should include paper oscillograph recordings of the time histories of the control and selected response channels. Additional quick-look analysis data in the form of Acceleration PSD plots should be available during testing as needed.

(5) Acoustic Noise

Acoustic noise results from the propagation of sound pressure waves through air or other media. During the launch of a rocket, such noise is generated by the release of high velocity engine exhaust gases, by the resonant motion of internal engine

components, and by the aerodynamic flow field associated with high speed vehicle movement through the atmosphere.

The fluctuating pressures associated with acoustic energy can cause vibration of structural components over a broad frequency band, ranging from about 20 Hz to 10,000 Hz and above. Such high frequency vibration can lead to rapid structural fatigue. Thus, the objective of a spacecraft acoustic noise requirement is to ensure structural integrity of the vehicle and its components in the vibroacoustic environment. A typical acoustic specification is provided in the figure below.

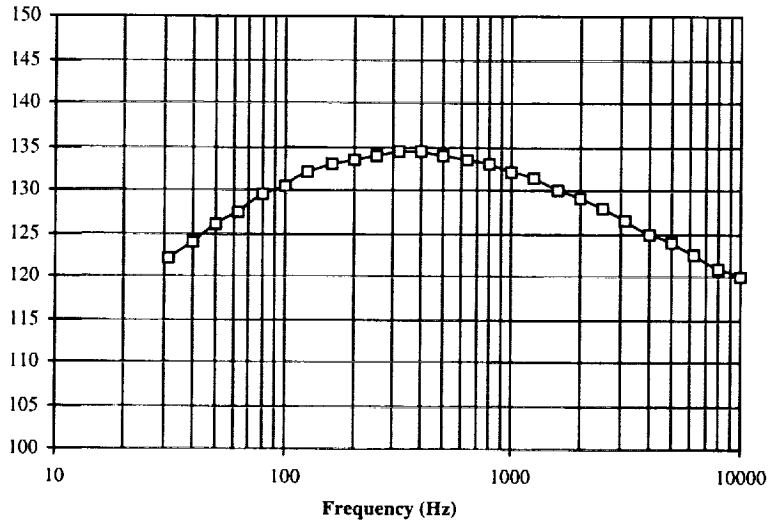

Figure A-7: Typical acoustic noise requirement.

Such a figure specifies the level of input sound pressure over the spectrum of frequencies at which the pressure can fluctuate. The pressure P is measured in decibels, defined as

$$dB = 20\log\left(\frac{P}{P_{ref}}\right)$$

where the reference pressure $P_{ref} = 2 \times 10^{-5}$ Pa is ostensibly the audible limit of the human ear.

The decibel pressure levels in acoustic noise spectra are not generally provided at each and every frequency. Instead, they are often specified over discreet bands of width Δf, which span 1/3 of a frequency octave. With this method, three sound pressure levels will be provided over any interval in which the frequency doubles. The table below is an example of such a 1/3 octave band specification, for the curve data above.

Acoustic Specification	
Center Frequency	**SPL (dB)**
31.5	122.0
40.0	124.0
50.0	126.0
63.0	127.5
80.0	129.5
100.0	130.5
125.0	132.0
160.0	133.0
200.0	133.5
250.0	134.0
315.0	134.5
400.0	134.5
500.0	134.0
630.0	133.5
800.0	133.0
1000.0	132.0
1250.0	131.5
1600.0	130.0
2000.0	129.0
2500.0	128.0
3150.0	126.5
4000.0	125.0
5000.0	124.0
6300.0	122.5
8000.0	121.0
10000.0	120.0

Table A-5: Acoustic specification table.

When pressure levels are defined with these methods, it is convenient to provide a measure of the overall acoustic noise intensity. The overall sound pressure level, or OASPL, provides just such a measure and, for 1/3 octave band specifications, can be calculated as the decibel equivalent of the root sum square, or RSS, pressure. The table below illustrates such a calculation for the data of the previous example, and shows that the OASPL is 144.9 dB. It should be noted that this OASPL exceeds any individual sound pressure level in the specification, because it represents an intensity of the spectrum as a whole.

Center Frequency	SPL (dB)	Pressure P (Pa)	Squared Pressure
31.5	122.0	25.2	633.9
40.0	124.0	31.7	1004.6
50.0	126.0	39.9	1592.2
63.0	127.5	47.4	2249.1
80.0	129.5	59.7	3564.5
100.0	130.5	67.0	4487.5
125.0	132.0	79.6	6338.7
160.0	133.0	89.3	7979.9
200.0	133.5	94.6	8953.6
250.0	134.0	100.2	10046.2
315.0	134.5	106.2	11272.0
400.0	134.5	106.2	11272.0
500.0	134.0	100.2	10046.2
630.0	133.5	94.6	8953.6
800.0	133.0	89.3	7979.9
1000.0	132.0	79.6	6338.7
1250.0	131.5	75.2	5649.4
1600.0	130.0	63.2	3999.4
2000.0	129.0	56.4	3176.9
2500.0	128.0	50.2	2523.5
3150.0	126.5	42.3	1786.5
4000.0	125.0	35.6	1264.7
5000.0	124.0	31.7	1004.6
6300.0	122.5	26.7	711.2
8000.0	121.0	22.4	503.5
10000.0	120.0	20.0	399.9
		RSS Pressure = 351.8 Pa	
		20 log(351.8/2E-5) = 144.9 dB	

Table A-6: Calculation of overall sound pressure level.

To quantify the acoustic environment, launch vehicles are often instrumented with internal microphones, which measure noise levels within the rocket fairing. This data is telemetered to the ground for processing, and ultimately plotted in the form of a sound pressure level versus frequency spectrum. Since the acoustic forcing function is stochastic, depending on many atmospheric and other variables, data from a number of such flights are generally gathered, and an envelope, such as that of the previous figure, is developed to encompass the historical record of microphone data.

This process can be extended and applied to data from a number of launch vehicles. If a launch platform has not yet been manifested for a particular payload, acoustic profiles from a number of candidate rockets can be enveloped, producing an aggressive specification which will ensure design adequacy for the spacecraft. The figure below reflects such a process, providing an envelope which encompasses the acoustic environments from three launch vehicles.

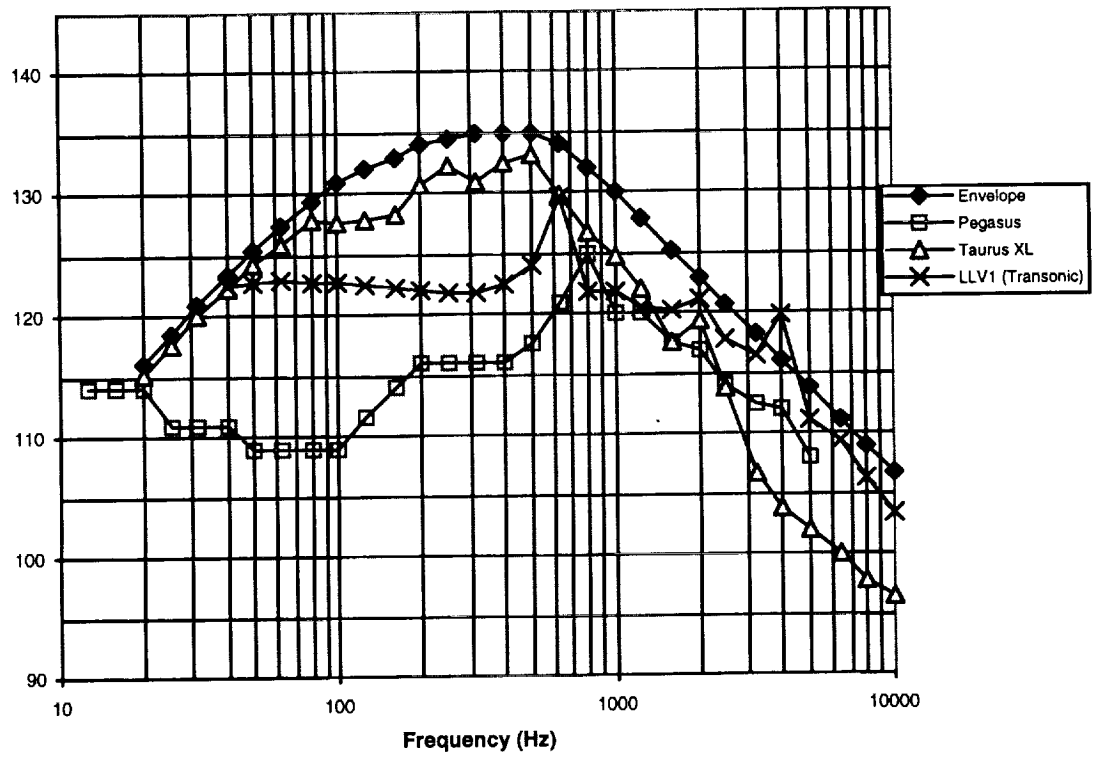

Figure A-8: Envelope of acoustic flight data.

The rationale for acoustic noise testing is straightforward, as acoustic energy is the primary source of vibration input to a space launch vehicle. During the initial phases of a rocket launch, high velocity gases are ejected from motor nozzles and reflected from the ground, creating turbulence in the surrounding air and inducing a vibratory response of the rocket structure. During the subsequent ascent phase of a launch, as the vehicle accelerates through the atmosphere to high velocity, aerodynamic turbulence induces pressure fluctuations which again cause structural vibration. These pressure fluctuations increase in severity as the vehicle approaches and passes through the speed of sound, due to the development and instability of local shock waves. The high-level acoustic noise environment continues during supersonic flight, generally until the maximum dynamic pressure, or max Q, condition is reached.

Acoustic energy gets transmitted to the mission payload in two ways. First, fluctuating pressures within the payload fairing impinge directly on exposed spacecraft surfaces, inducing vibration in high gain antennae, solar panels and other components having a large ratio of area-to-mass. Secondarily, the fluctuating external pressure field causes an oscillatory response of the rocket structure, which is ultimately transmitted through the spacecraft attachment ring in the form of random vibration. From the

spacecraft perspective, this random input is generally lowest at the launch vehicle attachment plane, and increases upward along the payload axis.

At the integrated spacecraft level acoustic noise is a primary source of vibration excitation. It should be included in virtually any space vehicle test program. At the subsystem level, however, and particularly in the context of space MEMS, acoustic testing is generally not conducted due to the obvious low ratio of area-to-mass exhibited by a microelectromechanical system.

The failure modes produced by acoustic noise excitation are generally identical to those associated with other types of vibratory structural fatigue. These include failures due to excessive displacement, in which one deflecting component makes contact with another, as well as fractured structural members and loose fasteners. Broken solder joints, cracked PC boards and wave guides can also occur. Electronic components whose function depends on the motion of structural parts, such as relays and pressure switches, are particularly susceptible.

Large flat panels are most easily influenced by, and therefore damaged by, acoustic energy, as they can undergo large displacements while oscillating at low frequency. For a typical spacecraft, this means that a fixed high gain antenna must be carefully designed and stiffened to avoid bending failures, debonding of composite members and related problems. In general, any structure with a high ratio of surface area to mass can be expected to experience potential problems in the acoustic noise environment.

Supporting data for acoustic noise design, analysis and testing can be found in the literature, as well as in various launch vehicle user manuals. The acoustic test has traditionally been severe, with the qualification environment generally established at 4 dB above the expected launch noise profile. The table below provides a sampling of problems detected during acoustic tests on several large programs.

Acoustic Test Problem/Failure History			
Program	**Year**	**Subsystem**	**Failure Mode**
Viking	1973	S/X Band Antenna	Cracked Epoxy
Viking	1973	S/X Band Antenna	Spacers Loosened
Viking	1973	S/X Band Antenna	Studs Loosened
Viking	1973	Infrared Mapper	Wire Shorted
Viking	1973	Radio Antenna	Screw Sheared
Voyager	1977	S/X Band Antenna	Magnetic Coil Debonded
Galileo	1983	Dust Detector	Sensor Cover Buckled
Mars Observer	1991	Telecom Subsystem	HGA Screws Backed Out
Mars Observer	1991	High Gain Antenna	HGA Struts Debonded
Mars Observer	1991	High Gain Antenna	Waveguide Broke
Topex	1992	Instrument Module	I/C Lead Wire Broke
Cassini	1995	High Gain Antenna	HGA Screws Backed Out
Cassini	1995	High Gain Antenna	HGA Struts Debonded

Table A-7: Acoustic test problem/failure history.

The testing has clearly identified improperly designed components. It is interesting to note that a majority of these problems have occurred in high gain antennas and related subsystems, which have the previously identified characteristics of large surface areas, low mass and bonded attachments.

Failure mode sensitivities and cost tradeoffs for the acoustic noise environment are illustrated in the table below. The primary test variables are acoustic noise input level, time duration for the test, frequency of noise input and whether or not power is on in the test article.

Each test parameter in an acoustic noise trial is generally a cost driver. This is primarily due to the fact that the test requires a large chamber, many support personnel and a significant amount of equipment.

Requirement	*Control Parameters*	*Failure Modes*	*Sensitivity to Increase*				*Cost*	
			dB	tdur	power	f		
Acoustic Noise	dB peak	intermittents	+	+	+	+	dB increase = more N2, etc.	+
	t duration	broken solder joints	+	+	0	-	t duration change	+
	power on	opens	+	+	0	+	power on = extra equipt	+
	frequency	shorts	+	+	0	+	f increase = better modulator	+
		broken connectors	+	+	0	-		
		broken wave guides	+	+	0	-		
		broken crystals	+	+	0	+		
		cracked diodes	+	+	0	+		
		relay chatter	+	+	+	+		
		fastener loosening	+	+	0	+		
		potentiometer slippage	+	+	0	+		

Table A-8: Control parameter sensitivity and cost.

Due to their typically low ratios of area to mass, space MEMS do not require independent testing in the acoustic environment. Instead, such devices are usually subjected only to random vibration, shock and possibly sine testing, with acoustic qualification deferred to the spacecraft level. Nonetheless, the acoustic environment drives many related dynamic specifications, and the informed reader should have some knowledge of common acoustic requirements.

The acoustic noise environment for a typical spacecraft and subassemblies is a reverberant random-incident acoustic field specified in 1/3 octave bands. The cumulative test duration should be no less than 1 minute in any acoustic trial, of which a minimum 35 seconds must be contiguous.

All test items should be in their launch/ascent mechanical and electrical configuration and should be suspended or otherwise positioned within the acoustic chamber such that no major surfaces are parallel to the chamber walls, floor or ceiling, with a minimum of 0.6 m (2 ft) of clearance from any chamber surface. A functional test should be performed before and after the acoustic trial to verify operational performance. Tolerances for SPLs should be as delineated in the table. The OASPL should be controlled to within ±1dB (true RMS) of the specification nominal.

The test should be controlled so that the square root of the average mean-square sound pressure at several locations surrounding the test object meets the test levels specified in the table, in 1/3 octave bands centered on the specified frequency. Test time should commence when the overall control SPL is raised to within 1 dB of that required and should terminate when the level is reduced to more than 1 dB below that required. The control microphone locations should be 12-18 inches from major exterior surfaces of the assembly or subsystem. The control microphones and their data acquisition systems should have flat frequency response characteristics within ± 1 dB from 30Hz to 10 kHz.

Frequency (Hz)	F.A. SPL (dB ref 20 μPa)	Qual SPL (dB ref 20 μPa)	Tolerance (dB)
31.5	129.0	132.0	+6, -3
40	131.0	134.0	+5, -3
50	132.5	135.5	+5, -3
63	134.0	137.0	+5, -3
80	135.0	138.0	+4, -3
100	135.5	138.5	±3
125	136.0	139.0	±3
160	136.0	139.0	±3
200	135.5	138.5	±3
250	135.3	138.3	±3
315	135.0	138.0	±3
400	134.0	137.0	±3
500	132.0	135.0	±3
630	130.5	133.5	±3
800	129.0	132.0	±3
1000	126.5	129.5	±3
1250	125.0	128.0	±3
1600	123.0	126.0	±3
2000	121.0	124.0	±3
2500	119.0	122.0	±3
3200	117.0	120.0	±3
4000	115.0	118.0	±3
5000	113.0	116.0	±3
6400	111.0	114.0	±3
8000	109.0	112.0	±3
10000	107.0	110.0	±3
OASPL	***145.8***	***148.8***	***±1***

Table A-9: Acoustic noise spectra.

The tested assembly or subsystem should be appropriately instrumented with response accelerometers. The accelerometers, in turn, should have flat frequency response characteristics within ±1 dB from 5 Hz to 2 kHz, as should associated data acquisition electronics.

(6) Pyrotechnic Shock

Pyrotechnic Shock is a design and test condition under which flight hardware is subjected to a rapid transfer of energy. The energy transfer is associated with the firing of an explosive device, usually for the purpose of initiating or performing a mechanical action. Spacecraft separation events or the release of propulsion system safing devices are typical such mechanical actions.

A typical pyrotechnic shock requirement is illustrated in the figure below.

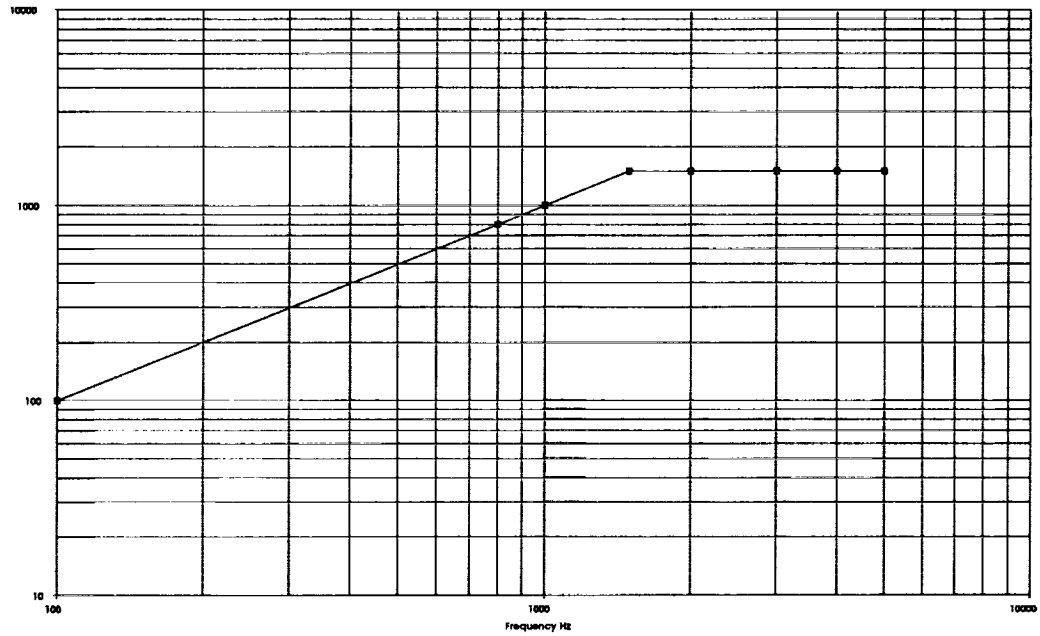

Figure A-9: Typical pyrotechnic shock requirement.

Another possible pyrotechnic shock environment requirement is presented in the following figure. The shock input is applied at the assembly mounting points in each of 3 orthogonal axes.

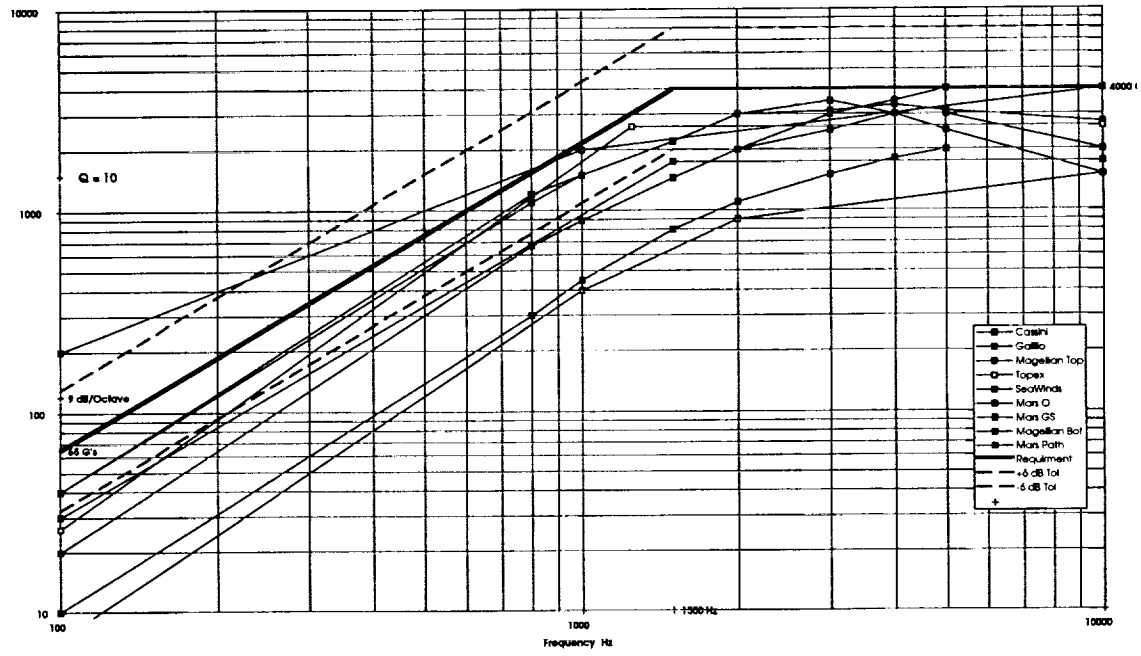

Figure A-10: Subassembly pyrotechnic shock design requirement.

This spectrum represents a 2σ environmental level. It is intended to encompass 95% of all expected shock environments for all available launch vehicles. For reference, shock levels from a number of previous programs are also indicated in the figure.

For test purposes, this environment should be considered a qualification level. Equipment should be exposed to the shock spectrum 3 times in each axis. For devices with self-contained ordinance, 3 self-induced shocks should also be applied.

The release of energy from an ordnance-containing device and the subsequent transfer to the surrounding structure represents a very complex event. As a result, it is difficult to describe the actual shape of the applied shock wave; it is generally not a simple time-based pulse such as a square or triangular wave. The figure below illustrates a typical acceleration versus time trace from an actual pyrotechnic shock event.

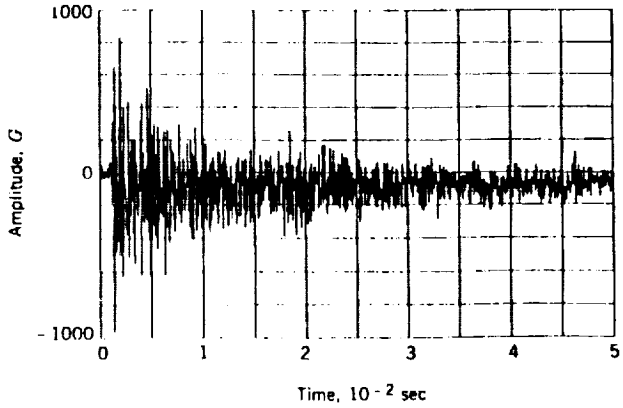

Figure A-11: Pyro shock acceleration time history.

Thus, in establishing a pyro shock requirement, no attempt is made to describe the input pulse, but the frequency-domain response of the structure subjected to the pulse is described instead. The figure below illustrates a typical measurement of this response.

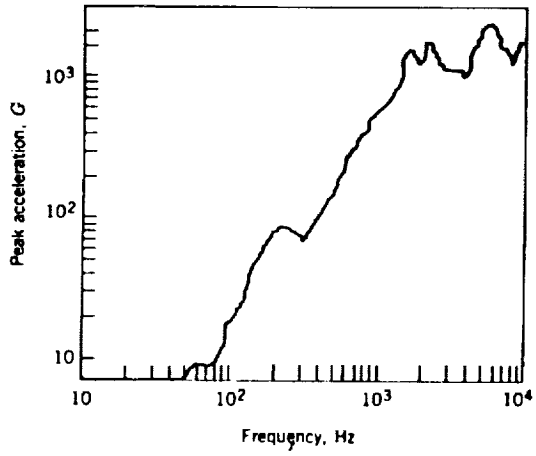

Figure A-12: Frequency response to pyro shock.

The failure modes produced by shock excitation can be broadly grouped into four categories. First are those failures associated with high stresses, such as buckling of long and slender structures, plastic deformation of structures or fracture in brittle components. Next are failures due to high acceleration levels, which can cause relays to chatter, potentiometers to slip and bolts to loosen. Third are problems associated with excessive displacement, which include broken solder joints, cracked PC boards and wave guides, or general problems associated with the impact of one structural component into another. The final category consists of transient electrical malfunctions, which occur only during application of the shock environment. Such malfunctions occur in capacitors, crystal

oscillators and hybrids, the latter of which can temporarily short circuit during a shock event due to contact between the device package and internal die bond wires.

Many studies regarding the effects of pyrotechnic shock have been conducted during the life span of the aerospace industry, but one of the best is perhaps that of Moening.[73] Conducted by the Aerospace Corporation under contract to the Air Force Systems Command Space Division, the study examined and summarized ordnance-related shock failures over a period spanning some 20 years, dating from the first missile-related pyro shock failures in the early 1960s to about 1982 when the study was concluded. A total of 85 flight failure events are summarized in the paper, reflecting events ranging from relay chatter, broken electrical wires and leads, cracked glass diodes or fracture of brittle ceramic components and a number of others.

Failure mode sensitivities and cost tradeoffs for the pyrotechnic shock environment need to be discussed in the context of a particular test technique. The three principal methods for shock testing include shaker synthesis, resonant plate testing and actual firing of pyro devices.

In the shaker synthesis technique, the article to be shock tested is mounted to an electrodynamic vibration shaker using an appropriate fixture. A function generator is connected to the shaker, and a series of complex sinusoids or similar time-based pulses are input to the test article in an attempt to generate the desired frequency response spectrum.

Generally, this is a trouble-prone and ineffective exercise because, as stated above, a pyro shock pulse rarely manifests itself as a simple function. Furthermore, the shaker synthesis technique tends to input excessive energy to the structure at low frequencies and insufficient energy at high frequencies. As a result, hardware subjected to such tests is often overtested in the low frequency regime and undertested elsewhere.

In an attempt to improve upon the synthesis method, many environmental test engineers have attempted to modify the input to the shaker using chirp techniques. In this case, output from the function generator is passed through a graphic equalizer before being routed to the shaker. The shaker input spectrum is then tuned through an increase in the gain of high frequency signals, and through an attendant gain reduction at low frequencies. Unfortunately, such efforts offer marginal improvements at best, due to the inherent low-pass filter characteristics of a mechanical shaker.

In the resonant plate technique, advantage is taken of the fact that a stiff, free metal plate can exhibit very high frequency resonances. The article to be tested is mounted to an aluminum or steel plate, and the plate is subsequently suspended in mid-air. A metal pendulum is then swung into contact with the plate, inducing transient vibration. If the frequency response of the mounted test article is measured with an accelerometer, a plot such as that illustrated in the figure below can result.

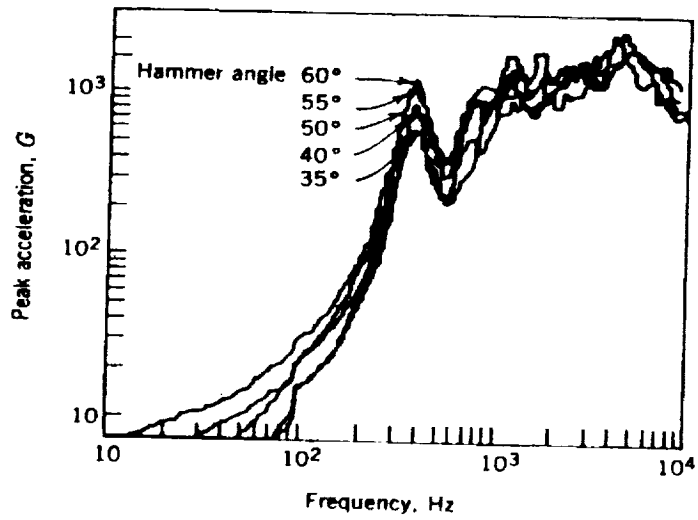

Figure A-13: Response spectrum in resonant plate test.

The Mechanical Impulse Pyro Shock, or MIPS, simulator is a test device which encapsulates the basic resonant plate shock test parameters in a single, relatively compact machine. In a MIPS simulator, an aluminum plate is fabricated and allowed to rest on a foam or plywood pad. The plate is then excited into resonance by the impact of a pneumatic actuator on a moveable bridge.

Shape of the resulting shock pulse is tailorable with a MIPS simulator, by way of experimentation. Dimensions of the resonant plate, the strike location of the hammer and the hammer actuation pressure all affect the resulting shock response spectrum. Interchangeable impactor heads, fabricated from lead, aluminum or steel, are used to alter the duration of the applied pulse.

The MIPS table produces a high fidelity simulation of a pyrotechnic event, in that it generates substantial energy at high frequency in an extremely repeatable manner. The figure below illustrates the basics of MIPS table construction.

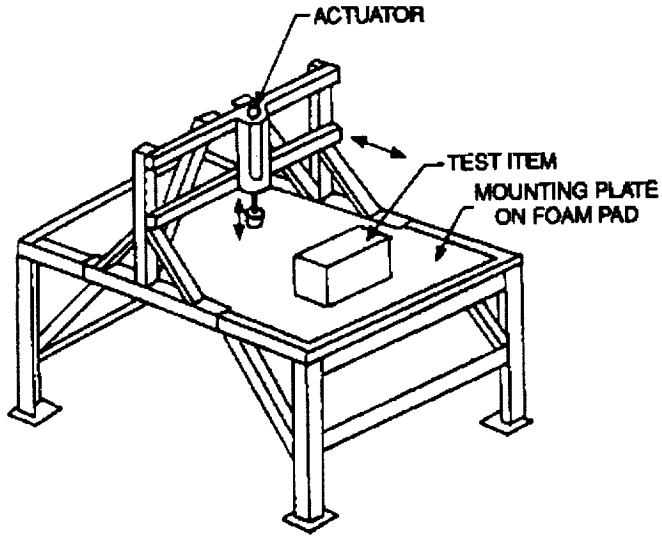

Figure A-14: Mechanical impulse pyro shock simulator.

Although resonant plate techniques can produce a response exhibiting the desired trend of increasing acceleration with increasing frequency, they are still less than ideal. Tuning of the response spectrum such that the correct accelerations occur at the desired frequencies is difficult, involving modification of the plate thickness, shape or suspension method, or modification of hammer characteristics. These activities are time consuming and generally based on trial and error, and do not guarantee generation of the correct response spectrum.

The best pyrotechnic shock test method, then, is one which utilizes pyrotechnic devices. Due to safety, facility and related requirements, this can be an expensive proposition. However, considering the time that might otherwise be wasted during the construct of a simulation, and considering the potential for overdesign or underdesign of hardware which could occur if the simulation is inaccurate, the pyro method may in fact be a bargain. It should be utilized if at all possible.

Armed with our vast knowledge of the primary shock testing methods, we can now present appropriate test control parameters, the sensitivity of failure modes to changes in these parameters, and cost tradeoffs associated with each. The table below provides a summary matrix of this information.

Control Parameters	Failure Modes	Sensitivity to Increase				Cost	
		g	tdur	trise	f	Shaker Synthesis Method	
g peak	intermittents	+	-	-	0	g increase = bigger shaker	+
t duration	broken solder joints	+	+	+	-	t duration change	0
t rise	opens	+	-	-	+	t rise redct = better fct gen	+
frequency	shorts	+	-	-	+	f increase = chirp test eqpt	+
	broken connectors	+	-	+	-		
	broken wave guides	+	-	+	-	Resonant Plate Method	
	broken crystals	+	-	-	+	g incr = plate/pendlm change	+
	cracked diodes	+	-	-	+	t duration change	0
	relay chatter	+	-	-	+	t rise reduction	0
	fastener loosening	+	-	-	+	f incr = plate/pendlm change	+
	potentiometer slippage	+	-	-	+		
						Pyro Device Method	
						g incr = charge change	+
						t duration change	0
						t rise reduction	0
						f increase	0

Table A-10: Control parameter sensitivity and cost.

Recommended Shock Test

Space microelectromechanical systems and related hardware should be tested to the shock spectrum (Q=10) provided in the table below, and plotted in the accompanying figure.

FREQUENCY (Hz)	ACCEPTANCE (G PK)	PROTOFLIGHT (G PK)
100	40	60
100-1500	9.2 dB per Octave	9.2 dB per Octave
10000	2500	3750

Table A-11: Shock response spectrum (Q=10).

The input shock pulse time history, applied to the base of the test item, should be oscillatory in nature and should decay to less than 10% of its peak value within 50 milliseconds. The spectrum shape should be controlled to within +6/-3 dB, and should be applied in each of three (3) orthogonal axes. At least 30% of spectrum amplitudes should exceed the nominal test specification. Components which are powered-on during spacecraft separation should be shock tested in the powered-on state.

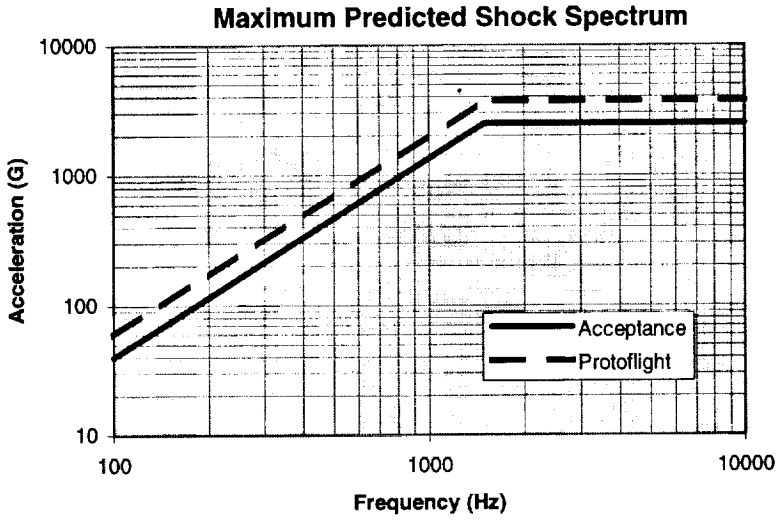

Figure A-15: Shock spectrum.

While dynamics testing is an integral part of preparing MEMS for the space environment, there are a number of other commonly used packaged parts screens as well.

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This guide is a reference for understanding the various aspects of microelectromechanical systems, or MEMS, with an emphasis on device reliability. Material properties, failure mechanisms, processing techniques, device structures, and packaging techniques common to MEMS are addressed in detail. Design and qualification methodologies provide the reader with the means to develop suitable qualification plans for the insertion of MEMS into the space environment.

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