

DEVELOPMENT OF THICK-FILM THERMOELECTRIC MICROCOOLERS USING ELECTROCHEMICAL DEPOSITION

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ABSTRACT

Advanced thermoelectric microdevices integrated into thermal management packages and low power, electrical source systems are of interest for a variety of space and terrestrial applications. By shrinking the size of the thermoelements, or legs, of these devices, it becomes possible to handle much higher heat fluxes, as well as operate at much lower currents and higher voltages that are more compatible with electronic components. The miniaturization of state-of-the-art thermoelectric module technology based on Bi_2Te_3 alloys is limited due to mechanical and manufacturing constraints for both leg dimensions (100-200 μm thick minimum) and the number of legs (100-200 legs maximum). We are investigating the development of novel microdevices combining high thermal conductivity substrate materials such as diamond, thin film metallization and patterning technology, and electrochemical deposition of thick thermoelectric films. It is anticipated that thermoelectric microcoolers with thousands of thermocouples and capable of pumping more than 200 W/cm^2 over a 30 to 60 K temperature difference can be fabricated. In this paper, we report on our progress in developing an electrochemical deposition process for obtaining 10-50 μm thick films of Bi_2Te_3 and its solid solutions. Results presented here indicate that good quality n-type Bi_2Te_3 , n-type $\text{Bi}_2\text{Te}_{2.95}\text{Se}_{0.05}$ and p-type $\text{Bi}_{0.5}\text{Sb}_{1.5}\text{Te}_3$ thick films can be deposited by this technique. Some details about the fabrication of the miniature thermoelements are also described.

INTRODUCTION

The drive for increased performance and miniaturization of a wide range of electronic systems requires higher power levels and higher packaging densities. However, thermal management problems are rapidly becoming a major issue for this technological process because they limit the degree of integration of devices and components [1]. In addition to reliability issues, significant performance improvement can be obtained by operating the active junction of semiconductor chips at temperatures near or lower than ambient, as well as by maintaining precise temperature control. This is especially true of several electronic and photonic devices such as microprocessors, power amplifiers and infrared lasers [2, 3]. For example, next generation SiC/GaN solid state power amplifiers used for microwave applications will have much higher power levels, with thermal power dissipation requirements increasing from 5 W to over 20 W within the same spatial region. That increase will multiply the heat flux that has to be removed from the back of the die from approximately 30 W/cm^2 to several hundreds W/cm^2 . This major thermal management problem must be addressed using novel cooling techniques and designs fully integrated with electronic components [4]. The very high heat flux densities in the immediate vicinity of the GaN active layers lead to an estimated 75-110°C temperature difference with respect to the back of the SiC substrate. It is thus imperative to offset this large temperature gradient between active layer and heat sink by using active cooling techniques.

The specific problem of spot cooling of electronic devices can be very effectively solved by using thermoelectric cooling combined with a complementary thermal management technique. For small thermal loads, high thermal conductivity materials can be used for conducting heat away to the heat sink, while for large thermal loads (high heat flux density), highly efficient heat removal techniques such as heat pipes, microchannels or spray cooling would be incorporated into the package [5-7]. Miniaturization of thermoelectric coolers offers several distinct advantages over current state-of-the-art technology that is established on bulk semiconducting materials. One obvious advantage is that for a given module configuration, the cooling power per unit area of thermoelectric coolers is inversely proportional to the thickness of its thermoelements, or legs. "Bulk" coolers are ill suited to further integration with electronic devices and components since they are typically much larger than the active region of the devices, both in cross-sectional area (typically over 1 cm^2) and thickness (thermoelements usually 1mm thick or higher). In addition, even the smallest coolers now commercially available [8-10] are limited in number of legs, (usually less than 200 legs) due to both thermo-mechanical restrictions and the often painstaking semi-manual assembly techniques, severely curbing the range of operating current and voltage. On the other hand, microcoolers could be manufactured using thin film deposition and integrated circuit techniques compatible with electronic device fabrication, and could literally have thousands of miniature legs interconnected in a variety of ways to provide operating voltage and current flexibility. Moreover, the response time of such microcoolers would be dramatically shortened and could prove to be compatible with transient operation of selected electronics [11]. In this paper, we report on progress made in studying critical issues and developing techniques associated with the fabrication of microcoolers.

ELECTRODEPOSITION OF THICK THERMOELECTRIC FILMS

Electrodeposition From Aqueous Solutions

Thick films (10-100 μm) can be difficult and time consuming to make using vacuum techniques such as sputtering or evaporation. In addition, some of these deposition techniques require quite elevated temperature that may not be easily compatible with microdevice fabrication processes [12]. An attractive route is a room temperature electrochemical process from aqueous solution. This is a very well known technique for the deposition of many metals and metallic alloys [13] but its application to semiconductors has been much more limited. However, there is an abundant literature on electrochemical deposition (ECD) of II-VI semiconductors such as CdSe, CdTe, $\text{CdSe}_{0.5}\text{Te}_{0.5}$ and $\text{CdSe}_{0.65}\text{Te}_{0.35}$ [14,15]. In this technique the elements are deposited on an electrode using an aqueous solution of anions or anionic compounds. ECD constitutes an inexpensive way to synthesize semiconducting films and, depending on the current density used in deposition, the deposition rate can be varied widely, up to several tens of microns per hour. In addition, slight variations in the deposition potential or solution concentration may possibly be used to induce off-stoichiometric films, thus providing p- or n-type doping through stoichiometric deviation. The electrodeposition of thermoelectric materials has not been widely investigated [16, 17] and new experimental methods must be developed to obtain p-type and n-type $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_{3-y}\text{Se}_y$ compositions which are optimal for thermoelectric cooling applications near room temperature. An additional advantage of ECD is that some of the interconnect layers necessary to the fabrication of these devices, such as Cu for the electrical path or Ni or Pt for the Cu diffusion barrier can also be deposited by using different aqueous solutions.

All experiments were run at room temperature using standard electrochemistry techniques: a three electrode cell with open beaker configuration but with separate vessels for the reference

electrode (saturated calomel electrode, SCE) and the counter/working electrodes. A salt bridge was used to electrically connect the two beakers. The counter electrode consisted of a fine Pt mesh while metallic foils or metallized high thermal conductivity substrates such as diamond, AlN or Si/SiO₂ were used for a working electrode. Solutions contained dissolved high purity elements (Bi, Sb, Te, Se) into an acidic aqueous medium, typically HNO₃ and deionized water (pH ~ 0). Concentration of the elements in the electrolyte was varied between 0.0001 and 0.01 M. In the case of Sb, a chelating agent must be added to prevent the spontaneous precipitation of an insoluble oxide compound and raise its maximum solubility (about 0.0008 M in 1 M HNO₃ aqueous solution). Both the electrodeposition and cyclic voltammetry measurements were carried out using mechanical solution stirring and a computer-controlled EG&G Princeton Potentiostat/Galvanostat 273A. The thickness of the films was measured using a Dektak profilometer and in some cases a scanning electron microscope. The atomic composition and the crystallographic orientation of the films were obtained using a Siemens D-500 x-ray diffractometer and a JEOL JXA-733 electron superprobe, respectively. Measurements of the electrical transport properties have been conducted in a 100-400K temperature range on some films. Van der Pauw electrical resistivity and Hall effect were measured in the plane of the deposited films (after removal from the metallized substrates), and the Seebeck coefficient was measured in a cross-plane direction using a simple differential thermocouple setup

Electrodeposition of Bi₂Te₃ Alloy Films

Bismuth and tellurium metals dissolve in HNO₃ to make the oxide cations BiO⁺ and HTeO₂⁺. Bi₂Te₃ is insoluble in dilute HNO₃, so reduction of HTeO₂⁺ to Te²⁻ at an electrode will result in the precipitation of Bi₂Te₃ on the electrode surface. The overall reaction for the process is:

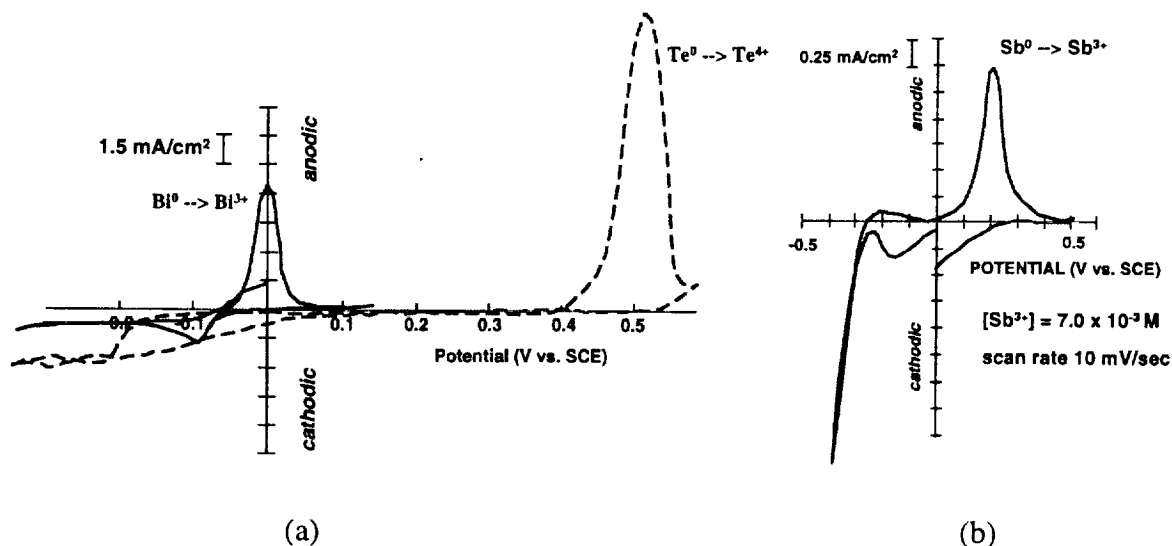


Figure 1: Current-Voltage graph for the electrochemical deposition of Bi, Te (a) and Sb (b) on a Pt substrate using a nitrate aqueous solution. The oxidation waves for Bi, Te and Sb can be seen for voltages of 0, 0.5 and 0.2 V respectively.

The combined current-voltage behavior of aqueous solutions of 7×10^{-3} M BiO⁺ and 1.0×10^{-2} M HTeO₂⁺ in 1 M HNO₃ is plotted in figure 1(a) and shows that the reduction regions for each of these compounds overlies each other in the range -50 to -200 mV versus SCE. BiO⁺ is reduced to

Bi^0 around -100 mV (not the operative mechanism for Bi and Te co-deposition). It is possible to obtain Bi_2Te_3 within this voltage range, probably most effectively in the range -5 to -75 mV than within the region of the reduction wave for BiO^+ . Ternary $\text{Bi}_2\text{Te}_{3-x}\text{Se}_x$ alloy films can also be obtained by adding Se to the dilute HNO_3 solution and by controlling the $[\text{Te}]/[\text{Se}]$ molar concentration ratio. Figure 1(b) plots the voltammogram for Sb ($[\text{Sb}] = 0.7 \times 10^{-3}$ M) in a pH = 0 aqueous solution. It can be seen that low cathodic current densities are obtained even at relatively large negative voltages (-100 mV and higher). It also shows that there is a rapid increase in current as voltage becomes more negative from 0 to -150 mV, indicating that it will be quite difficult to deposit Sb-rich $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$ films at lower voltages typically used for Bi_2Te_3 or $\text{Bi}_2\text{Te}_{3-x}\text{Se}_x$ films (-10 to -25 mV).

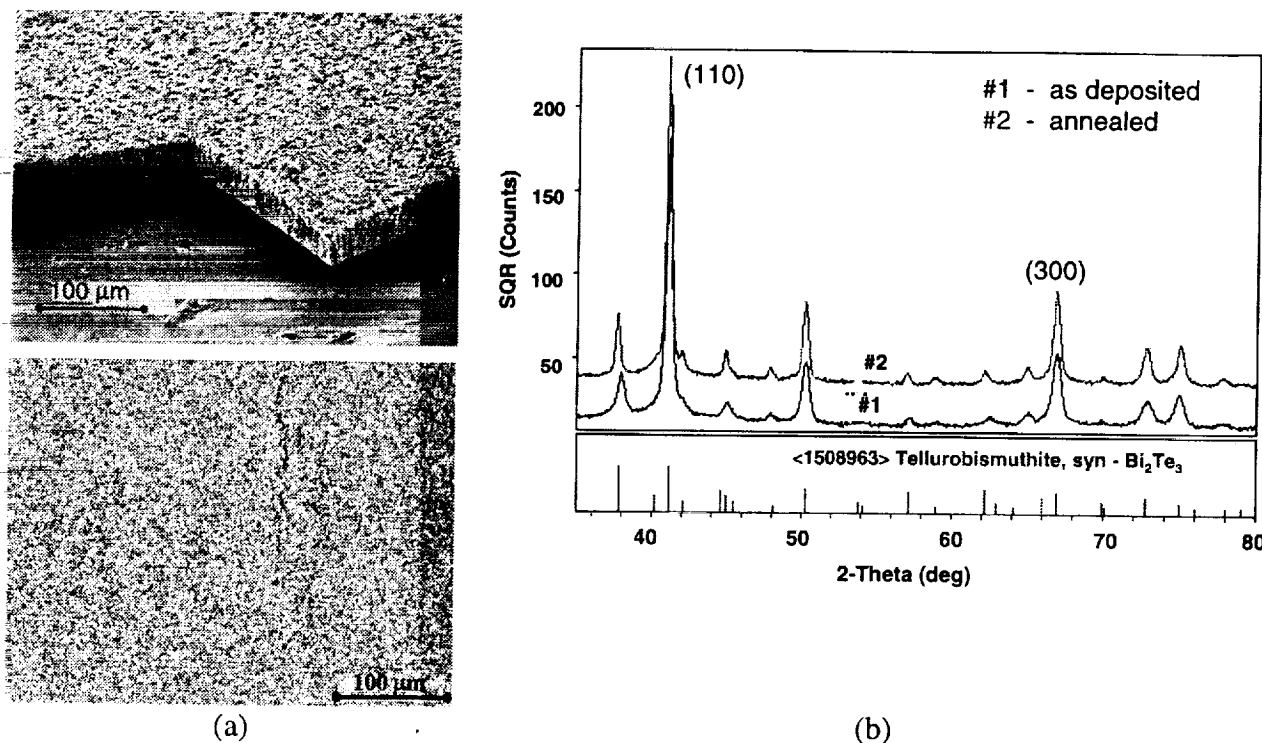


Figure 2: (a) Micrographs of 40 μm thick Bi_2Te_3 thick films: film lifted off its metallized silicon substrate (top, notice vertical cleavage planes) and film grown by pulsed deposition (bottom); (b) X-ray diffraction pattern for Bi_2Te_3 films, as-deposited and after a $200^\circ\text{C}/4$ hours anneal.

In addition to the deposition voltage, other parameters controlling the quality, composition and properties of the Bi_2Te_3 alloy films grown by ECD are: bath temperature, Bi, Te and Se molar concentrations in the HNO_3 solution, deposition time, substrate surface finish and geometry, convective diffusion in the bath (stirring), depletion rate of $[\text{Bi}]$ and $[\text{Te}]$ in the bath (volume), and current distribution between counter and deposition electrodes (distance and symmetry). Electrodeposition on Pt-coated substrates have shown that thick near-stoichiometric Bi_2Te_3 films could be grown from a 0.008 M $[\text{Bi}]$ and 0.01 M $[\text{Te}]$ solution. The thickness of the films ranged from 10 to 60 μm and the composition of the films was very close to the 40/60 at% ratio. In addition, back-scattering and secondary electron analysis indicated that films grown at low deposition voltages had relatively smooth top surfaces (about 1 μm of roughness). Even better results can be obtained through pulse deposition alternating growth and etch sequences (roughness of less than 100 nm). These results are illustrated in Figure 2(a). The growth rates ranged from 10 to 20 $\mu\text{m}/\text{hour}$ depending on the deposition voltage. The crystal orientation of

the films is very reproducible regardless of the substrate used, and x-ray diffraction data (Figure 2(b)) show that the c axis of the Bi_2Te_3 hexagonal unit cell is located in the plane of the film. This is a particularly important result, similar to previous reports for deposition on stainless steel substrates [17], since it means that the Bi_2Te_3 cleavage planes are perpendicular to the film surface. This is precisely the desired orientation considering the well-known transport property anisotropy of bulk Bi_2Te_3 and our vertically integrated module configuration.

Sb_2Te_3 -rich $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$ compositions are best for p-type thermoelements. Such alloys can also be obtained in electrodeposited films by controlling the $[\text{Sb}]/[\text{Bi}]$ ratio in the electrolyte while maintaining a constant $[\text{Te}]/([\text{Bi}]+[\text{Sb}])$ ratio, as shown in Figure 3(a). However, if no chelating agent is used, only low $[\text{Sb}]$ concentrations (up to 0.0008 M) and relatively high voltages (-120 mV and more negative values) can be used. This is illustrated in Figure 3(b) for such low $[\text{Sb}]$ concentrations where the atomic film composition (1.5 is stoichiometric) is plotted as a function of the deposition voltage for a constant $[\text{Te}]/([\text{Bi}]+[\text{Sb}])$ ratio in the electrolyte. At less negative voltages, Bi and especially Te deposition tend to dominate the process and off-stoichiometric films are obtained. Negative deposition voltages in excess of -100mV result in stoichiometric film compositions ($\text{Bi}_{0.4}\text{Sb}_{1.6}\text{Te}_3$) but with high porosity, dendritic-like structure. In addition growth rates are much smaller than achieved for Bi_2Te_3 , typically on the order of 1 $\mu\text{m}/\text{hour}$. Less negative voltages (-80mV or less) result in much improved morphology and higher deposition rates but require substantially increased $[\text{Sb}]$ electrolyte concentrations.

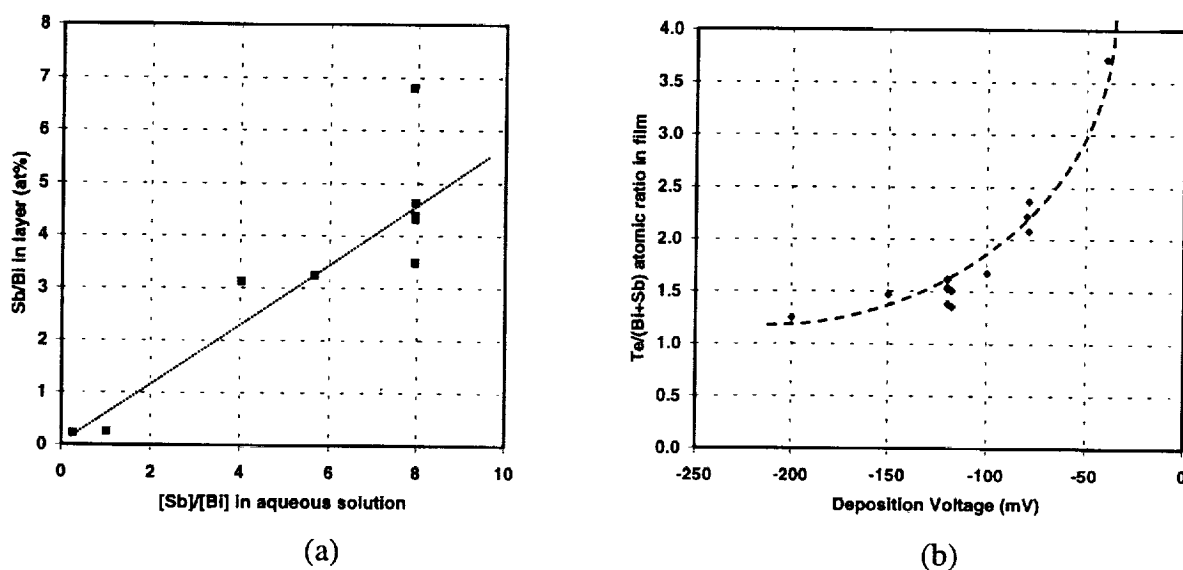


Figure 3: (a) Change in composition in stoichiometric $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$ films as a function of the aqueous $[\text{Sb}]/[\text{Bi}]$ ratio and (b) increase in Te content for film composition when depositing at less negative voltages (vs. SCE) but using same starting aqueous concentrations.

Transport property measurements on as-deposited Bi_2Te_3 films show heavily doped n-type behavior, similarly to results obtained previously [16] except for lower electron concentrations ($\sim 1 \times 10^{20} \text{ cm}^{-3}$) and higher Hall mobility values ($\sim 26 \text{ cm}^2/\text{Vs}$). Seebeck coefficient values range from -40 $\mu\text{V}/\text{K}$ to over -60 $\mu\text{V}/\text{K}$ near room temperature. However, one needs to take into account the anisotropy of the transport properties since a typical value of $10^{-5} \Omega\text{m}$ for the electrical resistivity is obtained for the in-plane direction. Values in the out-of-plane direction (through the film thickness) are expected to be about four times lower, based on data reported for bulk Bi_2Te_3 . Heat-treatments carried out under inert atmosphere at 200 to 300°C for a few hours result in much improved electrical properties due to an anneal of structural defects and reduction

in doping levels to the 10^{19} cm^{-3} range. This can be seen in Figure 4(a) plotting the temperature dependence of the in-plane electrical resistivity and Hall mobility for as-deposited and annealed samples. Seebeck values increase up to $-200 \text{ } \mu\text{V/K}$ at 300K, indicating that the film properties become quite similar to those of optimized n-type Bi_2Te_3 bulk samples. For p-type films, the only transport property measured so far is the Seebeck coefficient in a direction perpendicular to the plane of the film. For near stoichiometric $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$ films, values range from $+40$ to $+300 \text{ } \mu\text{V/K}$ depending on the Bi/Sb atomic ratio and a slight excess in Te content. The largest values are obtained for compositions that are slightly Te-rich. Some of our results are presented in Figure 4(b) for films grown from three different electrolytes with a constant $[\text{Bi}]/[\text{Sb}]$ ratio but increasing $[\text{Te}]$ concentration, and as a function of the deposition voltage. It has also been found that n-type stoichiometric ternary $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$ films could be prepared for $x < 1.0$.

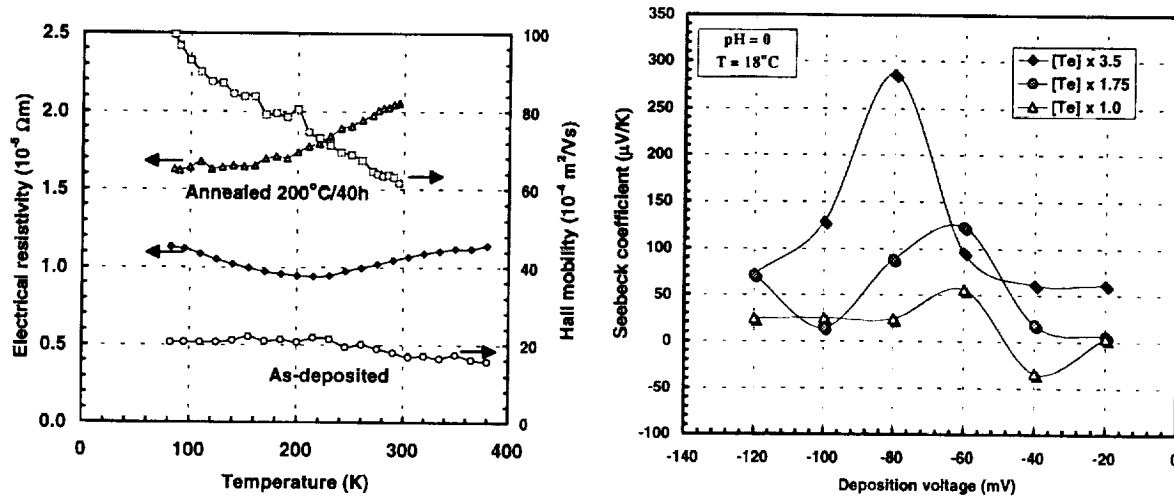


Figure 4: (a) In-plane electrical resistivity, Hall mobility as a function of temperature measured for a $30 \text{ } \mu\text{m}$ thick Bi_2Te_3 film, as-deposited and after a $200^\circ\text{C}/40\text{h}$ anneal in an inert atmosphere; (b) Seebeck coefficient as a function of deposition voltage for $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$ films using electrolytes with high Sb concentrations.

THERMOELECTRIC MICRODEVICE FABRICATION

Special Considerations for Heat Transfer and Electrical interconnects

By selecting a vertically integrated thermoelectric module configuration compared to a planar thin film configuration, device performance is not degraded significantly due to heat losses through the supporting substrate [11, 18]. However, with short legs and high heat flux values, the performance of microcoolers is much more sensitive to electrical and thermal contact resistances than that of bulk devices. For resolving the thermal issues, the use of substrates such as AlN or diamond (thermal conductivity respectively one and two orders of magnitude higher than alumina) is necessary so that as small a ΔT as possible is dropped across the substrate due to its thickness and cross-sectional area (heat spreading). For miniaturized devices comprised of thousands of legs, electrical contact resistances can become a very large fraction of the total internal resistance. Low contact resistances ($10^{-6} \text{ } \Omega\text{.cm}^2$ or lower) can relatively easily be obtained using thin film processing techniques developed for integrated circuit technology [19]. The development of thermally stable metallizations for high thermal conductivity substrates such as diamond, AlN or thermally oxidized Si [19] as well as effective diffusion barrier materials

based on amorphous transition metal-silicon nitride layers [20] was recently completed. In addition to thermal and electrical contact resistances, other issues such as heat losses, mechanical strength and stress analysis must be considered. These issues will be developed in a later report.

Fabrication of Thermoelectric Legs

It has been determined that to be able to “shape” the thick legs, electrodeposition should be conducted in an equally thick template. Experiments demonstrated that electrodeposits would rapidly cover the entire surface of the template once they grew out of their patterned “hole”. This template is prepared by depositing a thick photoresist layer and then, using conventional UV photolithography equipment, by etching square or round shaped patterns into it for leg deposition. Cylindrically shaped patterns etched into photoresist up to 65 μm thick deposited on top of a metallized silicon substrate have been successfully obtained. Micrographs in Figure 6 show part of arrays composed of thousands of Bi_2Te_3 legs covering a few mm^2 area that were electrodeposited using such a photoresist template.

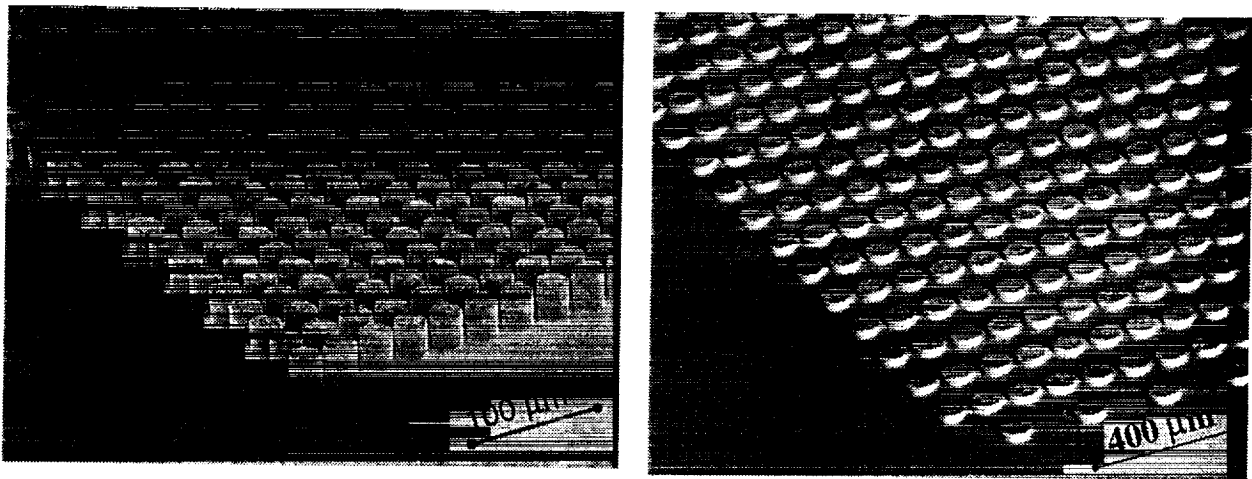


Figure 7: Micrographs showing Bi_2Te_3 legs obtained using electrochemical deposition techniques into thick photoresist templates on fully metallized Si substrates. Micrograph (a) is illustrative of a typical device configuration for power generation applications with an array of 10,000 legs with dimensions of 20 μm in diameter and 50 μm tall; the 70 μm in diameter and 20 μm tall 2500 leg array in micrograph (b) is based on specific cooling applications

CONCLUSION

Thermoelectric microdevices can contribute to solving thermal management issues related to the rapid development of high power, high density electronic components and devices. Low power electrical sources for remote or unattended electronics also offer attractive possibilities. To fabricate such microdevices in a “classic” vertically integrated module configuration, a combination of electrochemical deposition techniques and integrated circuit technology is now under development. It has been shown that both n-type and p-type thick Bi_2Te_3 alloy films (10-60 μm thick) could be synthesized with transport properties similar to that of bulk materials. We are currently focusing on improving the deposition conditions of thick p-type $\text{Bi}_{2-x}\text{Sb}_x\text{Te}_3$ films. We have developed thermally stable metallizations to high thermal conductivity substrates and effective diffusion barriers for fabricating the electrical interconnects between the n- and p-type legs. Thick photoresist templates up to 65 μm have been successfully developed and patterned using conventional UV photolithography, resulting in the reproducible fabrication of closely

packed arrays of thousands of legs as small as 12 μm in diameter. We are now focusing on establishing and completing all of the processing steps for depositing both n-type and p-type legs on fully metallized and patterned substrates in order to achieve the fabrication of several device prototypes. We expect that this effort can also be extended to even smaller configurations that could include recent advances in novel thermoelectric materials and low dimensional structures.

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