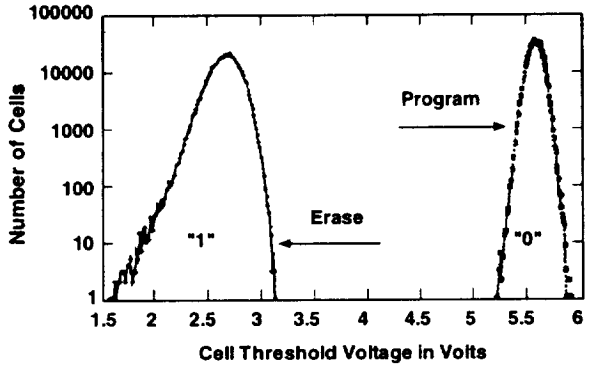
Radiation Effects on Advanced Flash Memories†

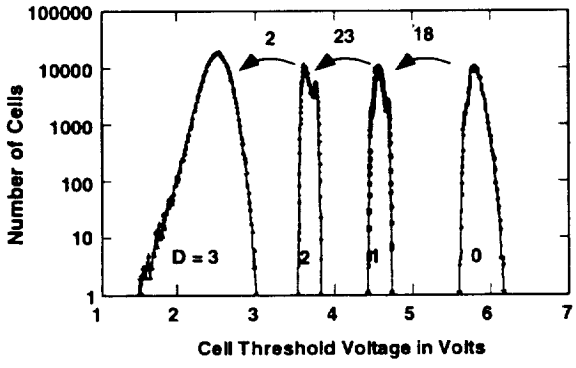
D. N. Nguyen, S. Guertin, G. M. Swift and A. H. Johnston
Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

Introduction

Flash memories have evolved very rapidly in recent years. New design techniques such as multilevel storage have been proposed to increase storage density [1,2], and are now available commercially. Figure 1 compares threshold voltage distributions for single- and three-level technologies [3]. In order to implement this technology special circuitry must be added to allow the amount of charge stored in the floating gate to be controlled within narrow limits during the writing and also to detect the different amounts of charge during reading.



(a) Single Level



(b) Multiple Level

Figure 1. Comparison of cell threshold voltage distributions for single- and mulit-level flash memories.

---

†The work described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration, Code AE. Work funded by the NASA Microelectronics Space Radiation Effects Program (MSREP).

Two devices from Intel that use multi-level flash architecture were selected for radiation testing. They include the 28F320 (32 Mb) and the 28F640 (64 Mb). Both parts operate with a 5 volt power supply. An internal charge pump is used to generate the higher voltage that is required to erase and write the memory.

Not all advanced flash memories use multi-level storage. The NAND architecture, which allows access only at the column level (similar to a shift register) [4], takes less area, and is easier to scale to higher densities. A Samsung 128 Mb devices, KM29U128, was also selected for radiation testing in order to compare the two architectures. The Samsung device uses a 3.3 V power supply. It also uses an internal charge pump to generate higher voltages for erasing and writing.

Earlier work comparing NAND and NOR flash technologies for 16- and 32 Mb devices showed that the NOR technology would operate at much higher total dose levels than the NAND technology if the internal charge pump was not used [5] (its use was optional in the older NOR technologies). Heavy-ion tests in earlier studies showed that upset did not occur in individual cells. Upset in both technologies occurred in the microcontroller and register regions, causing complex errors at the block level as well as address errors [6]. The purpose of the present work is to compare newer flash technologies with the results of the older work.

In evaluating flash memories for use in space, it is important to recognize that they are most likely to be used in applications where writing is done infrequently. In some applications they are unpowered except for brief periods when it is necessary to access their contents. Thus, it is important to distinguish about how they respond in unpowered, read, and full operation (erase/write/read) modes. The earlier work showed that both NOR and NAND technology devices were far more vulnerable to upset or damage when they were fully operational compared to read-only operation.

Total Dose Testing and Test Results

Total dose tests were done using the JPL cobalt-60 test facility at a dose rate of 100 rad(Si)/s. Devices were programmed in a pseudo-random sequence before testing. Tests were done with devices biased statically or unbiased during irradiation. Measurements were made after each irradiation step with an Advantest test system.

Intel Multilevel Flash Devices

Figures 2 shows test results for the 32-Mb Intel multi-level flash memory for statically biased and unbiased conditions. With bias applied, the standby current increased slightly during irradiation, and the device ceased to function at all after the second irradiation level [12 krad(Si)]. When it was tested without bias, the device continued to operate at somewhat higher levels. After 16 krad(Si) approximately 3,000 of the 32 million bits failed.

The 64-Mb multilevel flash memory behaved somewhat differently. As shown in Figure 3, the standby current increased much more rapidly with increasing radiation levels when bias was applied compared to the 32-Mb devices. Devices typically operated to levels well above 20 krad(Si), and failure occurred in only a small number of cell locations.

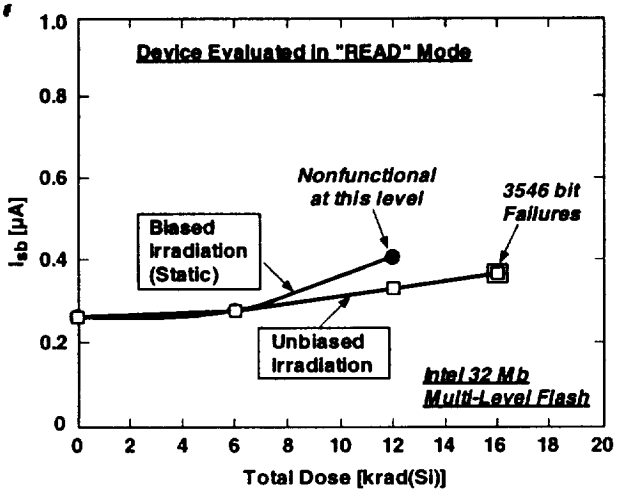


Figure 2. Total dose test results for the Intel 32-Mb flash memory (evaluated in read mode only).

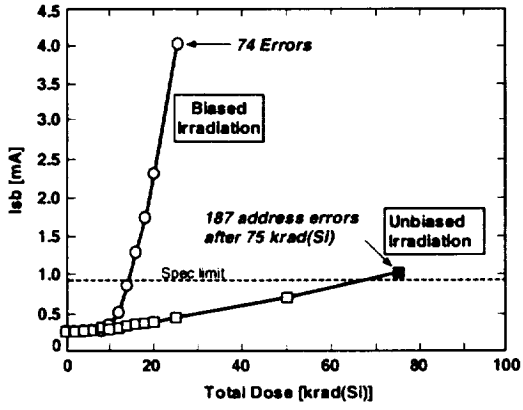


Figure 3. Total dose test results for the Intel 64-Mb flash memory (evaluated in read mode only).

When tested without bias the 64-Mb devices would function up to 50 krad(Si) with no functional failure and only slight increases in standby current. However, at 75 krad(Si) a large number of address errors suddenly occurred.

Test results for the 64-Mb Intel device in the fully operational mode are shown in Figure 4. With biased irradiation the device became nonfunctional at 12 krad(Si), in contrast to the tests in "read" mode (Figure 3) where the device continued to operate to levels about twice as great Without bias, the device also failed at much lower levels when fully operational tests were done between irradiations. Small numbers of write errors occurred between 30 and 40 krad(Si). Three write errors were also observed at 15 krad(Si), but were not present at the next irradiation level.

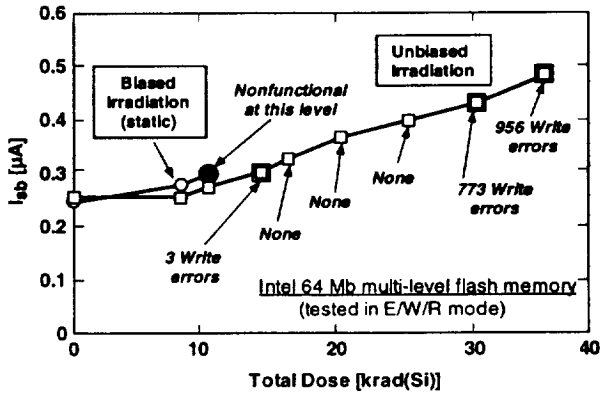


Figure 4. Total dose test results for the Intel 64-Mb flash memory with full functional tests between radiation levels.

Samsung NAND Technology

Test results for the 128-Mb Samsung devices in the "read" mode are shown in Figure 5. With biased irradiation, the standby current increased by several orders of magnitude at about 20 krad(Si). Older technology devices from Samsung behaved quite differently when tested in this mode, failing catastrophically at approximately 10 krad(Si) [5].

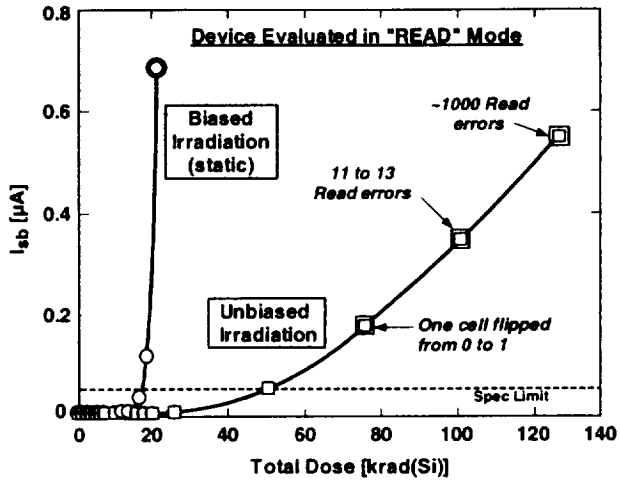


Figure 5. Total dose test results for the 128-Mb Samsung flash device, tested in "read" mode.

When tested without bias the 128-Mb Samsung device functioned to levels above 100 krad(Si) with only a small number of "read" errors. Errors of this type could be easily accommodated in most applications with basic error-detection-and-correction techniques. However, most applications require the device to be powered for significant amounts of time.

With full functionality tests between successive irradiation levels, erase-mode failures were observed at 15 krad(Si) under biased irradiation. This corresponded closely with the total dose level where the standby current first started to increase. When fully functional tests were done on devices that were unbiased during irradiation, erase failures occurred at 45 krad(Si).

Single-Event Testing and Test Results

Single-event testing was done at Brookhaven National Laboratory using several different ion species. The range of the ions exceeded 38 μm in all cases (these devices have very shallow structures, so that this range should be adequate, even at incident angles of 60 degrees).

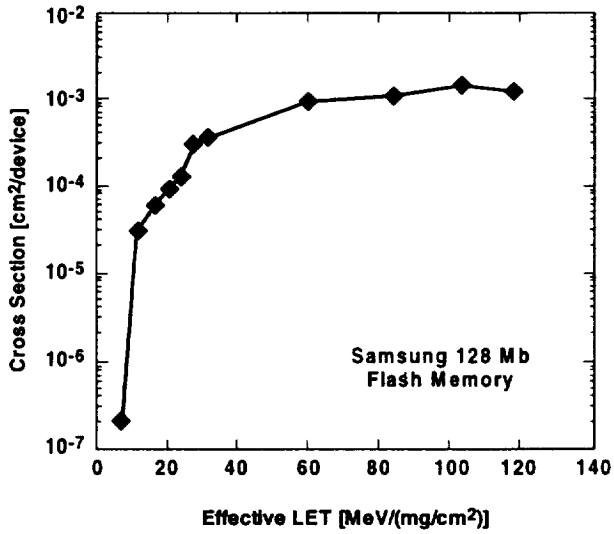


Figure 6. Single-event upset cross section for the Samsumg 128-Mb flash memory.

Just as for the older flash memories [6], errors did not occur in individual memory cells in the Samsung device, but occurred as a result of functional changes in the controller or registers. An example of these results is shown in Figure 6.

Errors associated with control or address upsets are very difficult to evaluate with high precision even in the read mode because of the finite time required to do a complete test of the memory contents (about 50 seconds). The results in Figure 6 were obtained by continually cycling through the address space, and thus are somewhat dependent on the operating frequency and ion flux for the run. In this case the device was tested by dynamically reading the contents of the memory at an access rate of approximately 3 MHz, with a flux of ~10^4 ions/(cm^2-sec).

Somewhat different results occurred for the Intel multi-level flash devices at high LET. Errors were observed in a small number of individual cells -- approximately 100 -- at an LET of 84 (ion at 45 degree angle of incidence). This may be caused by single-event microdose errors [7,8] that affect the distribution of threshold voltage for different logic states. The errors always caused the cell threshold voltage to shift in a more negative direction. The arrows in Figure 1(b) show the number of transitions that were observed for the 64-Mb Intel devices; the 32-Mb devices behaved similarly.

At lower LETs, small number of read errors were observed for the Intel devices. This is consistent with previous results for the older Intel technology. However, for the newer devices it is likely that the errors are due to microdose or soft gate breakdown that affects a small number of devices in the array. Multi-level flash technology is far more sensitive to gate voltage and leakage current than single-level flash technology.

Discussion

Tests of multi-level flash memories have shown that they typically fail at relatively low levels, below 20 krad(Si), when they are biased during irradiation. The advanced devices tested in the present work do not appear to be that different from earlier generation devices, even for multi-flash technology.

Just as for older devices, they undergo far less degradation when they are irradiated in an unbiased mode, and there are many applications where they can be used effectively in a mainly unpowered, read-only mode. However, they are far more vulnerable to failure in erase and write modes, which is probably caused by changes in the internal charge pump (erase and write functions require high internal voltages, with relatively tight tolerances [1,2,4]). Charge-pump failures were identified as the cause of failure at low total dose levels in older device types [5], where external write/erase voltages could be used instead of the internal charge pump. However, the newer devices do not provide this option.

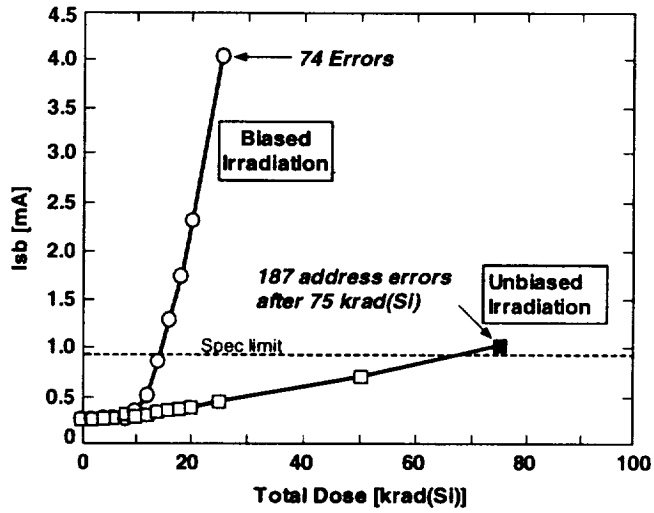
Single-event upset in the newer devices appears to be similar to the older parts except for ions with high LET. Functional failures caused by cell upsets in the very complex control and state registers used in flash memory architectures are the likely cause.

An important new finding is the identification of small numbers of cell transitions at high LET for multi-level flash technology devices. Although these errors only occur for ions with very high LET, it is possible that they may occur at much lower LET values where the effect is of more practical importance as multi-level flash memory technology evolves. This is consistent with the tight threshold voltage distribution that is required to implement multi-level flash technology.

Although the same mechanism is probably present for the Samsung devices, there is much more separation between the "0" and "1" cell threshold voltages than for multi-flash devices, providing increased margin for microdose errors.

References

1. B. Eitan, et al., "Multilevel Flash Cells and their Trade-offs," Digest of Papers from the 1996 IEDM, p. 169.
2. S. Lai, "Flash Memories: Where We Were and Where We Are Going," Digest of Papers from the 1998 IEDM, p. 971.
3. G. Atwood, et al., "Intel StrateFlash Memory Technology Overview," 1998 application note from Intel Corporation.
4. J. D. Choi, et al., "A Novel Booster Plate Technology in High Density NAND Flash Memories for Voltage Scaling-Down and Zero Program Disturbance," Digest of Papers from the 1996 IEDM, p. 238.
5. D. N. Nguyen, C. I. Lee and A. H. Johnston, "Total Ionizing Dose Effects on Flash Memories," 1998 IEEE Radiation Effects Data Workshop Record, p. 100.
6. H. R. Schwartz, D. K. Nichols and A. H. Johnston, "Single-Event Upset in Flash Memories," IEEE Trans. Nucl. Sci., 44, 2315 (1997).
7. T. R. Oldham, et al., "Total Dose Failures in Advanced Electronics from Single Ions," IEEE Trans. Nucl. Sci., 40, 1820 (1993).
8. G. M. Swift, et al., "A New Class of Single Event Hard Errors," IEEE Trans. Nucl. Sci., 41, 2043 (1994).


4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
Isb [mA]
74 Errors
Biased
Irradiation
187 address errors
after 75 krad(Si)
Unbiased
Irradiation
Spec limit
0
20
40
60
80
100
Total Dose [krad(Si)]