ADVANCED INTERCONNECT ROADMAP FOR SPACE APPLICATIONS

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INTRODUCTION

- Past: NASA CODE AE Parts & Packaging Functional Initiative Program: Effective Integration of Critical & Complex Electronic Packages & Technologies
- Now: NASA Electronics Parts & Packaging Program (NEPP)
  - Parts, Packaging, Radiation Testing, Information Management
- National Roadmap of NEMI includes
  - IPC, NSIC Magnetic & Optical Storage, SIA, OIDA, USDC Display
- Technology Challenges
- Recommendations for Research Directions
- Technology forecasts

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FORECASTS

- Package, Wafer, Flip Chip, and Hybrid Assembly Integrated into SMT
- Increased Use of Multiple Technologies in One Package such as Optoelectronics and MEMs
- Increased integration of power devices
- PBGAs Retain Highest Volume of BGA Use
- Increased Use of Flip Chip In Package (FCIP), Requiring:
  - Low Cost Bumping, Copper-based Silicon
  - More Cost Effective Substrates, Better Bare Die Testing
  - Shorter Underfill Time
  - More Efficient Rework

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FORECASTS, continued

- New Packaging Materials Meeting Greater Moisture Resistance
- Improved Underfill Materials: Fast Processing and Curing, Low Stress, Fine Gap, and Compatible with No-clean Fluxes
- Reduced Wicking Process Time for Underfills and Coatings Using Injection or Vacuum Methods
- Greatly increased implementation of integrated passives
- Increased high frequency applications ($\geq$ 1GHz)

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FORECASTS, continued

EXAMPLES

- **Continued NASA Research in HDP Use in Extreme Environments**
  - **DS2 Mars Microprobe Penetrator Tip COB Si Carbide Structure**
    80K g at tip impact into Mars soil
  - **X2000 First Delivery**
    HDP (MCM) Packaging Built into Integrated Avionics Structure

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TECHNOLOGY CHALLENGES

Performance Needs	Packaging Response
Increased Bandwidth	Higher Total Gate Count
Higher Number of Gates in CPU	Decreased Wiring Delay
Increased Clock Frequency	Min Distance Between Chips
Min Memory Access Bottlenecks	Min Distance Bet CPU & Memory

- Dense & Flexible Interconnects between Stacked HDPs
- Extreme environment polyimide flexible circuit reliability
- High Heat Dissipation Technology for SMT
- Improved Guidelines & Infrastructure for Packaging/integration Selection

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RESEARCH DIRECTIONS

- Blind and Buried Vias for Dense Small Form Factor PWAs
  - Laser Drilled, Photoimaging, and Plasma Etching
- Improve Wafer Bumping for Flip Chip and Optoelectronics Packaging
- Better Understanding of Effects of Miniaturization on Electromagnetic Interference and Compatibility Within and Between Modules
- NIST ATP Microelectronics Manufacturing Infrastructure:
  - Wafer Technology, Semiconductor Packaging
  - Very High Density Off-Chip Interconnects
  - Chip to Board Integration

RESEARCH DIRECTIONS FOR CHIP ON BOARD (COB)

- Design Guidelines for COB Passivation Techniques
- Validated Test Regime for COB Range of Flight Environments
- Integration with Design Validation of Chip Scale Packages, COB, and Flip Chip
- COB Manufacturing Process Control Guidelines
- Copper Cladding for COB Site Preparation

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RESEARCH DIRECTIONS FOR HDPs: MULTICHIP MODULES (MCMs)

- Process Evaluation of Micro-via Technology Using Plasma, Laser and Chemical Etch
- Integration of passives into MCM-L, -D, -C
  - Multiple Dielectrics/Ceramics
  - High Precision Resistors
- Polymeric Materials Evaluation:
  - High Density Deposited and Thin Film Dielectric Coatings
  - Low-K Dielectrics for High Frequency Applications
  - Integrated Thin Film Passive Logic & Thick Film Polymeric Sensors
- Laminate versus Ceramic Substrate Performance Evaluation and Usage Guidelines

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RESEARCH DIRECTIONS FOR HDPs: MULTICHIP MODULES (MCMs)

PROBLEM EXAMPLE

DS1 Ion Propulsion System Packaging Challenges

- Stacked HDPs (MCM): Layers Connected with Vertical Gold Fiber in Silicone Polymer
- During Environmental Testing:
  Developed a Permanent Cold Set Which Led to Intermittent Opens between Layers
- Dropped Use of the Stacked HDPs (MCM)

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RESEARCH DIRECTIONS FOR MICROELECTROMECHANICAL SYSTEMS (MEMs)

- Failure Mechanisms as a Function of Design, Materials, and Mission Length
- MEMs Materials Usage Mission Length & Environment Guidelines
- Critical Points for Inspections & Process Controls for MEMs Manufacturing
- Non-invasive Inspection & Test Methods for MEMs Manufacturing and Final Products
- System Level Quality & Reliability Methodology Development

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RESEARCH DIRECTIONS FOR PHOTONICS

- Solid State Laser, Ultra-stable Laser, and Semiconductor Laser
- Space-ready Single-Mode Microwave Fiber Optic Link Qualification
- Frequency Shifter Qualification
- Integration and Validation of Optical/Electronic Back Plane for Electro-optic Assemblies
- Evaluation of -80° C to +85° C Range Fiber Optic Cable

JPL RESEARCH DIRECTIONS FOR MATERIALS, cont'd

- **Resolution of No-Clean Fluxes & Solder Paste Issues**
  - Electrical Interference of Residue
  - Interference with Conformal Coating
  - Undetected Solder Balls
  - Fluxless Solder Attachment in Nitrogen/Argon Atmosphere
  - Validation of aqueous flux use

- **Encapsulants & Coatings Which Do Not Require High Temperature Curing**
  - Meeting NASA Outgassing & Adhesive Requirements
    NASA JSC SP-R-0022A