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THIN AND THICK FILM MATERIALS BASED INTERCONNECTION TECHNOLOGY FOR 500 ºC OPERATION

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Abstract

Precious metal based thick-film material was used for printed wires, wire bond pads, test lead-attach, and conductive die-attach for high temperature (up to 500 °C and beyond) chip level packaging. A SiC Shottky diode with a thin-film coated backside was attached to a ceramic substrate using precious metal based thick-film material as the electrically conductive bonding-layer. After a 500-hour soak test in atmospheric oxygen, these basic interconnection elements, including attached test diode survived both electrically and mechanically. The electrical resistance of these interconnections (including thick-film printed wire/pad, bonded wire, and test lead attach) were low and stable at both room and elevated temperatures. The electrical resistance of the die-attach interface estimated by I-V characterization of the attached diode, during and after high temperature heat treatment, remained desirably low over the course of a 500-hour anneal. Further durability testing of this high temperature interconnection technology is also discussed.

INTRODUCTION

Single crystal silicon carbide (SiC) possesses such excellent physical and electronic properties (wide energy gap and low intrinsic carrier concentration) that SiC based semiconductor electronics can operate at temperatures in excess of 600 °C, well beyond the high temperature limit for Si based semiconductor devices. Various SiC semiconductor devices have recently been demonstrated to be operable at temperatures as high as 600 °C,[1, 2] but only in a probe-station test environment partially because mature packaging technology for high temperature devices (500 °C and beyond) is not available (still in development). One of core technologies needed for successful high temperature electronic packaging is the development of high temperature electrical interconnections. For decades, precious metal thick-film materials (for metallization of ceramic substrates) have been used for hybrid-packaging traditional (room temperature to 150 °C) electronics. Recently, gold (Au) based thick film materials, which are normally processed at high temperatures (850 °C), have been proposed for hybrid packaging techniques to achieve 500 °C operation.[3] This paper reports test results, at both room and elevated temperatures, of thick- and thin-film based electrical interconnection components operable to 500 °C - 600 °C.

MATERIALS AND COMPONENTS

Thick Film Material

Thick film metallization materials are usually composed of (1) fine metal (such as gold) powder, (2) inorganic binder (such as metal oxides), and (3) organic vehicle. Screen printing technique is usually used for thick-film coating with thickness control. During the initial drying process

(at ~150 °C) the organic vehicle evaporates and the paste becomes a semi-solid phase mixture of metal powder and binder. In the following curing process (~ 850 °C recommended by DuPont for best adhesion on alumina substrate) the inorganic binder molecules migrate to the metal/substrate (e.g. Au/ceramic) interface and form reactive binding chains. Aluminum (Al) and Au thin wires can be bonded directly to Au thick film metallization pads to provide electrical interconnection in packaging. Some new thick film materials (DuPont5771) may be applicable to various ceramic substrates such as alumina and aluminum nitride (AlN).[4] The major application of thick film materials is for hybrid-packaging traditional electronic circuits (operable at T < 150 °C) for high performance and high reliability application. In this work thick-film material based electrical interconnections (electrical loop and conductive die-attach) were examined for high temperature chip level packaging.

Test Loops

The electrical test loops include thick-film (DuPont 5771) conductive wires, wire bond pads, thin gold wires bonded to the pads, and test leads, as illustrated in Figure 1. The geometry of the conductive wires and the metallization pads were so designed that the electrical resistances of test loops are dominated by the resistances of thin (0.001" diameter) bonded gold wires after subtracting the resistance contributed by the long test leads. The thick film conductive wires and pads were processed according to standard drying and curing processes (Processing and Performance Data of DuPont Thick Film Materials) suggested by the material manufacturer (DuPont). The thin gold wires were bonded to the thick-film pads on substrate or the thin-film metallization pads on SiC chip by parallel gap welding or thermal-press bonding techniques. The 0.010" (diameter) Au test leads were attached to the out-reach thick-film metallization pads on the test device by parallel gap welding first followed by thick-film coating to provide both mechanical reinforcement and larger electrical contact area.

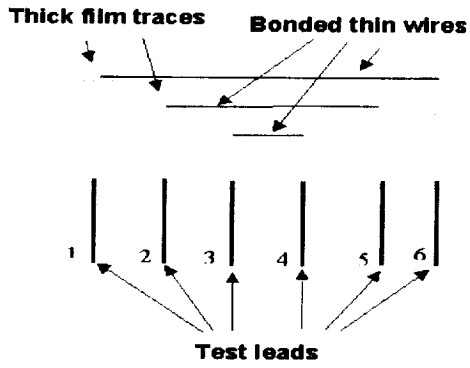

Figure 1: Schematic diagram of three test-loops.

Die-attach

The backside of SiC wafer was coated with nickel (Ni) thin film (~ 6000 Å) by electron beam evaporation. After the deposition of the Ni thin film the SiC wafer was annealed at 950 °C in argon tube furnace for 5 minutes forming low resistance ohmic contact on the backside of SiC wafer. Following the annealing, a second layer (3000 Å) of Ni was electron beam evaporated onto the wafer backside. The SiC diode was fabricated by sputter deposition of Au (4000 Å) and titanium (Ti) thin (100 Å) films on cleaned n-type (nitrogen, ~ $10^{18}/cm^3$) Si terminated 6H-SiC wafer. The Ti interlayer was used to improve interfacial adhesion of the metal (Au) thin film on the front side of SiC chip. After dicing, the diode chips measured 1 mm x 1 mm was then attached to ceramic substrate (either AlN or alumina) using DuPont 5771 Au thick-film material. This thin and thick film process results in an electrically conductive die-attach structure which is required for packaging many devices including field effect transistors (FET) based circuits. A slow drying process (120 °C – 150 °C) was critically important to keep thick-film bonding layer uniform. A lower temperature (600 °C) was used for final curing process in order not to alter the interfacial properties of Au/Ti/SiC. Thick film material was also used to reinforce the top Au thin film for

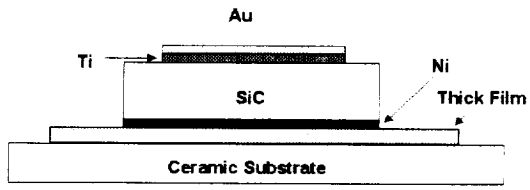

Figure 2: Schematic diagram of as-fabricated SiC device and die-attach structure.

better wire bonding. Au 0.001" (diameter) wire was bonded on the top Au thin-film metallization pad with a thick-film overlayer by thermal-press bonding technique.

TEST AND RESULTS

The electrical resistance of test loops (illustrated in Figure 1) include those of thick film conductive wire (pads), bonded thin Au wires, and Au test leads. The resistances of test loops 1-6, 2-5, and 3-4 were measured at various temperatures and for various accumulated heating time. The data of loops 1-6 and 3-4 are shown in Figure 3. The resistance, including that of the test leads, was first measured at room temperature. Following that the temperature was ramped to 500 °C and the resistance was monitored in air for 70 hours. The temperature was then reduced back to room temperature and the resistance was recorded again. After this temperature cycling, the loop resistance were continuously monitored for a total of 250 hours at 500 °C in air without current flow, followed by another 250 hours at 500 °C with 50 mA (DC) current though test Loop 3-4. The resistances under all these conditions were desirably low (basically dominated by the resistance of the thin bonded wire after subtracting the resistance of test leads) and stable (for each test temperature). The temperature was then increased to 550 °C for 120 hours. Finally, the temperature was increased to 600 °C which is our ultimate operation temperature and held there for 250 hours. The test lead resistance was measured and subtracted from the data of loop 3-4 measured at 600 °C, so that the data reflects the realistic interconnection resistance at 600 °C. The results of electrical tests of all test loops indicated that resistance of thick film based conductive wires, wire bond pads, wire bonds were stable and low from room temperature to 600 °C in atmospheric oxygen environment.

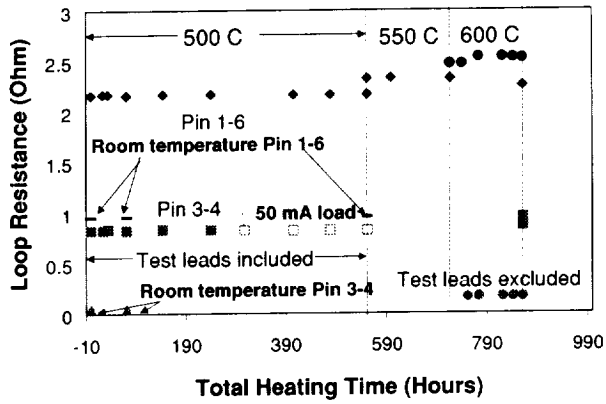

Figure 3: Resistances of test loops at various temperatures and heating time. – and ▲ room temperature data of Loop 1-6 and 3-4, respectively. ♦ data of Loop 1-6 500 °C - 550 °C. ■ and □ data of Loop 3-4 500 and 550 °C with and without current load, respectively. ● data of Loop 3-4 at 600 °C for both test loops.

The attached SiC Schottky diode (Figure 2) was characterized by current - voltage (I-V) measurements at various temperatures and for various accumulated heating time. A minimum dynamic resistance (dV/dI) in a high current (forward biased) region of the I-V curve was used to estimate the upper limit of resistance of the die-attach structure (interfaces and materials). This dynamic resistance includes the dynamic resistance of Au(Ti)/SiC (rectifying) interface, SiC wafer bulk resistance, the

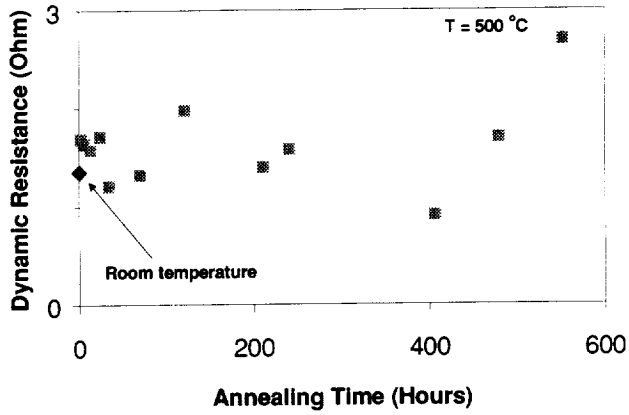

Figure 4: Minimum dynamic resistance calculated from I-V data vs. heating time at 500 °C. This resistance includes resistances contributed from the Au(Ti)/ SiC rectifying interface, SiC wafer, the die-attach materials/interfaces. Resistances of the bonded wire and the test leads have been subtracted.

die-attach materials/ interfaces resistance, bonded wire resistance, and the test leads resistance in series. The resistance contributed from test leads and bonded wire can be measured and subtracted. The attached diode was first characterized with I-V measurements at room temperature. The device exhibited rectifying behavior and the lowest dV/dI measured under forward bias was ~ 1.35 Ω, as shown in Figure 4. The temperature was then ramped up to 500 °C (in air) and the diode was characterized *in situ* by I-V measurement for 70 hours. The lowest resistance (dV/dI) under forward bias was less then 2 Ω. The diode was then cooled down to room temperature and characterized again. The lowest resistance (dV/dI) measured was 0.79 Ω. The diode was heated up to 500 °C in air and characterized for a total of 550 hours. The lowest dV/dI measured from I-V curves with forward bias was 1.4 - 2.7 Ω. It is worth while to note that the device's I-V curve changed somewhat with time during annealing at 500 °C. However, the electrical resistance of die-attach structure, which was characterized by the dynamic resistance measured, remained comparatively low within whole test ranges of temperature and time.

DISCUSSION

Au thick film (DuPont 5771) was electrically/electronically tested, especially, at elevated temperatures for application in electrical interconnection for high temperature operation. A SiC diode with backside thin-film metallization was successfully attached to ceramic substrates with low attach resistance, for the first time, for operation at a temperature range up to 500 °C in oxygen-containing ambient using thick-film as conductive bonding layer.

The room temperature mechanical properties of thick film metallization on various substrates, Au wire-bond on Au thick-film, and SiC semiconductor die-attach using thick-film materials have been evaluated previously.[3, 4] However, equivalent mechanical tests at elevated temperatures remain to be carried out in future planed work in order to more completely validate thick film material application for high temperature interconnections.

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