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A LOW COST RAD-TOLERANT STANDARD CELL LIBRARY†

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Abstract

This paper describes circuit design techniques developed at the NASA Institute of Advanced Microelectronics that have been shown to protect CMOS circuits from the deleterious effects of the natural space radiation environment. The IAμE is leading a program to incorporate e these radiation–tolerance providing design techniques into a commercial standard cell library that will be used in conjunction with available Electronic Design Automation tools to produce space flight qualified microelectronics fabricated at modern commercial CMOS foundries.

1 Introduction

Microelectronics used in space systems are subjected to the deleterious effects of the natural radiation environment found outside of the protection of the earth's atmosphere. During the 1970s and 1980s the United States Departments of Defense (DoD) and Energy (DoE) sponsored the development of radiation–hardened semiconductor processes. Government space agencies and the commercial satellite industry have been able to utilize many of these rad–hard components to increase system complexity and reliability while reducing size, weight, and power requirements for space–borne platforms. In the post–Cold War world the DoD and DoE push to cent inue to advance the rad–hard processes has waned. As a result, the performance capabilities of the available rad–hard components have lagged behind those that are manufactured using the latest commercial technologies. Space craft designers are facing an ever widening performance gap between available rad–hard and commercial devices [1]. Compounding the problems faced by the satellite industry, rad–hard components are becoming harder to get. At least six sources of rad–hard parts have exited this market in the last five years, leaving only two domestic suppliers. This paper describes design techniques which produce rad-tolerant CMOS circuits, and outlines a path currently being pursued to provide this technology to designers of Application Specific Integrated Circuits (ASICs).

2 Ionizing Radiation Effects in MOS Microelectronics

Ionizing radiation may be defined as exposure to charged particles that possess enough energy to break atomic bonds and crest e electron/hole pairs in the absorbing material. Such particles may include protons, electrons, atomic ions, and photons with energies greater than the material bandgap. There are two primary categories of ionizing radiation effects in microelectronics; total ionizing dose (TID) effects and transient effects [2]. TID effects are a function of ionizing radiation accumulation over months or even years, which can lead to performance degradation and functional failure. Transient radiation effects are primarily the result of photocurrents generated as energetic particles pass through the circuit.

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2.1 Total Ionizing Dose Effects

As ionizing particles pass through MOS devices, generating electron/hole pairs, charges can be trapped in the gate and field oxides and interface states are increased. Mobile electrons quickly transport through the oxide, but holes have a very low effective mobility in SiO_2 and are easily trapped. The trapped positive oxide charge shifts transistor threshold voltages in a negative direction. An increase in interface states shifts thresholds in the positive direction for n–channel devices and in a negative direction for p–channel devices. Generally, the trapped oxide charge shift is greater than the interface states shift and the magnitude of the NMOS V_t decreases while the magnitude of the PMOS V_t increases. The radiation–induced interface states also reduce the channel mobility, which decreases channel conductance reducing the transistor drive. Over time, the threshold voltages may shift to the point where the n–channel transistors cannot be turned off and the drive capability of the p–channel transistors is not sufficient for the chip to continue operating at the system clock rate, causing it to fail, In addition to the drawn transistors, threshold shifts also occur for parasitic MOS elements. As the parasitic n–channel transistors thresholds decrease, channels begin to form and leakage currents flow around the edges of the drawn n–channel gate regions, from drain to source, between drain/source regions of adjacent n–channel transistors, and from n–channel drain/source regions to the n–well/n–substrate. Leakage currents may cause parametric failures to occur before functional failures.

While the actual dose that a satellite receives is highly dependent on the orbit, satellites in low earth orbit can be expected to receive a TID exposure of less than 10K rads(Si) during missions of up to 20 years. For a satellite in geosynchronous orbit the TID can be expected to reach 10 OK rads(Si) after 10 years on orbit. The most severe ionizing radiation orbits are 1/2 geosynchronous, which can reach a 1M rad(Si) dose after 8 years on orbit [1]. The radiation hardness of a MOS process is a function of the rate at which oxide–t rapped charge and interface traps build up as the radiation dose increases. Scaling of commercial processes has naturally reduced the volume of the gate oxide and thus reduced drawn transistor threshold shifts, leaving leakage currents as the dominant TID effect. Some commercial processes have been shown to produce parts that exhibit TID hardness in the 100's of KRads [3, 4].

2.2 Ionizing Radiation Transient Effects

Single Event Effects (SEE) are produced in the natural space environment by galactic cosmic rays, solar enhanced particles and energetic protons and neutrons [2]. The passage of a single high–energy particle through a MOS device can create a high–density track of electron/hole pairs which results in charge collection in a localized region of the circuit. SEES are commonly divided into two categories, Single Event Latchup and Single Event Upset.

In complementary MOS (CMOS) devices containing both n–channel and p–channel devices on a silicon substrate, parasitic bipolar p-n-p-n devices exist, forming a silicon–cent rolled rectifier (S CR) structure, which under normal conditions is in its "off" (i.e. high–impedance) state. If a SEE injected photocurrent produces sufficient bias to turn on one of the parasitic base-emitter junctions, the SCR can be triggered, producing a low–impedance path between the power supply and ground rails. If the product of the effective current gain (β product] of the parasitic p-n-p and n-p-n devices is greater than unity, then a regenerative condition exists and a self–sustaining SCR high current mode is entered after the triggering event [5]. This condition is know as Single Event Lat chup (S EL) and can cause destructive failure. The SEL phenomenon is similar to the Electro–Static Discharge induced latch-up protected against in typical CMOS 1/0 structures, however in an ionizing radiation environment, a particle can strike anywhere in the circuit so merely protecting the 1/0 circuitry is not sufficient.

A Single Event Upset (SEU) occurs when the charge transferred as a result of the generated photo currents is of sufficient magnitude to alter the logic state of a susceptible node. An upset node may further cause the alteration of the contents of circuit memory elements or alter the operation of the circuit in such a way to cause an error in the logic function.

3 Ionizing Radiation Effect Immunity By Design

One spacecraft design approach is to address SEES at the system level while using commercial *off the shelf* (COTS) parts. Limiting the supply current to a device can save it from latchup destruction, but requires a power down and reset cycle whenever a SEL occurs. Logic malfunctions due to SEUs can be detected and corrected through system level redundancy. However, this strategy can be quite costly and still leaves unanswered the classic question, "who checks the checker?"? It has been demonstrated that circuit and layout design techniques can make it possible to provide a high degree of SEL and SEU immunity using commercial CMOS processes. In general, these techniques do increase cell area, decrease speed, and/or increase power consumption. An optimal solution should minimize these costs.

3.1 SEL Immunity

The techniques used to prevent latchup in CMOS devices involve degrading the β product of the parasitic n-p-n and p-n-p transistors and/or limiting the applied base bias [5]. Approaches to β product reduction include minority carrier lifetime degradation in the parasitic base (i.e. substrate and well) regions, accomplished by gold doping [6] or neutron irradiation [7]. Insuring some minimum spacing between source/drain regions in the substrate and the well edges decreases the β of the lateral parasitic by insuring a wide effective base region [8]. The base bias is reduced by lowering the effective base-emitter resistance in the parasitic SCR structure. Low–resistance connections from the substrate and well to the power and ground rails also reduce the base bias current by providing for capture and shunting away of injected minority carriers before they reach the parasitic base. Methods for reducing the substrate and well resistance and increasing charge carrier capture include the use of a lightly doped epitaxial layer on top of a heavily doped substrate [9] and the use of p^+ guard rings around the n–channel transistors and n^+ guard rings around the p–channel transistors [10]. It has been shown that latchup can occur in circuits fabricated using an epi layer process [11], and that the epi layer must further be "thin" in order to prevent latchup.

The minority carrier lifetime degradation and thin epi–layer solutions belong to the "technology hardening" class of solutions. These approaches rely on specifying and/or controlling some aspect(s) of the fabrication process and are not generally considered to be "commercial" CMOS. Guard rings are produced during the normal source/drain mask steps and require no special processing. The guard ring method has been shown through heavy ion testing using the Twin Tandem Van de Graaff accelerator at the Brookhaven National Laboratories (BNL) Single Event Upset Test Facility (SEUTF) to prevent SEL at LET levels ranging from 3.4 $MeV \cdot cm^2/mg$ up to at least 120 $MeV \cdot cm^2/mg$. These results have been obtained using multiple test chips fabricated through MOSIS in Hewlett Packard's $1\mu m$ double metal CMOS (CMOS34) process, and Hewlett Packard's $0.8\mu m$ triple metal CMOS (CMOS26b) process, as well as a 1.2 million transistor radio astronomy correlator chip implemented in the CMOS26b process, a 100,000 transistor Reed–Solomon error correcting code (ECC) encoder and a 200,000 transistor Reed–Solomon ECC encoder/decoder, both fabricated in American Microsystems Inc. (AMI) triple metal $1.0\mu m$ process (CYC) [12, 13]. The cell area cost of including guard rings scales with reduced feature size while the minimum spacing approach does not scale. A comparison of the results of Moss et. al. [8] with the IAμE results at BNL show that the guard ring met hod cost is lower for sub–micron processes.

3.2 SEU Immunity

Multiple strategies have been applied to harden microelectronic circuits against the effects of SEU. One approach is to reduce the charge collection capability of the material to the point that the circuit will not collect sufficient charge to initiate an upset [2]. This strategy belongs to the 'technology hardening" class. Other circuit design based approaches seek to raise the critical charge required to upset sensitive storage nodes. Finally, redundancy techniques have been applied at the circuit level to recover upsets. The primary goal of SEU hardening through circuit design techniques is to produce SEU–immune circuits using standard CMOS processing, with no additional mask or processing steps, while minimizing cell size, circuit speed costs, and power consumption.

The enhanced critical charge hardening techniques include increasing transistor drive, capacitive hard-

ening, and resistive hardening. A high drive transistor can quickly remove/replace SEU injected charge, shortening the time duration of the disturbance. Large high drive transistors also have increased node capacit ante, which reduce the voltage excursions caused by the SEU injected charge [14]. Increasing the capacit ante of critical nodes to reduce the voltage change due to SEU injected charge is the basic concept behind capacitive hardening of circuits [2]. Resistive hardening involves the use of resistors in the memory element feedback paths, to create, in conjunction with the gate capacitance, a low pass filter to reject the effects of SEU induced transients while passing the longer duration legitimate *signals [15].*

Power is consumed charging/discharging circuit capacitance each t ime the logic level of a node changes. Increasing circuit capacitance due to high drive transistors or other capacitive hardening methods also *increases* the ac power consumption of the circuit. Designing a cell to reject short duration signals places a constraint on the maximum speed at which the circuit can operate. Under *nominal conditions,* it is possible to design an RC filter to reject SEUs and still allow the circuit to operate at hundreds of megahertz. The resistances required to provide SEU immunity are typically 10 OK to 1M ohm, requiring high resistivit y polysilicon in order to keep the resistor elements small. High resistivit y polysilicon is very sensitive to doping concentration and therefore subject to wide resistance variations across a generally accepted variation in commercial processing parameters. The polysilicon resistance value control problem due to wafer processing is further exacerbated by a very large negative temperature coefficient. The result is that a cell properly designed to reject SEUs at one corner of the process parameter/operating condition design space suffers adverse performance impacts at other design space corners.

SEU hardening by redundant circuit design approaches are baaed on three fundamental concepts:

1. Information storage redundancy maintains a source of uncorrupted data after an SEU.
2. Feedback from the non–corrupted data storage location should cause the corrupted data to recover after a particle strike.
3. The "intelligence" needed in the feedback to cause recovery of the proper location can be derived from the fact that the current induced by a particle hit flows from n-type diffusion to p–type diffusion. If a memory cell is constructed from only p–type transistors then it cannot be upset to a O while storing a 1. A memory cell constructed from only n–type transistors cannot be upset to a 1 while storing a O.

The low power Whitaker cell[16, 17], developed at the IAμE and shown in Figure 1, consists of two loadable storage structures. The lower storage structure is a modified six transistor cell consisting of only n–type devices and the top structure is a modified six transistor cell consisting of only p–type devices. The lower structure stores incorruptible 0s and the top structure stores incorruptible 1s. In order for the feedback mechanism to effect recovery from SEU, transistors M2 and M4 are sized to be weak compared to M3 and M5 while M13 and M15 are sized to be weak compared to M12 and M14. Complementary n–channel devices M16 and M17 are added to disconnect the de-current path in the p-channel section eliminating the static power consumption that otherwise results from the weak 1 level produced at N1(N2) not turning M 13 (M15) completely off. Similarly p–channel devices M6 and M7 are added to disconnect the de-current path in the n–channel section. The other transistors are sized using the normal design considerations for a memory cell to meet the performance required. The cell buffer transistors M8, M9, M 18, and M 19 restore the output voltage levels to the rails, isolate the storage nodes from high capacitance loads, and tri–state the cell output during SEU recovery. By tri–stating during SEU recovery and not driving outputs to upset values, the capacitance on the cell output maintains the correct output voltage levels during recovery. Supplying separate input signals to the n–channel and p–channel sections combined with an inherent feature of the cell that requires both inputs to be the same in order for the value stored in the cell to change eliminates the capture of propagated upsets that are coincident with clock edges.

The number of transistors required for the SEU–hardened data latch shown in Figure 1 make it impractical for large static memory arrays. However, the design can easily be used to create SE Unhardened master-slave D–flip flops to design finite state machine controllers and other data path elements.

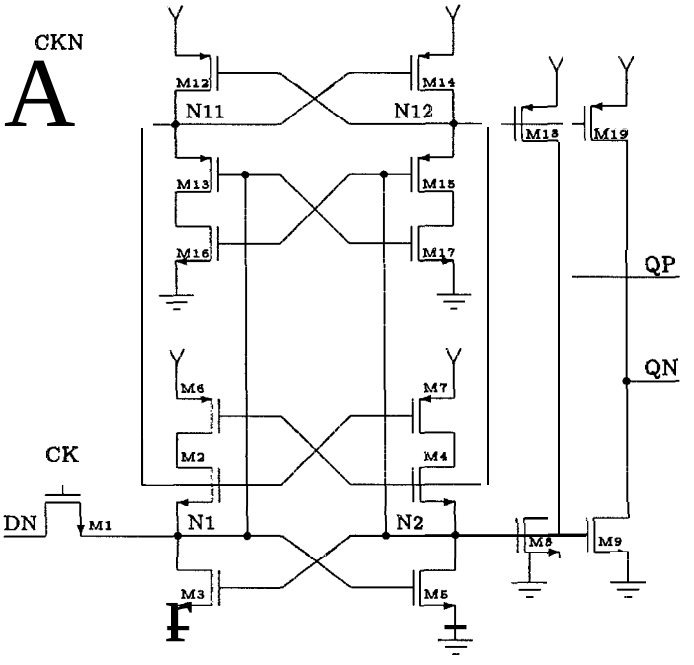

Figure 1: Buffered Low Power Whitaker Cell.

3.3 Rad–Tolerant VLSI Processors

In addition to several test chips, three special purpose rad–tolerant VLSI processors have been developed at the NASA Institute for Advanced Microelectronics utilizing guard rings for SEL immunity and using the low power Whitaker cell for SEU immunity. The rad–tolerant special purpose processors include:

- Error–correcting code (ECC) encoder that supports the Reed–Solomon (RS16) coding specified in the Consultative Committee for Space Data Systems (CCSDS) recommendation for Telemetry Channel Coding.
- Programmable Reed–Solomon ECC encoder/decoder (EDAC) [13]. This chip has been designed into solid–state recorders in support of EOS–AM, LandSat 7, and the Hubble '97 Upgrade Package.
- A 1024 channel autocorrelator chip used in the Naval Research Laboratories (NRL) Orbiting High Frequency Radio Interference Monitor (OHFRIM) experiment [18].

4 Future Work

Designing full–custom rad–tolerant VLSI processors to be fabricated at commercial foundries has been accomplished. However, for this technology to be truly valuable it must be made readily available to a wide range of space system designers. Under sponsorship of NASA, the Institute for Advanced Microelectronics is leading a consortium including academic, industrial, and government partners, to create, qualify, and make available a radiation–tolerant standard cell library utilizing the design techniques described in this paper that will be able to be targeted from a wide range of Electronic Design Automation (EDA) tool environments and fabricated at commercial foundries, The program includes participation by TRW, The Aerospace Corporation, NASA Goddard Space Flight Center and Johnson Space Center, and Aspec Technology, Inc.

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