Influence of the Polysilicon Gate on the Random Dopant Induced Threshold Voltage Fluctuations in Sub 100 nm MOSFETs with Thin Gate Oxides

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Abstract

In this paper for the first time we study the influence of the polysilicon gate on the random dopant induced threshold voltage fluctuations in sub 100 nm MOSFETs with tunnelling gate oxides. This is done by using an efficient 3D 'atomistic' simulation technique described elsewhere [1]. Devices with uniform channel doping and with low doped epitaxial channels have been investigated. The simulations reveale that the polysilicon gate is responsible for a substantial fraction of the threshold voltage fluctuations in both devices when the gate oxide is scaled to tunnelling thickness in the range of 1 - 2 nm.

1. Introduction

The use of a polysilicon gate in MOSFETs with tunnelling gate oxides introduces some problems associated with the polysilicon depletion effect [2], leading to a pronounced loss of inversion charge, which is complementary to the charge losses due to inversion layer quantisation. The associated reduction in the transconductance and drive current have a detremental effect on the device and circuit performance [3].

Another detremental effect associated with the polysilicon gate, not yet addressed in the literature, is an enhancement of the random dopant induced MOSFET parameters fluctuation. Fluctuations in the threshold voltage associated with the random number and position of discrete dopants in the MOSFET channel have been predicted in the early seventies [4], and confirmed now experimentaly [5] and in numerical simulation studies [1], [6], [7] for a wide range of devices. The polysilicon gate depletion, which increases the effective gate-oxide thickness, and introduces additional random dopant charge on the opposite side of the gate oxide to the channel , will enhance the threshold voltage fluctuations.

In this paper for the first time we investigate the effect of the polysilicon gate on the random dopant induced threshold voltage fluctuations in sub 100 nm MOSFETs with tunnelling gate oxides. The study is carried out using an efficient 3D 'atomistic' simulation technique [1] which takes into account in this case the discrete random dopant distribution not only in the MOSFET channel but also in the polysilicon gate.

2. Devices and Simulation Procedures

The simulations in this paper are focused on *n*-channel MOSFETs with 60 nm n^+-polysilicon gate length and 50 nm gate width. A junction depth $x_j = 7$ nm with 5 nm lateral sub-diffusion results in an

effective channel length $L_{eff} = 50$ nm for all simulated devices. Both devices with uniform channel doping, and with low doped epitaxial layer introduced in the channel region to reduce the threshold voltage fluctuations, have been investigated. The doping concentration in the channel or behind the epitaxial layer in most of the simulated devices is $N_A = 5\text{x}10^{18}$ cm^{-3}. The oxide thickness t_{ox} varies from 1 to 4 nm. The above choice of MOSFET parameters allows for a direct comparison with previously published atomistic simulation results [1], [8] in which the effect of the polysilicon gate has been neglected.

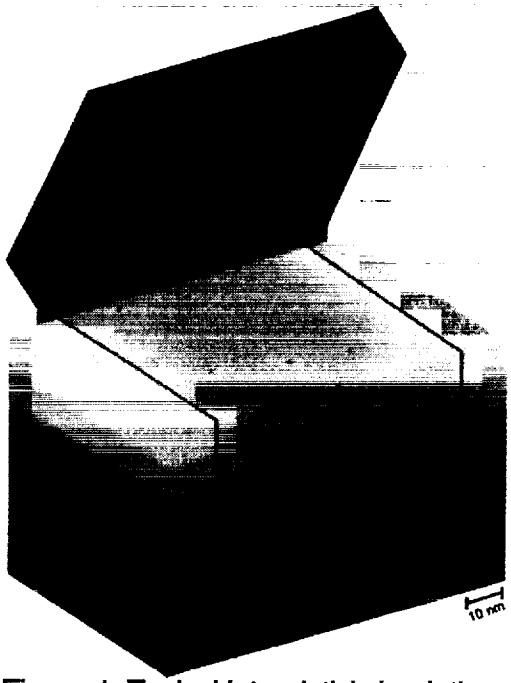

Figure 1. Typical 'atomistic' simulation domain for a MOSFET with a polysilicon gate

We investigate the random dopant induced threshold voltage fluctuations by using an efficient statistical 'atomistic' simulation approach described in more details elsewhere [1]. A typical 'atomistic' simulation domain for a MOSFET with a polysilicon gate is illustrated in Fig. 1. The polysilicon gate is flipped open like a cover of a book to give an idea of the random distribution of dopants at its interface with the silicon dioxide. The 'atomistic' regions in the channel and in the polysilicon gate are outlined in the figure. A current criterion $10^{-8}W_{eff}/L_{eff}$ [A] is used for determining the threshold voltage. The threshold voltage standard deviation σV_T is extracted from the simulation of samples containing 200 MOSFETs with microscopically different distributions of dopants. The corresponding relative standard deviation of the extracted σV_T is 5% for all results presented in this paper.

3. Simulation results

The dependence of the threshold voltage standard deviation σV_T on the oxide thickness for a MOSFET with an n^+ polysilicon gate is compared in Fig. 2 with previously published results for an analogous device with a metal gate [1]. Both MOSFETs have uniform channel doping $N_A = 5\text{x}10^{18}$ cm^{-3} and $L_{eff} = W_{eff} = 50$ nm. The doping concentration in the polysilicon gate is $N_D = 1\text{x}10^{20}$ cm^{-3}.

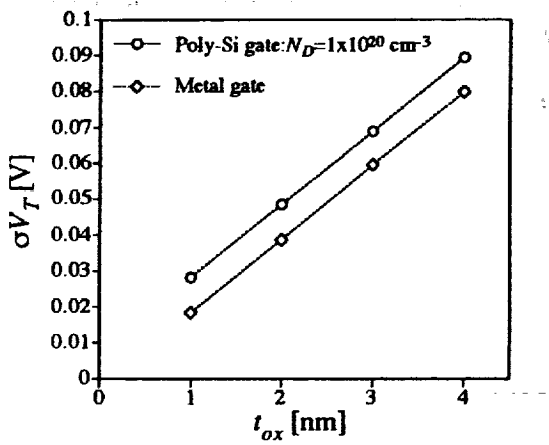

Figure 1. Dependence of σV_T on the oxide thickness t_{ox}: a comparison between an n^+ polysilicon and a metal gate MOSFETs

The term 'metal gate' is used here, and everywhere else in this paper, to indicate that in the simulations a Dirichlet boundary condition was applied at the gate electrode keeping constant value of the potential on top of the gate insulator in the whole gate

area. This is despite the fact that the fixed value of the potential was eventually adjusted to take into account the workfunction of the actual polysilicon gate.

For the metal gate MOSFETs in Fig 2 σV_T scales linearly to zero with the corresponding scaling of t_{ox} within the accuracy of the statistical estimation. The values of σV_T corresponding to the polysilicon gate MOSFETs with different thickness of the gate oxide are shifted up almost parallel by approximately 10 mV in respect to the metal gate results.

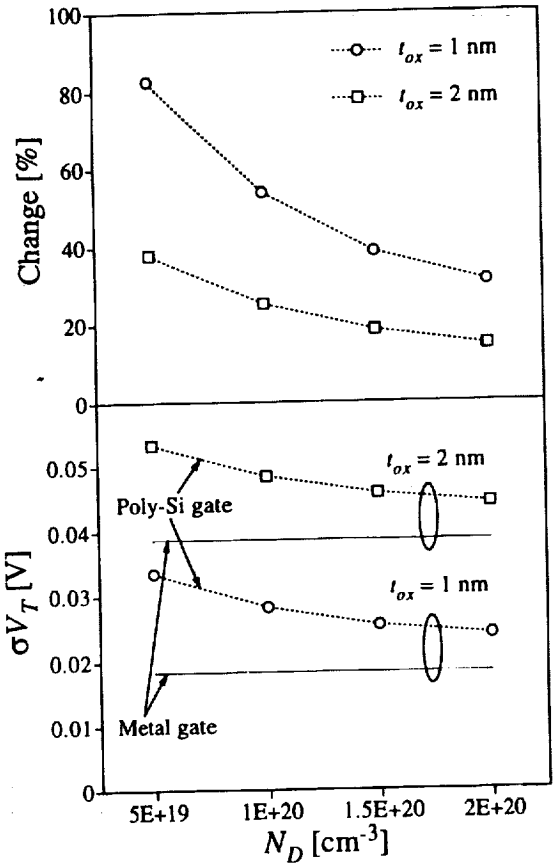

Figure 3. Dependence of the threshold voltage standard deviation σV_T on the pollisilicon doping concentration N_D. Uniform channel doping

The displacement associated with the polysilicon gate depends on the doping concentration in the polysilicon. The polysilicon doping concentration dependence of σV_T is plotted in Fig. 3 for two MOSFETs with gate oxide thickness 1 nm and 2 nm respectively, and with the same dimensions and channel doping concentrations as the devices in Fig. 2.

The percentage increase of σV_T compared to the metal gate simulations is illustrated in the same figure. The effect of the polysilicon gate increases rapidly when the doping concentration falls below $1x10^{20}$ cm^{-3}. There is a general agreement that the minimum thickness of the gate oxide, restricted primarily by the total on chip gate leakage current, will be between 1 and 2 nm. Since the dependence of σV_T on t_{ox} is linear it is easy to interpolate the results presented in Fig. 3 for any oxide thickness in this range. For oxide thickness 1.5 nm for example the contribution to the threshold voltage fluctuations varies from approximately 30% at polysilicon doping $2x10^{20}$ cm^{-3} to approximately 60% at polysilicon doping $5x10^{19}$ cm^{-3}.

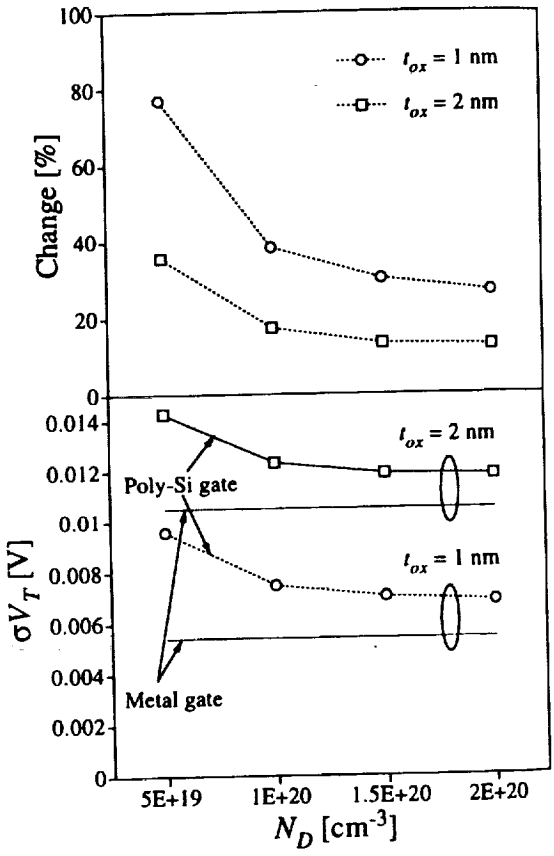

Figure 4. Dependence of the threshold voltage standard deviation σV_T on the pollysilicon doping concentration N_D. Epitaxial channel devices

An efficient approach to reduce the random dopant induced threshold voltage fluctuations without a drastic change in the MOSFET architecture is the introduction of a low doped epitaxial layer in the channel region. The polysilicon doping concentration dependence of σV_T is plotted in Fig. 4 for two epitaxial channel MOSFETs with gate oxide thickness 1 nm and 2 nm respectively, and with the same dimensions and channel doping concentrations as the devices in Fig. 3. Similarly to Fig. 3 the percentage increase of the threshold voltage fluctuations compared to the metal gate simulations is illustrated in the same figure. It has to be pointed out that over the whole range of polysilicon doping concentrations the relative increase of the threshold voltage fluctuations in the epitaxial channel MOSFETs is smaller than the corresponding increase in the devices with uniform channel doping.

Furher simulation experiments are needed in order to separate the contributions to the polysilicon gate threshold voltage fluctuation enhancement due to the effective increase in the oxide thickness associated with the polysilicon depletion from the direct contribution of the random dopants in the gate polisilicon depletion layer.

4. Conclusions

The polysilicon gate is responsible for a significant fraction of the random dopant induced threshold voltage fluctuations in sub 100 nm MOSFETs with tunnelling gate oxides. The polysilicon gate enhancement of σV_T increases with the reduction of the polysilicon doping concentration at the poly-Si/SiO_2 interface and may exceed 50% in 50x50 nm devices with tunnelling gate oxides in the range of 1 - 2 nm.

5. Acknowledgement

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6. References

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