Increase in the Random Dopant Induced Threshold Fluctuations and Lowering in Sub 100 nm MOSFETs due to Quantum Effects: A 3-D Density-Gradient Simulation Study

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Abstract

In this paper we present a detailed simulation study of the influence of quantum mechanical effects in the inversion layer on random dopant induced threshold voltage fluctuations and lowering in sub 100 nm MOSFETs. The simulations have been performed using a 3-D implementation of the density gradient (DG) formalism incorporated in our established 3-D atomistic simulation approach. This results in a self-consistent 3-D quantum mechanical picture, which implies not only the vertical inversion layer quantisation but also the lateral confinement effects related to current filamentation in the 'valleys' of the random potential fluctuations. We have shown that the net result of including quantum mechanical effects, while considering statistical dopant fluctuations, is an increase in both threshold voltage fluctuations and lowering. At the same time, the random dopant induced threshold voltage lowering partially compensates for the quantum mechanical threshold voltage shift in aggressively scaled MOSFETs with ultrathin gate oxides.

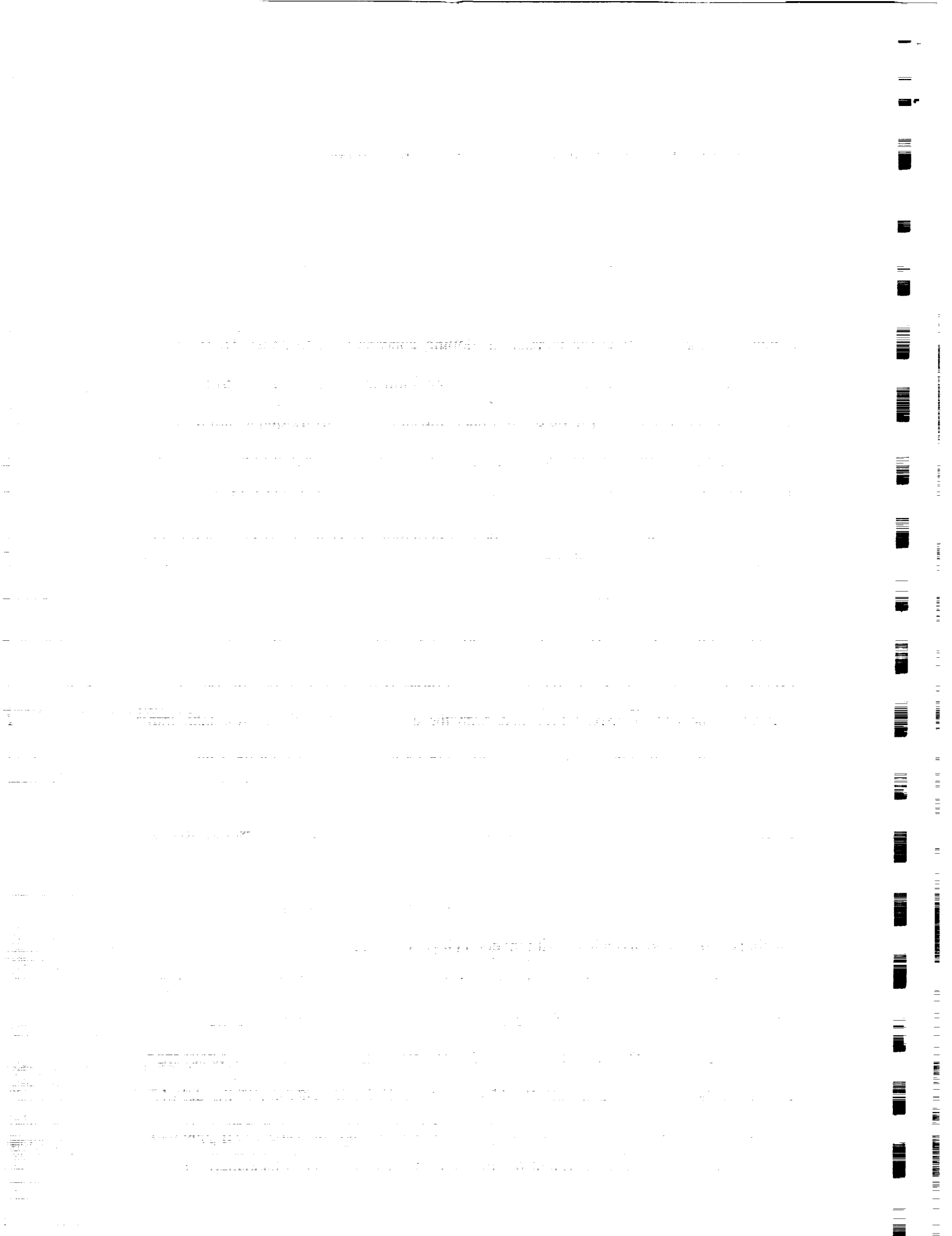
Index Terms - Dopant fluctuation, quantum effects, MOSFETs, numerical simulation, 3-D, threshold

I. Introduction

MOSFET threshold voltage variation due to statistical fluctuations in the number and position of dopant atoms [1],[2],[3],[4] becomes a serious problem when MOSFETs are scaled to sub 100 nm dimensions [5],[6],[7],[8]. This is complemented by a pronounced threshold voltage lowering [4], [8] associated with current percolation through valleys in the potential distribution at the interface due to the random position of dopants. At the same time the increase in doping concentration to above 1×10^{18} cm^{-3}, and the reduction in the oxide thickness to below 3 nm in sub 100 nm MOSFETs [5], result in a large surface electric field, even near threshold, and strong quantization in the direction perpendicular to the channel [9],[10],[11], with a corresponding increase in threshold voltage, and reduction in gate capacitance and drive [12],[13],[14],[15].

The realistic modelling of dopant fluctuation effects in deep submicron MOSFETs requires a 3-D numerical simulation, with fine grain discretization, and a statistical analysis of the results from the simulation of a statistical sample of devices [4], [8], [16]. All previous 3-D simulation studies of random dopant fluctuation effects [4],[7],[8],[16],[17],[18],[19],[20],[21] use a simple drift-diffusion or, in one case, hydrodynamic [22] approximation, and, with the exception of [22], do not take into account quantum effects. However, [22] does not explicitly demonstrate the role of the quantum effects on MOSFET parameter fluctuations. Until now it was unclear to what extent the quantum effects would affect the random dopant induced threshold voltage fluctuations and lowering in aggressively scaled MOSFETs with ultrathin gate oxides, and to what degree the threshold voltage lowering may compensate for the increase in the threshold voltage associated with inversion layer quantization.

In this paper we study the influence of the quantum effects in the inversion layer on the random dopant induced threshold voltage fluctuations and lowering in sub 100 nm MOSFETs. The quantum mechanical effects are incorporated in our established 3-D atomistic simulation approach [8], [16] using a 3-D implementation of the density-gradient (DG) model [23]. This results in a self-consistent, fully 3-D, quantum mechanical picture which accounts for the vertical inversion layer quantization, lateral



confinement effects associated with the current filamentation in the 'valleys' of the potential fluctuation, and, according to [24],[25], tunnelling through the sharp potential barriers associated with individual dopants. The next section describes the 3-D implementation of the DG model in an atomistic context, outlining the equations, the solution domain, the boundary conditions and the numerical procedures. In Section III we calibrate and validate the DG simulations with respect to comprehensive quantum mechanical calculations based on the full band formalism [11], comparing the published quantum mechanical threshold voltage shifts and inversion layer charge distributions with the results of DG simulations. 3-D atomistic simulation results highlighting the influence of the quantum mechanical effects on the random dopant induced threshold voltage fluctuations and lowering are presented and analysed in Section IV.

II. Simulation Approach

A Hydrodynamic interpretation of the quantum mechanics and quantum corrections to the fluid equations was proposed in the late twenties [26] and elaborated further by several authors [27]. In a form similar to the form adopted in this paper, density gradient quantum corrections have been used in 2-D hydrodynamic simulations of MESFETs and HEMTs [28]. As demonstrated in [29], to lowest order, the quantum system behaves as an ideal gradient gas for typical low-density and high-temperature semiconductor conditions. Assuming a scalar effective mass, quantum corrections have been included in the drift-diffusion set of semiconductor equations by introducing an additional term in the carrier flux expression

$$F_n = n\mu_n \nabla\psi - D_n \nabla n + 2\mu_n \nabla\left(b_n \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} \right), \tag{1}$$

where $b_n = \hbar^2 / \left(12\, q m_n^*\right)$, and all other symbols have the conventional meaning. The quantum correction term in (1) is referred to as 'quantum diffusion' since its inclusion yields a theory, that contains both quantum confinement effects and quantum-mechanical tunnelling [24, 25, 29]. A robust approach has been proposed in [23] to avoid the discretization of fourth order derivatives when using (1) in multidimensional

numerical simulations. By introducing a generalised electron quasi-Fermi potential ϕ_n according to the expression $F_n = n\mu_n \nabla \phi_n$, the unipolar drift-diffusion system of equations with QM corrections, which in many cases is sufficient for MOSFET simulations, becomes:

$$\nabla \cdot (\varepsilon \nabla \psi) = -q\left(p - n + N_D^+ - N_A^-\right) \tag{2}$$

$$2b_n \frac{\nabla^2 \sqrt{n}}{\sqrt{n}} = \phi_n - \psi + \frac{kT}{q} \ln \frac{n}{n_i} \tag{3}$$

$$\nabla \cdot (n\mu_n \nabla \phi_n) = 0 \tag{4}$$

where ψ, ϕ_n and $\sqrt{n}$ are independent variables. The right-hand side of (3) represents the Boltzmann statistics for electrons and the left-hand side can be interpreted as a quantum mechanical correction to the Boltzmann statistics. At the same time, (3) is a nonlinear partial differential equation, which closely resembles the Schrödinger equation, and a microscopic expression for the macroscopic factor b_n has been derived in [29] based on this analogy.

Similarly to the approach outlined in [16], at low drain voltage, in linear mode of MOSFET operation, we consider a constant quasi-Fermi potential in the simulations which decouples (2) and (3) from (4). Therefore we solve self-consistently the 3D Poisson equation (2) for the potential, and equation (3) for the electron concentration. In the iterative solution process the electron concentration obtained from the solution of (3), together with Boltzmann statistics for the hole concentration p, are used in the solution of (2).

A typical atomistic simulation domain used in the simulation of a 30×50 nm n-channel MOSFET with oxide thickness $t_{ox} = 3$ nm and a junction depth $x_j = 7$ nm is outlined in Fig. 1. The uniform doping concentration in the channel region $N_D = 5\times10^{18}$ cm^{-3} is resolved down to an individual dopant level using fine grain discretization with typical mesh spacing 0.5 nm, much less than the typical spacing between impurities. The number of dopants in the random dopant region of each

individual transistor follows a Poisson distribution. The position of dopants is chosen at random and each dopant is assigned to the nearest grid node. By varying the mesh spacing we have checked that the error associated with the charge assignment is less than 1% for the devices simulated in this paper. More complex doping profiles in the random dopant region of the device may be introduced using a rejection technique.

Standard boundary conditions are used for the potential in the Poisson equation (2) with zero bias applied at the source and drain contacts according to the adopted constant quasi Fermi level approximation. Dirichlet boundary conditions are applied to electrons in the DG equation (3) at the contacts and Si/SiO_2 interface introducing charge neutrality and vanishingly small values respectively, and Neumann boundary conditions are applied at all other boundaries of the solution domain. One step Newton-SOR iterations are used for solving both the Poisson (2) and the DG (3) equations [30]. At the beginning of the self-consistent iteration, the nonlinear Poisson equation is solved using Boltzmann statistics for both electrons and holes.

The current at low drain voltage is calculated by solving a simplified current continuity equation (5), in a drift approximation only [16], in a thin slab near the Si/SiO_2 interface engulfing the inversion layer charge:

$$\nabla \cdot \mu_n n \nabla V = 0 \tag{5}$$

Dirichlet boundary conditions are applied for the 'driving' potential, V, at the source and drain contacts, with $V = 0$ and $V = V_D$ respectively, and Neumann boundary conditions are applied at all other boundaries of the slab. Drain voltage $V_D = 10$ mV is used in all simulations. The current is extracted by integrating the drift current density $J_n = \mu_n n \nabla V$ along a cross section of the slab. The described procedure is equivalent to calculating the conductance of the device. We have demonstrated [16] that at low drain voltage, in the drift-diffusion approximation, the approach described above reproduces with high accuracy the results obtained from the self consistent solution of the Poisson and the electron drift-diffusion equation.

The current criterion $I_T = 10^{-8} W_{eff}/L_{eff}$ [A] is used to estimate the threshold voltage, V_T. Typically, samples of 200 microscopically different transistors are simulated for each combination of macroscopic design parameters, in order to extract the average threshold voltage, $\langle V_T \rangle$, and its standard deviation σV_T. The corresponding relative standard deviation of the extracted σV_T is $\sigma_{\sigma V_T}$=5% for all results presented in this paper.

Fig 2 illustrates the potential distribution obtained from the self-consistent solution of (2) and (3) in the solution domain outlined in Fig. 1 at gate voltage equal to the threshold voltage. Strong potential fluctuations at the Si/SiO_2 interface associated with the discrete dopants can be observed. One electron equi-concentration contour which corresponds to this solution is presented in Fig. 3. The equi-concentration contour highlights the basic features of the quantum charge distribution. The quantum confinement in the channel results in a maximum in the electron concentration which is located approximately 1.5 nm below the interface. The 3-D solution of (3), within the limitations of the scalar effective mass approximation, captures the lateral confinement in current channels percolating through the 'valleys' in the fluctuation surface potential.

III. Calibration

Since the DG model accounts for lowest-order quantum effects, and equation (3) can be considered only as an approximation to the Schrödinger equation, the DG model has to be carefully validated (and eventually calibrated) against a full, self-consistent solution of the Poisson-Schrödinger equation before being used further in our atomistic simulations. To some extent such validation/calibration has already been carried out in [23] in comparison with an ellipsoidal band Poisson-Schrödinger solver, but only in respect of C-V calculations. Here we are more concerned about correct prediction of the threshold voltage shift and the quantum mechanical charge distribution in the inversion layer, which will be affected further by the random dopant induced potential fluctuations.

The DG validation/calibration is a difficult task in 3-D, particularly in a complex solution domain representing a MOSFET, and potential incorporating fluctuations from discrete dopants. Therefore we validate the DG approach against rigorous full band

Poisson-Schrödinger simulations [11] in the 1-D case only, and for continuous doping. The DG results for the quantum mechanical threshold voltage shift, $V_T(QM) - V_T(Classical)$, shown in Fig. 4, using a value of electron effective mass, $m^* = 0.19m_0$, as recommended in [23], are in good agreement with the shift reported in [11]. The range of doping concentrations in this comparison corresponds to the channel doping in properly scaled MOSFETs with channel lengths below 100 nm. Although the above value of the effective mass is identical to the transverse electron mass in Si, there is no physical reason for using the transverse electron mass in (3). Indeed in the [001] direction considered here the interface confinement lifts the degeneracy of the sixfold ellipsoidal (at low k) conducting bands of Si. The total electron concentration in the inversion layer is composed of the electron concentrations in the subbands corresponding to the two ellipsoids with longitudinal effective mass normal to the interface ($m^* = 0.916m_0$) and the four ellipsoids with transfer effective mass parallel to the interface ($m^* = 0.19m_0$). Although not only the lowest subband related to $m^* = 0.916m_0$ is occupied at room temperature and contributions from the subbands corresponding to $m^* = 0.19m_0$ can be expected, the effective mass needed to calibrate the DG model is unphysical low and has to be treated as a fitting parameter. To illustrate this point further, we present in Fig. 5 the dependence of the quantum mechanical threshold voltage shift as a function of the value of m^* used in the DG simulations for doping concentration $N_A = 3\times10^{18}$ cm^{-3} and oxide thickness t_{ox} =4 nm. Exact agreement with the shift predicted in [11] at this doping concentration occurs for $m^* = 0.175m_0$ which is even lower that the value suggested in [23].

Fig. 6 compares the electron concentration distributions obtained using the DG model with a full band Poisson-Schrödinger simulation. The parameters in both simulations are selected to allow a direct comparison with the results presented in [11]. Good agreement between the electron distributions obtained from the two models is observed with an inversion charge distribution slightly narrower and a charge centroid slightly closer to the interface in the DG simulation. Similar level of accuracy has to be expected in the [010] and the [100] directions which are equivalent to the [001] direction

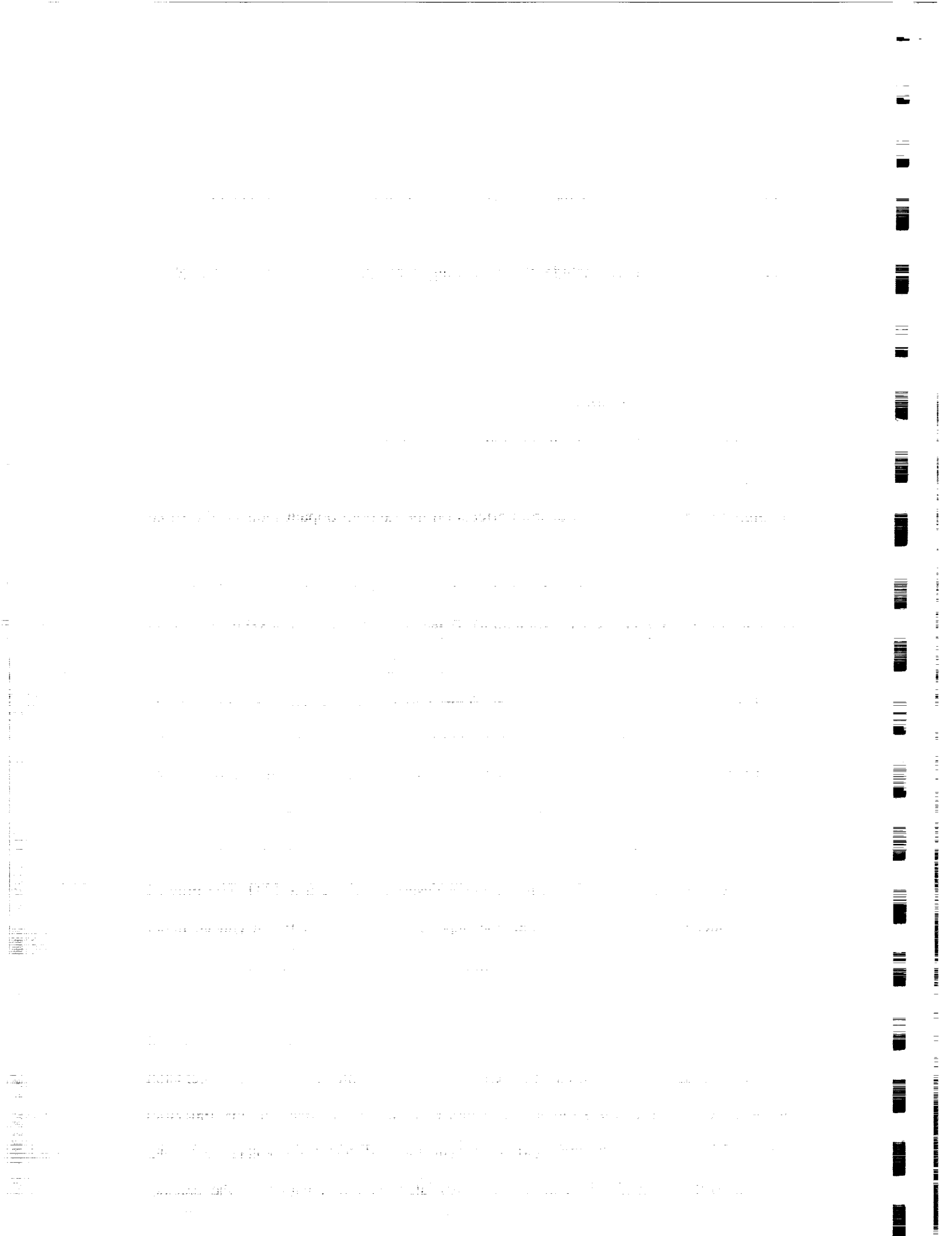
in terms of band structure end the expected quantum confinement effects. In an arbitrary direction we have to accept the limitation of the single effective mass in this first attempt to incorporate quantum mechanical effects in the 3-D 'atomistic' simulation picture.

Although theoretically the DG approach also accounts for tunnelling [24][25], which in our case may include the tunnelling through the Coulomb potential of individual dopants, no attempt has been made to calibrate the DG approach in respect of this phenomenon.

IV. Results and Discussion

In this section, we compare the results of DG atomistic simulations with previously published, purely classical atomistic simulation results [8], in order to highlight the influence of the quantum effects on the random dopant induced threshold voltage fluctuations and lowering.

The dependence of the threshold voltage on oxide thickness, obtained from classical and from quantum DG simulations, is presented in Fig. 7 for MOSFETs with uniform doping concentration in the channel region $N_A = 5\times10^{18}$ cm^{-3}, effective channel length $L_{eff} = 50$ nm, channel width $W_{eff} = 50$ nm and junction depth $x_j = 7$ nm. Results for the average threshold voltage, $\langle V_T \rangle$, obtained from atomistic simulations, and for the threshold voltage, V_{T0}, obtained from continuous charge simulations are compared. For completeness we provide here and in all following figures also results which take into account the poly-Si depletion and the random dopant distribution in the poly-Si gate, together with the quantum effects, in a manner described in detail in [31]. The poly-Si doping concentration used throughout the paper is $N_D = 1\times10^{20}$ cm^{-3}. It can be noted that for oxide thickness $t_{ox} = 4$ nm the quantum mechanical shift in the threshold voltage obtained from full 3-D DG simulation of MOSFETs with continuous doping agree well with the 1-D DG result presented in Fig. 4. As expected [11] the quantum mechanical threshold voltage shift decreases with the reduction in the oxide thickness. The inclusion of the poly-Si gate in the simulations results in additional increase in the threshold voltage. Most importantly the random dopant induced threshold voltage lowering, inherent to the atomistic simulations, and associated with percolation of the channel



current through 'valleys' in the potential fluctuations, is enhanced in the quantum case. This becomes clear from Fig. 8 where the threshold voltage lowering $\langle V_T \rangle - V_{T0}$ extracted from the data presented in Fig. 7 is plotted as a function of the oxide thickness and compared for the classical and quantum simulations. Although the magnitude of the threshold voltage lowering decreases almost linearly with the reduction of the oxide thickness in both cases, the relative quantum mechanical increase of the lowering becomes larger than 50% for oxide thicknesses below 2 nm and reaches almost 100 % for the limiting oxide thickness of 1 nm.

The dependencies of the threshold voltage standard deviation, σV_T, as a function of the oxide thickness, extracted from classical and from quantum atomistic simulations, are compared in Fig. 9 for MOSFETs with the same parameters as the devices in Fig. 7. In the classical simulations σV_T scales linearly to zero with the corresponding scaling of t_{ox}, within the accuracy of the statistical estimations. This derives from the fact that a Dirichlet boundary condition was applied at the gate electrode during the simulations, keeping constant the value of the potential on top of the gate insulator. Such a 'metal gate' boundary condition completely screens and flattens the potential fluctuations at the Si/SiO_2 interface when the oxide becomes infinitesimally thin. This in turns kills the threshold voltage fluctuations since the maximum of the classical inversion layer charge distribution and channel current density occurs at the interface. The values of σV_T corresponding to the quantum simulations are shifted up with respect to the classical simulations, and the shift increases slightly with the increase in the oxide thickness. This shift can be partially explained by the fact that the inversion layer centroid in the quantum simulations is below the interface and results in an increase in the effective oxide thickness. Using a relatively crude approximation, this can be taken into account simply by shifting the straight line approximating the classical dependence of σV_T on the oxide thickness along the oxide thickness axis by:

$$\Delta = \varepsilon_{ox} z_i / \varepsilon_{Si} \tag{6}$$

where z_i is the inversion layer centroid. According to [32], at doping concentration $N_D = 5\times10^{18}$ cm^{-3} the inversion layer centroid is z_i = 1.12 nm which corresponds to a shift of $\Delta = 0.37$ nm. The classical σV_T dependence shifted by this value lies below but rather close to the values of σV_T obtained from the quantum mechanical. This is an indication that substantial fraction of the quantum increase of the threshold voltage fluctuations can be attributed to the effective increase in the oxide thickness. Other factors like the lateral confinement effects in the current channels and the quantum mechanical broadening of the inversion layer charge have additional contributions.

It should be noted also that the inclusion of the poly-Si gate in the simulations results in additional increase of σV_T which, in combination with the increase associated with the quantum mechanical effects, almost doubles the threshold voltage fluctuations for oxide thicknesses below 2 nm.

The atomistically simulated average threshold voltage, $\langle V_T \rangle$, for a set of MOSFETs with different channel lengths is compared in Fig. 10 with the threshold voltage, V_{T0}, of devices with continuous doping. The devices have oxide thickness $t_{ox} = 3$ nm, and all other parameters similar to the MOSFETs from Fig. 7. Both results from classical atomistic simulation and simulations including DG correction for the quantum mechanical effects are presented in the same figure. Let us focus first on the classical and the quantum mechanical simulations with continuous doping. The quantum mechanical shift in the threshold voltage exhibits a channel length dependence, and decreases with the reduction in the channel length, from 292 mV at $L_{eff} = 100$ nm to 271 mV at $L_{eff} = 30$ nm. This can be interpreted as an increase in the short channel effects in the quantum mechanical simulations as a result of an increase in effective oxide thickness associated with the location of the inversion charge centroid below the Si/SiO_2 interface. The inclusion of the poly-Si gate increases even more the effective oxide thickness as a result of the poly-depletion and results in a further increase in the short channel effects.

In order to interpret clearly the results of the atomistic simulations presented in Fig 10 we compare in Fig. 11 the corresponding threshold voltage lowering, $\langle V_T \rangle - V_{T0}$,

in the classical and quantum case. The threshold voltage lowering in the quantum mechanical atomistic simulations increases faster than the threshold voltage lowering in the classical simulations with the reduction of the channel length. This can be interpreted as an additional increase of the short channel effects in the quantum mechanical atomistic case. Bearing in mind that the threshold voltage lowering results from an early percolation of current through valleys in the potential fluctuations in the plane of current flow we speculate that the increase of the threshold voltage lowering with the reduction of the channel length has two aspects. Firstly the length of the percolation paths decreases which reduces the percolation threshold. Secondly the discrete doping distribution results in localized regions with higher and lower than the average doping concentrations. In the regions with lower doping concentration the 2-D effects associated with the penetration of the source/drain potential in the channel are stronger and in interaction with dominant percolation paths this results in further threshold voltage lowering when the channel length is reduced. In the quantum mechanical case the increased effective thickness of the oxide increases further the influence of the source/drain potential on the potential distribution and lowering in the channel region and hence through the second mechanism increases the threshold voltage lowering. The threshold voltage lowering, which reaches more than 110 mV in a 30 nm MOSFET, compensates for a significant portion of the quantum mechanical threshold voltage shift.

Finally, Fig. 12 compares channel length dependence of the standard deviations in the threshold voltage σV_T calculated using classical and quantum mechanical atomistic simulations. The quantum mechanical increase in σV_T is more pronounced at the shorter channel lengths and ranges from 23% at the 100 nm MOSFETs to 25% at transistors with 30 nm channel length. The inclusion of the poly-Si gate in the simulations increases σV_T by another15% over the whole range of channel lengths.

V. Conclusions

In this paper we have presented a 3-D atomistic Density Gradient simulation approach for determining the threshold voltage in aggressively scaled MOSFETs, which takes into account both the discrete random dopant distribution in the channel region

and the quantum effects in the inversion layer. It accounts for random dopant induced threshold voltage fluctuations and lowering, and quantum mechanical threshold voltage shift in a self consistent manner.

We have demonstrated that the introduction of quantum effects in the previously published 3D statistical atomistic simulations results in an increase in both threshold voltage fluctuations and lowering. The quantum increase in the threshold voltage fluctuations amounts to more than 50% in MOSFETs with oxide thicknesses below 1.5 nm, expected near the end of the Silicon Roadmap [5]. If, in addition, the poly-Si depletion and the discrete random dopants in the poly-Si gate are taken into account, the increase reaches 100% in devices with ultrathin gate oxides. At the same time, the quantum mechanical increase in the threshold voltage becomes partially compensated by the threshold voltage lowering due to atomistic effects. This compensation varies from 16% in 100 nm MOSFETs up to 40% in 30 nm devices.

The combination of quantum mechanical and random dopant effects, which are closely interlinked and may enhance or compensate each other, becomes very important in sub 100 nm MOSFETs and poses serious challenges for the development of the next generation of simulation tools.

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Figure Captions

Fig. 1 Typical atomistic simulation domain and dopant distribution used in the simulation of a 30×50 nm *n*-channel MOSFET with oxide thickness t_{ox} = 3 nm, junction depth x_j = 7 nm and channel acceptor concentration $N_A = 5\times10^{18}$ cm^{-3}.

Fig. 2 Potential distribution at threshold voltage obtained from the atomistic DG simulation of a 30×50 nm MOSFET with design parameters given in Fig. 1.

Fig. 3 One equi-concentration contour corresponding to the potential distribution in Fig. 2. The inversion charge distribution peaks below the Si/SiO_2 interface.

Fig. 4 Quantum mechanical threshold voltage shift as a function of the doping concentration. A comparison between 1-D DG and full band Poisson-Schrödinger results [11] at oxide thickness t_{ox} = 4 nm.

Fig. 5 Quantum mechanical threshold voltage shift as a function of the electron effective mass m^*, in 1-D DG simulation for acceptor concentration $N_A = 3\times10^{18}$ cm^{-3} and oxide thickness t_{ox} = 4 nm.

Fig. 6 Comparison of the 1-D charge distribution obtained from DG and full band Poisson-Schrödinger simulations for acceptor concentration $N_A = 5\times10^{17}$ cm^{-3}, oxide thickness t_{ox} =4 nm and inversion charge density 1.67×10^{11} cm^{-2}.

Fig. 7 Threshold voltage as a function of the oxide thickness in a 50×50 nm MOSFETs with channel doping concentration $N_A = 5\times10^{18}$ cm^{-3} and poly-Si gate doping $N_D = 1\times10^{20}$ cm^{-3}.

Fig. 8 Threshold voltage lowering as a function of the oxide thickness extracted from the data in Fig. 7.

Fig. 9 Threshold voltage standard deviation as a function of the oxide thickness for devices with the same parameters as in Fig. 7.

Fig. 10 Threshold voltage as a function of the effective gate length for MOSFETs with channel width W_{eff} =50 nm, channel doping concentration $N_A = 5\times10^{18}$ cm^{-3}, oxide thickness t_{ox} =3 nm and poly-Si gate doping $N_D = 1\times10^{20}$ cm^{-3}.

Fig. 11 Threshold voltage lowering as a function of the effective channel length extracted from the data in Fig. 10.

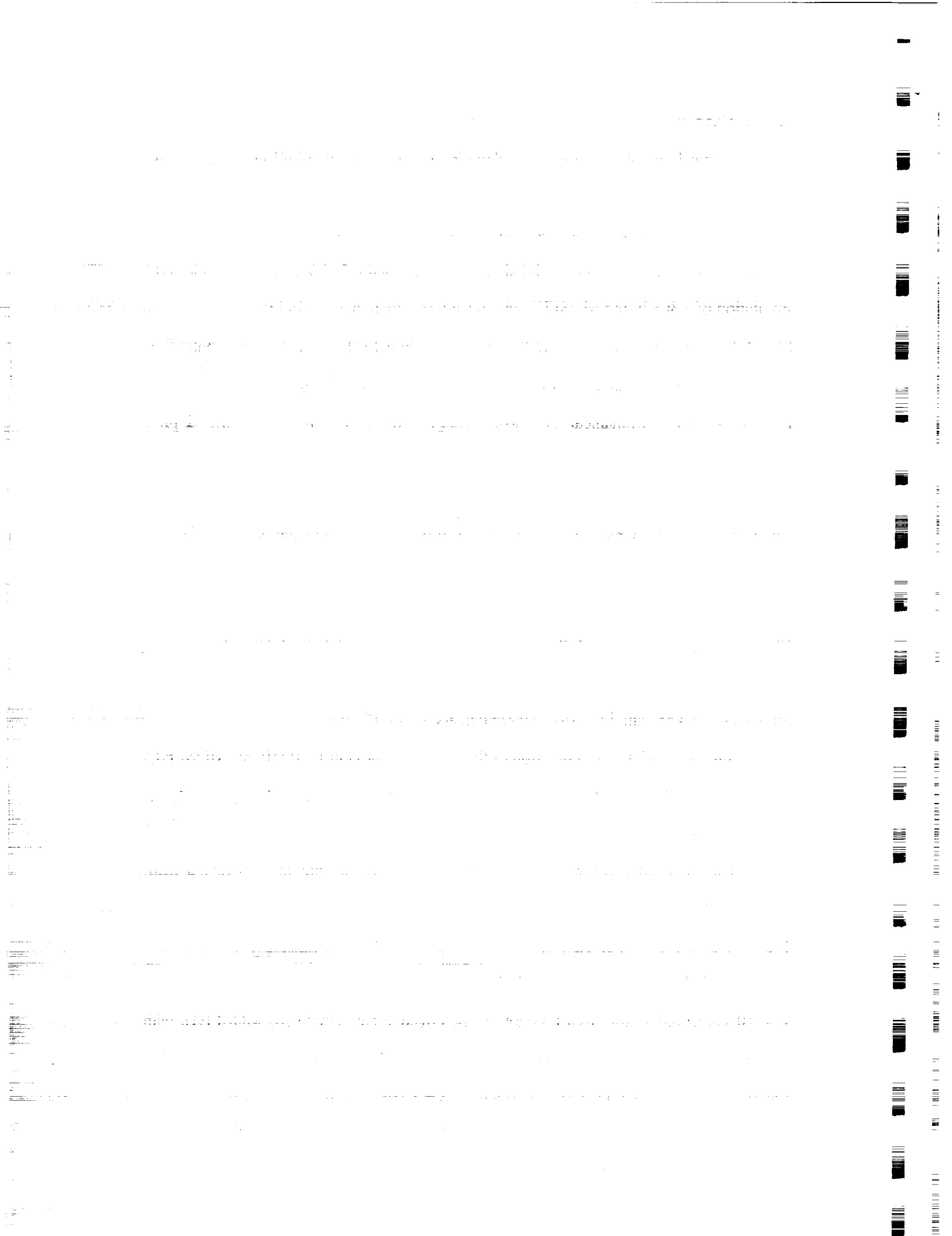


Fig. 12 Threshold voltage standard deviation as a function of the effective channel length for devices with channel doping concentration $N_A = 5\times10^{18}$ cm^{-3} and poly-Si gate doping $N_D = 1\times10^{20}$ cm^{-3}.

Biographies

A. Asenov

Asen Asenov (M'96) received his MSc degree in solid state physics from Sofia University, Bulgaria in 1979 and PhD degree in physics from The Bulgarian Academy of Science in 1989. He had 10 years industrial experience as a head of the Process and Device Modelling Group in IME - Sofia, developing one of the first integrated process and device CMOS simulators IMPEDANCE. In 1989–1991 he was a visiting professor at the Physics Department of TU Munich. He is currently Head of Department of Electronics and Electrical Engineering at the University of Glasgow. As a leader of the Device Modelling Group and academic director of the Process and Device Simulation Centre he also co-ordinates the development of 2D and 3D device simulators and their application in the design of FETs, SiGe MOSFETs and IGBTs. He has over 130 publications in process and device modelling and simulation, semiconductor device physics, 'atomistic' effects in ultra-small devices and parallel computing.

G. Slavcheva

Gabriela Slavcheva received her PhD degree in physics from The Bulgarian Academy of Sciences (BAS) in 1997 for theoretical work on the electron and phonon spectra and transport phenomena in low-dimensional disordered systems. She is currently working on a postdoctoral fellowship at the University of Glasgow. Before coming to Glasgow she was a Research Associate at the Institute of Biophysics and Institute of Solid State Physics, BAS, Sofia. She has spent two periods as a Visiting Professor at the Physics Department, Forum for Theoretical Science, Chulalongkorn University, Bangkok, Thailand working on path-integral calculation of electronic properties at the interface of disordered heterostructures and as a Research Fellow in the Institute of Acoustics, Rome, Italy, working on development of a 2D-solver for calculation of the acoustic phonon modes in composite membranes. Her research interests include theoretical investigation and modelling of electronic and optical properties of low-dimensional

disordered systems with special attention to the effect of random impurity distribution on the ultra-small device characteristics.

A. R. Brown

Andrew Brown received the B.Eng degree in Electronics and Electrical Engineering from the University of Glasgow in 1992. Since this time he has been a researcher in the Electrical Engineering Department at the University of Glasgow working on the development of parallel 3D simulators for semiconductor devices. He is currently developing a parallel 3D 'atomistic' simulator to investigate random dopant induced parameter fluctuations in sub-0.1 micron MOSFETs. Previous work include the simulation of Insulated Gate Bipolar Transistors (IGBTs). His interests include high performance parallel computing, device modelling and visualisation.

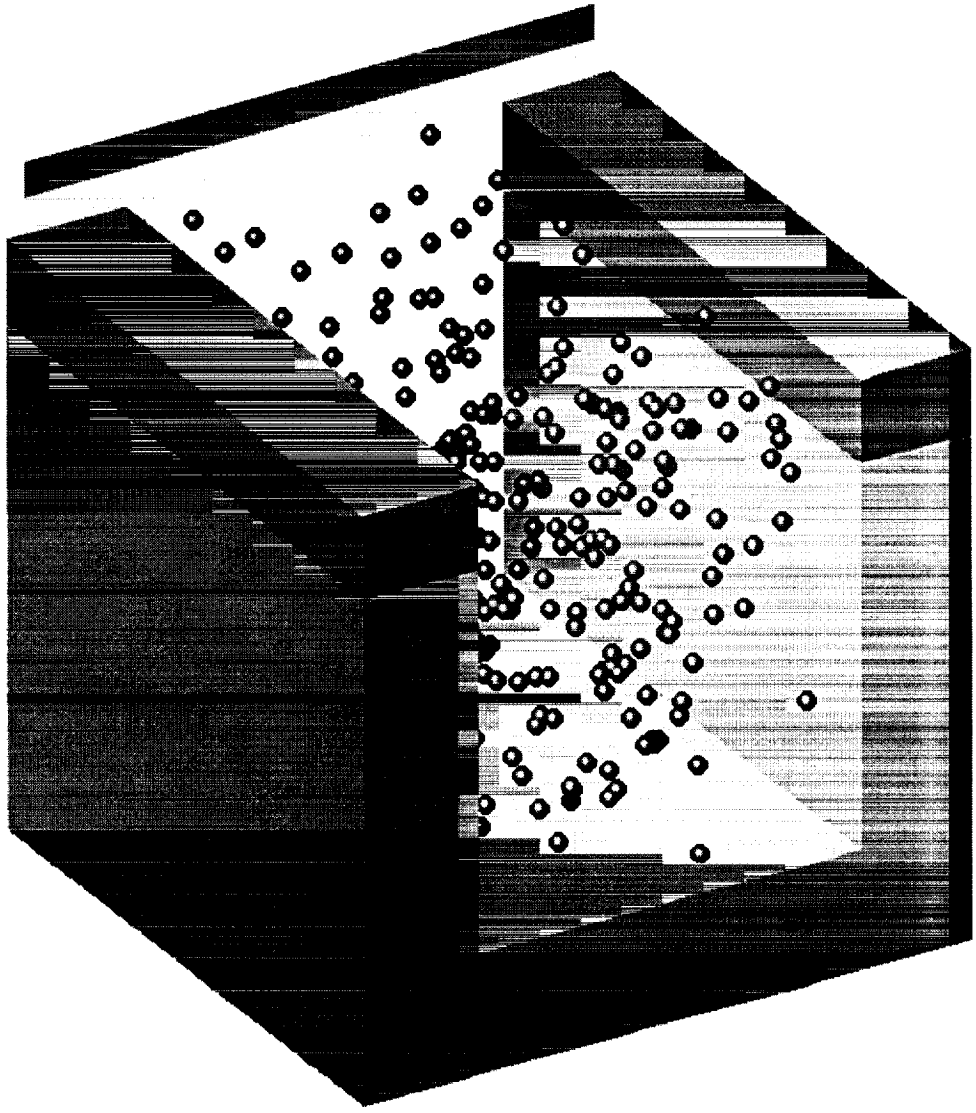
J. H. Davies

John H. Davies received his PhD from the University of Cambridge in 1982 for theoretical work on the electronic properties of amorphous semiconductors. He was a Research Fellow at Cornell University before coming to Glasgow University in 1986, and has since spent two periods of leave at Ohio State University and the University of California at Santa Barbara. Most of his research is centred on the physics of transport in III-V heterostructures. This has included the modelling of surfaces and gates, including the effect of stress from patterned surfaces and gates. He has been interested in the effect of discrete, random donors for many years, and previous research showed their destructive effect on quantum transport in ballistic devices at low temperature. Other interests include the theory of resonant tunnelling, conduction in lateral superlattices, and the calculation of magnetic fields in permanent-magnet motors.

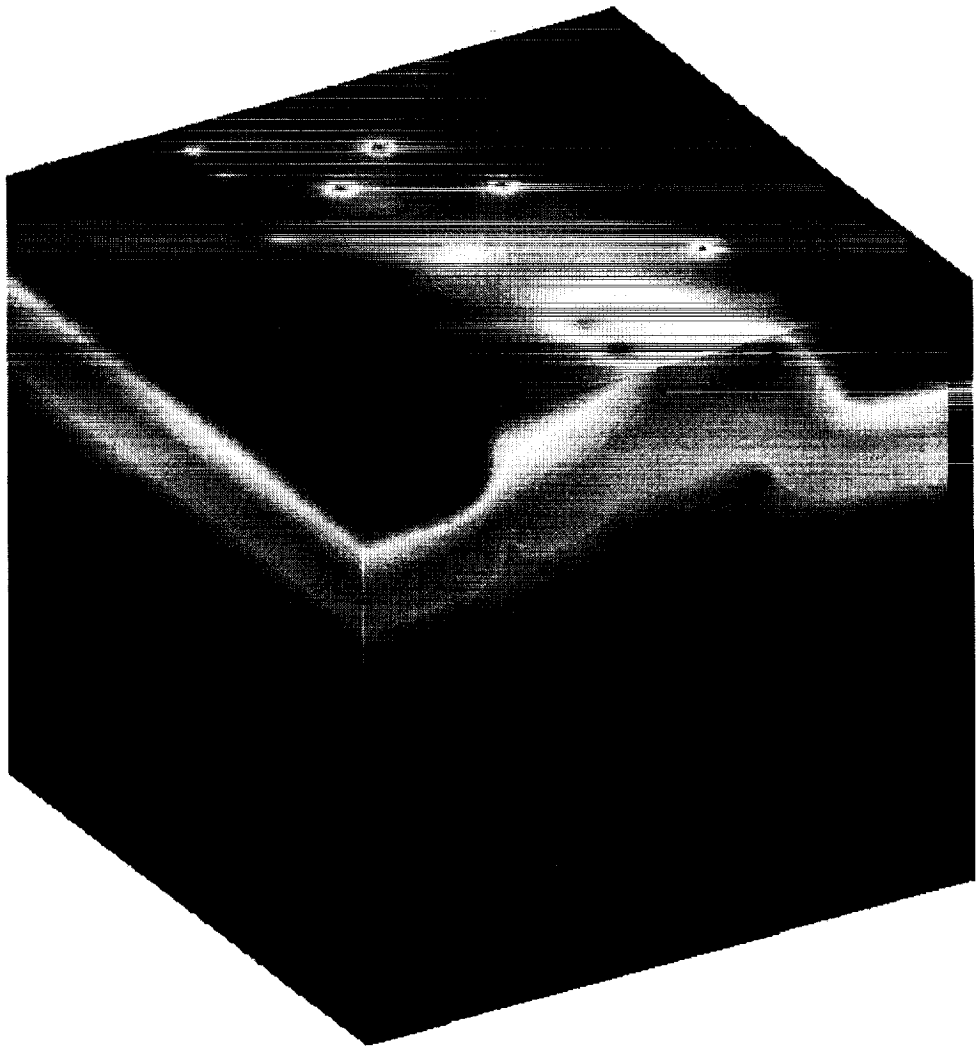
S. Saini

Subhash Saini received his Ph.D from the University of Southern California and has held positions at University of California at Los Angeles (UCLA), University of

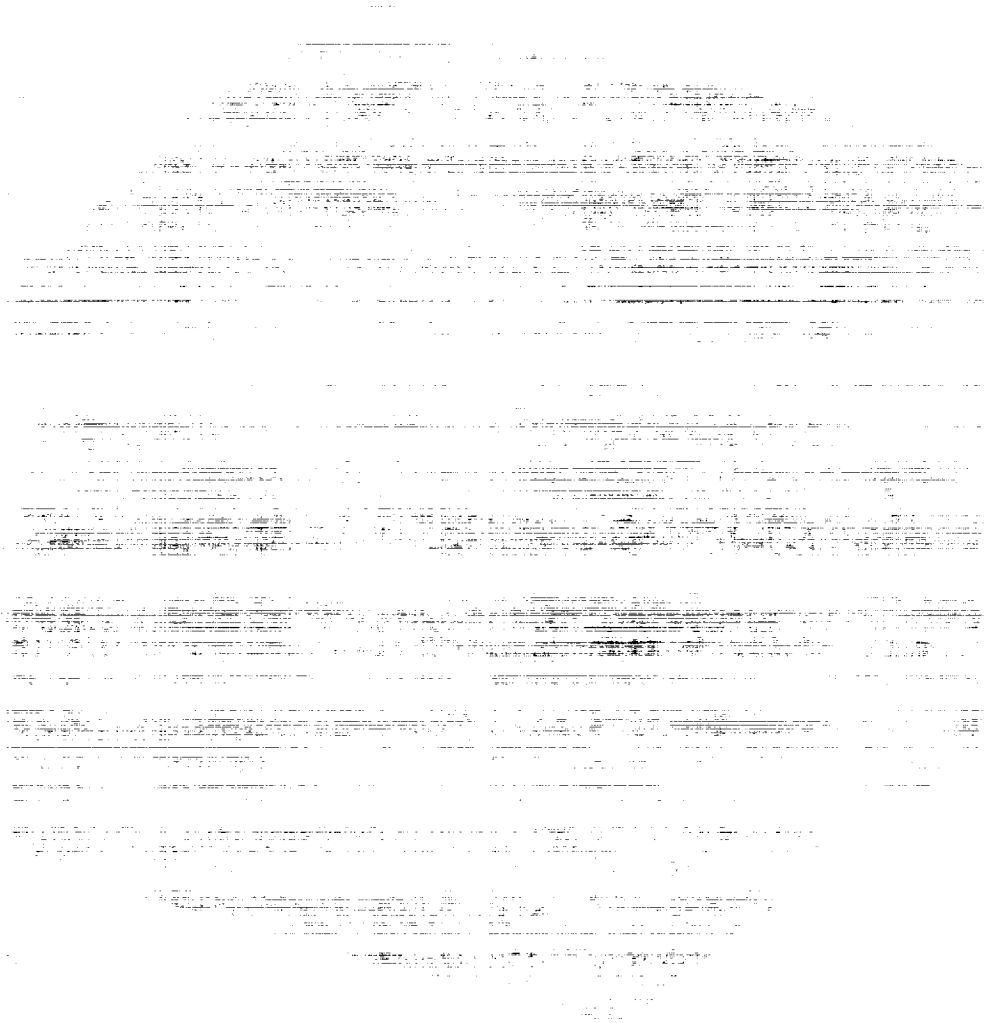
California at Berkeley (UCB), and Lawrence Livermore National Laboratory (LLNL). He has over 10 years experience of teaching Physics at B.S (Hons) and M.S level. His research interests involve performance evaluation and modeling of new generation of CMOS based processors and highly parallel computers. He has published over 80 technical papers in nuclear engineering, quantum scattering, nanotechnology, high temperature materials, operating systems, computer architectures and performance modeling of high-end computers, and presented over 100 technical talks. He joined NAS in 1989 and he was named the NAS-NASA employee of the year in 1991. Currently, he is manager of a department at NASA Ames Research Center which includes several groups such as Information Systems Performance Modeling; Algorithms, Architectures and Application; Information Power Grid Architectures; Legacy Codes Modernization; Higher Level Languages; Nanotechnology; and Device Modeling.

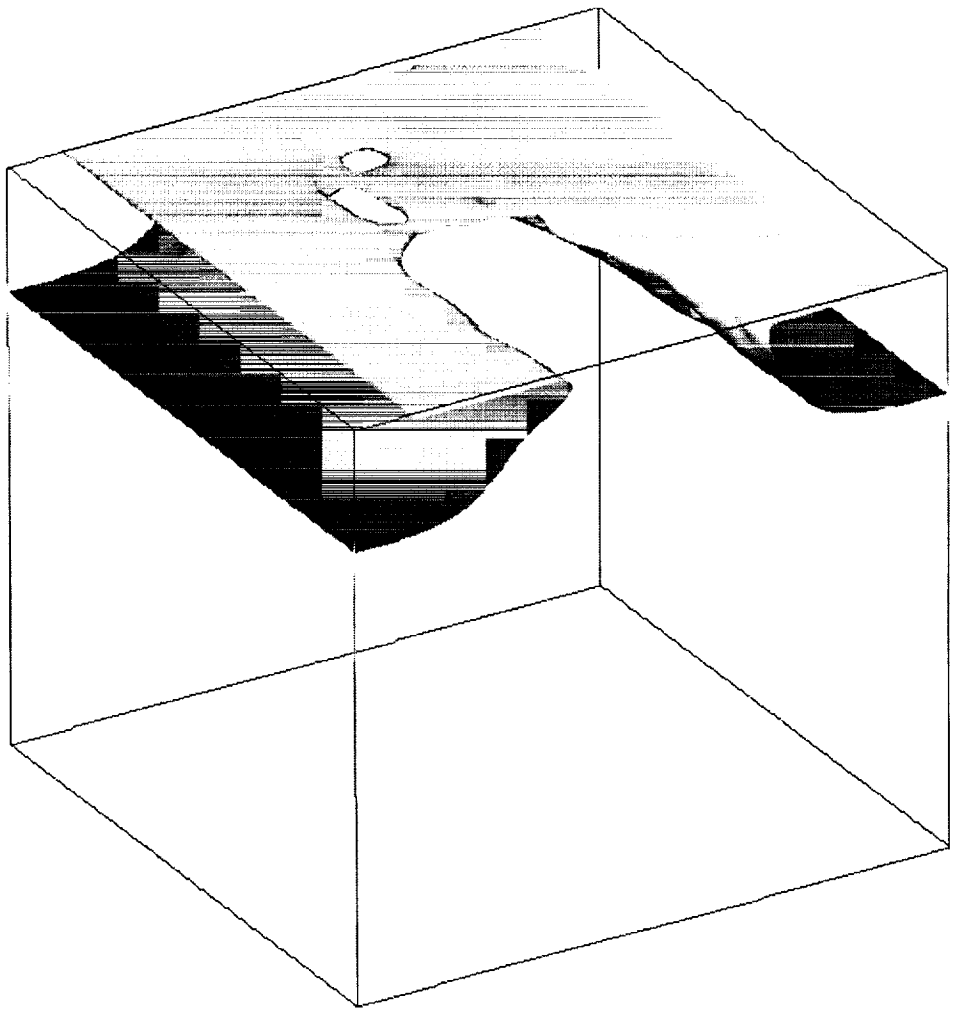


A. Asenov, *et al.* Fig. 1

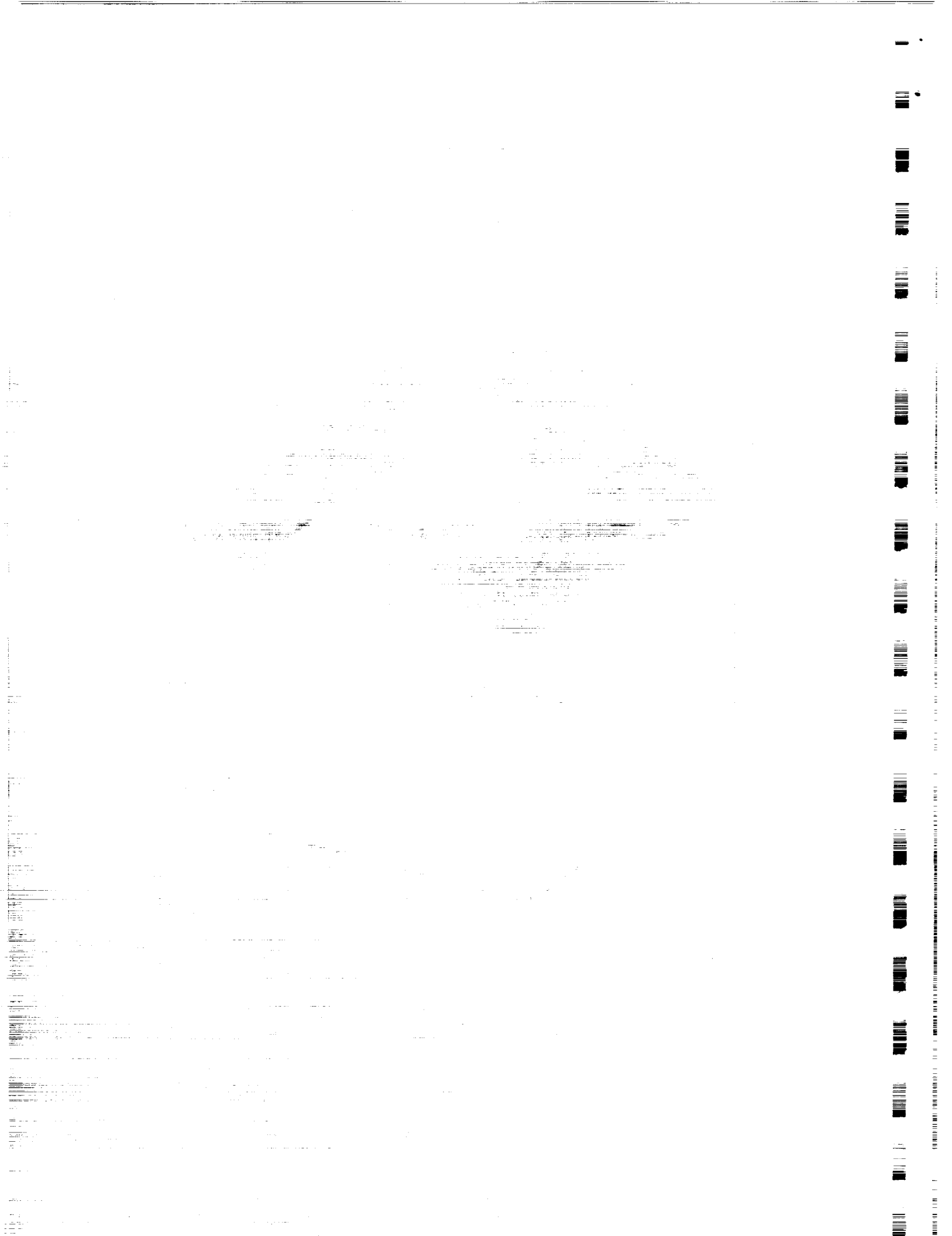


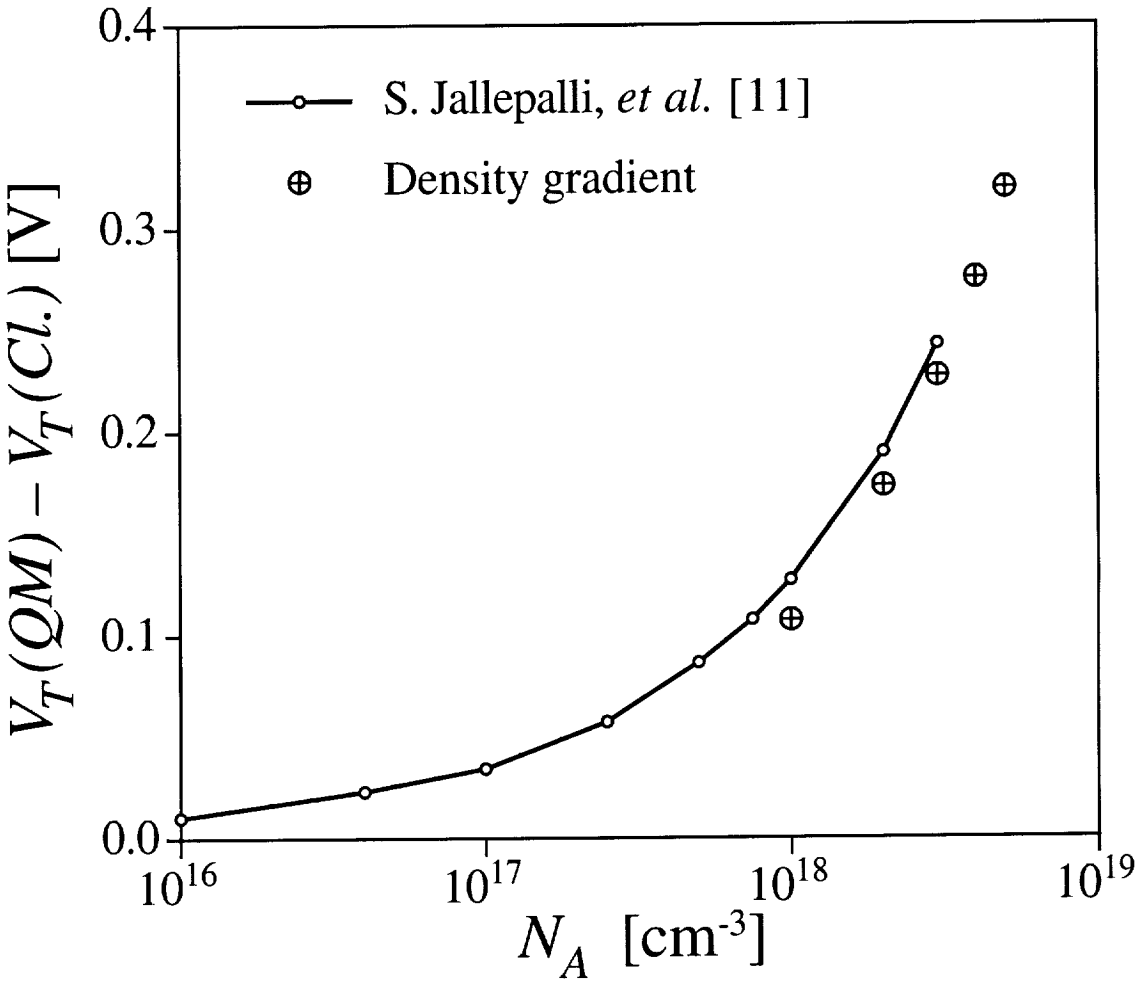
A. Asenov, *et al.* Fig. 2



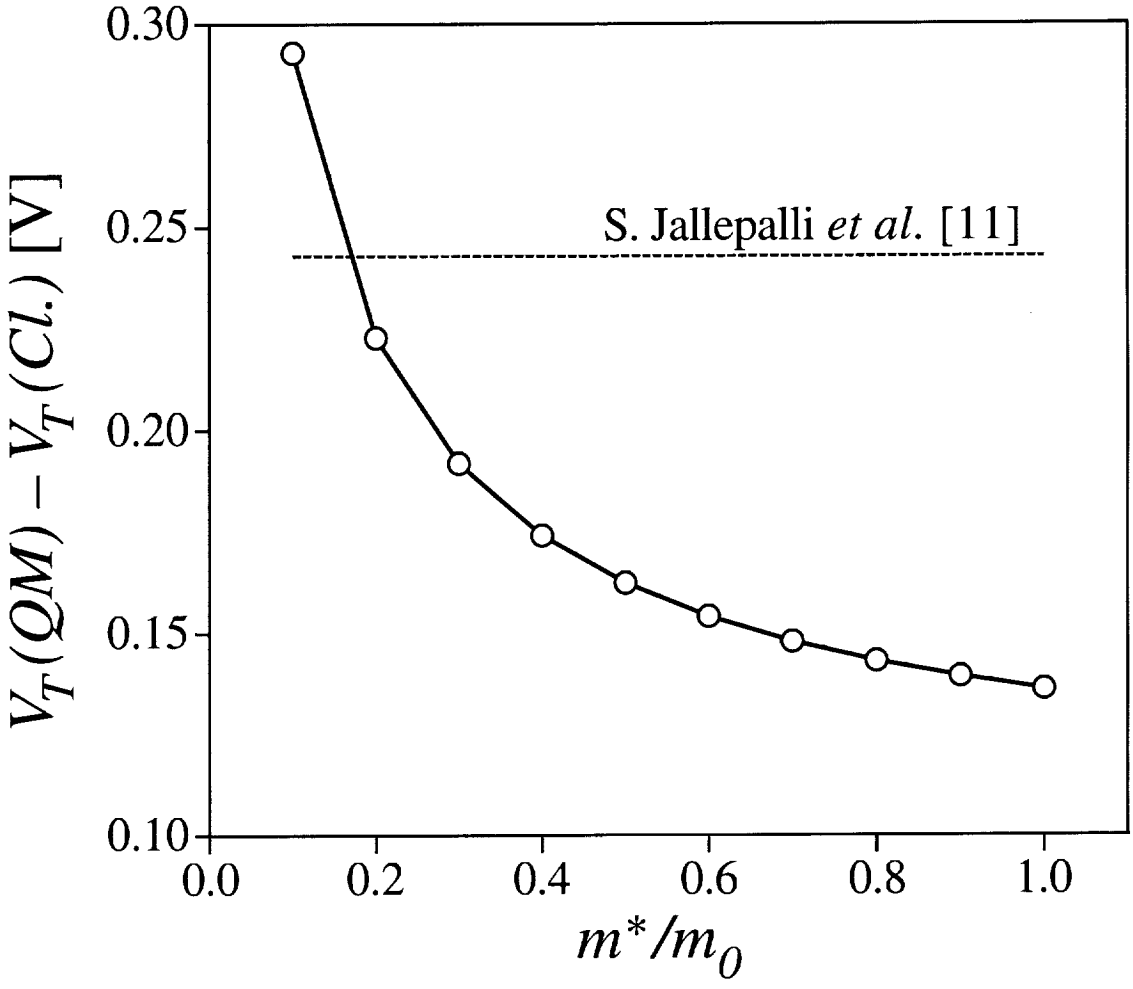


A. Asenov, *et al.* Fig. 3

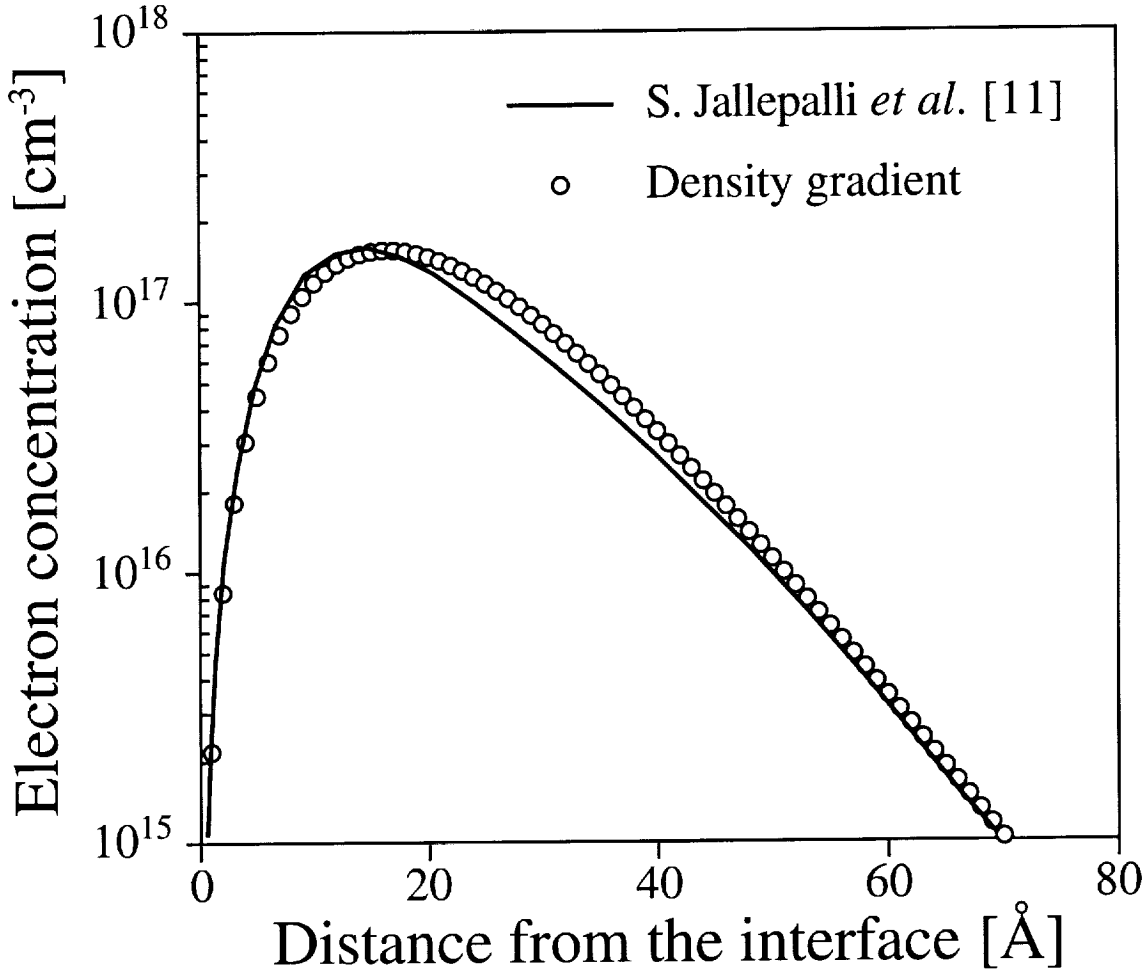




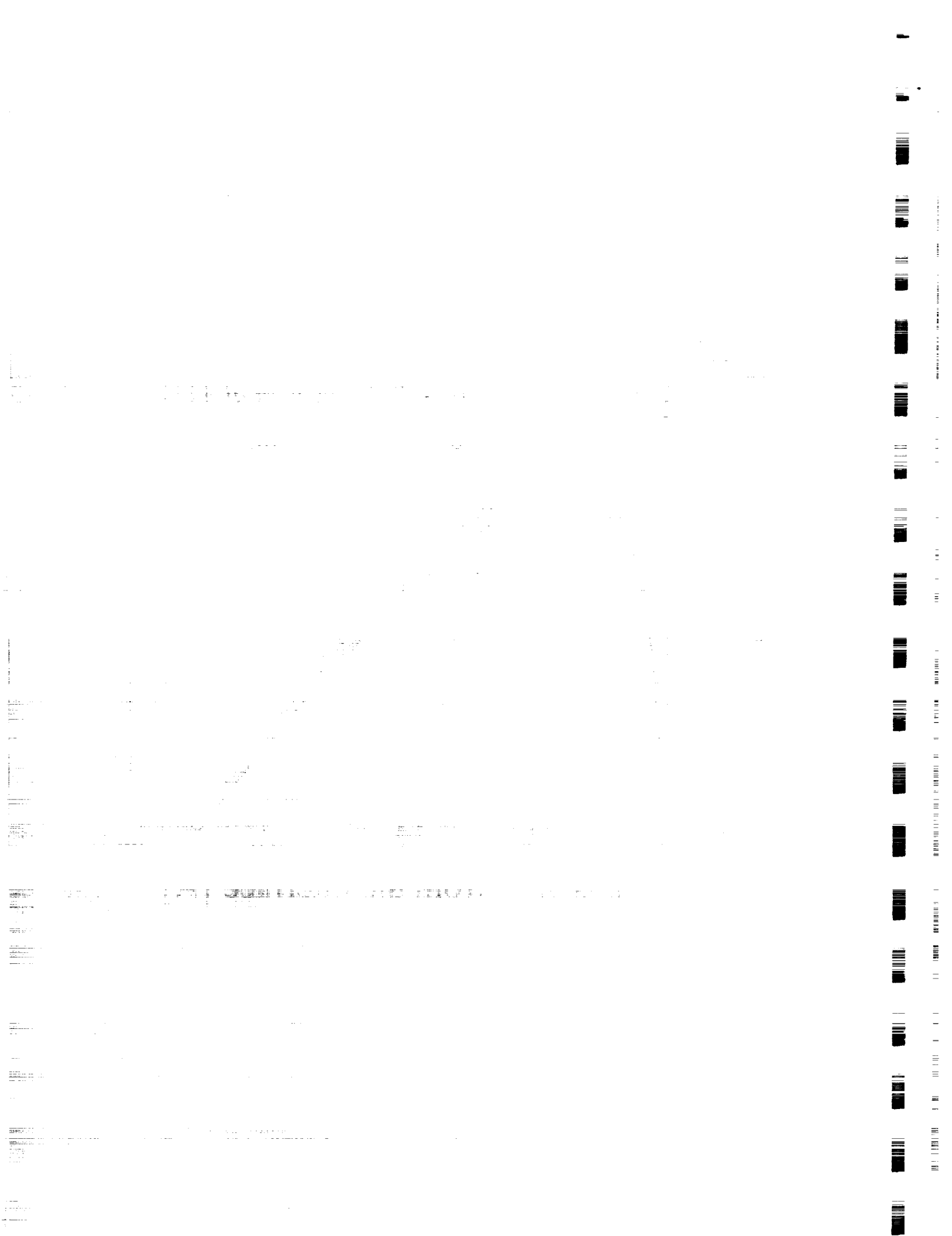
A. Asenov, *et al.* Fig. 4

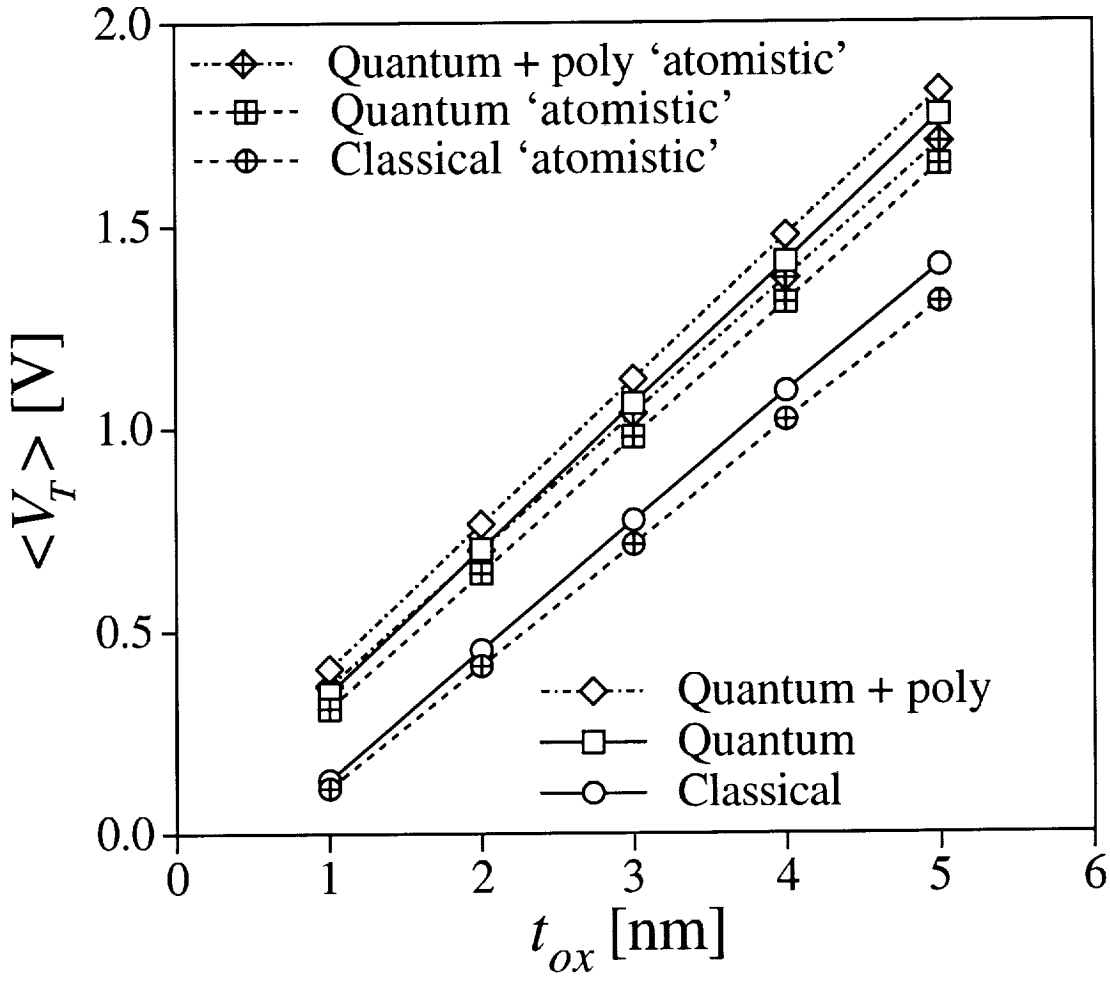


A. Asenov, *et al.* Fig. 5

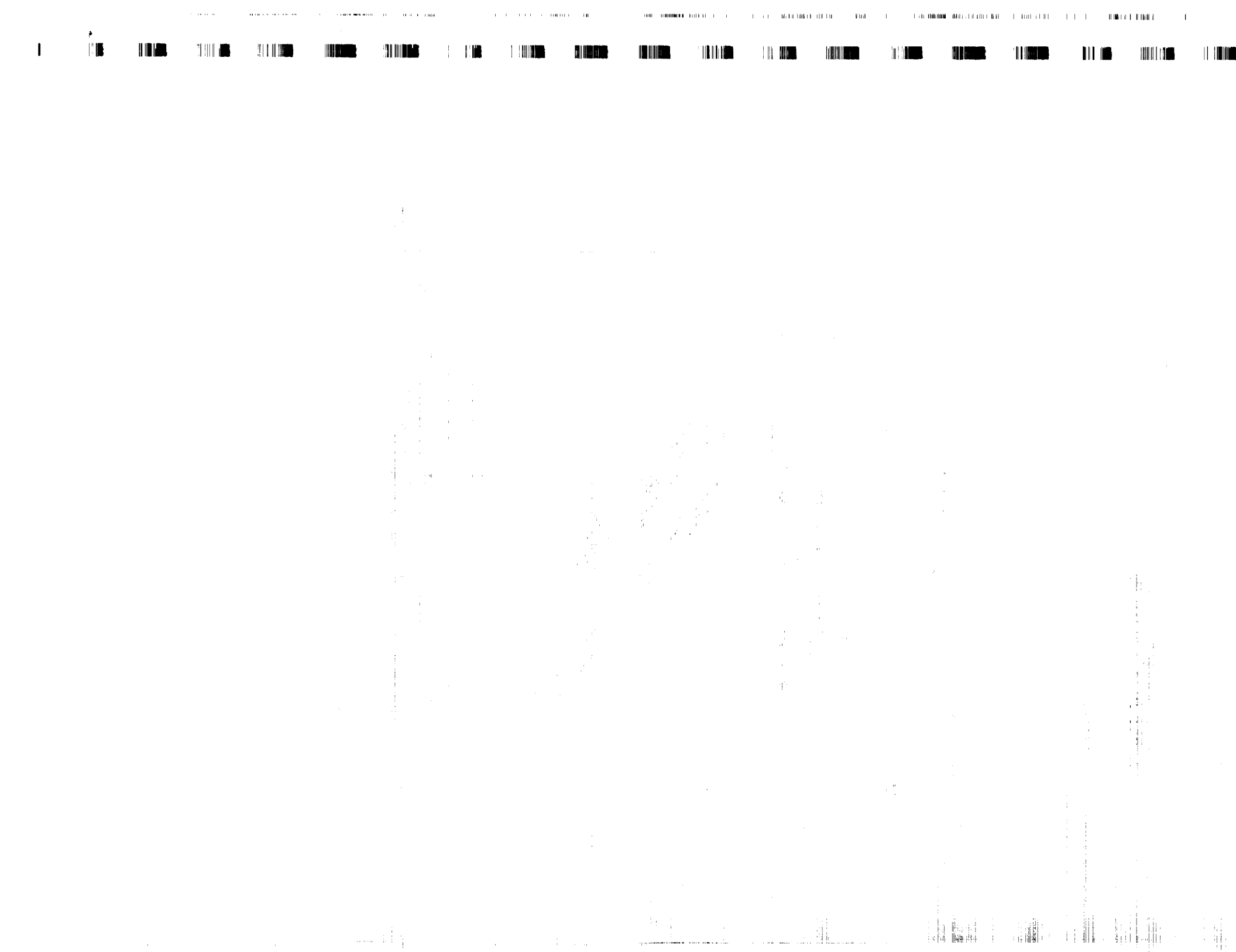


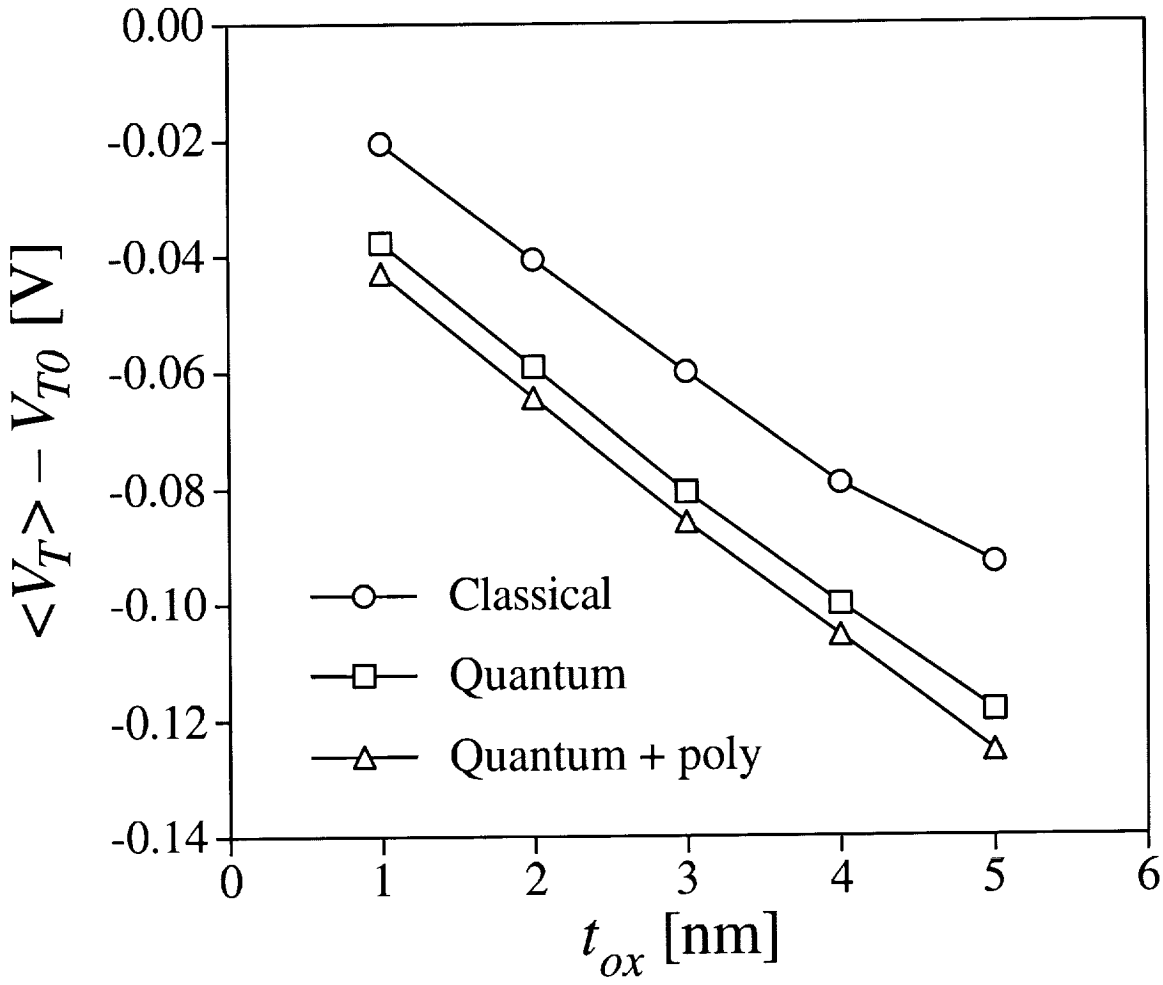
A. Asenov, *et al.* Fig. 6



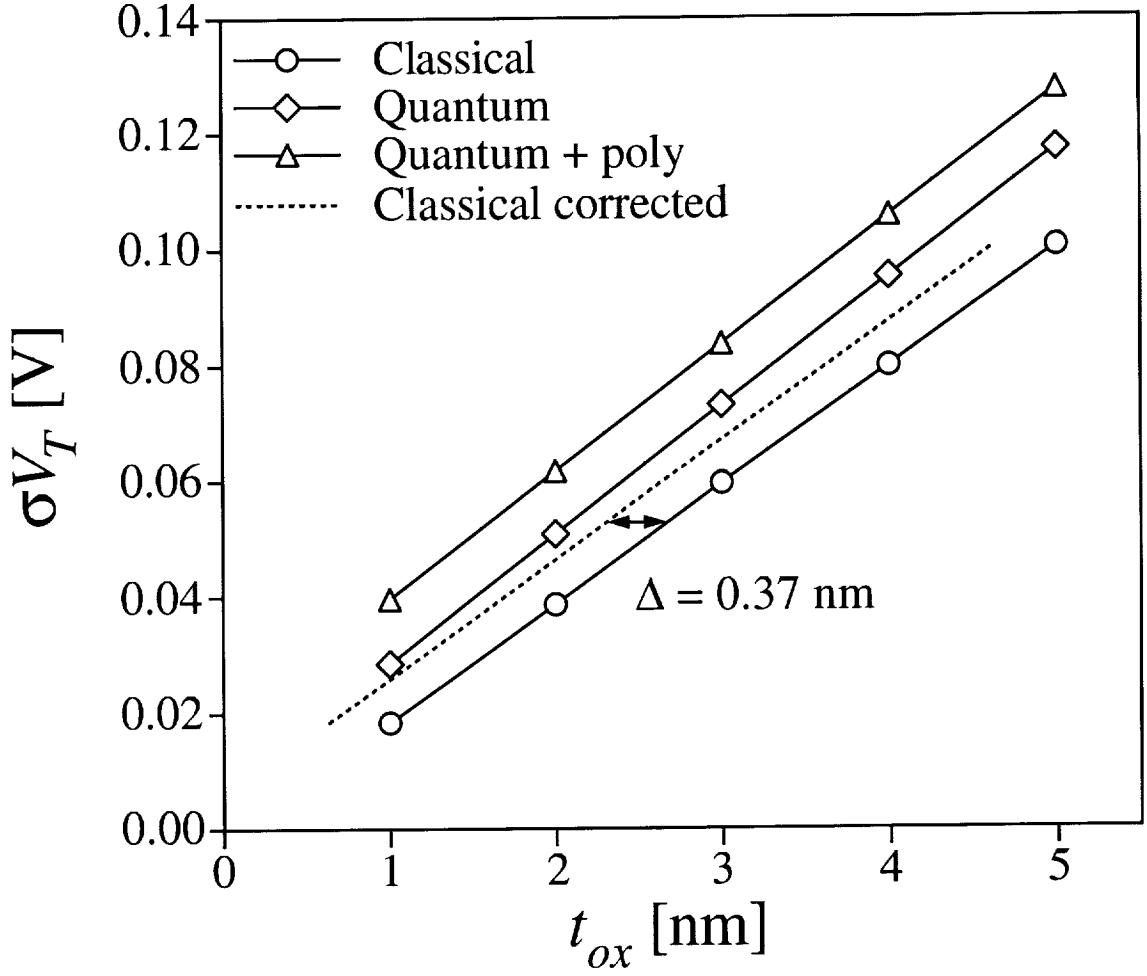


A. Asenov, *et al.* Fig. 7

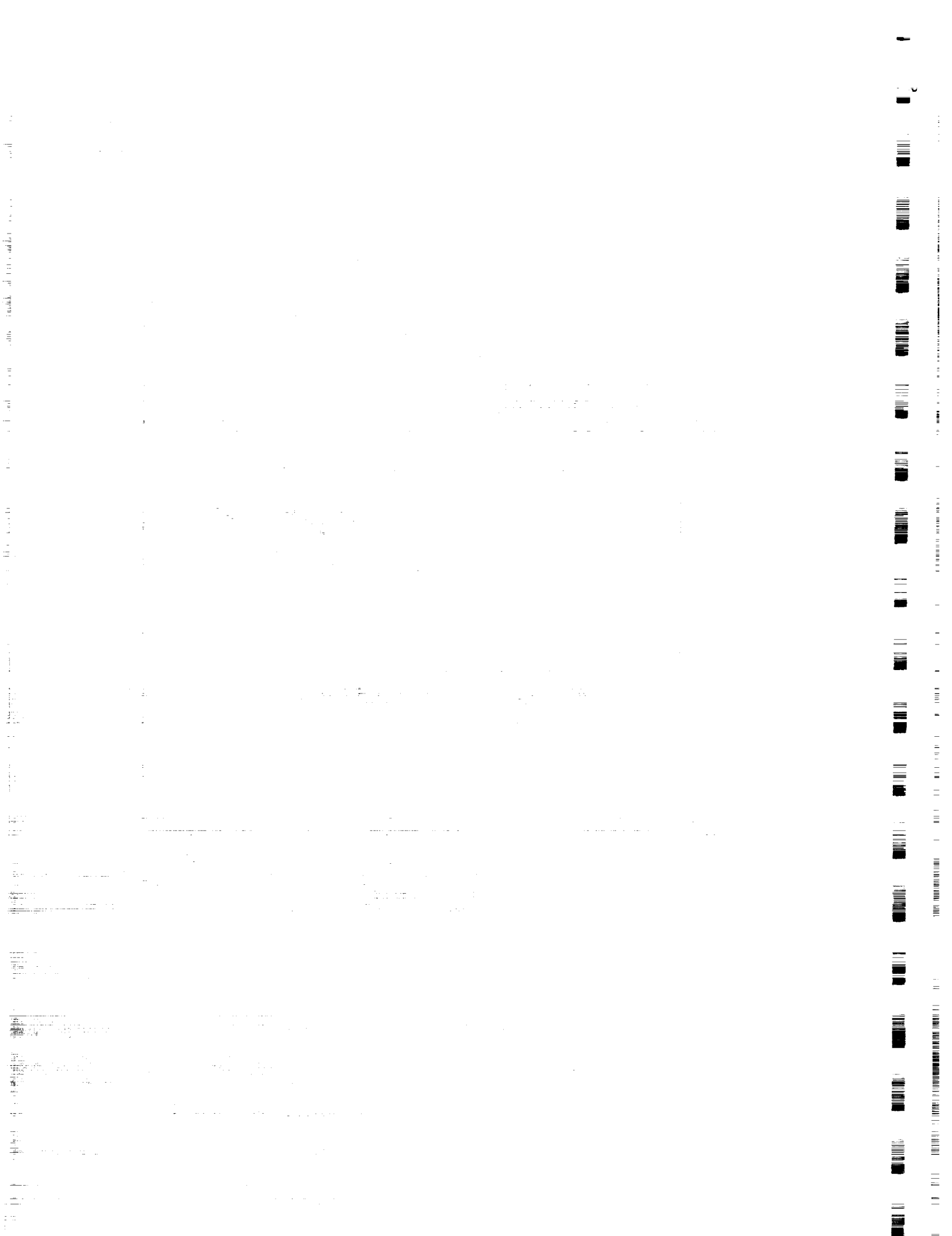


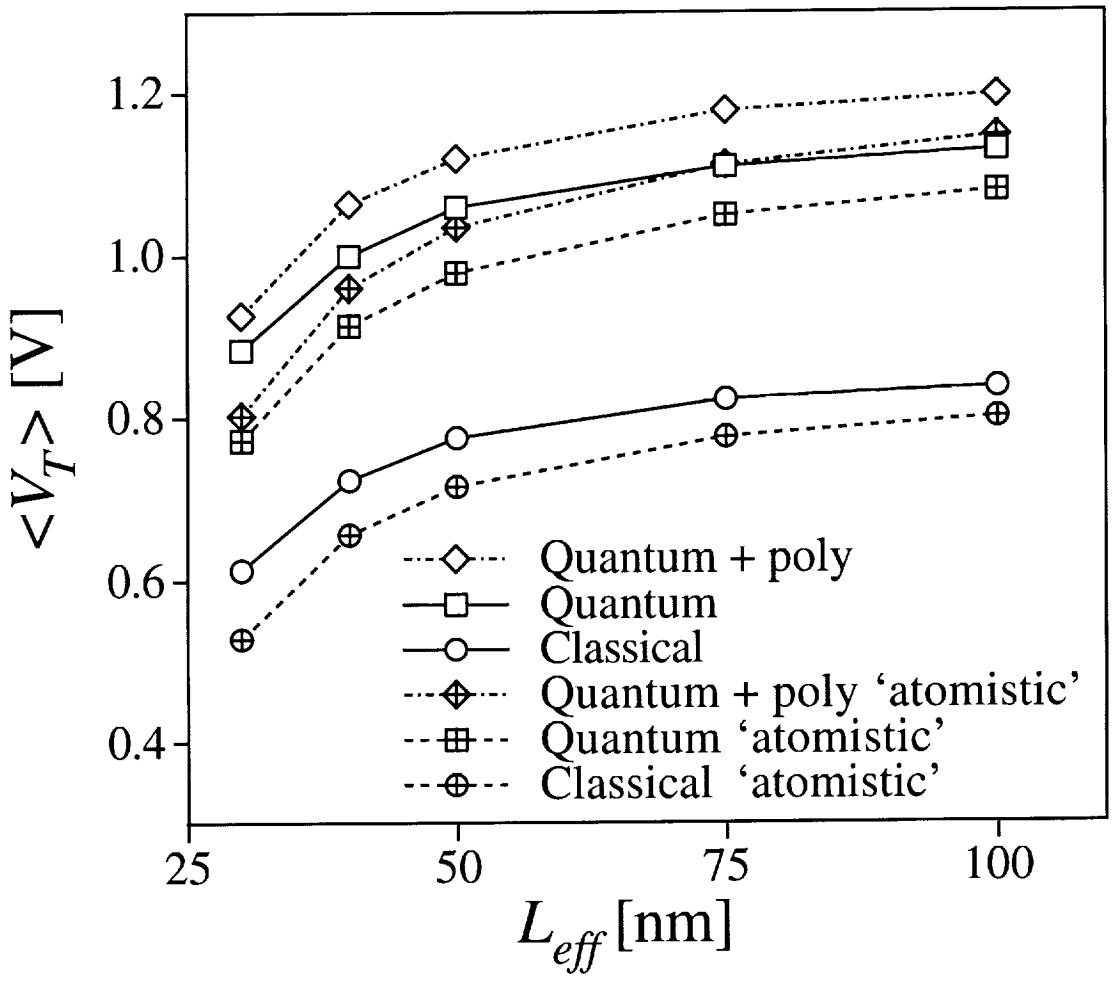


A. Asenov, *et al.* Fig. 8

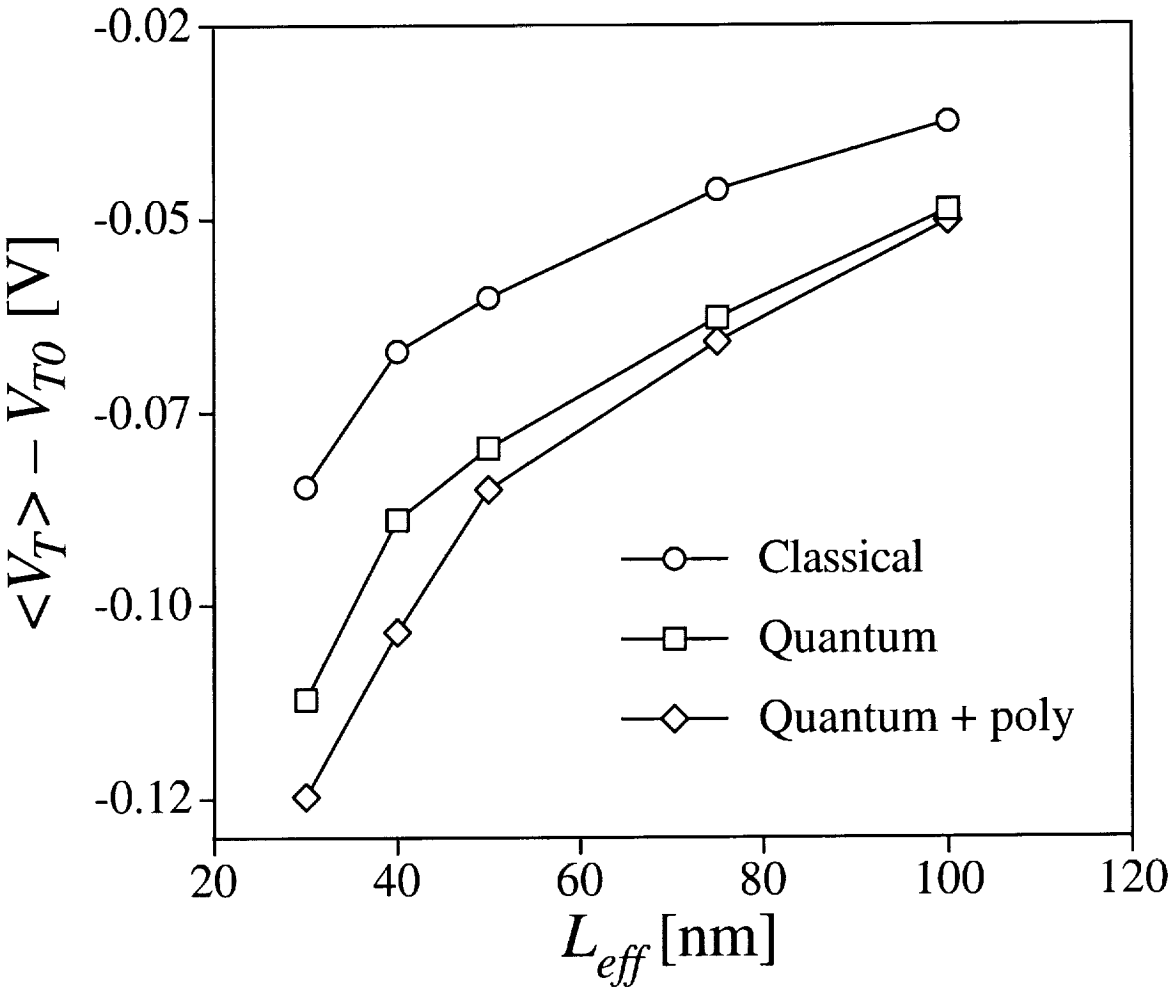


A. Asenov, *et al.* Fig. 9

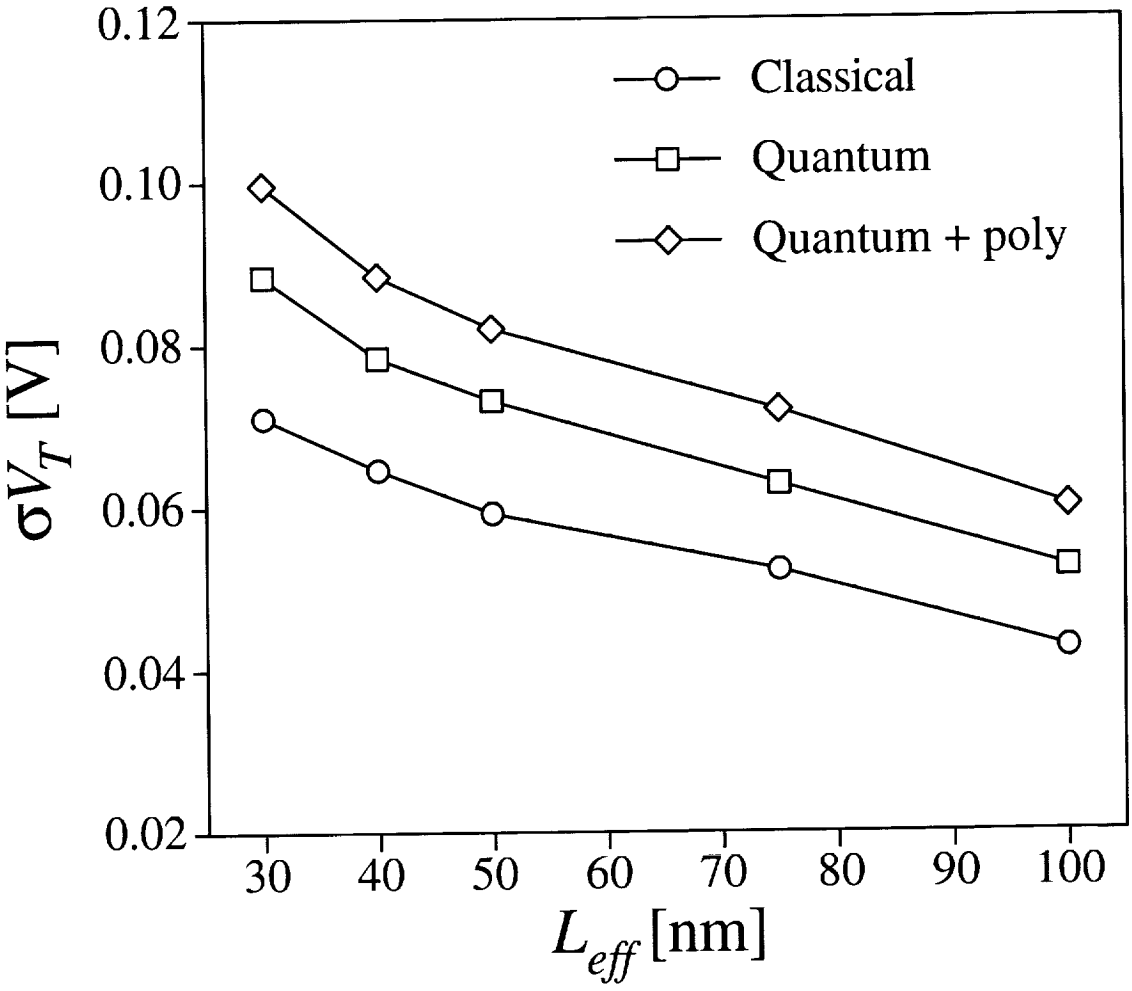




A. Asenov, *et al.* Fig. 10



A. Asenov, *et al.* Fig. 11



A. Asenov, *et al.* Fig. 12