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Final Technical Report
Summary of Research for Dr. Karen Panetta
Tufts University

During the duration of Dr. Panetta's NASA JOVE grant, she has secured over 1.19 Million Dollars to support the Simulation and Visualization laboratory she started at Tufts University in 1996 (See appendix A). The laboratory, supported by NASA, the National Science Foundation and major industrial supporters such as Compaq Computer, Intel Corporation, Teradyne and Draper Laboratories, is well equipped, and, with her grants, provide her with the environment she needs to investigate the problems of simulating large complex systems.

She has published over 20 papers in prestigious journals, conferences and workshops (See appendix B). In addition, she has successfully introduced her research into the classroom. She has developed upper level courses in simulation, testing and modeling that are now part of the Computer Engineering curriculum at Tufts University, while her undergraduate courses use the standard hardware description languages required of today's successful computer and electrical engineers. Her efforts have been recognized with numerous awards for teaching and mentorship (See appendix C).

Karen Panetta's principal research has been in the areas of digital logic simulation and system level simulation of multidiscipline systems. Her work in digital logic simulation seeks to develop tools that can efficiently and accurately model entire systems, such as new computer designs before any physical prototype is built. The system level simulation work attempts to extend the digital techniques to structures of a more general nature, such as electrical/mechanical systems. Dr. Panetta's approach involves extensive use of fault simulation algorithms. This is a method that inserts erroneous behaviors into an error free system model to examine their effect. The insertion of these behaviors, called "faults", emulates defects in the design. It allows engineers to evaluate design robustness and to measure the effectiveness of processes used to detect such defects.

There are very few simulators available either commercially or through academia that can simulate multiple fault types occurring simultaneously. Furthermore, the observation into the cause-effect relationships of experiments is unique to this research. The major Findings of the research are proving that development of test patterns under a single failure mode is a major detriment to the quality and robustness of current test methodologies.

Dr. Panetta has integrated undergraduates in her research and the impact it has had on their careers is impressive. She has sent former NASA JOVE supported students to Brown University, (Daniel Keefe) to complete a Ph.D in visualization, Harvard University for a Ph.d in physics (Jason Draut), and several of her students are in industry at corporations such as Intel, Compaq, Asic-alliance and SUN Microsystems. All of her undergraduates researchers have earned a Master's Degree. Their involvement in the

project, not only advanced Dr. Panetta's research goals but gave the students strong research and refined technical skills that the classroom lecture could not provide.

Technical Summary:

The research goals are to create a simulation framework that can accept any combination of models written at the gate or behavioral level. The framework provides the ability to fault simulate and create scenarios of experiments using concurrent simulation. In order to meet these goals we have had to fulfill the following requirements. The ability to accept models written in VHDL, Verilog or the C languages. The ability to propagate faults through any model type. The ability to create experiment scenarios efficiently without generating every possible combination of variables. The ability to accept adversity of fault models beyond the single stuck-at model. Major development has been done to develop a parser that can accept models written in various languages. This work has generated considerable attention from other universities and industry for its flexibility and usefulness. The parser uses LEXX and YACC to parse Verilog and C. We have also utilized our industrial partnership with Alternative System's Inc. to import vhdl into our simulator.

For multilevel simulation, we needed to modify the simulator architecture to accept models that contained multiple outputs. This enabled us to accept behavioral components. The next major accomplishment was the addition of "functional fault models". Functional fault models change the behavior of a gate or model. For example, a bridging fault can make an OR gate behave like an AND gate. This has applications beyond fault simulation. This modeling flexibility will make the simulator more useful fordoing verification and model comparison. For instance, two or more versions of an ALU can be comparatively simulated in a single execution. The results will show where and how the models differed so that the performance and correctness of the models may be evaluated. A considerable amount of time has been dedicated to validating the simulator performance on larger models provided by industry and other universities.

Curriculum Development:

The education activities have been numerous. Two sets of new laboratory projects have been added to the curriculum. The first is using simulation and modeling in the DIGITAL TESTING course (EE202). This is the only course that introduces students into Design for Testability issues and exposes them to modeling. The second set of projects were added to the computer architecture class (EE126). Students did verification and added BIST to designs. Students even wrote their own digital logic simulators using one of the traditional simulation methods, serial, parallel, deductive or concurent simulation. One of the projects won the IEEE student design competition. Furthermore, another student project won the University Wide Research Competition. Students have presented their work at conferences and have published with Dr. Panetta. Undergraduates interested in multimedia have also done projects animating our research algorithms to help visualize the concepts. This has helped us train new students and introduce the concepts of simulation in the classroom.

Insights into the behavior of multiple fault types occurring simultaneously have been investigated. Research in this area has stated that the single stuck-at model is adequate for detecting multiple stuck-at faults. Since there are few research papers that discuss multiple fault types occurring at the same time, there is little discussion on the quality of test patterns used to detect these kind of occurrences. Our research has simulated bridging faults along with single stuck-at faults. We have discovered that the patterns developed for single stuck-at faults do not perform well for bridging faults or in the case when multiple fault types occur. This implies that test pattern development is missing a critical component for robustness, namely, a methodology that does not rely soley on the single stuck-at patterns. This is very important for modeling and simulating ram interconnect failures. In the future, we hope to prove that using concurrent simulation, we can not only simulate these multiple fault types efficiently, but be able to distinguish the differences caused by the interaction of both types of faults.

Educational and Training:

Every person on the project is involved in writing research papers and communicating their progress. Team members have researched specific areas such as parser development, model development, behavioral modeling, vhdl, and verilog, where each member became the resident expert on their selected area. They have interacted with other university professors and industrial professionals and kept schedules to meet paper deadlines and project timelines. The students involved in the project are using their experience as their required senior projects. This means that in addition to development work, they must deliver an oral presentation to the department. Each member understands simulation and has become very proficient with test methodologies as well as hardware description languages.

Outreach Activities:

Every friday afternoon during the month of October, we have 'open lab' hours. This provides pre-freshman and their parents the opportunity to come see firsthand what we are working on. Students get the chance to talk to student members of the team. This shows that undergraduates can do research and be a major technical contributor to real projects. It is mutually beneficial for the team members because they have to learn to express their technical goals to others not skilled in the area. During the summer, we always host 1 or 2 female high school students, either through the CRA program or through the internal "Tufts Women in Engineering" program. Both of these programs bring female students into a working research environment and teach them what real engineers do.

Appendix A: Grants

Pending:

- "A Unified Simulation and Fault Modeling Environment for Mixed Signal Systems Including MEMS Components", National Science Foundation $797,883 submitted, Co-PI with Dr. Steve Morrison, Dr. Mark Cronin-Golomb, and Dr. Fred Nelson, September 2000.

Fellowships, awards, grants or other prizes

Grants over $20,000.00

- Intellectual Partnership for simulating the ALPHA 21064 RISC Architecture, National Science Foundation Industrial Matching with Compaq Computer, $25,000.00, August 2000.
- 2000 - Teradyne Inc., Support for Simulation Laboratory, Co-PI with Dr. Denis Fermental, $26,000.00, March 2000.
- 1999- National Science Foundation Intranet-II, $500,000.00, Wilson Dilloway, Ioannis Miaoulis,
- 1999 – Selmer/ Steinway Networked Database, Co-PI with Dr. Alva Couch $24,000.00, Feb. 1999.
- 1999- Mellon Research Grant, Tufts University, Sept. 1999.
- 1997 – National Science Foundation, CAREER Award. "Robust Behavioral Fault Simulation Algorithms for Multilevel Simulation". MIP-9733584 PI, $250,000.00.
- 1997 – Viacom Multimedia grant, Co-PI, with Dr. Alva Couch and Dr. Ioannis Miaoulis, $40,000.00.
- 1996 - NASA JOVE (NASA/ Joint University Venture) Grant PI, $186,000.00.
- 1996- Beveridge Foundation, Co-PI, with Dr. Alva Couch, Dr. Ioannis Miaoulis, $75,000.00.

Grants under $20,000.00

- 2000 - National Science Foundation Research Experiences for Undergraduates, PI, $10,000.00, July 2000.
- 2000 - National Science Foundation, Travel Grant, PI, $10,000.
- 1999 - National Science Foundation Research Experiences for Undergraduates, PI, $10,000.00 May 1999.
- 1999 - National Science Foundation Equipment Grant, PI, $20,000, March 1999.
- 1999 - National Semi-Conductor, PI, $10,000. January 1999.
- 1998 - National Science Foundation Research Experiences for Undergraduates, PI, $10,000, March 1998.
- 1998 - National Science Foundation Computing Research Association student support grant, PI $10,000.00 Feb. 1998.

- 1998 - Microtouch Corporation, Equipment grant, touch screen monitor, PI, $2885.00,

  February 1998.

- 1998 – General Scanning Inc., Equipment grant, thermal printer, PI, $2300.00, June 1998.
- 1997 – Selmer/ Steinway proposal for multimedia, Co-PI with Dr. Alva Couch

  $11,000.00,

  Oct. 1997.

- 1997 – Digital/INTEL equipment grant, PI, 4 machines @4k=$16,000.00, October

  1997.

- 1997 – Tufts University, FRAC, Co-PI, with Dr. David Locke, " Music and Media",

  $2000.00

- 1996 – National Science Foundation, National Science Foundation, Planning Grant Award. "Compression and Interaction Algorithms for Modeling and Simulation Envrionments". MIP-9528194, PI, $18,000.00.
- 1996 – Tufts University, FRAC, "Interactive Media Environments for Occupational Therapy", $2200.00, March 1996.
- 1995 – Massachusetts Cultural Council (MCC), FY96-EP-MED-0795, "Multimedia in the Classroom", $3000.00, August 1995.

Awards

- Tufts University Mentorship/Research Award, with graduate student Terry Orfanos.
- 1998 – Outstanding Contributions to NASA Research 1998.
- 1998 - NASA Excellence in Research Award 1998.
- 1998 - NASA Curriculum Development Award for EE202: "Digital System Testing and Simulation".
- 1998 – NASA Curriculum Development Award for the Tufts University Multimedia Minor.
- 1998 – NASA Best Team Poster Presentation, JOVE conference.
- 1998 – Outstanding Contributions to NASA Research 1997.
- 1997 - NASA Excellence in Research Award.
- 1997 - NASA Curriculum Development Award for "Animation for Technical Communications".
- 1996 – NASA Langley Research Scientist Fellow.

- 1996 – Massachusetts Interactive Media Council (MIMC), third place for student CD-ROM project on African Drum music, "Gahu of the Ewe" in collaboration with the Music department.

Other Honors

- IEEE Best Student Paper Competition, Daniel Keefe, for his collaborative work on Dr. Panetta's NASA Grant.
- IEEE Silver Medal for the Tufts University IEEE Student Chapter web design.
- IEEE 2000 Micromouse competition, third place. Dr. Panetta supervised this project.

Appendix B: Publications published during the duration of the NASA JOVE grant
Duration: 1996-2000
Journal Articles

- S. Agaian, K. Panetta Lentz and A. Grigoryan, "Transform Based Image Enhancement Algorithms", accepted for publication, IEEE Transactions on Digital Signal Processing, May 2000.

- K. Panetta Lentz, J. Heller and P. Montessoro, " System Verification Using Multilevel Concurrent Simulation", IEEE MICRO Vol. 19, No 1. Jan/Feb 1999.

- K. Assiter, K. Panetta Lentz, A. Couch and C. Currey, "Locating Anomalies in Large Data Sets", Society for Computer Simulation Military, Government and Aerospace Simulation, Vol. 30, no. 4, pages 218-223 April 5, 1998.

- K. Panetta Lentz, E. Manolakos, and E. Czeck and J. Heller, "Multiple Experiment Environments for Testing". Journal of Electronic Testing: Theory and Applications (JETTA), Vol. 11, No. 3, pp. 247-262, December 1997.

Refereed Conference and Workshop Publications

- K. Panetta and J. Heller, "Simulation Techniques for Modeling Large System Designs", Proceedings of the World Multiconference on Systemics, Cybernetics and Informatics (SCI 2000), Vol. VIII, pages 300-305, July 2000.

- K. Panetta and J. Homer, "Handling Behavioral Components in Multilevel Concurrent Fault Simulation", Advanced Simulation Technologies Conference, The 33rd Annual Simulation Symposium, pages 149-151, April 2000.

- J. Heller and K. Panetta Lentz, "TUFTsim: A Multiple Domain Simulator for Experimentation", The 32nd Annual Simulation Symposium, pages 44-49, May 1999.

- J. Heller and K. Panetta Lentz, "A Modular and Extensible Concurrent Fault Simulator", IEEE North Atlantic Test Workshop, pages 6-11, May 1998.

- K. Panetta Lentz, J. Heller and P. Montessoro, "Multi-Level Concurrent Simulation: An Extensible Architectural Environment", IEEE Workshop on Embedded Fault Tolerant Systems (EFTS98), pages 136-142, May 22, 1998.

- K. Panetta Lentz, J. Heller and P. Montessoro, "Multi-Level Concurrent Simulation", Proceedings the 31st Annual Simulation Symposium, pages 42-47, April 5, 1998.

- R. Kogan, S. Agaian, K. Panetta Lentz, "Visualization Using Rational Morphology and Zonal Magnitude Reduction", Proceedings of the International Society for Optical Engineering (SPIE), Nonlinear Image Processing IX, pages 153-163, San Jose California, January 26, 1998.

- K. Panetta Lentz, E. Manolakos, and E. Czeck, "A Multiple Domain Environment for Efficient Simulation", 1997 Simulation MultiConference: 30th Annual Simulation Symposium,
  pages 76-85, April 6-10, 1997.

- K. Panetta Lentz, E. Manolakos, and E. Czeck, "Compressing Large Simulations Using Multiple Domain Concurrent and Comparative Simulation", IEEE North Atlantic Test Workshop,
  May 1996.

- E. Weststrate, K. Panetta, "Multiple Fault Models for Concurrent Simulation", IEEE Embedded Fault Tolerant Workshop, September 2000.

- Sos S. Agaian, K. Panetta and Artyom M. Grigoryan, "A New Measure of Image Enhancement", IASTED International Conference on Signal Processing and Communications, accepted for publication, September 19-22, 2000, Marbella, Spain.

Book Chapters:

- Contributor to the book, "The Handbook of Multimedia Computing", Co-author of Chapter 13: Edited by Dr. Furht, CRC Press, May 1998.

Media and Educational Publications

- K. Panetta Lentz, C. Dornbush and K. Loomis, ASEE Journal of Engineering Education, "A Collaboration Learning Methodology for Enhanced Comprehension Using *TEAM*Think Software", Submitted for publication, January, 2000.

- K. Panetta Lentz, "Multimedia as a Method for Technical Communications", ASEE 1996 Conference Proceedings, April 26, 1996.

- K. Panetta Lentz, "Multimedia on Campus: New Multimedia Lab at Tufts University", Professional Journal of the Special interest Group on CD Applications and Technology (SIGCAT), vol. 10, no.5, 1996.

Poster Presentations

- S. Agaian, R. Kogan and K. Panetta Lentz, "Visualization using Rational Morphology", AeroSense, SPIE 12th Annual International Symposium on Aerospace/Defense Sensing, Simulation and Controls, pages 3387-37, April 1998.

Invited participation in professional and other similar activities

Talks

- 1999 - National Science Foundation, "CAREER Awardee Workshop", invited presenter.
- 1998 - Boston University, College of Engineering. Title: "Multilevel Concurrent Simulation".
- 1998 – Syllabus Conference, July 1998. Title: "Adding Multimedia to the Curriculum: Issues and Approaches".
- 1998 NASA JOVE Conference, Cocoa Beach Florida, Guest Speaker.
- 1996 - University of Lowell, Electrical Engineering department. Title: "Stimulating Simulating".

Appendix D: Curriculum, course or instructional innovations developed

Courses developed for Electrical Engineering and the Interdisciplinary Multimedia Minor.

- EE120 Animation for Technical Communications, new course developed.
- EE202 Digital System and Testing with VHDL, new course developed.
- EE194 New course on Embedded System Design.

Improvements to existing courses

- 2000, ES4 Introduction to Digital Logic Created and designed with Dr. Denis Fermental, all new laboratory assignments.

- 2000, Advanced Computer Architecture. Introduced the use VHDL and Design for Testability approaches for architecture design. Added new laboratory assignments.

- 1999, ES4 Introduction to Digital Logic, Introduced the VHDL (Hardware Description Language) into each laboratory assignment.
- 1997, Tufts Sixth University-Wide Teaching Conference, workshop director in Multimedia.
- 1996, "Educating Educators with Multimedia", Taught a 5 day workshop to K-12 Educators on how to integrate multimedia in the classroom.

NASA/University JOint VEnture (JOVE)Program

FINAL TECHNICAL REPORT

I. **Summary of research and related education and outreach efforts conducted under this NASA/JOVE grant.** ***(Attach additional page(s) and/or relevant documentation as necessary.)***

Please see attached.

NASA/University JOint VEnture (JOVE)Program

FINAL TECHNICAL REPORT

II. Subject Inventions

Provide a complete list of all subject inventions or patents resulting from work performed under the award or provide a statement that there were none.

None

Karen Pamblis
Signature

12/15/00
Date

For Summaries of Research and published reports, one Micro-reproducible copy shall be sent to the NASA Center for AeroSpace Information (CASI), Attn: Acquisitions Department, 7121 Standard Drive, Hanover, Maryland 21076-1320.