Imaging Electron Spectrometer (IES) Electron Preprocessor (EPP) Design

Final Report

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Prepared by

J. F. FENNELL and J. V. OSBORN
Space Science Applications Laboratory
Laboratory Operations

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THE AEROSPACE CORPORATION
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IMAGING ELECTRON SPECTROMETER (IES)
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Abstract

The Aerospace Corporation developed the Electron PreProcessor (EPP) to support the Imaging Electron Spectrometer (IES) that is part of the RAPID experiment on the ESA/NASA CLUSTER mission. The purpose of the EPP is to collect raw data from the IES and perform processing and data compression on it before transferring it to the RAPID microprocessor system for formatting and transmission to the CLUSTER satellite data system. The report provides a short history of the RAPID and CLUSTER programs and describes the EPP design. Four EPP units were fabricated, tested, and delivered for the original CLUSTER program. These were destroyed during a launch failure. Four more EPP units were delivered for the CLUSTER II program. These were successfully launched and are operating nominally on obit.

Contents

Figures

1. Introduction

The RAPID EPP, developed under this contract, supports the Imaging Electron Spectrometer (IES) that is one component of the RAPID experiment on the ESA/NASA CLUSTER II mission satellites. The other component is the Imaging Ion Mass Spectrometer (IIMS) sensor that is provided by the Max-Planck-Institute für Aeronomy (MPAe) in Germany. The principal investigator for the RAPID experiment is Berend Wilken from MPAe. The IES is provided by Los Alamos National Laboratory and Boston University under the guidance of Prof. T. Fritz at Boston University. A flight-ready RAPID unit is shown in Figure 1 for reference.

The purpose of the EPP is to gather the raw data from the IES and convert it to science data. The EPP also acts as the interface between the IES and the RAPID digital processing unit (RDPU). It monitors the data from the IES and provides the control interface for it. The EPP status is monitored by the RDPU, and mode commands received by or generated within the RDPU are maintained in the EPP, passed through to the IES, and continuously reinforced by the EPP. In essence, the EPP operates as a specialized processing unit that can provide onboard processing of the IES data. This reduces the processing load on the RAPID microprocessor. In fact, the standard radiation-hardened microprocessors were not fast enough to provide the processing needed by the IES. The EPP provides both science data output and, upon command, provides a summary of the raw data in a special "histogram mode," which is used to monitor the performance and drifts of the IES amplifiers and detectors.
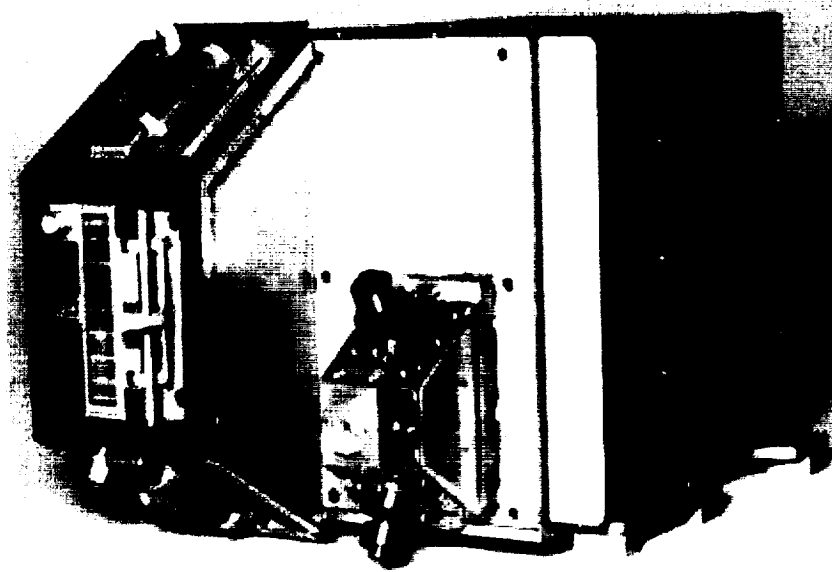

Figure 1. RAPID experiment. The sensor head on the left is IIMS with its doors open. The sensor head on the right is IES with two of its aperture covers on and the center aperture exposed. The EPP is in the RAPID box behind the IES.

The goal in developing the EPP was to provide a simple, yet compact and powerful, real-time processor for reducing the raw IES outputs to science data to monitor the performance of the IES and modify the sensor amplifier integration times to avoid saturation effects (see Appendix). The EPP interface with the RDPU had to be relatively simple, and the EPP operation as autonomous as possible. To meet these goals, it was decided to implement a modification of a design that performed a nearly identical function for a similar IES in the CEPPAD experiment that was flown on the NASA GGS/Polar mission. This design had heritage and had proven effective and flexible. The required modifications are discussed below.

2. EPP Development

The Imaging Electron Spectrometer (IES) that is flown as a part of the RAPID (Research with Adaptive Particle Imaging Detectors) Experiment on CLUSTER II[1,8] is identical to the sensor units[2,3,4] that were destroyed during the failure of the first Ariane V launch of the CLUSTER satellites. It is also very similar to the IES that is flying as a part of the CEPPAD experiment on the NASA GGS/Polar satellite.[5,6] In all cases, the IES used an Electron Preprocessor (EPP) of similar design.

The Polar/CEPPAD IES had a much larger telemetry and weight allocation than was available for RAPID. The CEPPAD IES/EPP was designed to take full advantage of the higher telemetry rate and greater mass resource. Both the IES and EPP had to be somewhat redesigned to fit within the constrained RAPID resources while still performing nearly identical functions. This was achieved by requiring the IES to run off of a shared power system instead of the independent power supply it had on CEPPAD. All the components of the RAPID experiments shared the same "box," power supplies and RAPID digital processing unit (RDPU). On CEPPAD they were in separate "boxes."

The RAPID EPP had to fit on a logic board that plugged into the RDPU "mother board" to interface with the RDPU microprocessor bus and received its power and control from there. As a result, the EPP board geometry had to be modified somewhat, and the component layouts had to be fit to it. In addition, the "double buffering" scheme that was used to off-load time-critical demands from the CEPPAD microprocessor was eliminated. Only half as much memory and more limited control functions were to be used in the RAPID EPP. The digital logic changes were made by changing the programming in the EPP's Actel FPGA (field-programmable gate array) logic. The combined memory and FPGA changes plus other differences between the RDPU and the CEPPAD DPU required that the software to interface the EPP with the RAPID DPU's microprocessor system be modified and integrated differently with the rest of the RDPU microprocessor software.

The redesigned EPP system was built up into a flight configuration as an engineering model (EM). The EPP EM was thoroughly tested electrically and was interfaced with an EM RDPU and IES for functional and interface verification. The EPP EM was also used to develop the required control software that could be run on the RDPU microprocessor. The tested EPP EM unit was delivered to the P.I. institution (Max-Planck-Institute für Aeronomie; MPAe) for their testing and development work. In addition, five flight versions of the EPP were fabricated, tested, and delivered to MPAe for the first RAPID units (four flight units and a spare).

Figure 2 shows an EPP board with the main components identified. Figure 3 shows a schematic block diagram, and Figure 4 shows a schematic logic diagram for the EPP. Since most of the digital logic resides in the Actel FPGAs, the complex and fast processing functions fit on the single board. The RAMs provide the storage element of the science data "scalars" plus the data sorting tables used to generate the science data. The Actel logic is the heart of the system. It processes each event produced by the IES, determines which detector it came from, selects the appropriate data sorting table,
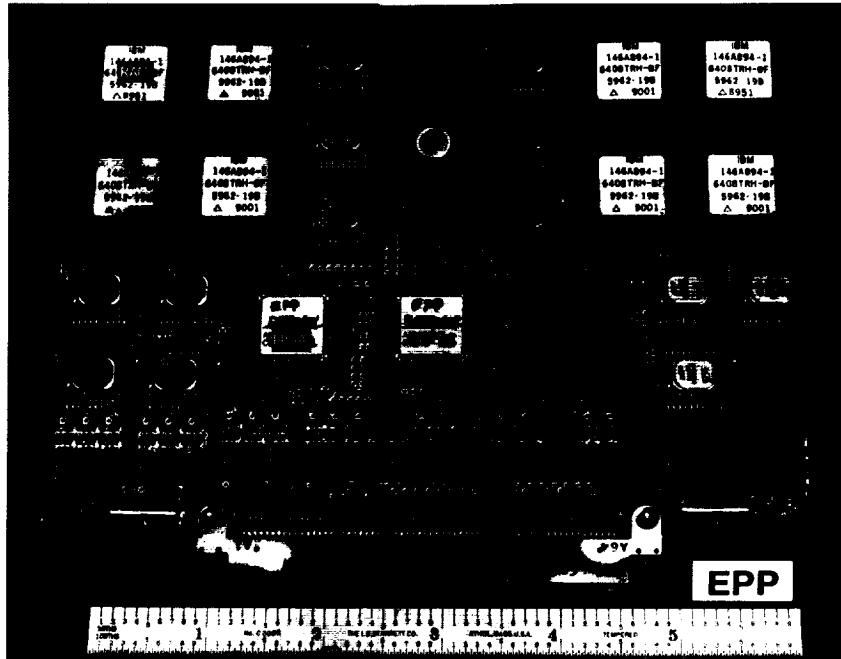
Figure 2. EPP board. One each of the RAMs and Actel FPGAs are identified. The EPP interfaces to the RAPID power system and microprocessor via the high-density edge connector.
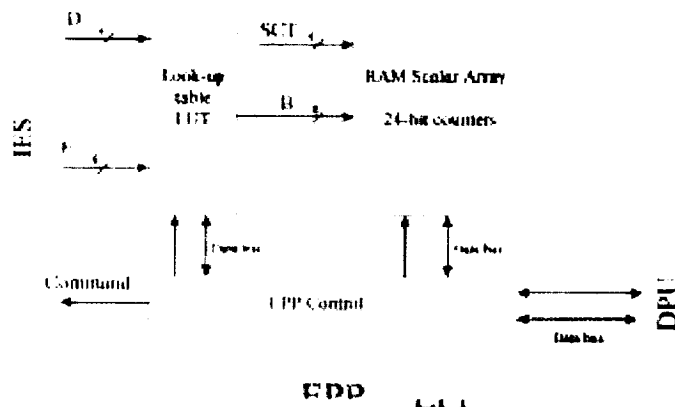

Figure 3. Schematic block diagram of the EPP. The Electron input data [energy E and detector (pixel) number D] are passed through a sorting and reduction process to reduce the data volume. The EPP provides the complete interface between the IES and the Rapid DPU (RDPU).

and using the table values, increments the appropriate "counter" in the RAM (see Figure 4). There are 16 different sets of "counters" in the RAM to provide data accumulation over 16 different angular sectors in inertial space as the satellite spins. The CLUSTER satellite spin clock is routed to the EPP and is used by the Actel logic to generate the appropriate data "sectoring" addresses (see Figure 4).

4

After the failure of the first CLUSTER launch, it was decided, by ESA and NASA, to rebuild the CLUSTER satellites and instruments. The original flight spare satellite was renamed Phoenix,[7] and the revived mission was called CLUSTER II.

Aerospace refurbished the flight spare EPP and proceeded to fabricate four new EPP units. However, we quickly learned that new memory chips were needed and that the original supplier (IBM) had sold its rights for the chips used in the EPP to another company. It took weeks to determine which of the many memory chips that were offered by the new company were the correct chips. In the end, it was necessary to purchase samples of the likely candidates and test them to determine which were compatible. Similarly, it was necessary to search for electronic parts distributors that still had a stock of flight-quality Actel FPGAs like those used in the original EPP units. Our contacts at Goddard Space Flight Center and our CLUSTER program COTR there (L. Christensen) were instrumental in making the acquisition of the parts possible. Some of the parts were provided directly from Goddard Space Flight Center.

After the parts had been purchased, we had the original PCB supplier fabricate a set of boards. We waited to make sure that the parts package dimensions and pin-outs had remained the same; otherwise, a new board layout would have been required, and the whole development phase would have been repeated. It turned out that it was not necessary. The parts fit on the original board layouts, and only the functional and environmental testing was required. The four new IES EPP boards were fabricated, tested, and delivered to MPAe (Max-Planck-Institut für Aeronomie at Katlenburg-Lindau Germany) by J. Osborn (project engineer) in July 1998. The parts provided by Goddard Space Flight Center (Octal Buffers 54HC5245KMSR) arrived just in time to complete the board fabrications and meet the July delivery.

Following their delivery to MPAe, the boards were moved to IDA (Institüt für Datenverarbeitungsanlagen) at Braunschweig Germany. IDA fabricated the RAPID DPUs. Each EPP board was integrated with the RDPU EM unit and run through a series of test to verify its correct function in the system. The new EPP boards were then integrated into their respective RAPID flight units and went through environmental testing with their unit. The first RAPID instrument was delivered to the CLUSTER II satellite contractor in January 1999. Successive RAPID units went through the same integration and environmental testing exercises over the next year and were delivered to the satellite contractor according to the ESA schedule.

During 1999, the IES system was calibrated in an electron beam at Goddard Space Flight Center. The results of all the testing are too voluminous to show here but are available in a reduced form with significant textual description via a single Internet site maintained by the Rutherford Appleton Laboratory (RAL) part of the RAPID team (URL: http://sspg1.bnsc.rl.ac.uk/Share/Rapid/rapid/ rapid.html). That site also provides a detailed description of how the temperature variations and integration times are changed and accommodated. Another source of detailed operational information for IES is to be found in an MPAe document entitled "Phoenix and CLUSTER II RAPID: Customizing the IES Software" at URL ftp://unix1.mpae.gwdg.de/pub/mpae/cluster/ies_h_b.pdf. These resources plus the description in the Appendix provide the information necessary to operate and use the IES/EPP system and understand the data.

The CLUSTER II spacecraft were successfully launched in summer of 2000, and the commissioning of the satellites and instruments proceeded throughout the fall. In December 2000, the CLUSTER II spacecraft performed a series of on-orbit EMC tests. The EMC testing is just ending at the time this report was being drafted.

All the goals for the EPP were achieved, and all the units have performed perfectly on orbit during the commissioning phase. All the logical functions of the EPPs were tested for the RAPID units on all four CLUSTER II spacecraft. At present, the initial data taken during the commissioning phase are being analyzed. The results of this analysis will be used to optimize the IES/EPP operations for the science data taking phase of the mission.

Table A1. The 0-255 bins of the IES ADC output related
to the 16 (0–15) data channels of transmitted
data. The pedestal is normally contained in the
bottom four channels. The channels get renum-
bered as ep0–ep3 and E0–E11; see text.

E-ADC Channel Range Range: 0...255	Bin Number Range: 0...15
0	0
1...(P–2S–1)	1
(P–2S)...(P–S–1)	2
(P–S)...(P–1)	3
P...(P+S–1)	4
(P+S)...(P+3S–1)	5
(P+2S)...(P+B1–1)	6
(P+B1)...(P+B2–1)	7
(P+B2)...(P+B3–1)	8
(P+B3)...(P+B4–1)	9
(P+B4)...(P+B5–1)	10
(P+B5)...(P+B6–1)	11
(P+B6)...(P+B7–1)	12
(P+B7)...(P+B8–1)	13
(P+B8)...254	14
255	15

ues may be further compressed by the RDPU, either by combining values to get long-term averages
and/or the reducing the 24-bit values to 8-bit values in a floating-point representation.

The LUT mapping is based on the calibration of the flight sensor system with electrons, X-ray
sources, and precision reference pulsers. Each detector-amplifier string has to be separately charac-
terized. In the end, there is an association in terms of the energy in keV/ADC channel and an offset
for each string. The pedestal is a major contributor to "offset" and results from a combination of
leakage current in the RAL chip and system noise. Usually, the pedestal has a relatively narrow
spread but is offset significantly from zero in ADC channel space. The lowest useful telemetered
energy channel must be set above the pedestal. To get a match between all 12 non-pedestal detectors'
energy channels means that the lowest useful energy channel ($E_{0,x}$ in the 12-channel RSC space) for
all the detectors is determined by the "noisiest" of the 9 detector-amplifier strings (the xth string).
Thus, $E_{0,x}$ is the lowest electron energy that can be usefully measured by the IES system. This rela-
tionship between one E_0 and the Pedestal is shown schematically in panel (a) of Figure A1. This E_0
becomes the reference energy for all remaining energy channels derived from this detector string.
The lower bounds, in keV, for channels E_0 through E_{11} are equally spaced in a logarithmic sense. E_{11}
is an integral channel. The lower bound of E_{11} is determined by the measured proton sensitivity. It
should be set so that the lower energy channels are proton free. These constraints give rise to an algo-
rithm for determining the 16 E_i for each detector string. If $ADC_{L,j}$ is the ADC channel number for
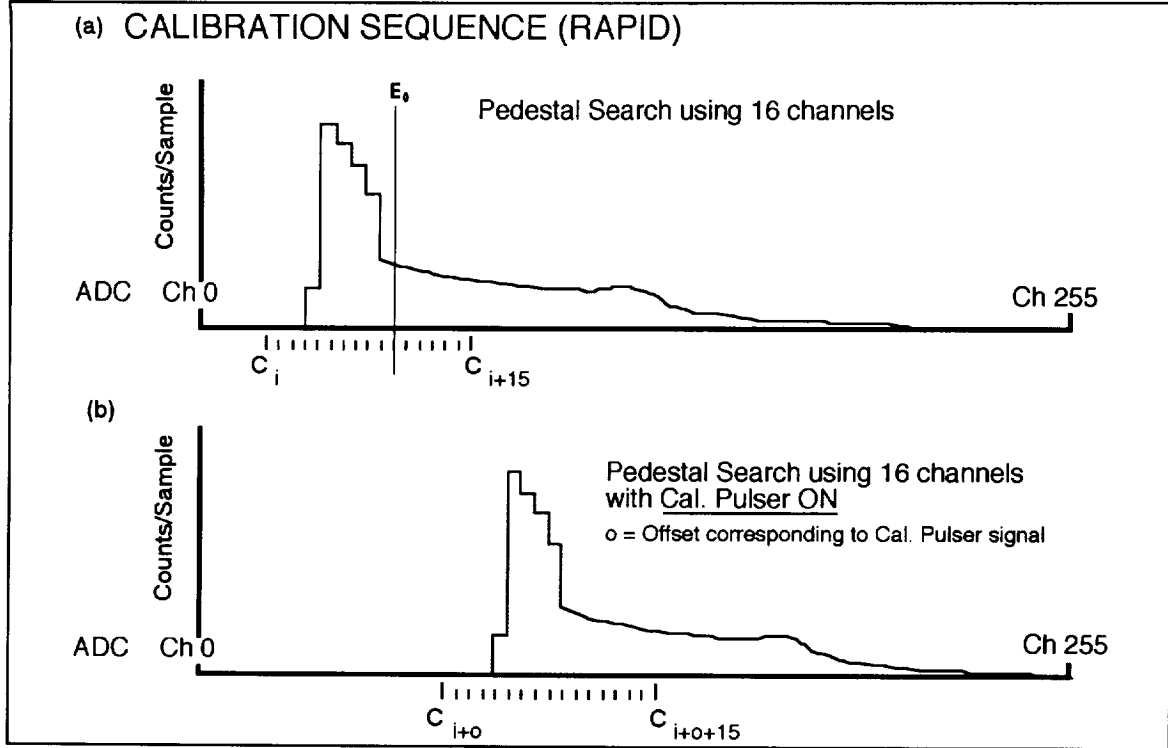string j that corresponds to the lowest useful energy for the IES ($E_{0,x}$) and $ADC_{U,j}$ corresponds to the

Figure A1. IES "calibration sequences" showing the readout of the channel I–i+15 around the nominal pedestal position (panel (a)) or channel i+o and i+o+15 around the offset (o) pedestal position when the calibration pulser is on (panel (b)). The E_0 in panel (a) shows the nominal position of the lower ADC channel boundary for the 0th rate scalar.

highest useful electron energy for IES ($E_{11,y}$; i.e. proton free with string y having lowest value) then the thresholds for E_0 through E_{11} can be determined as:

$$ADC(E_{i,j}) = ADC_{L,j} \bullet 10^{\left\{ i \bullet \left[\log(ADC_{U,j}) - \log(ADC_{L,j}) \right] / 11.0 \right\}},$$

where ADC ($E_{i,j}$) is the first ADC channel number corresponding to channel $E_{i,j}$. This should then define the break points for $E_{0,j}$ through $E_{10,j}$. $E_{11,j}$ is the sum of $E_{2,j}$ through $E_{10,j}$ and is an integral channel that is defined to be relatively free of protons. If need be, the upper energy range of $E_{11,j}$ could be lowered to $E_{9,j}$ or $E_{8,j}$ to guarantee a proton-free integral channel.

2.   Pedestal Shifts and Its Accommodation

In addition to the above channels, on RAPID, we also sample the pedestal itself using, nominally, four data channels ep0–ep3 in high-rate data and two, centered on the pedestal, in normal mode. These pedestal monitoring data are used to determine whether there is a shift in the pedestal position because of rate or temperature effects. Small shifts in the pedestal position that occur slowly can be removed from the science data using algorithms developed for the Polar/CEPPAD program. These

13

algorithms allow one to produce a "clean" and resampled dataset that represents the unshifted data quite accurately.

In automatic mode, IES counting rates are monitored by the EPP and microprocessor to determine whether pulse height pileup may be occurring. Such pileup distorts the electron spectrum. When the IES counting rates exceed predetermined values (based on laboratory test data), a signal is sent to switch the RAL chip to a shorter integration time, and the EPP then processes the incoming data using the LUTs appropriate to the new integration time. (Normally, the longer the integration time the shorter the sensor deadtime and the more sensitive the measurement is. At shorter integration time, the deadtime increases, and the number of non-pedestal counts decreases.) This integration time auto-switching is shown schematically in Figure A2. The system monitors the IES rates continuously to determine whether to step up or step down in integration time. The rates must exceed the threshold level for one cycle time before the integration time is changed. This is done to avoid oscillation in the integration times. Experience with this procedure on the Polar/CEPPAD IES has shown that the switches are rare, occurring only a few times per orbit as the satellite comes from large distances towards the Earth and traverses the intense fluxes of the radiation belts. The automatic mode can also be commanded off with the IES integration time fixed at one of the four times noted above. Since the normal CLUSTER II operating mode is to turn experiments off as it approaches perigee, the fixed integration time mode will be used relatively often.

3.   Calibration Sequence

The detectors and electronics suffer radiation damage and degrade with time on orbit. The thermal control materials on the IES will also degrade with time allowing the temperature to rise. The degradation will give rise to increased "noise," changes in offsets, and changes in gain in each detector string. There is no guarantee that all detector strings will degrade in the same way. In any case, the changes must be monitored and the transmitted data channel definitions created, by the LUT mapping, corrected and matched on a continuous basis. This requires that the IES be run through a "Calibration Sequence" (denoted ECAL) periodically to monitor the performance of the sensor system and
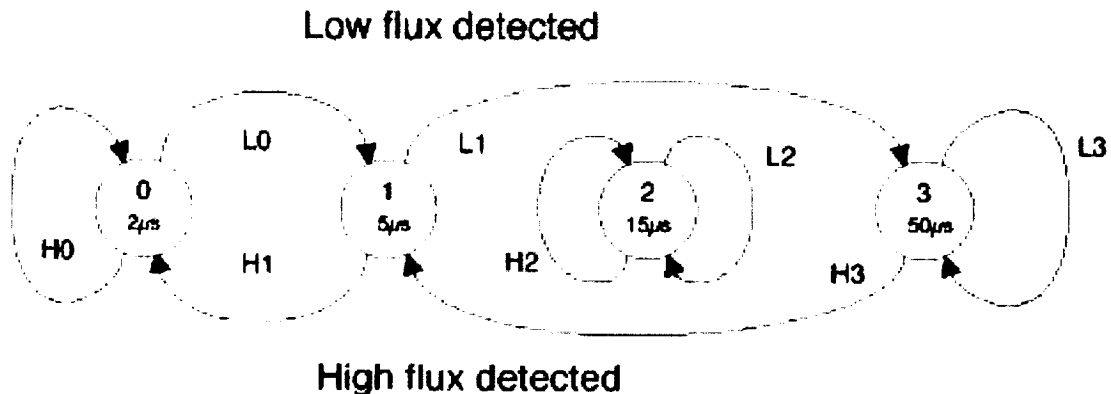
Low flux detected

High flux detected

Figure A2. The automatic switching of the IES integration time by the EPP. The arrows show the direction of change. The 15-μs mode can be substituted in the logic chain in place of either the 5-μs or 50-μs integration time. At launch, the nominal switching includes the 2, 5, and 50 μs deadtime.

gather data for redefining the E_i break points as necessary. The ECAL has two parts. In the first part, the ADC channels near the known pedestal position are transmitted so that pedestal drift can be detected and corrected for. The second part utilizes the IES's built-in test pulser (BIT) to stimulate the amplifier inputs for all strings. The position of the BIT signal in ADC channels is determined for each string and used to check the system gain. The pedestal data and gain data for each channel are processed, and the $E_{i,j}$ thresholds are "tweaked" as necessary.

4.   Rapid Calibration

The RAPID ECAL is complicated since the T/M bandwidth of RAPID, and its RDPU handling of the data is much different from that done on Polar/CEPPAD upon which it is based. In RAPID, we are able to transmit only eight data channels at a time. Thus, the CAL takes much longer since we must scan through the ADC channel regions where the pedestal and pulser responses are expected to be. This is done by defining a table of initialization points in ADC channel space, $C_{i,j}$, for each of the j detectors. This tells the RDPU which of the 256 ADC channels is the first to be read out for the jth detector during the pedestal search. Eight channels are read out, starting with $C_{i,j}$. This is incremented by 8 on successive readouts until the remaining ADC channels for the jth detector have been transmitted or until some fixed number of channels has been read out [e.g., 16 or 32 channels is the strawman proposal for RAPID.] A second set of initialization points, $C_{k,j}$, is used to read out the region containing the BIT pulser data for the jth detector string. Again, this is incremented by 8 on successive readouts until the remaining ADC channels for the jth detector have been transmitted or until some fixed number of channels has been read out [e.g., 16 channels].

Clearly, the most efficient use of T/M and orbital time is gained by reading out the minimum number of ADC channels for each string that will guarantee that the necessary data is obtained. For RAPID, this is done by reading out no more than 16 or 32 ADC channels for the pedestal and the same number for the BIT pulse. Figure A1(a) shows the relationship between nominal ADC outputs and a 16 data channel readout interval defined by $C_{i,j}$. If the calibration pulse is on, then the ADC channels selected for output are determined by the known calibration "picket" position, and 16 channels surrounding that position are read out to determine the corresponding amplifier gain (see Figure A1(b)). These are different ways of mapping portions of the 256 ADC channels into the 16 data channels.

15