Power SiGe Heterojunction Bipolar Transistors (HBTs) Fabricated by Fully Self-Aligned Double Mesa Technology

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***Abstract*- Multifinger SiGe HBTs have been fabricated using a novel fully self-aligned double-mesa technology. With the novel process technology, a common-emitter 2×2×30 μm^2 device exhibits high maximum oscillating frequency (f_{max}) and cut-off frequency (f_T) of 78 and 37 GHz, respectively. In class-A operation, a multifinger device with 10×2×30 μm^2 emitter is expected to provide an output power of 25.6 dBm with a gain of 10 dB and a maximum power added efficiency (PAE) of 30.33% at 8 GHz.**

I. INTRODUCTION

Recent advances in the growth of exitaxial SiGe layers have led to high quality SiGe heterojunctions and consequently high performance SiGe heterojunction bipolar transistors (HBTs)[1]-[3]. With the mature Si process technology, the Si-based microwave monolithic integrated circuits (MMICs) have received great attention as a potential candidate for the wireless communication market. Microwave circuits such as low-power broadband amplifiers[4], Gilbert mixers[5] and voltage controlled oscillators[6] have been demonstrated using SiGe HBTs. However, it is still a challenge to implement power amplifiers at frequencies above X-band. The availability of high-performance SiGe power devices will be the key to the success of realizing a microwave system on a chip using Si substrate.

Double-mesa technology has been widely used to investigate the HBT performance. In this work, a novel fabrication technology has been developed to achieve a fully self-aligned double-mesa structure for power SiGe HBTs, resulting in a significant reduction of device parasitics. Common-emitter multifinger devices have been fabricated and characterized for both small-signal and large-signal operations.

II. DESIGN AND FABRICATION

The epitaxial growth of the power SiGe HBT structure starts with a high-resistivity Si substrate (ρ=3000 Ω-cm), followed by a CVD buried layer for subcollector. Then complete heterostructure is grown in one step by molecular beam epitaxy (MBE) as shown in Table 1. In this design, a $Si_{0.7}Ge_{0.3}$ base layer with a thickness of 200 Å has been employed to optimize the f_{max} of the device, while a relatively thick Si collector layer has been designed to achieve high power operation.

Table 1 Power SiGe HBT structure.

Emitter cap	Si	n^+	1×10^{20}	150 nm
Emitter	Si	n	1×10^{18}	50 nm
Spacer	$Si_{0.7}Ge_{0.3}$	i		5 nm
Base	$Si_{0.7}Ge_{0.3}$	p^+	1×10^{20}	20 nm
Spacer	$Si_{0.7}Ge_{0.3}$	i		5 nm
Collector	Si	n^-	1×10^{16}	500 nm
Subcollector	Si	n^+	1×10^{19}	1 μm
Substrate	Si	p^-	1×10^{12}	540 μm

Multifinger HBT devices have been designed and fabricated in common-emitter configuration. Effort has been made to design the layout of the unit cell with minimal parasitics. For device layout, the emitter finger with a dimension of 2×30 μm^2 was surrounded by two base electrodes with a width of 1.5 μm, and contact has been made through emitter pads, which were isolated from the intrinsic part of the device. In order to alleviate the thermal stability problems, the spacing between two emitter fingers was chosen to be 12 μm. In addition, collector electrodes were inserted in between the emitter fingers,

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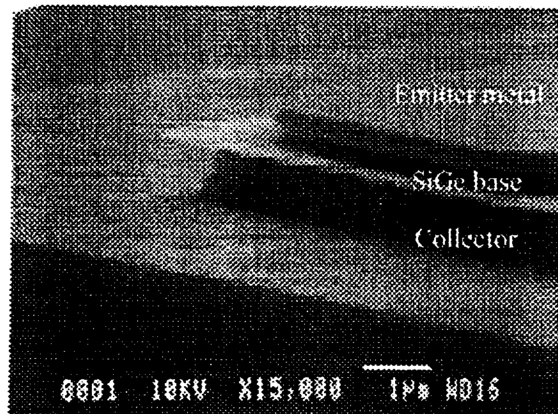
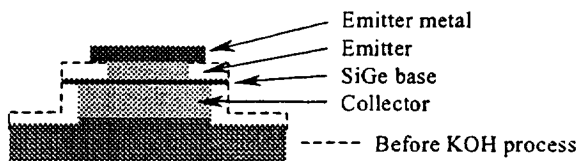
minimizing the collector resistance of the HBT devices.

A novel fully self-aligned process technology has been developed to fabricate the double-mesa SiGe HBT. The fabrication started with emitter metal (Cr/Au) deposition, followed by two consecutive reactive ion etch (RIE) steps for base mesa formation and device isolation, respectively. Up to this point, either p^+ base nor n^- subcollector has been exposed for contact. Then a KOH etch step has been performed to expose base and collector contact simultaneously without lithography patterning. Due to the etch selectivity of KOH between Si and SiGe, only Si layers have been etched away, creating undercuts underneath the emitter metal and the SiGe base as shown in Fig. 1. After the KOH process, Ti/Au was deposited for base and collector metallization simultaneously, resulting in a fully self-aligned double-mesa structure. A 1 μm-thick PECVD SiO_2 deposition was employed for device passivation, followed by via hole formation using RIE. Then a deposition of 1.5 μm-thick interconnection (Ti/Al/Ti/Au) completed the device fabrication.



(a)



(b)

Fig.1 Base/subcollector exposure using KOH etch. (a) Photomicrograph. (b) Cross section.

This unique process technology provides several advantages; First of all, self-aligned base and collector metal are available, resulting in a reduction in both base and collector access resistance. Secondly, the laterally etched undercut created underneath the SiGe base layer reduces the area accountable for extrinsic base-collector capacitance C_{BC}. As a result, the f_{max} of the device can be improved significantly. In addition, the KOH process, which has been performed after the device isolation, also removed the Si layers underneath the emitter metal outside the intrinsic region. As a result, isolated pads for emitter contact are available for this technology, resulting in smaller parasitic capacitance between base and emitter. Figure 2 shows the photomicrograph of the fabricated SiGe HBT with 10 emitter fingers.

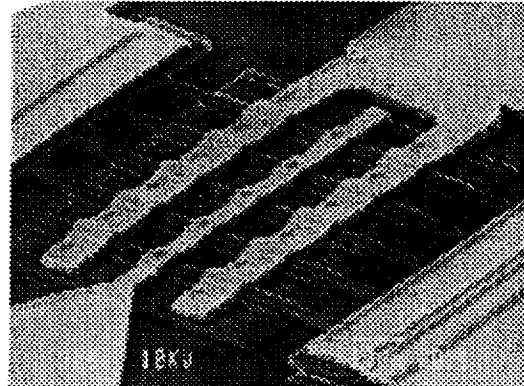


Fig. 2 Photomicrograph of the fabricated 10-finger common-emitter power HBT.

III. DEVICE CHARACTERISTICS

The DC characteristics of the devices have been measured with HP4155 semiconductor parameter analyzer. With a collector thickness of 5000Å and a doping concentration of $1\times10^{16}cm^{-3}$, the open-base breakdown voltage BV_{CBO} and the open-emitter breakdown voltage BV_{CEO} are 25 V and 10 V, respectively. The I-V characteristics of a 2-finger device is shown in Fig. 3, and it exhibit a maximum DC current gain β of 26 and a maximum differential current gain Δβ of 33.

For small-signal RF characteristics, on-wafer probing S-parameter measurement has been performed using HP8510C network analyzer from 2 to 40 GHz. Figure 4 shows the current

gain |h21| and the unilateral power gain U of the two-finger device at a DC bias of I_C=28 mA and V_{CE}=6V. The values of f_T and f_{max}, extrapolated with the assumption of −20 dB/decade roll-off, are 37 and 78 GHz, respectively. In order to investigate the improvement on device parasitics by employing the process technology, parameters of the small-signal equivalent circuit have been extracted the measured S-parameters. The small-signal equivalent circuit and the extracted parameters are shown in Fig. 5. Compared with the standard double-mesa technology, a significant reduction of C_{BC}, up to 40%, has been observed.

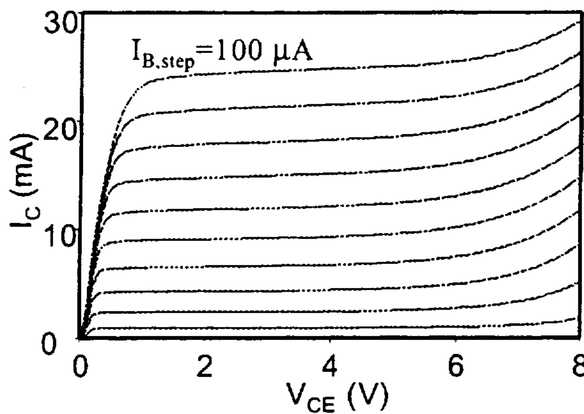


Fig. 3 The I-V characteristics of the 2-finger common-emitter device.

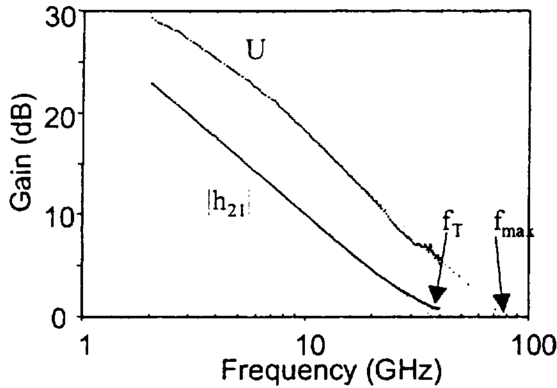
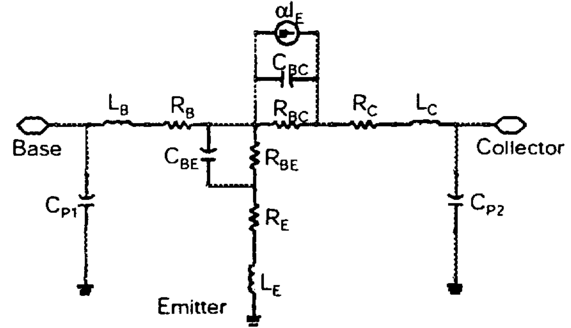


Fig. 4 Measured small-signal frequency response of the 2-finger device. (I_C=28 mA, V_{CE}=6 V)

In addition to the small-signal operation, load-pull power measurement and Gummel-Poon model have been used to characterize the large-signal operation of the multifinger HBTs. Both standard and fully self-aligned technologies have been employed to fabricate HBT devices on a CVD grown structure. Table 2 shows the results of the power measurement performed on the fabricated devices to compare the performance of different process technologies. As shown in Table 2, enhanced small-signal and power performance can be achieved by applying the fully self-aligned technology.



R_B	1.7 Ω	R_{BC}	33 kΩ
L_B	50 pH	C_{BC}	79 fF
R_{BE}	1.81 Ω	R_C	14 Ω
C_{BE}	270 fF	L_C	30 pH
R_E	1.1 Ω	$C_{P1,2}$	17 fF
L_E	30 pH	α_0	0.96

Fig. 5 Small-signal equivalent circuit and the extracted parameters of a 2-finger device. (I_C=28 mA, V_{CE}=6 V)

Large-signal Gummel-Poon models of multifinger HBTs on CVD and MBE grown wafers were extracted from multi-bias S-parameters and DC measurement. In the case of CVD grown devices, the large-signal models showed very good agreement with load-pull power measurement. In the case of MBE grown devices, the large-signal model was used to predict the power performance of the 10-finger HBT. (also shown in Table 2)

Since the MBE grown devices with fully self-aligned structure have much higher f_{max} than CVD grown devices, it is expected that their power performance be better than CVD grown devices. This is also observed from the large-signal modeling of these devices as shown in Fig. 6. A common-emitter 10-finger device in class-A at 8 GHz exhibits a maximum PAE of 30.33%

and output power of 25.6 dBm at an input power of 15 dBm.

Table 2. The load-pull power measurement of CVD grown devices at 8 GHz. (* simulated power performance of MBE grown devices)

Technology	Finger #	f_{max} (GHz)	Pin (dBm)	Pout (dBm)	PAE (%)
Standard double-mesa (CVD)	8	33	17.1	19.9	22.8
	10	28	-	-	-
Fully self-aligned (CVD)	10	32	19.8	23.1	29.9
Fully self-aligned (MBE)	10	43	15*	25.6*	30.3*

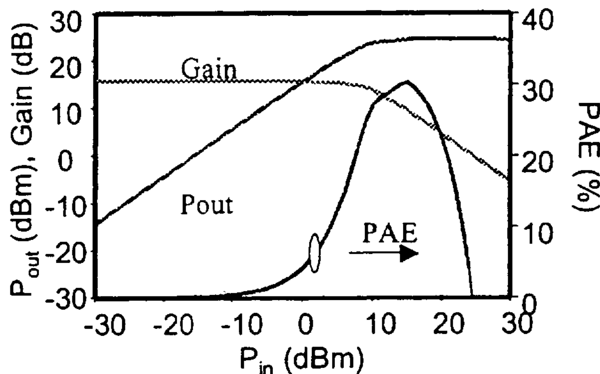


Fig. 6 The simulated power performance of 10-finger device at 8 GHz for optimized class-A PAE.

IV. CONCLUSION

Using KOH process to expose the p^+ base and n^+ subcollector layers after double-mesa formation, a SiGe HBT with self-aligned base and collector contacts has been demonstrated. By adopting this technology, the lateral undercut in the collector layer underneath the base contact also reduces the base-collector capacitance, C_{BC}, resulting in a significant improvement on f_{max}. In addition, DC, small-signal and large-signal characterization have been performed on the multifinger devices for circuit applications. Load-pull measurement of the MBE grown power devices will be presented and discussed.

ACKNOWLEDGEMENT

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