



Novel Low Loss Wide-Band Multi-Port Integrated Circuit Technology for RF/Microwave Applications

Rainee N. Simons
QSS Group, Inc., Cleveland, Ohio

Kavita Goverdhanam
Bell Laboratories, Murray Hill, New Jersey

Linda P.B. Katehi
University of Michigan, Ann Arbor, Michigan

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Rainee N. Simons
QSS Group, Inc., Cleveland, Ohio

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NOVEL LOW LOSS WIDE-BAND MULTI-PORT INTEGRATED CIRCUIT TECHNOLOGY FOR RF/MICROWAVE APPLICATIONS

Rainee N. Simons,¹ Kavita Goverdhanam,² and Linda P.B. Katehi³

Abstract – In this paper, novel low loss, wide-band coplanar stripline technology for RF/microwave integrated circuits is demonstrated on high resistivity silicon wafer. In particular, the fabrication process for the deposition of spin-on-glass (SOG) as a dielectric layer, the etching of microvias for the vertical interconnects, the design methodology for the multiport circuits and their measured/simulated characteristics are graphically illustrated. The study shows that circuits with very low loss, large bandwidth and compact size are feasible using this technology. This multilayer planar technology has potential to significantly enhance RF/microwave IC performance when combined with semiconductor devices and microelectromechanical systems (MEMS).

I. INTRODUCTION

Recently, silicon/silicon germanium (Si/SiGe) based technology has emerged as a viable approach for integrating analog, RF and digital functions on a single integrated circuit (IC) needed for advanced wireless communications systems [1]. The Si/SiGe technology also has the advantage of low cost since the devices and circuits are fabricated using established silicon CMOS processes. The above ICs are now being introduced in products with more functions in a small volume, involving greater circuit/function integration. To accomplish this goal, multiport three-dimensional interconnects are needed.

In this paper, we present several new design concepts for low loss, wide bandwidth multiport integrated circuits on a high resistivity (HR) silicon wafer. The multiport circuits are made of small sections of coplanar stripline (CPS) or a junction formed by the intersection of several CPS interconnects printed at two levels separated by a thin layer of spin-on-glass (SOG) and connected by metallized vias. The CPS has the advantage of eliminating backside processing due to its uniplanar nature and allows simplified vertical integration by the use of metallized vias. In addition, CPS allows easy integration of other transmission media, such as, slotline, finite width coplanar waveguide (FW-CPW) and micro-CPS [2] for greater design flexibility. The SOG has the advantage of low dielectric constant [3] and hence low parasitic coupling capacitance. In addition, the SOG planarizes the circuit, facilitating vertical integration [4]. The HR silicon wafer

($\rho > 3000 \Omega \text{ cm}$) has the advantage of lowering signal attenuation in addition to improving isolation between adjacent circuits. In the following sections, first, the fabrication process is briefly explained. Next, design considerations, measured insertion loss, return loss and isolation are presented for: (a) a two-port CPS overpass with vertical interconnect, (b) a three-port CPS T-junction with vertical interconnect and (c) a four-port CPS crossover. The results are discussed extensively. The numerical simulations are carried out using the CST Microwave Studio™. In the simulations, the CPS conductors are assumed to be perfectly conducting. In addition, the silicon substrate as well as the SOG layer are considered as perfect dielectrics.

II. INTERCONNECT FABRICATION

The first step is the fabrication of the buried strip conductors using titanium/gold on the HR silicon wafer. These conductors are fabricated using a lift-off process. The thickness of the metal is about $0.8 \mu\text{m}$. Next, a thin insulating spacer layer to support the elevated strip conductors is built-up to the required thickness by multiple spin-coats. Accuglass® 512 SOG of thickness h_1 about $2.0 \mu\text{m}$ is used as the dielectric spacer layer. Third, the vias for the vertical interconnect is patterned using photoresist and dry etched in a fluorocarbon-based plasma. As a last step, the elevated strip conductors are fabricated using titanium/gold by a second lift-off process. This step also metallizes the via holes to ensure electrical continuity between the buried and elevated strip conductors. The thickness of the elevated strip conductor is about $2.0 \mu\text{m}$. The cross-section of the CPS is shown in Fig. 1.

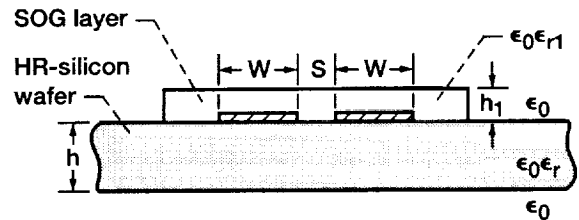


Figure 1.—Coplanar stripline (CPS) on a HR-silicon wafer with a SOG layer on top, $h = 400 \mu\text{m}$, $\epsilon_r = 11.7$, $h_1 = 2 \mu\text{m}$, $\epsilon_{r1} = 3.1$.

¹NASA Glenn Research Center, QSS, Inc., Cleveland, Ohio 44135

²Bell Laboratories, Lucent Technologies, Murray Hill, New Jersey 07974.

³University of Michigan, Radiation Laboratory, EECS Department, Ann Arbor, Michigan 48109-2122.

III. DESIGN, RESULTS AND DISCUSSIONS

The design considerations for the via hole and probe pads for each of the aforementioned interconnects are as follows: each via is symmetrically located on the strip conductor and has a diameter (d) which is a function of the strip width (W). A via pair is designed as a small section of a vertical balanced transmission line with characteristic impedance $Z_{0(\text{via})} = 50 \Omega$. The $Z_{0(\text{via})}$ is related to the diameter (d), separation between vias (S_1) and the dielectric constant of the medium surrounding the via (ϵ_{r1}) through the expression:

$$Z_{0(\text{via})} = (60/\sqrt{\epsilon_{r1}})\cosh^{-1}(N)$$

where $N = 0.5[(2S_1/d)^2 - 2]$.

The probe pads are about $100 \times 100 \mu\text{m}$ in size for compatibility with the signal-ground RF probes for on-wafer characterization. In all of the measurements the parasitics associated with the probe pads and the $700 \mu\text{m}$ long lines between the pads and the circuits are de-embedded using on-wafer CPS Thru-Reflect-Line (TRL) calibration standards. The coplanar stripline circuits investigated here are uniplanar in construction and hence do not have a ground plane on the opposite side of the wafer. Therefore, the wafer is supported on a Styrofoam™ block, instead of the regular metal vacuum chuck, in the RF probe station while measuring the S-parameters.

A. Two-port CPS overpass with vertical interconnect:

This circuit is shown in Fig. 2. The characteristic impedance $Z_{0(\text{CPS})}$ is 50Ω . The length of the overpass is $>(2W+S)$ to ensure a clear passage below for a 50Ω line. The measured (de-embedded) and simulated insertion loss (S_{21}) and return loss (S_{11}) are shown in Fig. 3. The S_{21} and S_{11} are better than -0.5 and -22.0 dB, respectively. The S_{21} includes losses due to the $216 \mu\text{m}$ long CPS overpass and the vias at either ends. The loss in the $216 \mu\text{m}$ line is 0.08 dB at the center frequency of 10.0 GHz [4]. Hence the loss per via pair is about 0.21 dB. The numerical simulations of this circuit show that the insertion loss is negligibly small and the return loss is better than -35 dB across the 3 to 18 GHz frequency range.

B. Three-port CPS T-junction with vertical interconnect:

A schematic and a microphotograph of the circuit are shown in Figs. 4(a) and 4(b), respectively. From the microphotograph it is seen that the width of the elevated strip conductor is reduced by symmetrically notching out a rectangular portion of the strip at the location of the overlap with the buried strip conductor. The notch compensates for the parasitic parallel plate capacitance at the overlap region. The characteristic impedance $Z_{0(\text{CPS})}$ of each arm is 50Ω . No attempt was made to match the junction in the initial

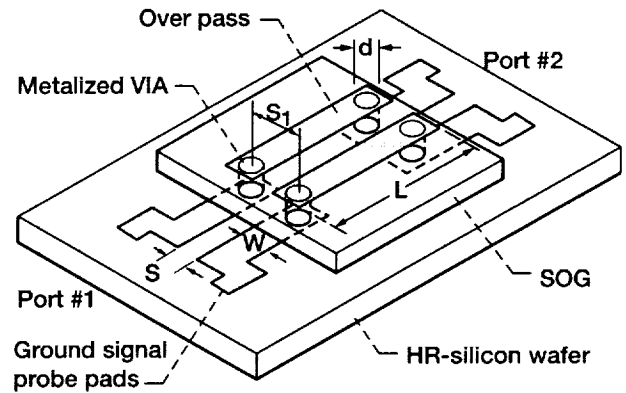


Figure 2.—CPS overpass with vertical interconnects, $W = 54 \mu\text{m}$, $S = 4 \mu\text{m}$, $d = 45 \mu\text{m}$ and $L = 216 \mu\text{m}$.

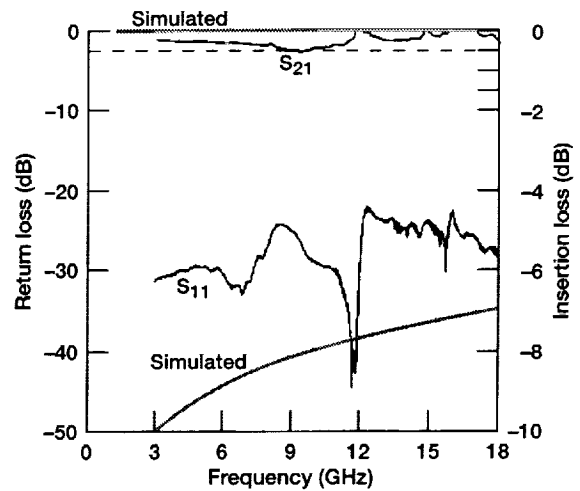


Figure 3.—Measured (de-embedded) and simulated insertion loss (S_{21}) and return loss (S_{11}) of CPS overpass.

investigation. Contrary to a conventional slotline T-junction, the new circuit can provide equal phase at both output ports.

The measured (de-embedded) and simulated insertion loss (S_{21} and S_{31}) at the two output ports and the input return loss (S_{11}) are shown in Fig. 5. It is observed that the power output from ports 2 and 3 are unequal but it is within -3.0 ± 0.5 dB over the frequency range of 8.5 to 9.5 GHz. The phase of S_{21} and S_{31} differ by 20° at the center frequency $f_0 = 9.0$ GHz. The above insertion loss includes the losses associated with the right angle bend integrated at the output ports of the circuit to facilitate in-line characterization using straight CPS TRL calibration standards and RF probes. The numerical simulations show that the power output from ports 2 and 3 (S_{21} and S_{31}) are about -3.5 dB and the return loss (S_{11}) is about -9.5 dB across the frequency range of 1 to 18 GHz.

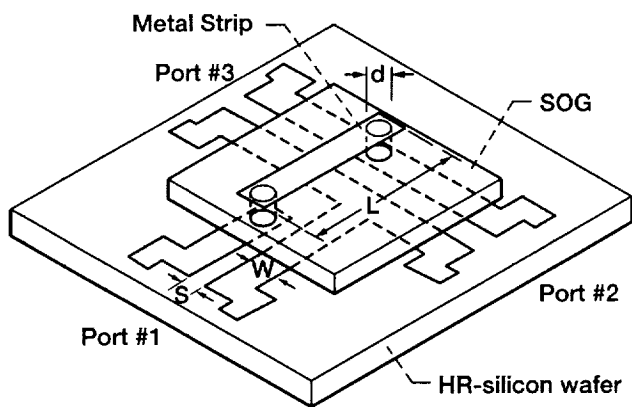


Figure 4(a).—CPS T-junction with vertical interconnects, $W = 40 \mu\text{m}$, $S = 3 \mu\text{m}$, $d = 45 \mu\text{m}$ and $L = 243 \mu\text{m}$.

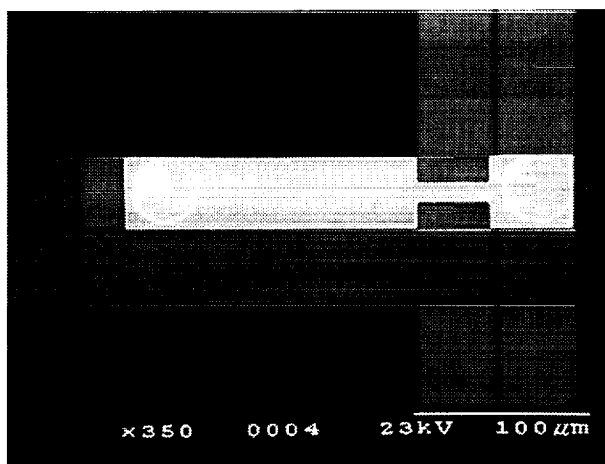


Figure 4(b).—Microphotograph of CPS T-junction.

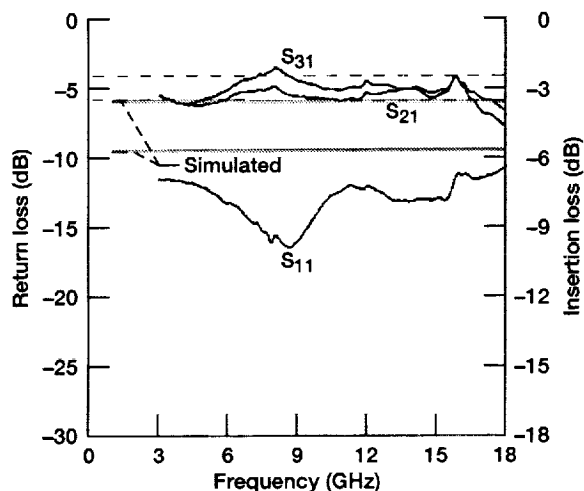


Figure 5.—Measured (de-embedded) and simulated insertion loss (S_{21} and S_{31}) and input return loss (S_{11}) of CPS T-junction.

C. Four-port CPS crossover with vertical interconnect:

A schematic and a microphotograph of the circuit are shown in Figs. 6(a) and 6(b), respectively. The simulated characteristics using FDTD technique are presented in [4]. In this paper, the experimentally characterized results are reported. The measured (de-embedded) and simulated insertion loss (S_{21}) and return loss (S_{11}) of the in-line ports are better than -0.5 and -30.0 dB, respectively (Fig. 7). The measured (de-embedded) and simulated isolation (S_{31}) between the orthogonal ports is better than -45.0 dB up to 8.0 GHz and is -22.0 dB at 18.0 GHz (Fig. 8). The numerical simulations show that insertion loss (S_{21}) negligibly small and the return loss (S_{11}) is better than -45 dB across the 1 to 18 GHz frequency range. The isolation (S_{31}) is also better than -45 dB across the same frequency range. Since this interconnect has low loss and excellent isolation, it has potential applications in the construction of multilayer CPS circuits [5] and MEMS-based actuators for reconfigurable antennas [6].

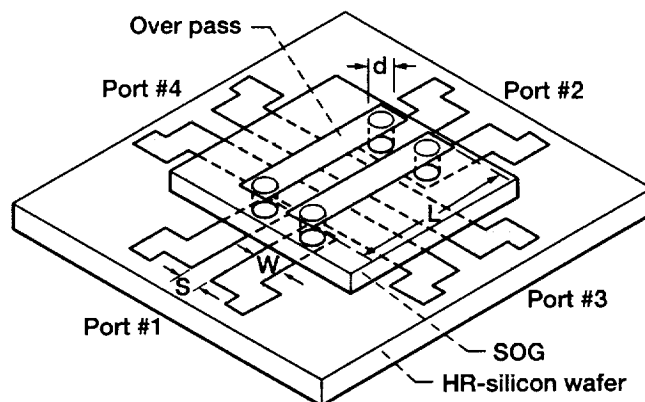


Figure 6(a).—CPS Vertically interconnected overpass, with crossover $W = 40 \mu\text{m}$, $S = 3 \mu\text{m}$, $d = 33 \mu\text{m}$ and $L = 243 \mu\text{m}$.

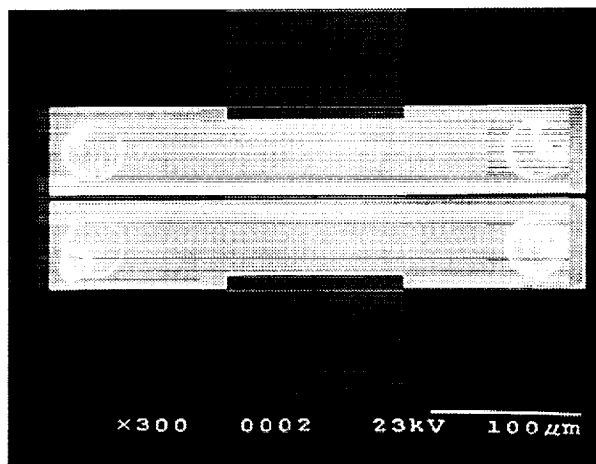


Figure 6(b).—Microphotograph of CPS overpass with crossover.

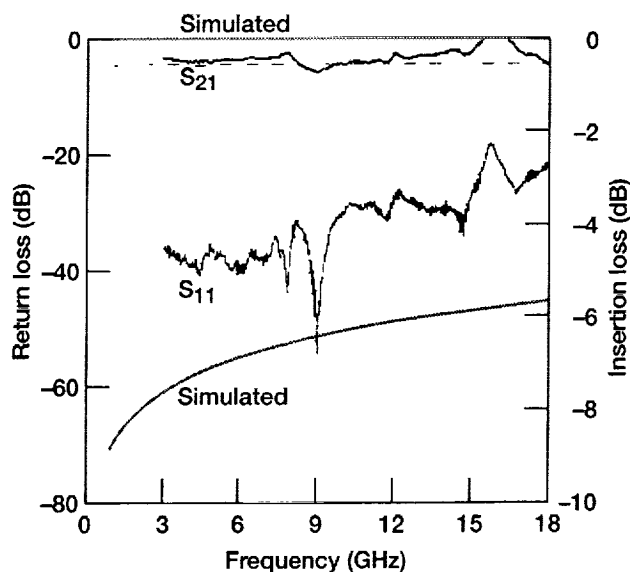


Figure 7.—Measured (de-embedded) and simulated Insertion loss (S_{21}) and return loss (S_{11}) of CPS overpass with crossover.

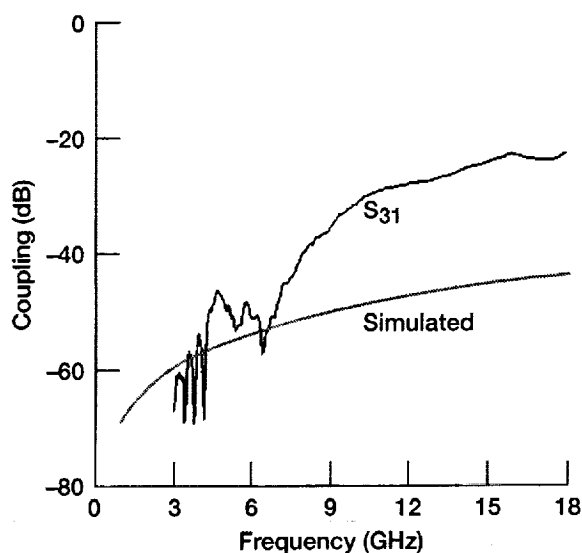


Figure 8.—Measured (de-embedded) and simulated coupling (S_{31}) of CPS overpass with crossover.

IV. CONCLUSIONS

A novel low loss wide bandwidth multiport integrated circuit technology suitable for applications at RF/microwaves has been proposed. These CPS multiport circuits have small dimensions compared to the wavelength of operation, resulting in low parasitics. Consequently these circuits have an almost ideal performance with low loss, good impedance match, good isolation and large bandwidth. As examples, a two-port CPS overpass with vertical interconnect, a three-port CPS T-junction with vertical interconnect and a four-port CPS crossover with vertical interconnect have been presented. The results presented demonstrate the potential of the proposed approach in enhancing Si/SiGe RF/microwave IC performance.

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