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Adaptive Instrument Module: Space Instrument Controller "Brain" through Programmable Logic Devices

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Abstract

The Adaptive Instrument Module (AIM) will be the first true demonstration of reconfigurable computing with field-programmable gate arrays (FPGAs) in space, enabling the "brain" of the system to evolve or adapt to changing requirements. In partnership with NASA Goddard Space Flight Center and the Australian Cooperative Research Centre for Satellite Systems (CRC-SS), APL has built the flight version to be flown on the Australian university-class satellite FEDSAT.

The AIM provides satellites the flexibility to adapt to changing mission requirements by reconfiguring standardized processing hardware rather than incurring the large costs associated with new builds. This ability to reconfigure the processing in response to changing mission needs leads to true evolveable computing, wherein the instrument "brain" can learn from new science data in order to perform state-of-the-art data processing. The development of the AIM is significant in its enormous potential to reduce total life-cycle costs for future space exploration missions. The advent of RAM-based FPGAs whose configuration can be changed at any time has enabled the development of the AIM for processing tasks that could not be performed in software. The use of the AIM enables reconfiguration of the FPGA circuitry while the spacecraft is in flight, with many accompanying advantages. The AIM demonstrates the practicalities of using reconfigurable computing hardware devices by conducting a series of designed experiments. These include the demonstration of implementing data compression, data filtering, and communication message processing and inter-experiment data computation. The second generation is the Adaptive Processing Template (ADAPT) which is further described in this paper.

The next step forward is to make the hardware itself adaptable and the ADAPT pursues this challenge by developing a reconfigurable module that will be capable of functioning efficiently in various applications. ADAPT will take advantage of radiation tolerant RAM-based field programmable gate array (FPGA) technology to develop a reconfigurable processor that combines the flexibility of a general purpose processor running software with the performance of application specific processing hardware for a variety of high performance computing applications.

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1. Adaptive Processing Template (ADAPT)

In the past, system flexibility was primarily associated with system software. New functions and applications were accomplished by changing the sequence of instructions executed by a general-purpose processor. The next step forward is to make the hardware itself adaptable and the ADAPT pursues this challenge by developing a reconfigurable module that will be capable of functioning efficiently in various applications. ADAPT will take advantage of radiation tolerant RAM-based field programmable gate array (FPGA) technology to develop a reconfigurable processor that combines the flexibility of a general purpose processor running software with the performance of application specific processing hardware for a variety of high performance computing applications. This improved performance along with the adaptability of this technology provides significant benefits at several levels:

1. Although the basic physical hardware design remains unchanged, the hardware for the control and data interfaces can easily be programmed for a specific instrument and/or spacecraft data system architecture. This allows flight qualification of the basic hardware independent of the detailed hardware design for a specific system. This minimizes the cost of developing the basic hardware for each instrument and allows the physical design to be easily reprogrammed for any system architecture.

2. This approach also minimizes overall instrument or system development time by allowing physical and electrical testing of the hardware to proceed concurrently with the detailed design and programming of the FPGAs. Also, if an error in the design is detected during system level testing, the hardware can be easily reconfigured without having to physically remove the processor from the system. This minimizes the impact on the project schedule and risk to the flight hardware.

3. The use of RAM-based FPGA technology enables the hardware design to be reconfigured in flight to overcome both hardware and software errors that may be detected after launch during mission operations. This reduces overall mission risk which is becoming more important as flight system development times and budgets decrease in the current faster, cheaper, and better environment.

4. The ability to reconfigure the ADAPT in flight allows the processor functions to adapt to changing mission conditions and also allows improved on board processing algorithms to be uploaded to the instrument. The reconfigured processor can optimize mission operations to exploit science "targets of opportunity" as the mission progresses and also take advantage of improved data processing algorithms to return the most science for the minimum cost.

5. Reconfigurable hardware provides another level of fault tolerance. The hardware can be reprogrammed in flight to replace the function of faulty circuit components that might otherwise cause the instrument to fail. If some part of the FPGA fails, the circuitry can be redesigned and the hardware reprogrammed to avoid the faulty portions of the component. This essentially provides inherent redundancy to improve the overall mission probability of success with none of the traditional costs associated with redundant processors.

6. The use of multiple FPGAs in a processor provides a scalable architecture. The hardware can be configured as a parallel processor by sending the data to multiple FPGAs simultaneously or configured as a pipeline processor by sending the data to one FPGA first and then a second FPGA to complete the necessary processing. This allows the architecture to be optimized for the specific data processing algorithms required for an instrument providing improved performance without redesigning the basic physical hardware for each application.

An Advanced Technology Development (ATD) project at JHU/APL is developing a standalone reconfigurable logic/ASIC Simulator board that has many similarities to the ADAPT. This board stores configurations in flash memory, and allows new configurations to be downloaded by a host processor over an RS-232 link. It uses a Xilinx Virtex FPGA, the same type planned for use in the ADAPT. A photo of the module is shown in Figure 1., and a block diagram in figure 2.

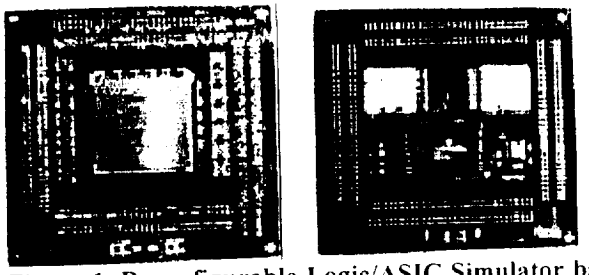

Figure 1. Reconfigurable Logic/ASIC Simulator based on Virtex FPGA

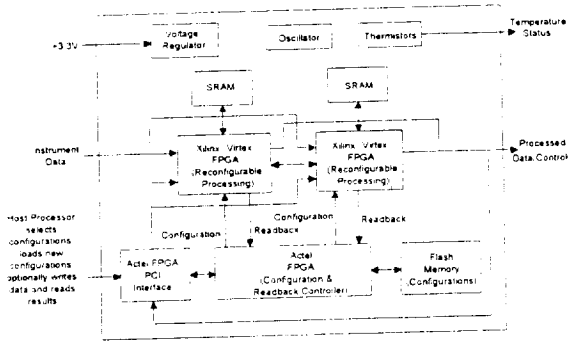

Figure 2. ADAPT System Hardware Architecture

2. ADAPT Hardware Design

The ADAPT implements complex algorithms directly in reconfigurable hardware for processing of high rate instrument data. A diagram of the ADAPT hardware architecture is shown in Figure 3. Two state of the art Xilinx Virtex FPGAs are the heart of the ADAPT. Each contains the equivalent of 1.1 million gates and 131,000 bits of RAM. A wide range of cores are available for these FPGAs, including DSP functions, processors, and math functions. New designs can be implemented with a wide range of development tools. In the ADAPT design, each Virtex FPGA is connected to SRAM memory to implement additional storage for intermediate results, coefficients, and variables that some algorithms may require. The Virtex FPGAs are interconnected to allow data to pass between them. Each is connected to the instrument data input, and each can output processed data or control information. Having at least two FPGAs on the board also provides some redundancy in case of device failure.

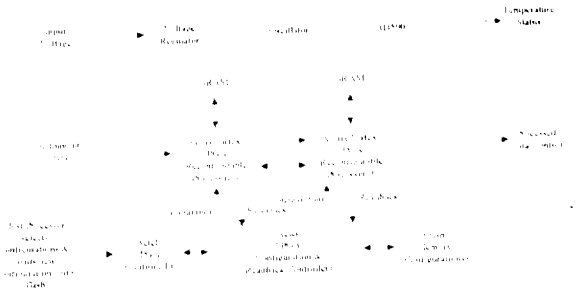

Figure 3. ADAPT Hardware Architecture

The ADAPT stores multiple FPGA configurations in flash memory. The host processor selects which configurations are to be used. This allows the instrument data processing algorithms to be changed in realtime. A fuse-programmed Actel FPGA implements the system backplane PCI interface to allow the system host processor to select the configurations to be loaded into the Virtex FPGAs. A second Actel includes the circuitry to read back the configuration from the Xilinx FPGAs and compare it to the original configuration in flash memory. If any discrepancies are detected, the configuration is autonomously reloaded, and the host processor is notified that data processing will be halted for a few seconds. Instrument data may either inputted either through the PCI bus or an I/O connector. Processed data may be either outputted over the PCI bus or an I/O connector.

The ADAPT includes a voltage regulator to supply power to the Virtex FPGAs. The voltage regulator is kept on the ADAPT board so that the host system will not have to generate +2.5V. It is expected that the card will only need to be supplied with +3.3V from the backplane. An oscillator supplies the clock needed to run the Actel FPGAs. The temperature of the Virtex parts and the linear regulator will be measured by thermistors. The thermistors will be connected to an I/O connector.

3. Spacecraft Architecture with ADAPT

An instrument that uses the ADAPT card can either have its own Compact PCI chassis, or it could be integrated directly into the spacecraft Compact PCI chassis. The second approach would yield a lower mass system, since the digital electronics for the instrument (the ADAPT card) could exist as an additional card in the spacecraft chassis, rather than as a standalone chassis. An example of this architecture is shown in figure 4. Since the bulk of the instrument processing is done in the ADAPT card, the spacecraft processor card can do the remainder of the processing with a small percentage of its resources, for example packetizing the reduced science data or

transferring the packets to the spacecraft solid state recorder. If the extra mass is available, a separate Instrument Compact PCI chassis with a dedicated processor could be implemented.

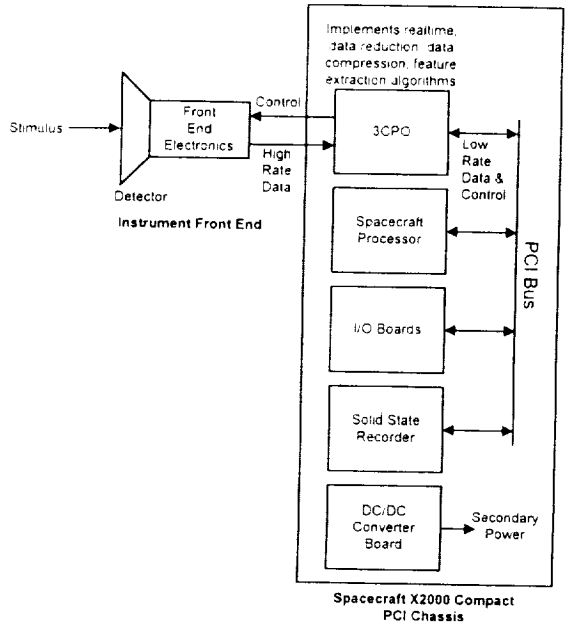

Figure 4. Spacecraft and Instrument Architecture with ADAPT

4. Technology Description and Benefits

In the past, system flexibility was primarily associated with system software. New functions and applications were accomplished by changing the sequence of instructions executed by a general-purpose processor. The next step forward is to make the hardware itself adaptable and the ADAPT pursues this challenge by developing a reconfigurable processor board that will be capable of functioning efficiently in various applications. ADAPT will take advantage of radiation tolerant RAM-based field programmable gate array (FPGA) technology to develop a reconfigurable processor that combines the flexibility of a general purpose processor running software with the performance of application specific processing hardware for a variety of high performance computing applications.

5. Potential Science Application

One of the most challenging aspects of planetary spectroscopy is identifying previously unknown sites which have a sought after mineralogic signature, measuring them, and downlinking the data. The simplest method, measuring and downlinking data that cover the entirety of a surface of interest, is appropriate for a limited volume of data having relatively low spatial resolution. However it is impractical for high spatial resolution data due to the consequently very high data volume. A somewhat more sophisticated approach would be to acquire a large volume of data, analyze it onboard, and downlink only selected portions. However this method too fails at very high spatial resolutions.

ADAPT would provide an alternative implementation that is far more efficient in usage of spacecraft resources: the ADAPT would allow an instrument to acquire and discard data continually in a standby mode, analyzing it "on the fly" and deciding autonomously when a valuable data segment should be saved. For example, taking as an example the Martian case, as few as 14 channels could be analyzed continuously (3 parameterizing ferric iron absorption bands at 660 and 860 nm, 3 parameterizing the 2000-nm atmospheric CO_2 band, 3 parameterizing the 2350-nm carbonate band, and 2 parameterizing the 3000-nm H_2O band). These absorptions are diagnostic of key aqueous phases. Key parameters for data calibration and processing would be stored in the ADAPT, including offset and gain corrections for dark current and radiometric sensitivity and a model atmospheric spectrum. The selected wavelengths from data acquired continuously in "standby" mode would be calibrated on the fly, and a first-order atmospheric correction would be performed by scaling the model atmospheric spectrum using measured 2000-nm CO_2 band depth. The processed spectra would then be parameterized and thresholded to determine when one of the mineralogic absorptions exceeded a critical value indicative of interesting mineralogy. At that point an autonomous decision would be made whether to begin a predetermined sequence of appropriate instrument operations and data storage. Similar analysis of spectra being saved would determine whether continued acquisition of new data warranted the overwriting of an existing data segment saved previously, via the same decision making process.

These algorithms will be designed for implementation in the Xilinx FPGA on the ADAPT. They will be simulated on a Mentor Graphics workstation, and simulated spectrometer data will be used as the stimulus. This will validate the design and ability of the ADAPT to meet the SSE goals of reducing downlink and operation autonomously. The planned increase in information extraction for a given downlink is 1000:1. The reduction in time to resume mission operations after mission interruption due to engineering anomaly, as well as engineering setup time for science observations, should be reduced to the time to select and load one of the pre-stored FPGA configurations on the ADAPT. Once commanded to a new configuration, the ADAPT should load it in well under 10 seconds.

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