# An SEU-Hard Flip-Flop for Antifuse FPGAs

R. Katz[1], J.J. Wang[2], J. McCollum[2], B. Cronquist[2],
R. Chan[2], D. Yu[2], and I. Kleyner[3]

[1]NASA Goddard Space Flight Center, Greenbelt, MD
[2]Actel Corporation, Sunnyvale, CA
[3]Orbital Sciences Corporation, Greenbelt, MD


# *Abstract*

An SEU-hardened flip-flop has been designed and developed for antifuse FPGA application. Design and application issues, testability, test methods, simulation and results are discussed.



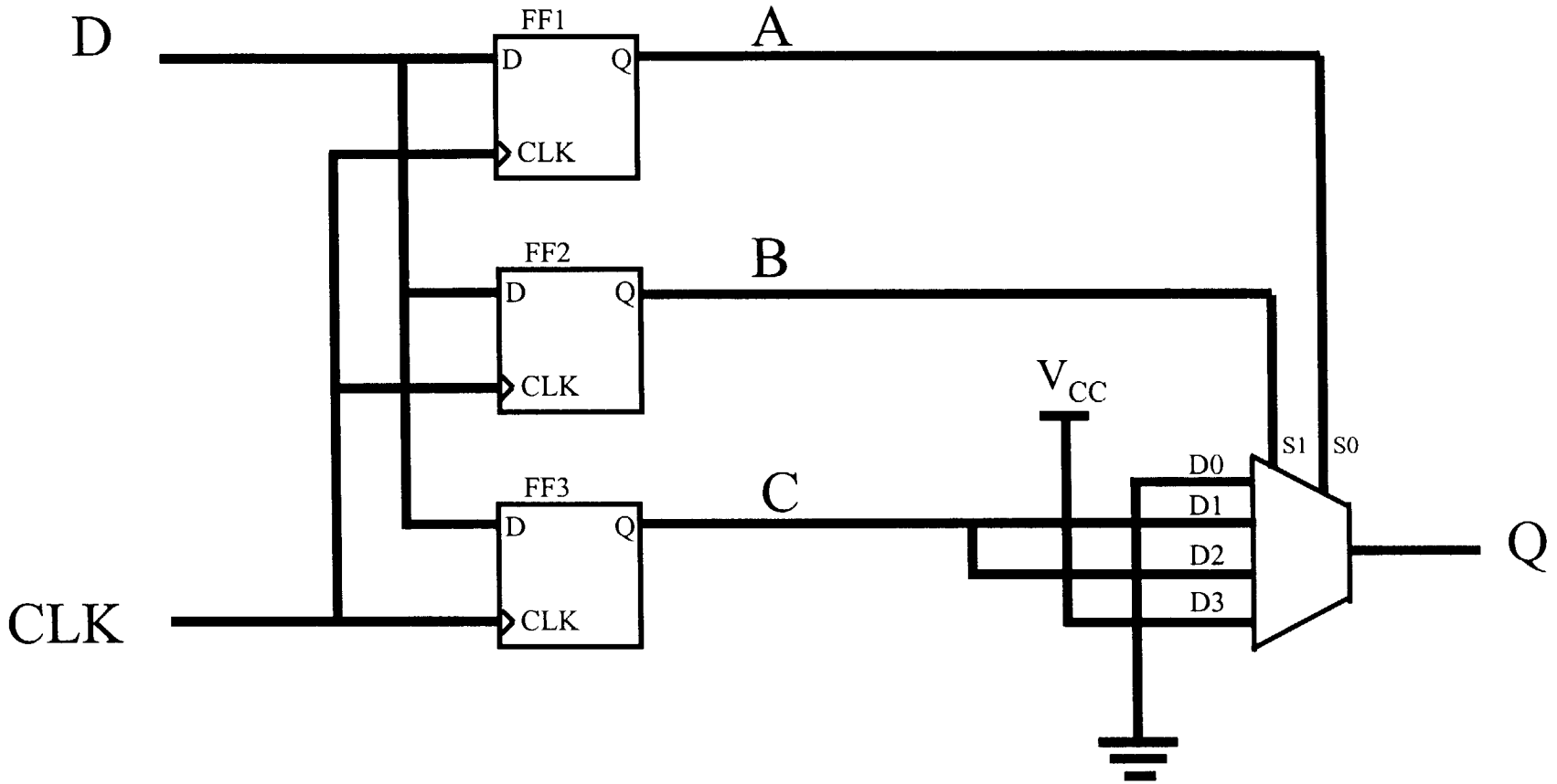


*Figure 1. SEU-hardening using available device resources.*

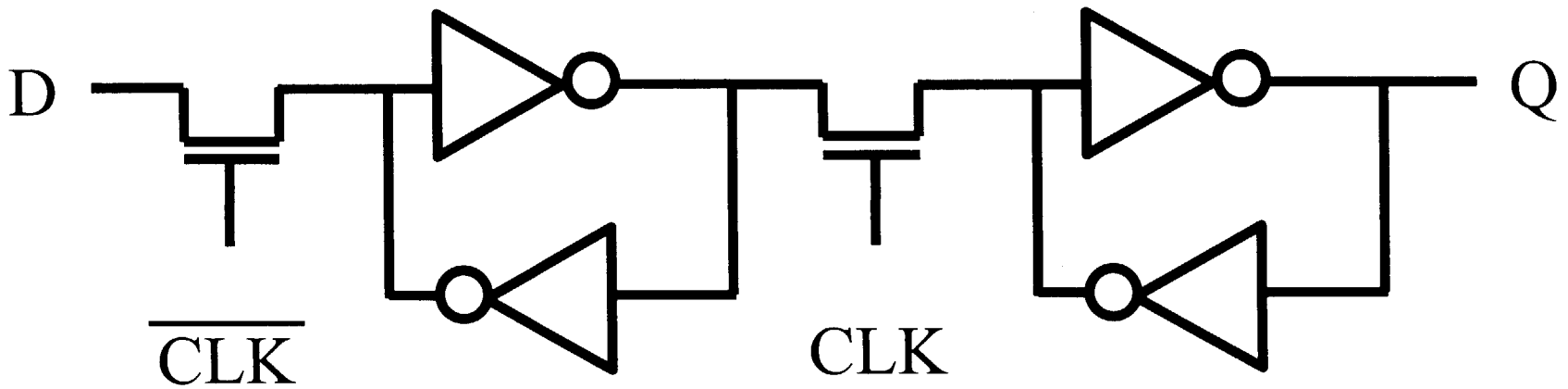


*Figure 2. Standard master-slave flip-flop.*

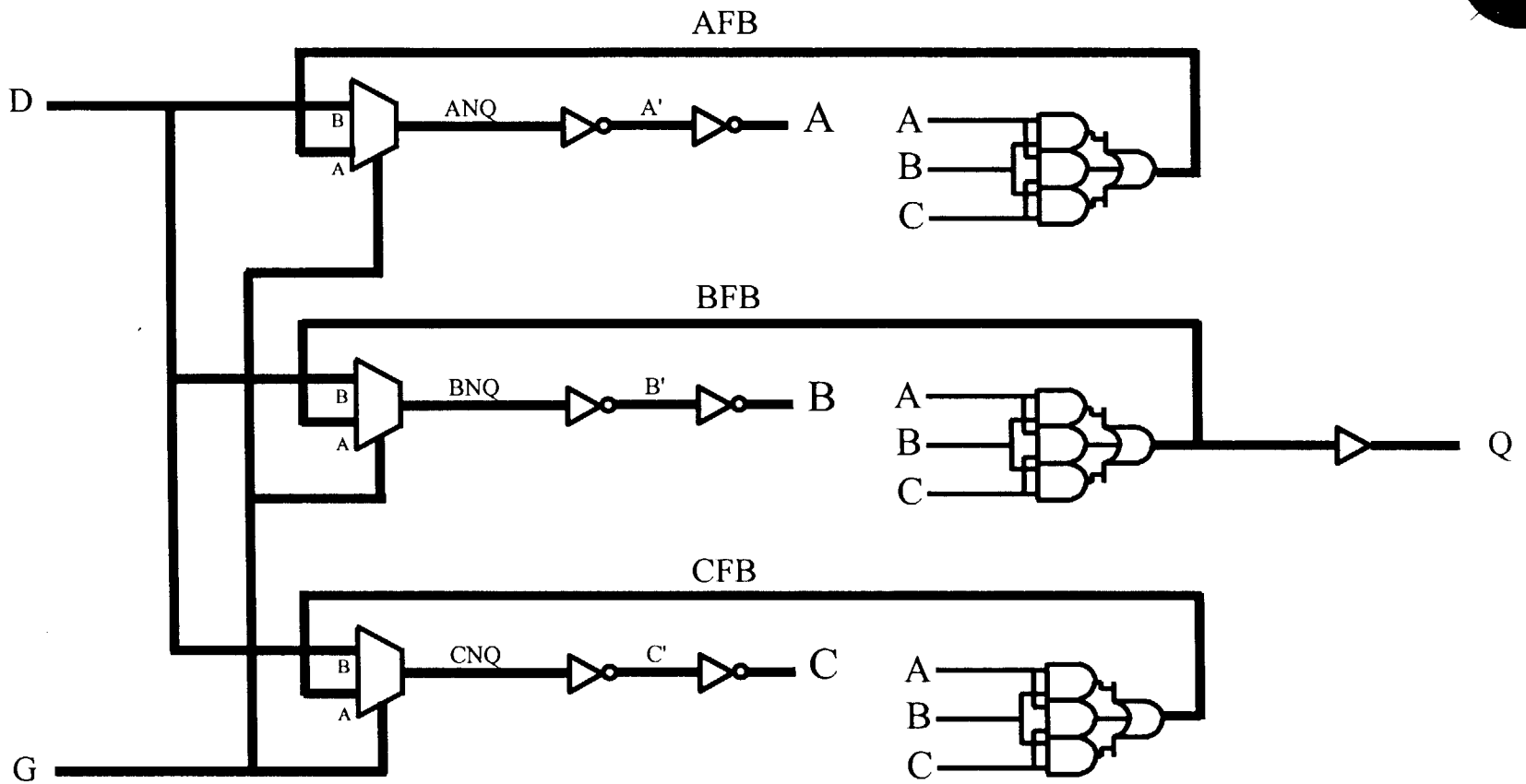


*Figure 3. K-Latch schematic, simplified. The asynchronous structure and interlocks eliminate the need for a free running clock to scrub SEUs.*

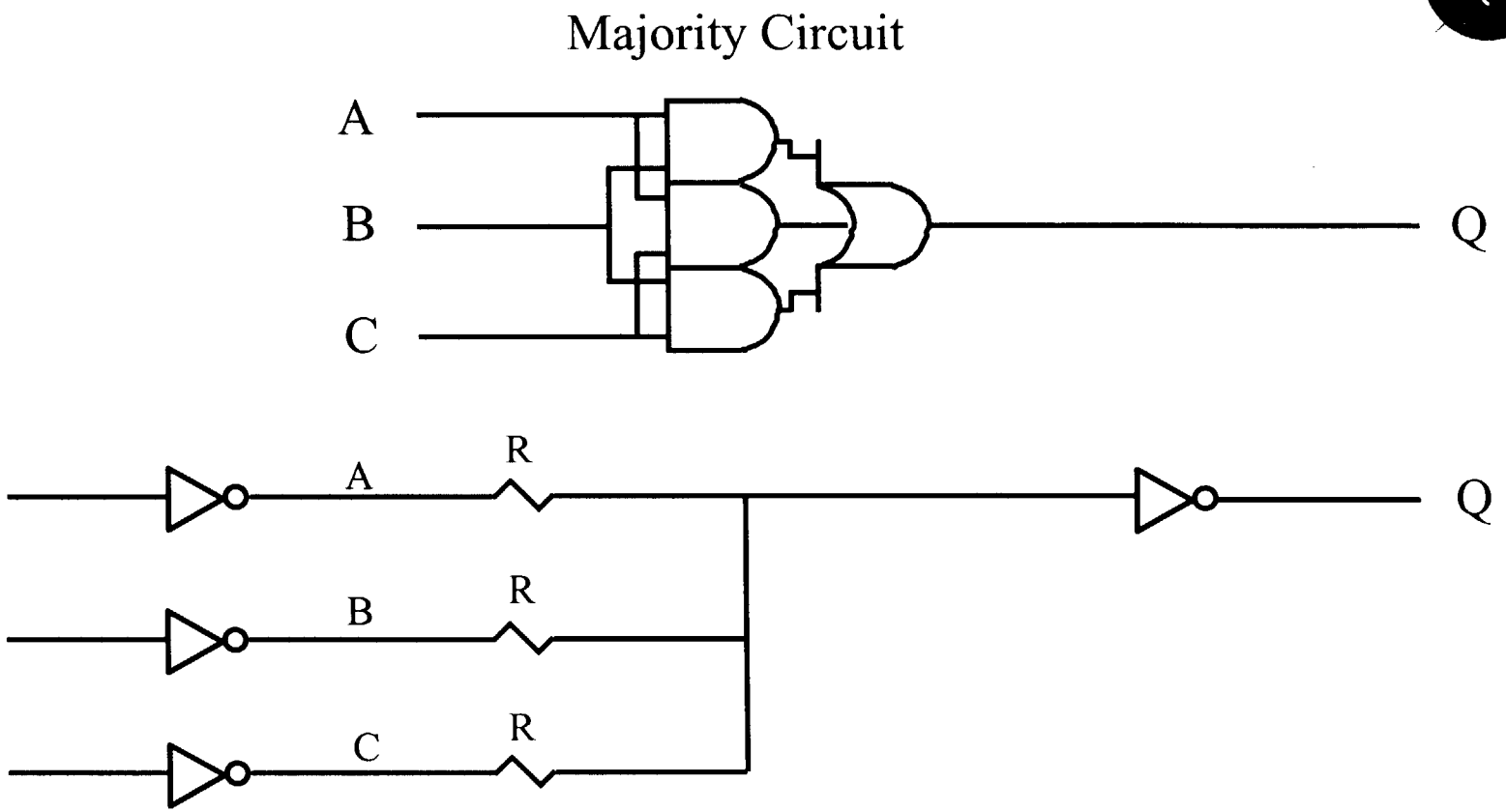


*Figure 4. Voter circuit implementations. The top approach uses a traditional majority circuit that is designed to be glitch-free. The lower half is an application of threshold logic principles.*

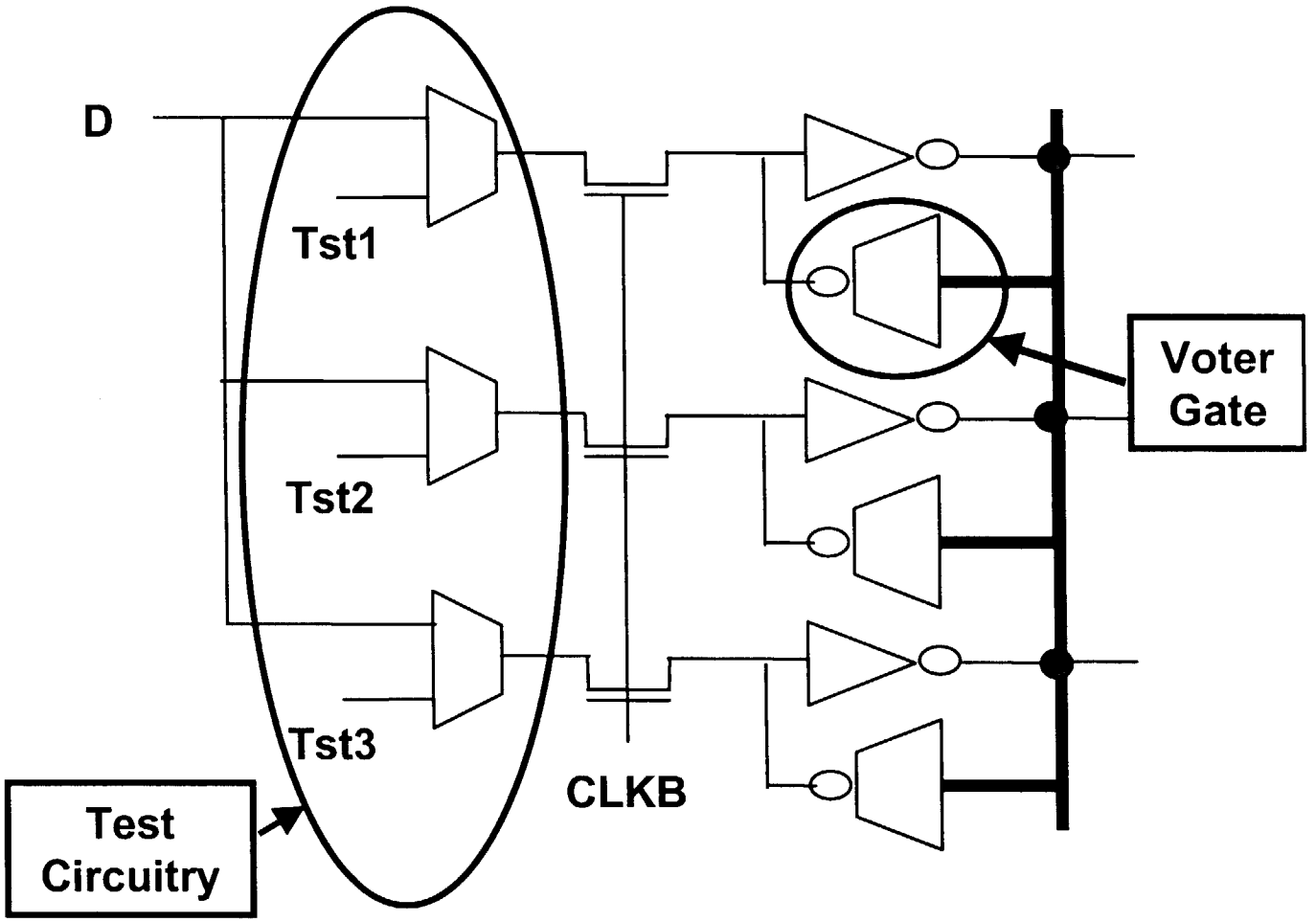


*Figure 5. Simplified test circuitry logic.*

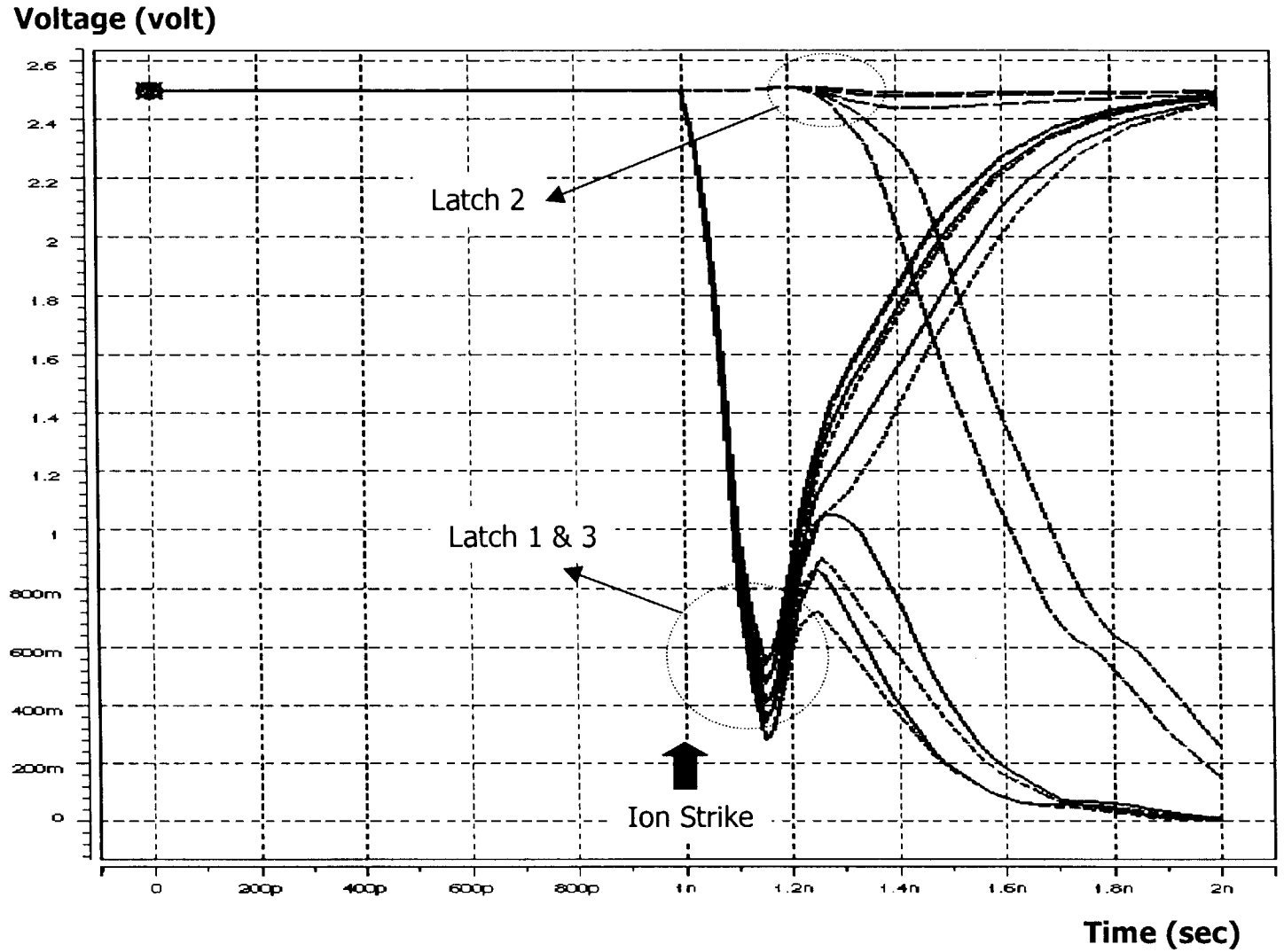


*Figure 6. SPICE simulation showing the voltage transient of the sensitive node in the sub-latches. A heavy ion strikes latch 1 and 3 right at the junctions simultaneously. The collected total charges was used as a parameter to generate a family of curves and to determine the critical charge, which is 0.15pC.*

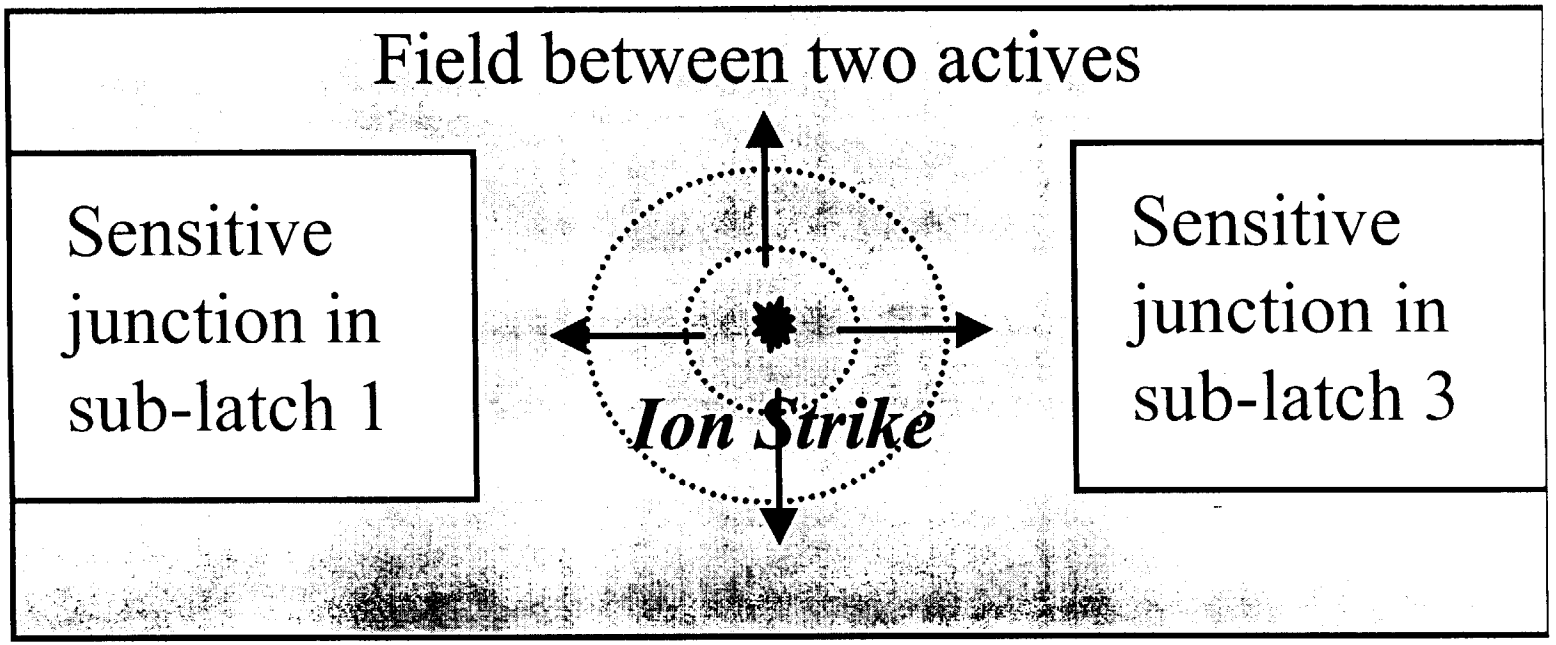


*Figure 7. Schematic of 3D mixed-mode simulation, showing a heavy ion strike at the center of the space between the sensitive junction in latch 1 and 3. The induced carriers reach to the junctions by lateral diffusion.*

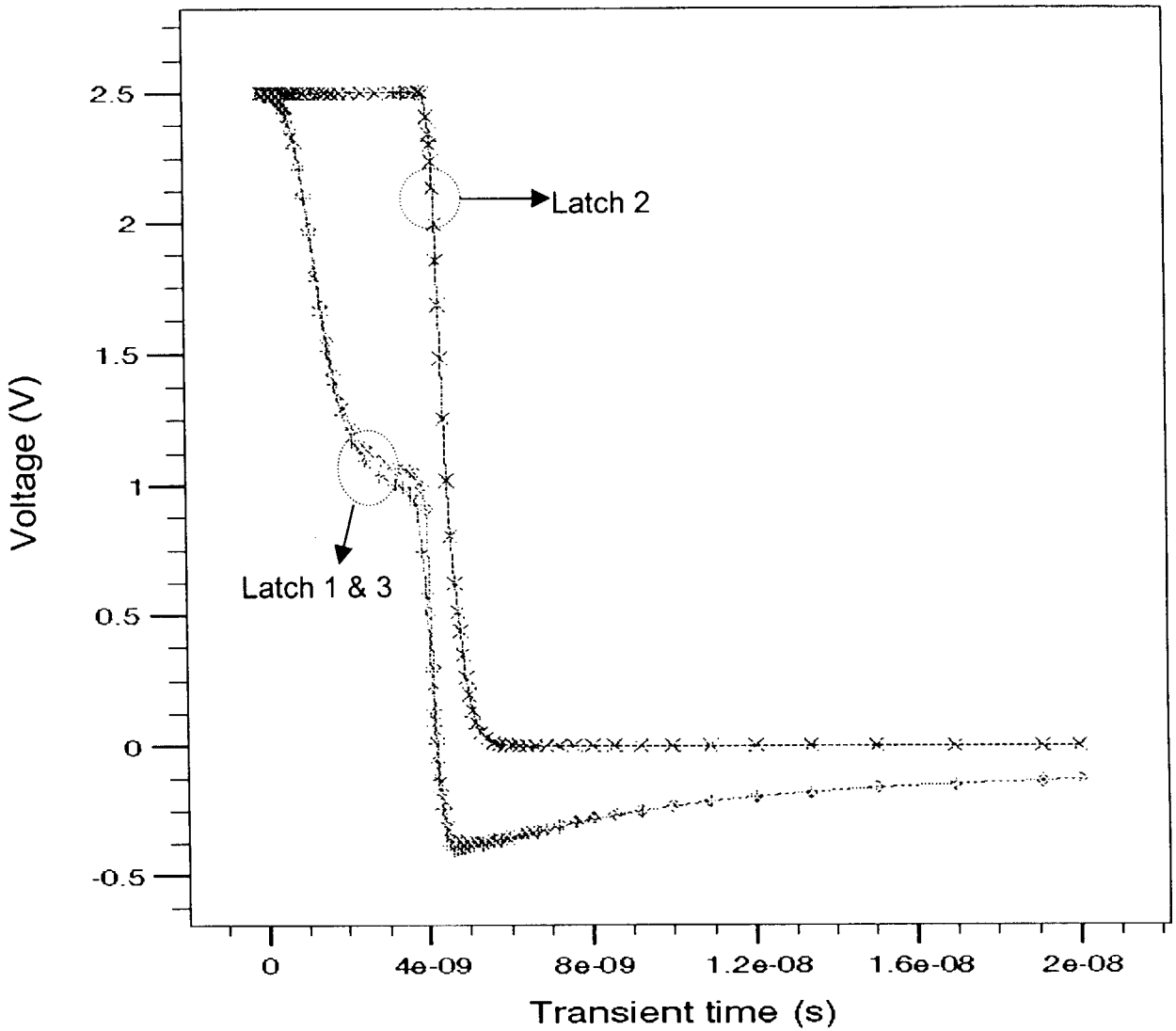


*Figure 8. Showing 3D mixed-mode simulation results. Voltage transient of the active node. A heavy ion with LET=129MeV-cm$^2$/mg stroke at the center of the space (see Figure 7) between the sensitive junctions of latch 1 and 3. When the voltages in both latch 1 and 3 reach the logic trip point, the triple redundant latch has an upset.*

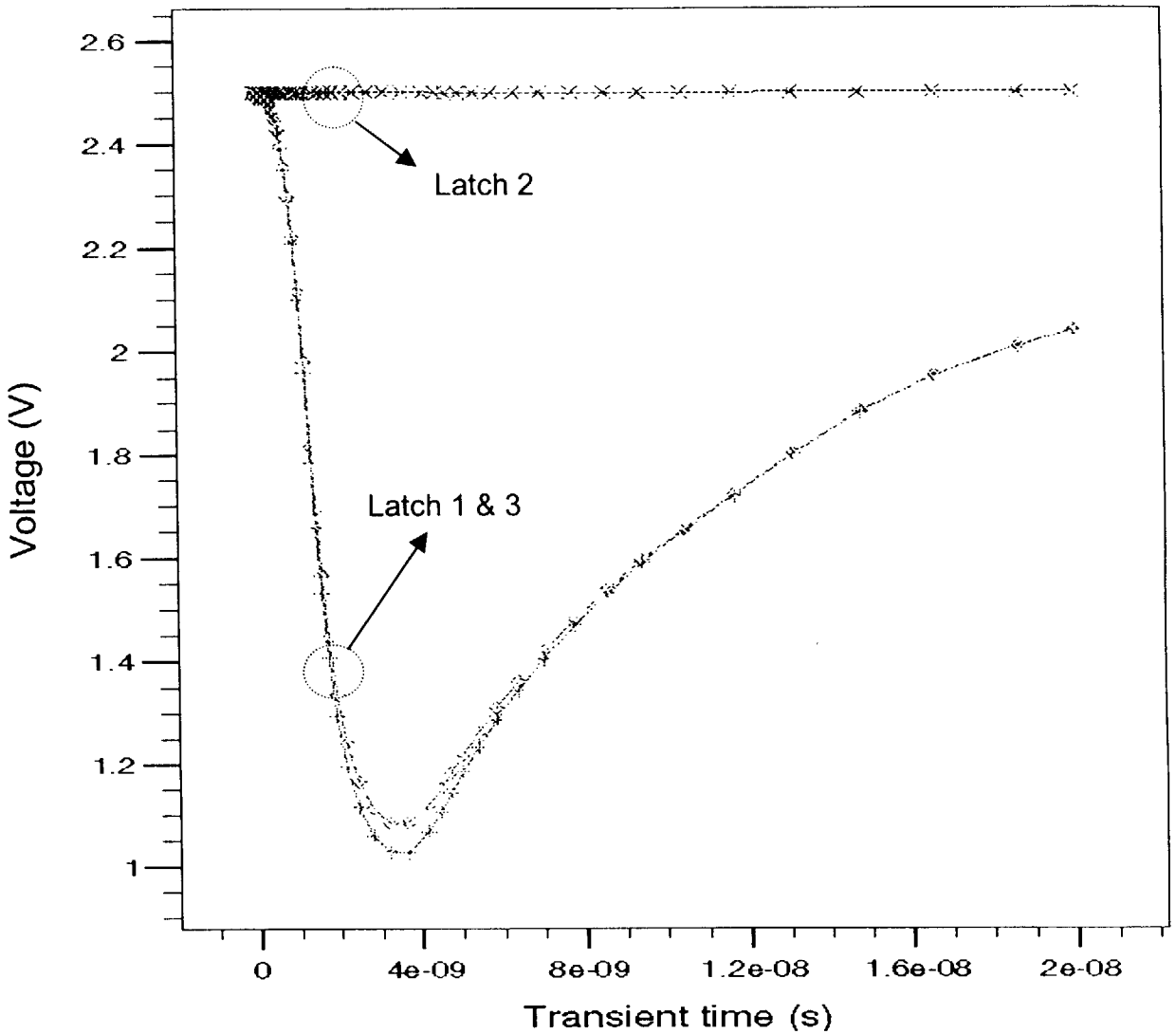


*Figure 9. Showing 3D mixed-mode results. Voltage transient of the active node. A heavy ion with LET=128MeV-cm$^2$/mg stroke at the center of the space (see Figure 7) between the sensitive junctions of latch 1 and 3. The voltages in both latch 1 and 3 recovered, the triple redundant latch has no upset.*

# Test Pattern Description
## Overview

The primary section of the TMRSX32 pattern consists of 4 shift registers, all clocked by a common clock pin. Each shift register design is different, to measure different aspects of the architecture. The length of each shift register is 100 stages, although more then one flip-flop is used for a stage in two of the designs, in addition to some extra logic.

# Test Pattern Description
## Clocking

The CLKBUF and HCLKBUF macros are used to drive the global clock and is available off-chip for external monitoring. No provisions are made to satisfy $t_H$ other than the normal place and route algorithms. That is, there are no buffers intentionally added between flip-flops to increase delays. There are some buffers added in some shift registers, for example, to measure SETs.

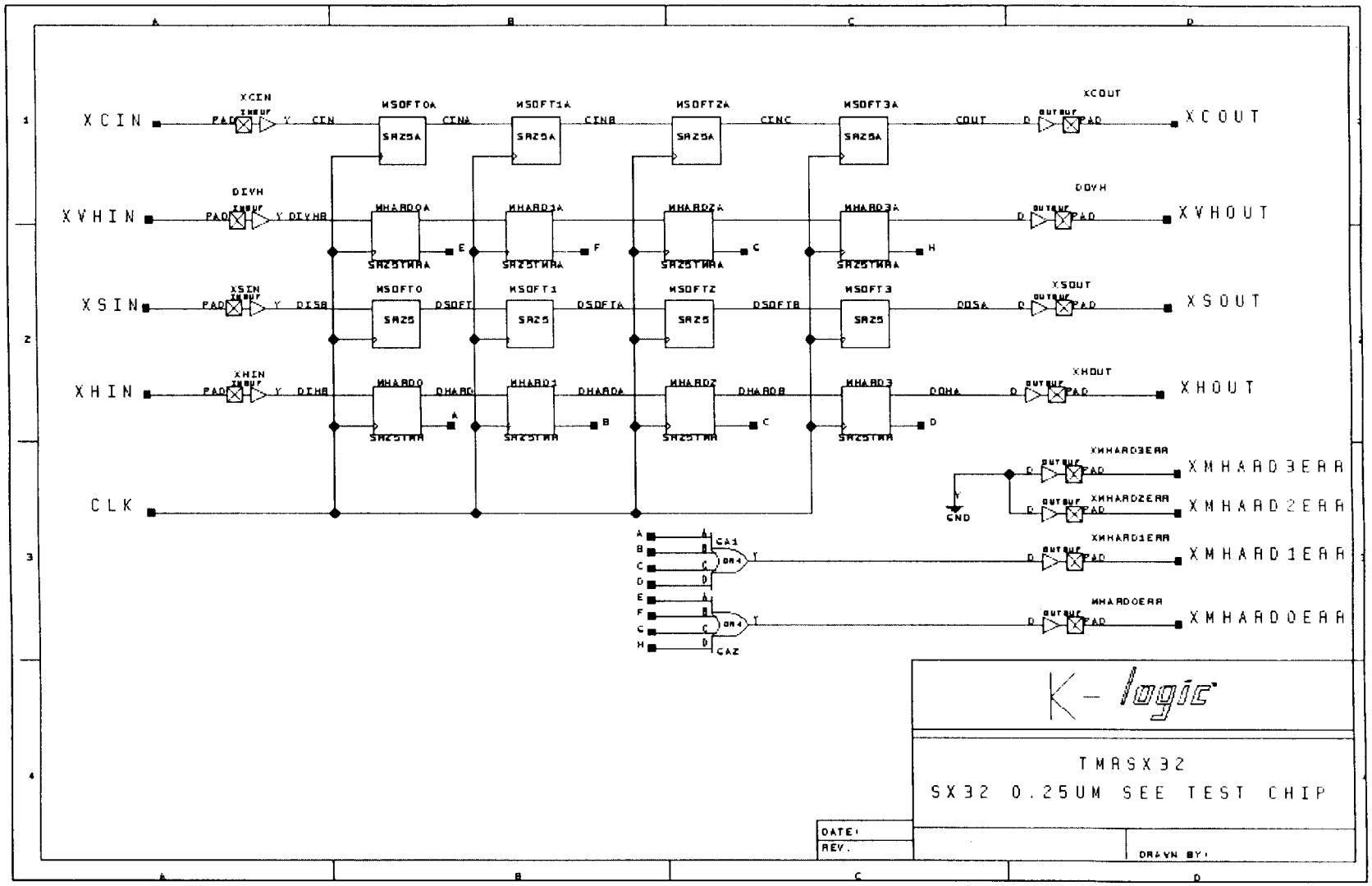


*Figure 10. Overview of the logic in the TMRSX32 SEE test chip.*

# Test Pattern Description
## MSOFT0A Shift Register

This 100-stage shift register is composed of DF1 R-Cell elements, each of which is separated by a BUFF. Each BUFF has a PRESERVE attribute attached to its output to ensure that the Combiner does not eliminate this "unnecessary" logic. Since the BUFF has a fanout of 1, it permits the fastest type of connection, a Direct Connect. The Direct Connect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns. The output of this shift register is DOC.

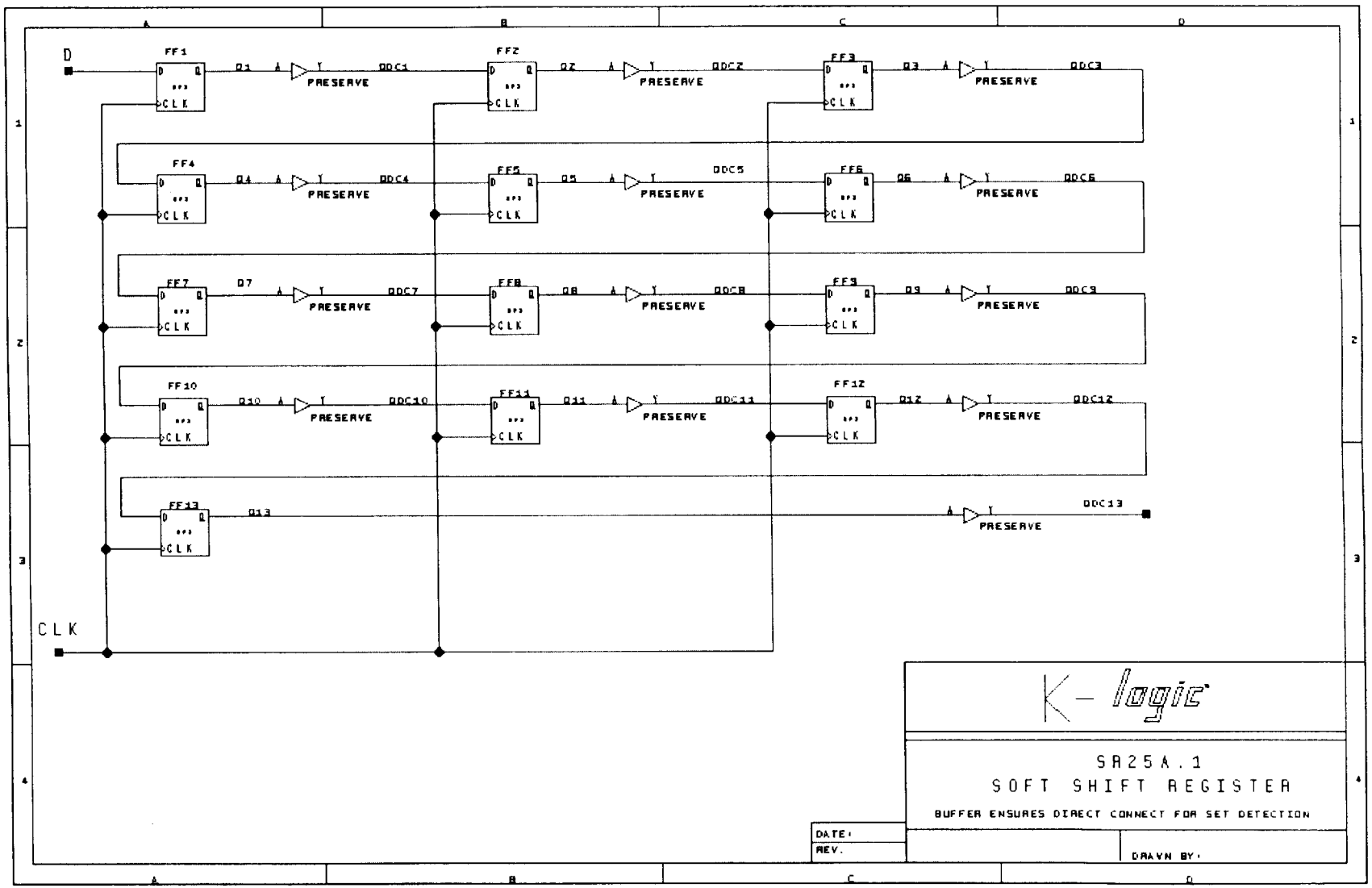


*Figure 11. Schematic of a portion of the MSOFT0A shift register. Buffers placed between flip-flops aid in the measurement of SET's.*

# Test Pattern Description
## MSOFT0 Shift Register

This shift register is identical to the MSOFT0A shift register described above except that there are no BUFFs separating the shift register elements. It is composed of 100 DF1 R-Cell elements.

The output of this shift register is DOS.

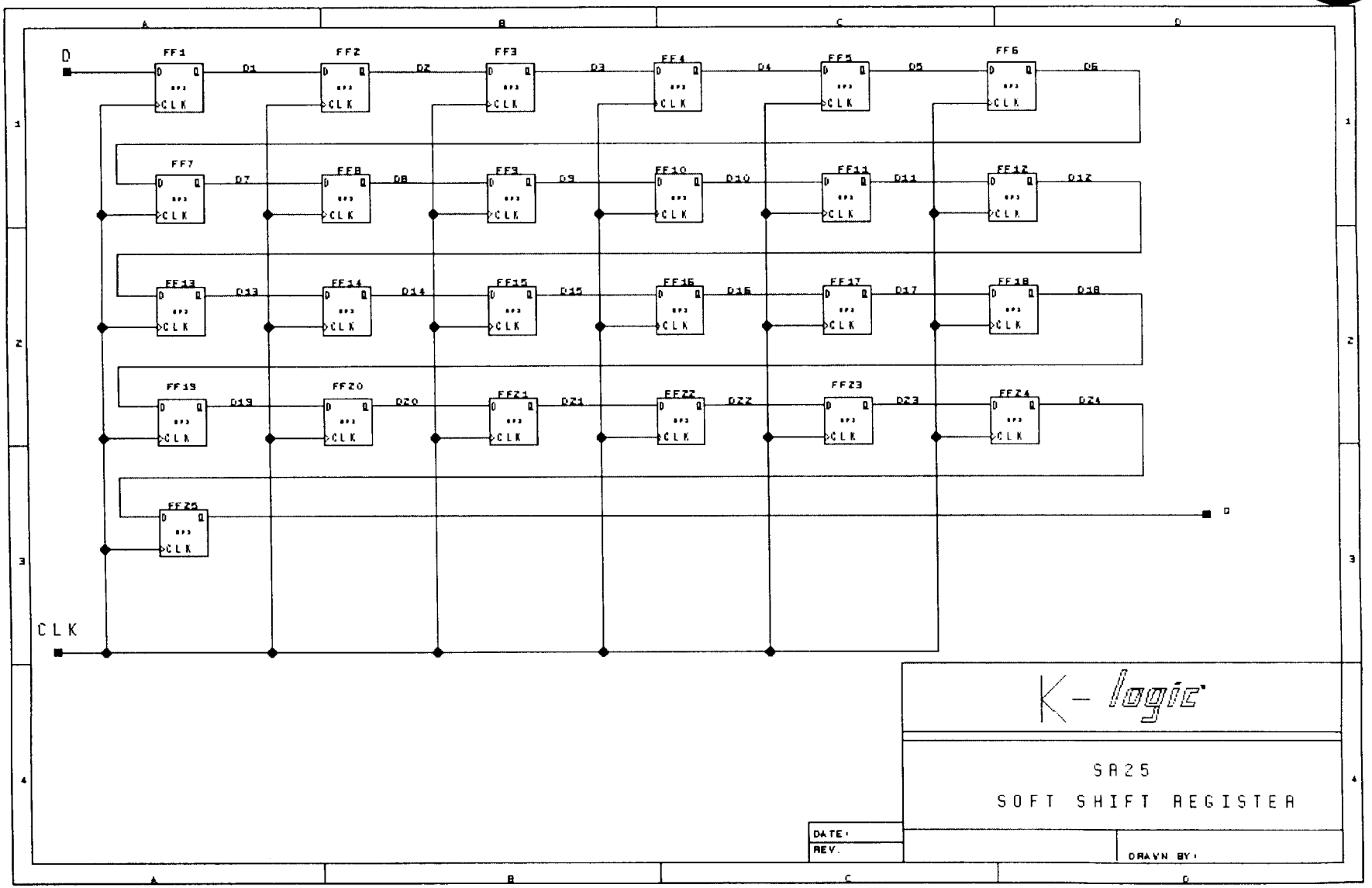


*Figure 12. Schematic of a portion of the MSOFT0 shift register. This circuit is used to measure the hardness of the K-Latch-based flip-flops, implemented in the S-Cell.*

# Test Pattern Description
## MHARD0 Shift Register

This 100-stage shift register is composed of TMR-hardened [at the user level] flip-flops. Each of these TMR-hardened elements consists of three DFPCB flip-flops and two MX4 muxes and an INV inverter. The first mux functions as a majority voting element. The second MX4 and the INV functions as a disagreement detector. The outputs of all disagreement detectors for this register are logically OR'd.

The output of the shift register is DOH. The output of the OR'd disagreement detectors is 1_ERR.

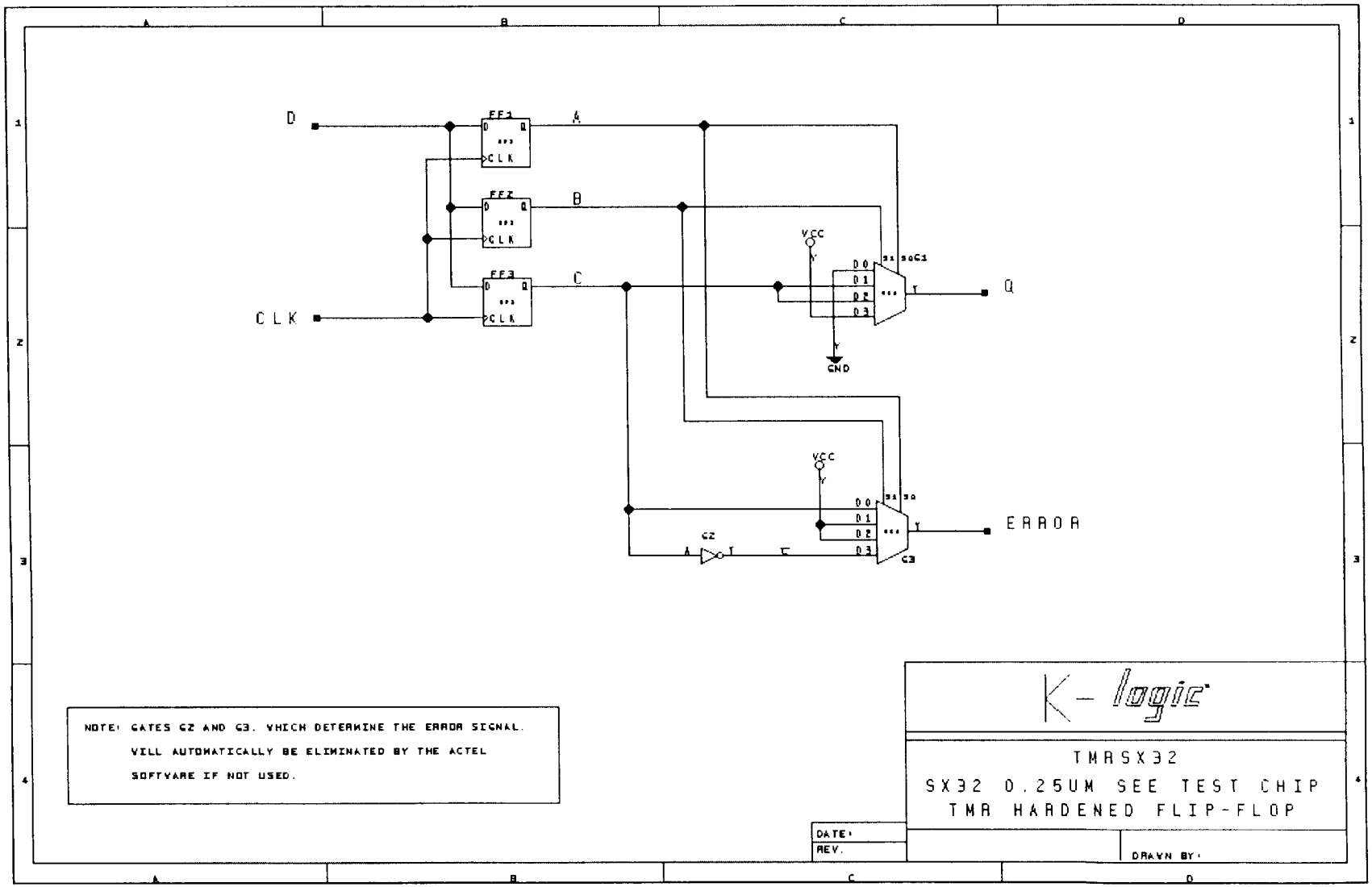


*Figure 13. Schematic of a stage in the MHARD0 shift register. Each stage is composed of a TMR-triplet, voter, and disagreement detector.*

# Test Pattern Description
## MHARD0A Shift Register

This 100-stage shift register is composed of TMR-hardened [at the user level] flip-flops modified to detect SETs. Each of these TMR-hardened elements consists of three DFPCB flip-flops and two MX4 muxes and an INV inverter. The first mux functions as a majority voting element. The second MX4 and the INV functions as a disagreement detector. The outputs of all disagreement detectors for this register are logically OR'd.

Each TMR-hardened triplet has been modified by the use of additional BUFF and INV elements. The INV's input is grounded and the output is connected to the CLR* inputs of each of the three DFPCB flip-flops. Similarly, the input of the BUFF is tied to $V_{CC}$ and its output is connected to the three PRE* inputs of the three flip-flops. Any hit on either the INV or the BUFF would be "caught" by the flip-flops. This may result in a combination of logic errors or activation of the disagreement detector, depending on how many of the flip-flops were effected by the SET.

The output of the shift register is DOVH. The output of the OR'd disagreement detectors is 0_ERR.

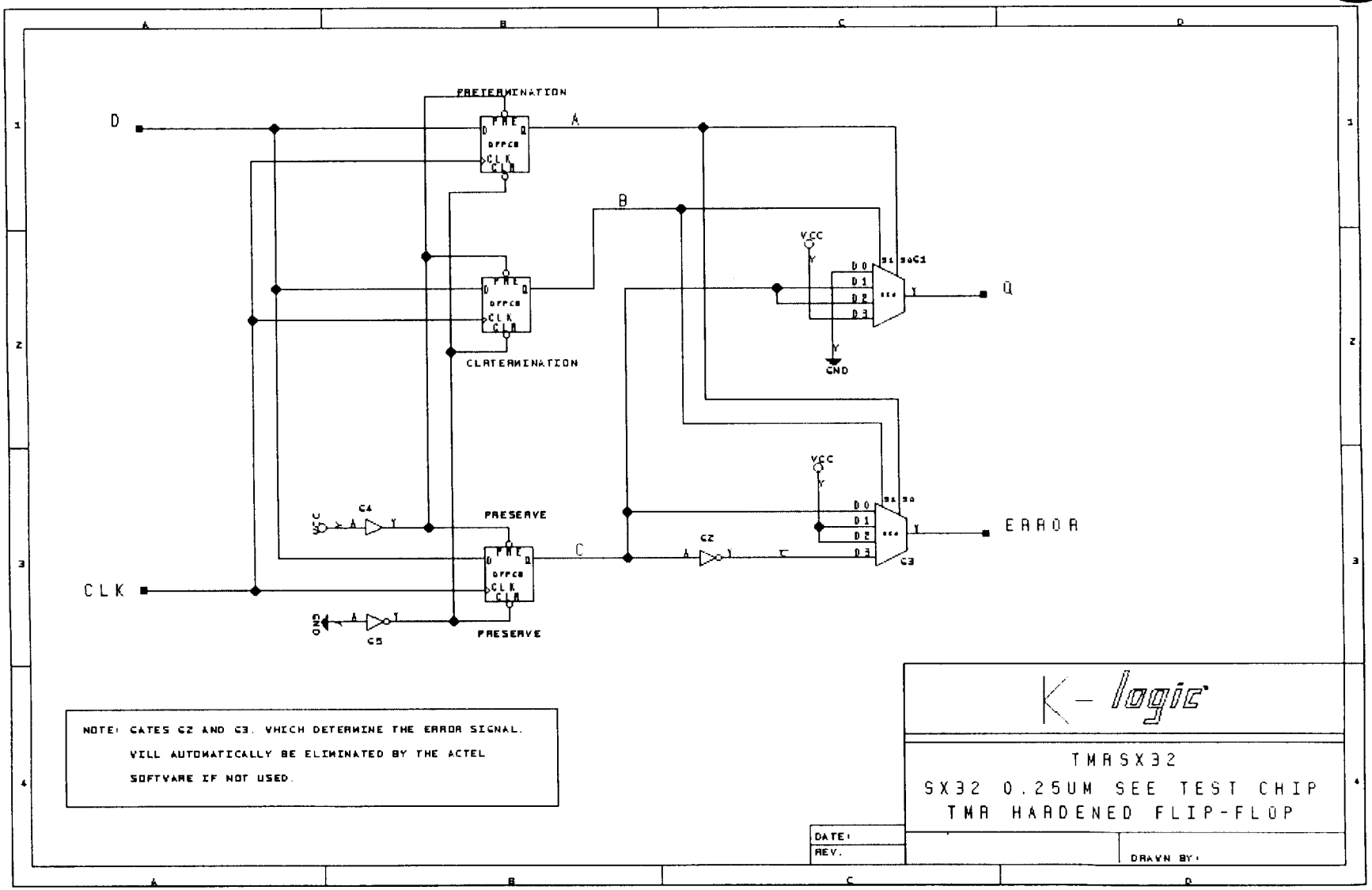


*Figure 14. Schematic of a stage in the MHARD0A shift register. The buffer and inverter driving PRE and CLR are used to detect SETs.*

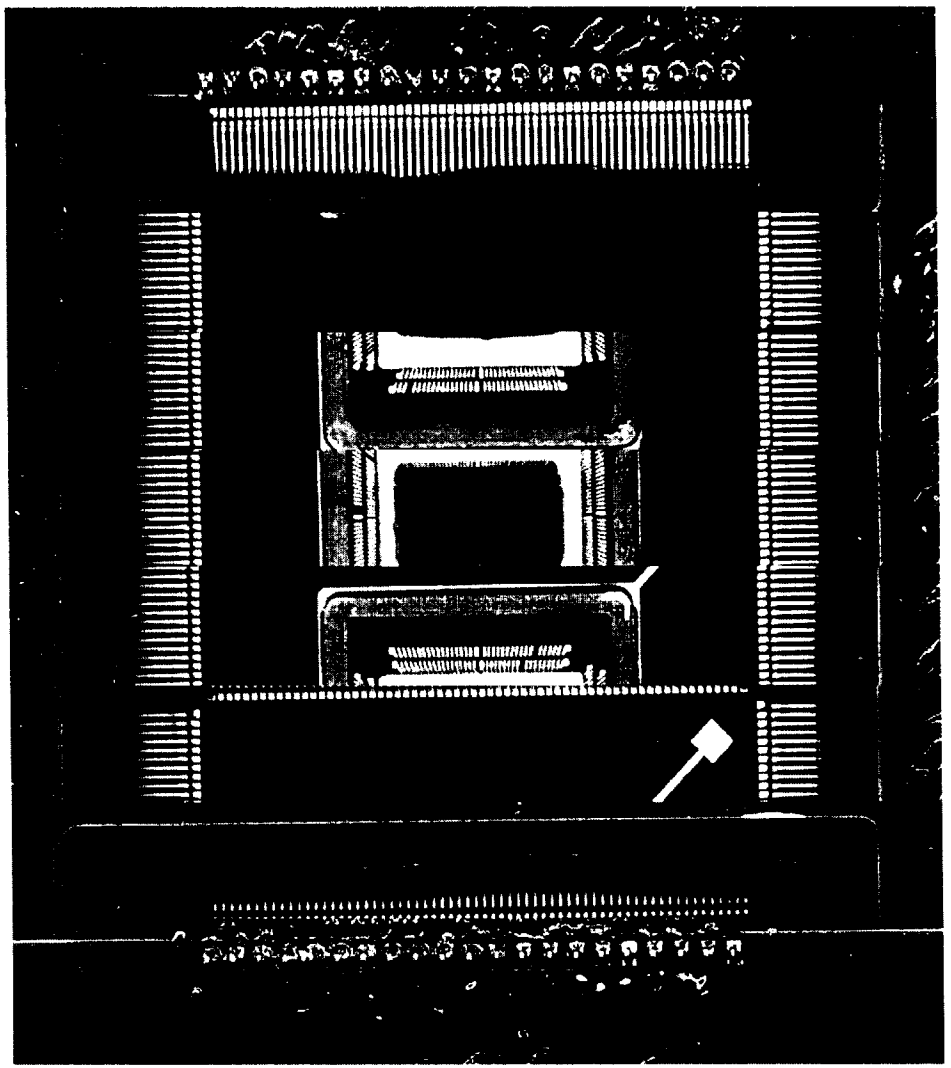

*Figure 15. DUT mounting. The use of a socket requires "reverse" mounting of the die, slightly limiting beam angles.*

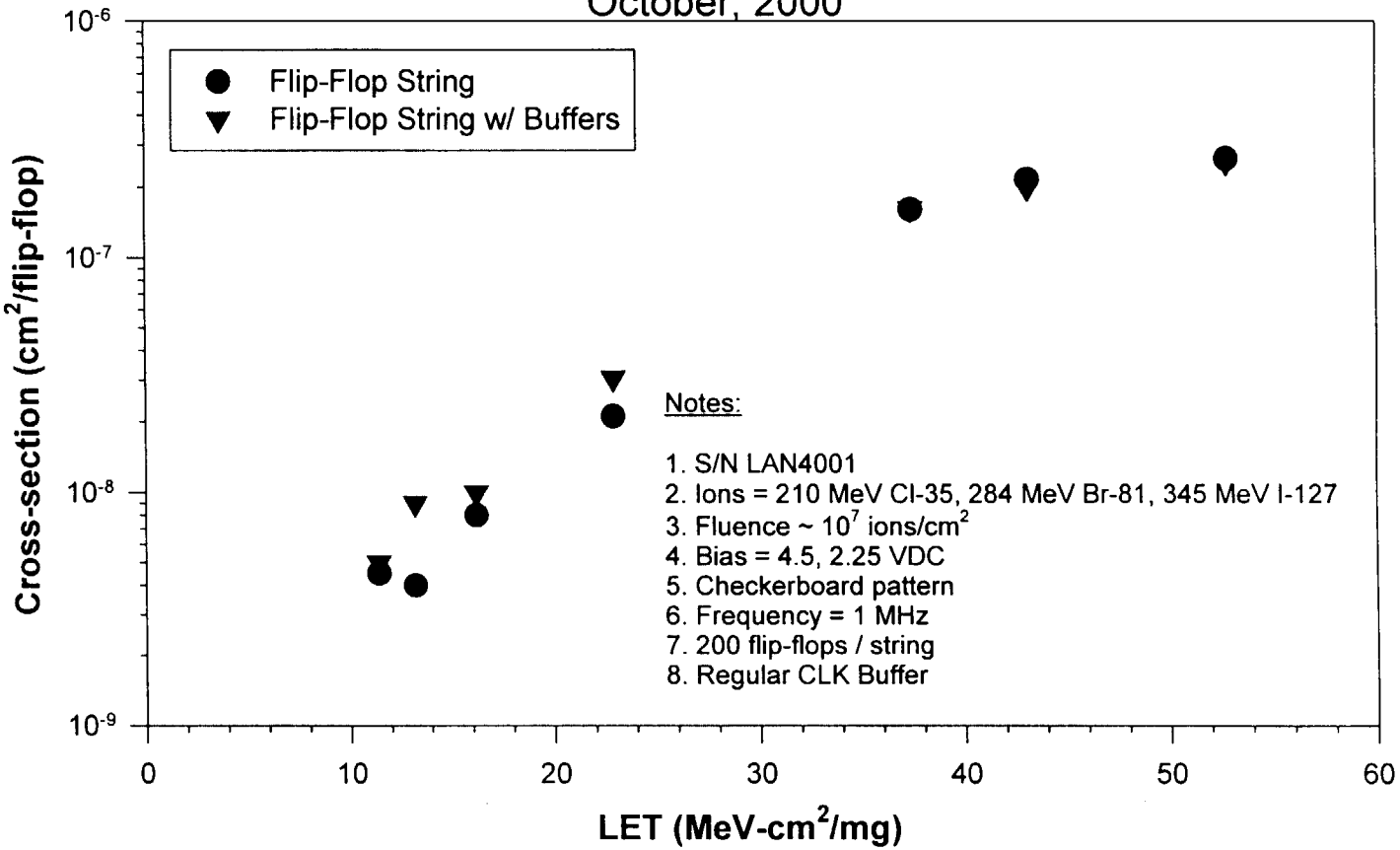


*Figure 16. Cross section-LET curve for a commercial A54SX32-A. Few SEUs were detected for the hardened device at an LET ≥ 60 MeV-cm²/mg.*

## Test Data for the RT54SX32-S Prototype

| UT S/N | Ion | LET MeV-cm²/mg | Tilt, Roll (degrees) | Supply Voltages | Time (sec) | Flux (p/cm²/s) | Fluence (p/cm²) | 1_Err | DOC | DOVH | DOS | DOH | 0_ERR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3421 | Cl | 22.9 | 60, 0 | 4.5,2.25 | 218 | $4.6x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3421 | Cl | 22.9 | 60, -90 | 4.5,2.25 | 217 | $4.6x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | | | | | |
| 3421 | Br | 37.4 | 0,0 | 4.5,2.25 | 202 | $2.0x10^4$ | $4.1x10^6$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3421 | Br | 37.4 | 0,0 | 4.5,2.25 | | | $1.0x10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3421 | Br | 65.1 | 55,0 | 4.5,2.25 | 233 | $2.4x10^4$ | $5.6x10^6$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3421 | Br | 65.1 | 55,0 | 4.5,2.25 | 116 | $1.9x10^4$ | $2.2x10^6$ | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | | | | | |
| 3421 | I | 59.9 | 0,0 | 4.5,2.25 | 123 | $9.4x10^4$ | $1.2x10^7$ | 0 | 1 | 0 | 0 | 0 | 0 |
| 3421 | I | 104.4 | 55,0 | 4.5,2.25 | 235 | $4.3x10^4$ | $10^7$ | 0 | 2 | 0 | 0 | 0 | 0 |
| 3421 | I | 104.4 | 55, -90 | 4.5,2.25 | 282 | $3.5x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3421 | I | 104.4 | 55, -45 | 4.5,2.25 | 381 | $2.6x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3421 | I | 69.1 | 30, -45 | 4.5,2.25 | 304 | $3.3x10^4$ | $10^7$ | 0 | 1 | 0 | 0 | 0 | 0 |
| 3421 | I | 59.9 | 0, 0 | 5.5, 2.75 | 309 | $3.2x10^4$ | $9.9x10^6$ | 0 | 1 | 0 | 0 | 0 | 0 |
| 3421 | I | 59.9 | 0, 0 | 5.5, 3.0 | 392 | $2.6x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3421 | I | 104.4 | 55, 0 | 5.5, 3.0 | 775 | $1.3x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | | | | | | | |
| 3422 | I | 59.9 | 0,0 | 4.5, 2.25 | | | $\sim 0.75x10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3422 | I | 59.9 | 0,0 | 4.5,2.25 | 137 | $8.4x10^4$ | $1.1x10^7$ | 0 | 2 | 1 | 2 | 0 | 0 |
| 3422 | I | 104.4 | 55,0 | 4.5,2.25 | 247 | $4.1x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3422 | I | 104.4 | 55, -89 | 4.5,2.25 | 289 | $3.5x10^4$ | $10^7$ | 0 | 0 | 0 | 1 | 0 | 0 |
| 3422 | I | 104.4 | 55, -45 | 4.5,2.25 | 339 | $3.0x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3422 | I | 69.1 | 30, -45 | 4.5,2.25 | 314 | $3.2x10^4$ | $10^7$ | 0 | 0 | 1 | 0 | 0 | 0 |
| 3422 | I | 59.9 | 0, -60 | 5.5, 3.0 | 302 | $3.3x10^4$ | $9.9x10^6$ | 0 | 0 | 0 | 0 | 0 | 0 |
| 3422 | I | 104.4 | 55,-89 | 5.5, 3.0 | 608 | $1.6x10^4$ | $10^7$ | 0 | 0 | 0 | 0 | 0 | 0 |

# Conclusion

It is both feasible and practical to design and produce an SEU-hardened antifuse-based FPGA on a 0.25 µm commercial process. As a result, this logic can be used reliably in the radiation environment at costs far less then devices produced on a radiation-hardened process. Additionally, single event transients in this high-speed, small feature sized process do not appear to be significant. The overhead of the redundant elements and the correction circuitry has at most only a small impact on system performance.