

Novel Vertical Interconnects With 180 Degree Phase Shift for Amplifiers, Filters, and Integrated Antennas

Kavita Goverdhanam
Bell Laboratories, Murray Hill, New Jersey

Rainee N. Simons
QSS Group, Inc., Cleveland, Ohio

Linda P.B. Katehi
University of Michigan, Ann Arbor, Michigan

Prepared for the
2001 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems
cosponsored by the IEEE MTT-S, ARO, NASA GRC, and NSF
Ann Arbor, Michigan, September 12-14, 2001

Prepared under Contract NAS3-00145

National Aeronautics and
Space Administration

Glenn Research Center

Acknowledgments

The authors are grateful to ONR (N00014-95-1-0546) for their support.

This report contains preliminary findings, subject to revision as analysis proceeds.

Trade names or manufacturers' names are used in this report for identification only. This usage does not constitute an official endorsement, either expressed or implied, by the National Aeronautics and Space Administration.

Available from

NASA Center for Aerospace Information
7121 Standard Drive
Hanover, MD 21076

National Technical Information Service
5285 Port Royal Road
Springfield, VA 22100

Available electronically at <http://gltrs.grc.nasa.gov/GLTRS>

NOVEL VERTICAL INTERCONNECTS WITH 180 DEGREE PHASE SHIFT FOR AMPLIFIERS, FILTERS, AND INTEGRATED ANTENNAS

Kavita Goverdhanam,¹ Raine N. Simons,² and Linda P.B. Katehi³

Abstract – In this paper, novel low loss, wide bandwidth, compact coplanar stripline/coplanar waveguide vertical interconnects with 180° phase shift and vertically interconnected baluns for RF/microwave integrated circuits are demonstrated. The interconnects and baluns are fabricated on high resistivity silicon wafer with a thin layer of spin-on-glass as an insulator between the buried and the elevated strip conductors which are interconnected by microvias. The measured and simulated characteristics of these interconnects are presented and they show that very compact, low loss and wide bandwidth circuits are feasible with this technology. This technology has the potential to significantly enhance the performance of amplifiers, filters, and integrated antennas in Si/SiGe based RF/microwave ICs.

I. INTRODUCTION

Silicon/silicon germanium (Si/SiGe) based RF/ microwave integrated circuits (ICs) [1] for wireless communications/sensors require linear amplifiers for low distortion and filters for interference suppression. In some situations they may also require an integrated planar antenna for transmission/reception, in applications such as automobile collision avoidance. The amplifiers may require a balun to realize a push-pull circuit to suppress the second-order intermodulation products and thus enhance the spurious free dynamic range. The filters may require a phase inverter for impedance transformation. The antenna such as, log-periodic dipole array may require a fixed 180° phase shift for generating an endfire beam.

In this paper, we present several new integrated circuit design concepts for: (a) wide bandwidth vertical interconnects with 180° phase shift and (b) vertically interconnected baluns. These interconnects and baluns are fabricated on a high resistivity (HR) silicon wafer. The vertical interconnects discussed here constitute a small section of coplanar stripline (CPS) and coplanar waveguide (CPW) at two levels separated by a thin layer of spin-on-glass (SOG). The interconnections between the two levels are realized by metallized vias. The CPS and CPW have the advantages of eliminating backside processing due to uniplanar construction, thus simplifying vertical integration by the use of metallized vias. In addition, CPS and CPW allow easy integration of other transmission media, such as, slotline, and micro-CPS [2] for greater design flexibility. The SOG has the advantage of low dielectric constant [3] and hence low parasitic coupling capacitance. In addition,

the SOG planarizes the circuit and this facilitates vertical integration [4]. The HR silicon wafer ($\rho > 3000 \Omega \text{ cm}$) has the advantage of lowering the signal attenuation in addition to improving the isolation between adjacent circuits.

In the following sections, first, the fabrication process is briefly explained. This is followed by a discussion of the design considerations, measured insertion loss and return loss of the CPS vertical interconnects with 180° phase shift. The interconnects considered are: (a) CPS vertical interconnect with 180° phase shift, (b) CPW vertically interconnected by CPS overpass and with 180° phase shift, (c) CPW vertical interconnect with 180° phase shift and (d) CPS-to-elevated CPW balun. The numerical simulations of the circuits are carried out using the CST microwave studio™. In the simulations, the CPS and CPW conductors are assumed to be perfectly conducting. In addition, the silicon substrate as well as the SOG layer are considered as perfect dielectrics.

II. INTERCONNECT FABRICATION

As a first step in fabricating the aforementioned interconnects, the buried strip conductors are fabricated on the HR silicon wafer. The strip conductors are fabricated using a lift-off process. The thickness of the titanium/gold metal is about 0.8 μm . Next, a thin insulating spacer layer to support the elevated strip conductors is built-up to the required thickness using multiple spin-coats of Accuglass® 512. The thickness h_1 of the SOG used here is about 2.0 μm . Following this, the vias for the vertical interconnect are patterned using photoresist and dry etched in a fluorocarbon-based plasma. Finally, the elevated strip conductors are fabricated with titanium/gold by a second lift-off process. During this step the via holes are metallized to ensure electrical continuity between the buried and the elevated strip conductors. The thickness of the elevated strip conductor is about 2.0 μm . The cross-sections of the CPS and CPW with a SOG overlay are shown in Fig. 1.

III. DESIGN, RESULTS AND DISCUSSIONS

The design considerations for the via hole and probe pads required for each of the aforementioned interconnects are as follows: each via has a diameter d which is about 0.75 times the strip width S and is symmetrically located on the strip conductor. The probe pads in the case of CPS circuits for on-wafer characterization using signal-ground RF probes are about 100×100 μm in size. In the case of CPW circuits,

¹Bell Laboratories, Lucent Technologies, Murray Hill, New Jersey 07974

²NASA Glenn Research Center, QSS, Inc., Cleveland, Ohio 44135

³University of Michigan, Radiation Laboratory, EECS Department, Ann Arbor, Michigan 48109-2122

™Registered Trademark of CST of America, Inc., Wellesley, MA.

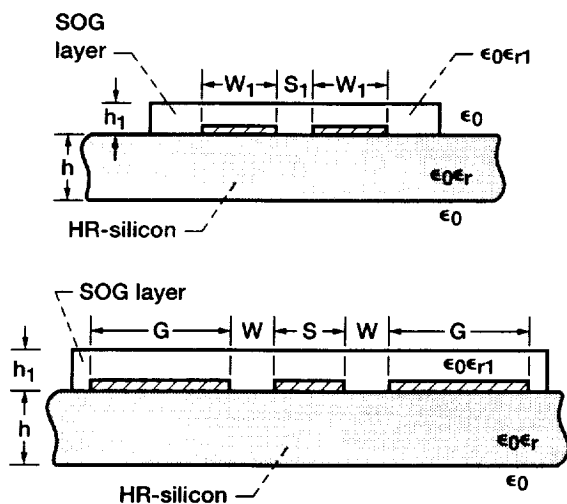


Figure 1.—Coplanar stripline (CPS) and Coplanar waveguide (CPW) on a HR-silicon wafer with a SOG overlay, $h = 400 \mu\text{m}$, $\epsilon_r = 11.7$, $h_1 = 2 \mu\text{m}$, $\epsilon_{r1} = 3.1$.

the center strip conductor as well as the ground planes are extended to form the probe pads. These CPW interconnects are characterized using ground-signal-ground RF probes. The length of the CPS and the CPW between the input/output ports of the circuit and the probe pads is $700 \mu\text{m}$ for all the circuits investigated here. The losses associated these connecting lines and the probe pads are de-embedded using on-wafer CPS and CPW Thru-Reflect-Line (TRL) calibration standards. The coplanar stripline and coplanar waveguide circuits investigated here are uniplanar in construction and hence do not have a ground plane on the opposite side of the wafer. Therefore, the wafer is supported on a Styrofoam™ block, instead of the regular metal vacuum chuck, in the RF probe station while measuring the S-parameters.

A. CPS vertical interconnect with 180° phase shift:

A schematic and microphotograph of the circuit are shown in Figs. 2(a) and 2(b), respectively. In this circuit, the strip conductors are transposed to provide the 180° phase shift. This type of inter-connect is ideally suited for adding a 180° phase shift to the terminals of each element in a log-periodic array as explained in [5]. The characteristic impedance $Z_{0(\text{CPS})}$ is 50Ω .

The measured (de-embedded) and simulated insertion loss (S_{21}) and return loss (S_{11}) are better than -0.5 dB and -20.0 dB respectively over the frequency range of 3 to 18 GHz (Fig. 3). The numerical simulations of this circuit show that the insertion loss is negligibly small and the return loss is better than -18.0 dB across the 3 to 18 GHz frequency range. The measured phase difference between the CPS vertical interconnect with 180° phase shift and a CPS through line of equivalent length is shown in Fig. 4.

The phase difference is 180° at the center frequency of 10.5 GHz and deviates from 180° by 8° at the two band edges which are at 3 and 18 GHz respectively. The phase is

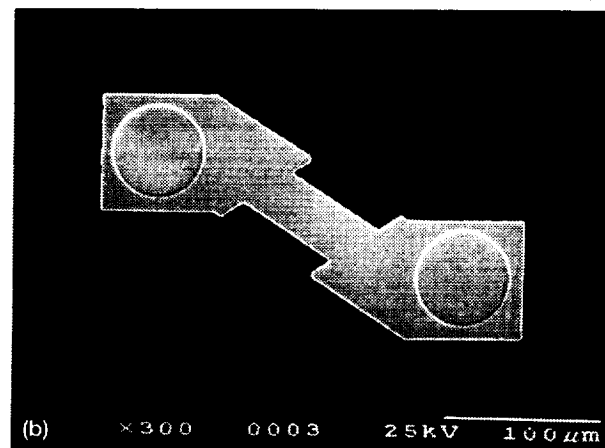
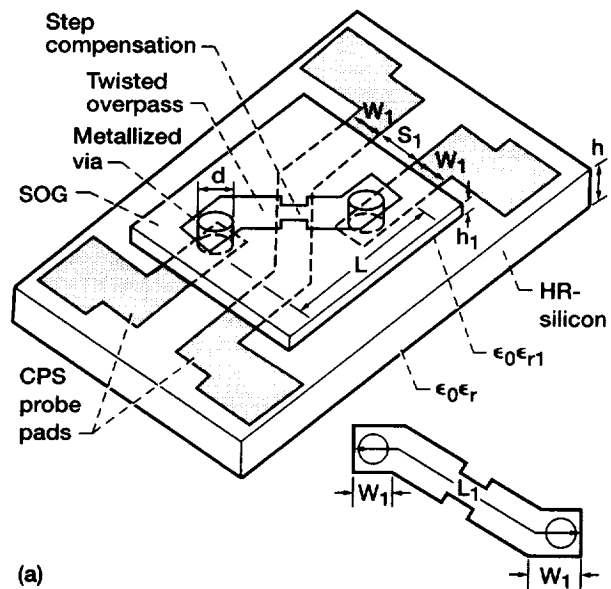


Figure 2.—(a) CPS vertical interconnect with 180° phase shift $W_1 = 65 \mu\text{m}$, $S_1 = 5 \mu\text{m}$, $d = 40 \mu\text{m}$, $L = 265 \mu\text{m}$, $L_1 = 282.1 \mu\text{m}$. (b) Microphotograph of CPS vertical interconnect with 180° phase shift.

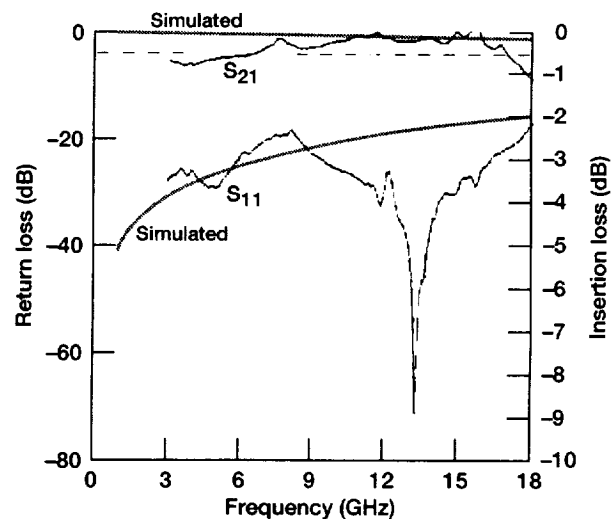


Figure 3.—Measured (De-embedded) and simulated insertion loss (S_{21}) and return loss (S_{11}) of CPS vertical interconnect with 180° phase shift.

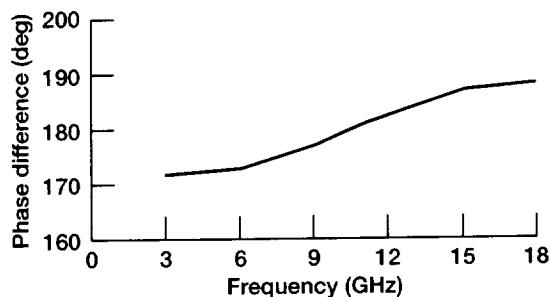


Figure 4.—Measured phase difference between an equivalent CPS through line and the CPS vertical interconnect with 180° phase shift.

within $\pm 3^\circ$ from 180° over 3 GHz band centered at 10.5 GHz which results in a bandwidth of 28.5 percent.

B. CPW vertically interconnected by CPS overpass with 180° phase shift:

A schematic and microphotograph of the circuit are shown in Figs. 5(a) and 5(b), respectively. The characteristic impedance $Z_{0(CPS)}$ and $Z_{0(CPW)}$ are 50Ω . The measured (de-embedded) and simulated insertion loss (S_{21}) and the return loss (S_{11}) are shown in Fig. 6. The insertion loss and the return loss are better than -1.0 dB and -17.5 dB respectively up to 6.0 GHz which includes the ISM bands. The maximum insertion loss of the circuit is -1.75 dB. The measured return loss is better than -13 dB across the entire frequency range of 3 to 18.0 GHz. The discrepancies in the measured and modeled S-parameters are attributed to the simplifications in the simulated geometry. Specifically, the compensating notches in the elevated lines were not included.

C. CPW vertical interconnect with 180° phase shift:

A schematic and microphotograph of the circuit are shown in Figs. 7(a) and 7(b), respectively. The line has a characteristic impedance $Z_{0(CPW)} = 50 \Omega$. The measured (de-embedded) and simulated insertion loss (S_{21}) and the return loss (S_{11}) are better than -1.0 dB and -15.5 dB respectively up to 6.5 GHz. The measured return loss is better than -11 dB across the entire frequency range of 3 to 18.0 GHz. These characteristics are shown in Fig. 8. As in case B, the discrepancies between measured and simulated S-parameters are attributed to the absence of compensating notches in the simulations.

D. CPS-to-elevated CPW balun with vertical interconnects:

In this circuit shown in Fig. 9, the CPS and the elevated CPW are fabricated on the HR silicon wafer and on the SOG layer respectively. One of the strip conductors of the CPS is extended below the SOG layer to form the buried center strip conductor of the CPW, while the other CPS strip conductor is terminated in a via. This via provides a vertical interconnection to the elevated finite width ground planes of the CPW. The elevation or the height provides an

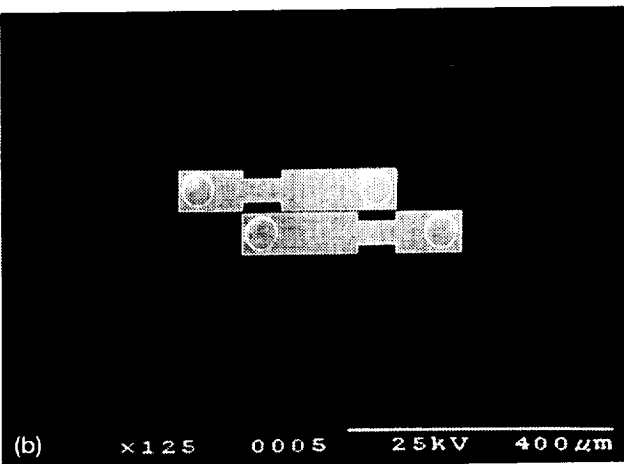
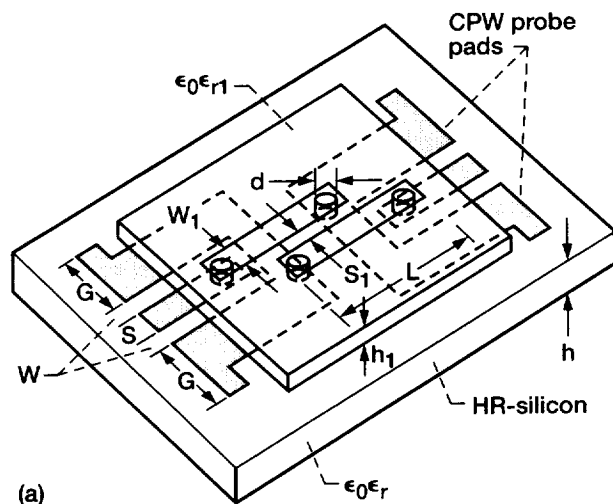


Figure 5.—(a) CPW vertically interconnected by CPS overpass with 180° phase shift. $W = 34 \mu\text{m}$, $G = 239 \mu\text{m}$, $S = 54 \mu\text{m}$, $S_1 = 4 \mu\text{m}$, $d = 40 \mu\text{m}$, $W_1 = 54 \mu\text{m}$, $L = 300 \mu\text{m}$. (b) Microphotograph of CPW vertical interconnect by CPS overpass.

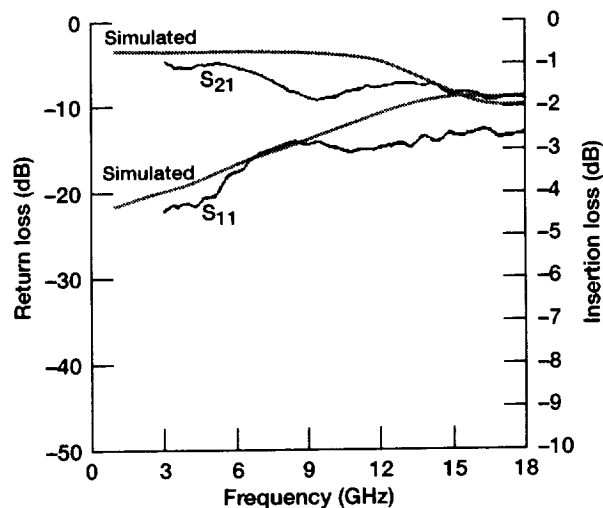


Figure 6.—Measured (De-embedded) and simulated insertion loss (S_{21}) and input return loss (S_{11}) for CPW vertically interconnected by CPS overpass and with 180° phase shift.

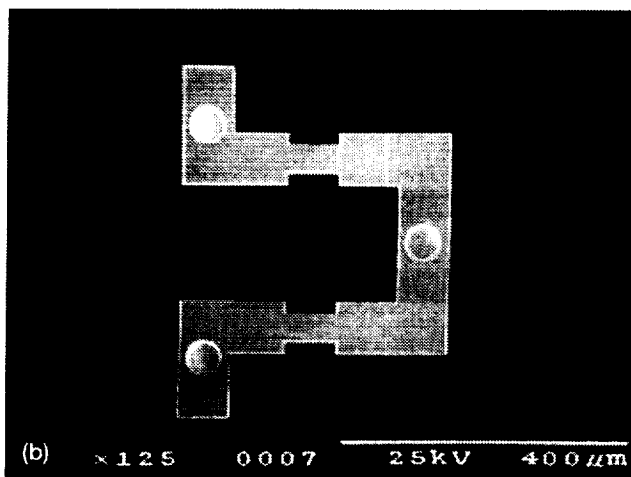
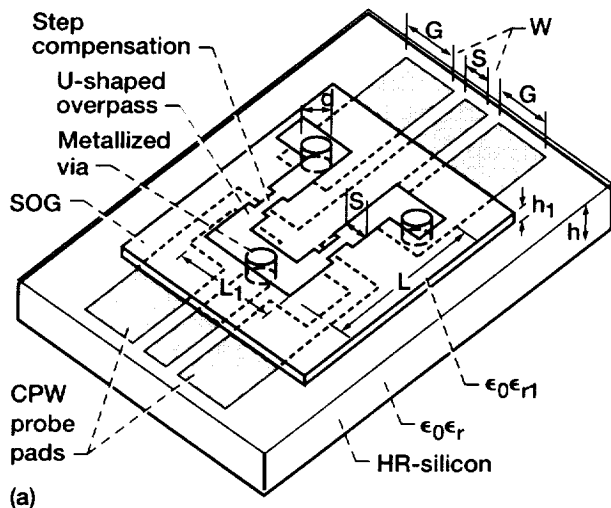


Figure 7.—(a) CPW vertical interconnect with 180° phase shift $S = 54 \mu\text{m}$, $W = 34 \mu\text{m}$, $G = 239 \mu\text{m}$, $d = 54 \mu\text{m}$, $L = 298 \mu\text{m}$, $L_1 = 230 \mu\text{m}$. (b) Microphotograph of CPW vertical interconnect with 180° phase shift.

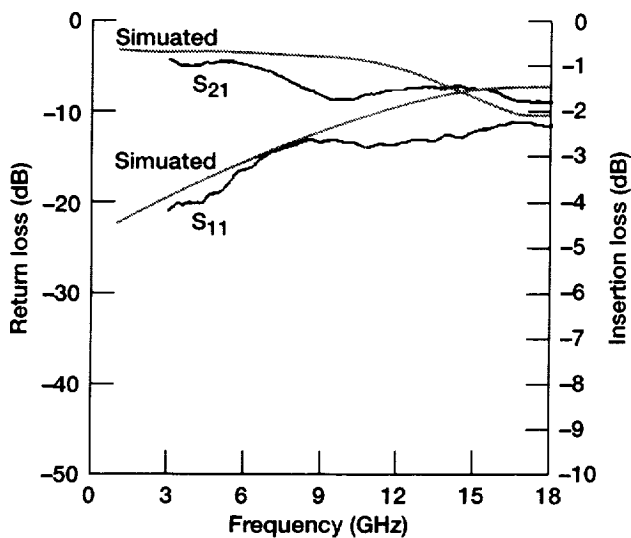


Figure 8.—Measured (De-embedded) and simulated insertion loss (S_{21}) and input return loss (S_{11}) for CPW vertical interconnect with 180° phase shift.

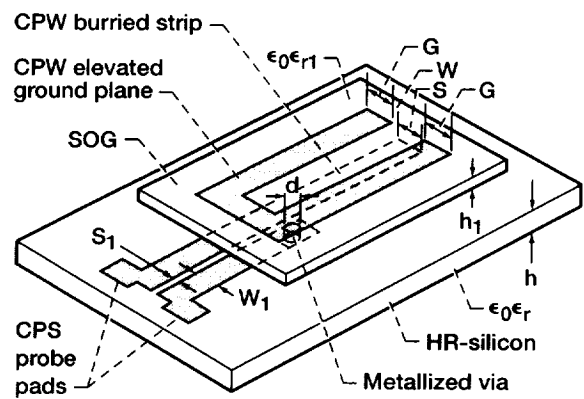


Figure 9.—CPS to CPW balun with buried center strip conductor and vertical interconnects $W = 34 \mu\text{m}$, $G = 239 \mu\text{m}$, $S = 54 \mu\text{m}$, $S_1 = 4 \mu\text{m}$, $W_1 = 54 \mu\text{m}$, $d = 40 \mu\text{m}$.

additional design parameter which can be used first, to obtain a target Z_0 , and second, to lower the attenuation as explained in [6]. The characteristic impedance $Z_{0(\text{CPS})}$ and $Z_{0(\text{CPW})}$ are both 50 Ω. The results for this structure will be presented at the conference.

II. CONCLUSIONS

Novel vertical interconnects with 180° phase shift and vertically interconnected balun for integrated circuit applications at RF/microwaves frequencies have been demonstrated. The vertical interconnects have small dimensions compared to the wavelength of operation, resulting in low parasitics. The CPS vertical interconnect with 180° phase shift has almost ideal performance with low loss, good impedance match, and very wide bandwidth extending from 3 to 18 GHz. The CPW vertical interconnects have low loss and good impedance match up to 6.5 GHz which includes the ISM bands. The results presented demonstrate the potential of the vertical interconnects with 180° phase shift/baluns for amplifiers, filters and integrated antennas in Si/SiGe based RF/microwave ICs.

III. REFERENCES

- [1] J. Browne, "SiGe Technology Makes Practical Advances," (Special Report), *Microwaves & RF*, vol. 38, no. 10, pp. 121–126, Oct. 1999.
- [2] K. Goverdhanam, R.N. Simons, and L.P.B. Katehi, "Micro-Coplanar Striplines—New Transmission Media for Microwave Applications," 1998 IEEE MTT-S Inter. Microwave Symp., Dig., vol. 2, Baltimore, Maryland, pp. 1035–1038, 1998.
- [3] Accuglass® 512 Spin-on-Glass (SOG), Product Bulletin, Allied-Signal Inc., Planarization and diffusion products, 1090 S. Milpitas Blvd., Milpitas, California 95035.
- [4] K. Goverdhanam, R.N. Simons, and L.P.B. Katehi, "Novel Three-Dimensional Vertical Interconnect Technology for Microwave and RF Applications," 1999 IEEE MTT-S Inter. Microwave Symp., Dig., vol. 2, Anaheim, California, pp. 641–644, 1999.
- [5] C.A. Balanis, *Antenna Theory Analysis and Design*, Second Edition, John Wiley & Sons, Inc., New York, 1997, Section 11.4.2, p. 555.
- [6] H. Kamitsuna, "A Very Small, Low-Loss MMIC Rat-Race Hybrid Using Elevated Coplanar Waveguides," *IEEE Microwave & Guided Wave Lett.*, vol. 2, no. 8, pp. 337–339, Aug. 1992.

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188	
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.				
1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE June 2001	3. REPORT TYPE AND DATES COVERED Final Contractor Report		
4. TITLE AND SUBTITLE Novel Vertical Interconnects With 180 Degree Phase Shift for Amplifiers, Filters, and Integrated Antennas		5. FUNDING NUMBERS WU-755-08-0B-00 NAS3-00145		
6. AUTHOR(S) Kavita Goverdhanam, Rainee N. Simons, and Linda P.B. Katehi				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) QSS Group, Inc. 2000 Aerospace Parkway Brookpark, Ohio 44142		8. PERFORMING ORGANIZATION REPORT NUMBER E-12025-2		
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Aeronautics and Space Administration Washington, DC 20546-0001		10. SPONSORING/MONITORING AGENCY REPORT NUMBER NASA CR-2001-209680		
11. SUPPLEMENTARY NOTES Prepared for the 2001 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems cosponsored by IEE MTT-S, ARO, NASA GRC, and NSF, Ann Arbor, Michigan, September 12-14, 2001. Kavita Goverdhanam, Bell Laboratories, Lucent Technologies, Murray Hill, New Jersey 07974; Rainee N. Simons, QSS Group, Inc. 2000 Aerospace Parkway, Brookpark, Ohio 44142; and Linda P.B. Katehi, University of Michigan, Radiation Laboratory, EECS Department, Ann Arbor, Michigan 48109-2122. Project Manager, Thomas P. Burke, Systems Engineering Division, NASA Glenn Research Center, organization code 7800, 216-433-5172.				
12a. DISTRIBUTION/AVAILABILITY STATEMENT Unclassified - Unlimited Subject Category: 33 Available electronically at http://gltrs.grc.nasa.gov/GLTRS This publication is available from the NASA Center for AeroSpace Information, 301-621-0390.			12b. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words) In this paper, novel low loss, wide-band coplanar stripline technology for RF/microwave integrated circuits is demonstrated on high resistivity silicon wafer. In particular, the fabrication process for the deposition of spin-on-glass (SOG) as a dielectric layer, the etching of microvias for the vertical interconnects, the design methodology for the multiport circuits and their measured/simulated characteristics are graphically illustrated. The study shows that circuits with very low loss, large bandwidth and compact size are feasible using this technology. This multilayer planar technology has potential to significantly enhance RF/microwave IC performance when combined with semi-conductor devices and microelectromechanical systems (MEMS).				
14. SUBJECT TERMS Coplanar waveguide; Stripline circuits; High resistivity silicon; Spin-on-glass; Monolithic microwave integrated circuits			15. NUMBER OF PAGES 10	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT Unclassified	18. SECURITY CLASSIFICATION OF THIS PAGE Unclassified	19. SECURITY CLASSIFICATION OF ABSTRACT Unclassified	20. LIMITATION OF ABSTRACT	