FPGAs in Space Environment and Design Techniques

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Goals

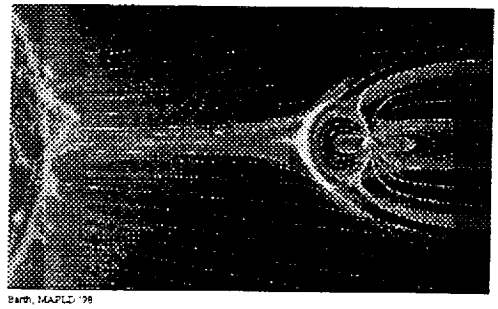
- Brief overview of the radiation environment
- What type of radiation effects are there?
- How are devices tested?
- How should the results be interpreted?
- How can we protect our systems?

Outline

- Environment and Effects
- Total Dose
- Single Event Upset
- Single Event Latchup
- Single Event Transient
- Antifuse and Rupture
- Protons
- Loss of Functionality
- Miscellaneous

Environment and Effects

The Radiation Environment



Barth, MAPLD '98

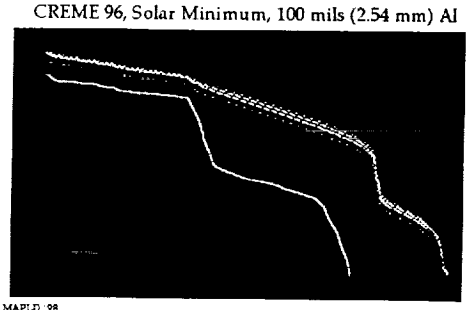
Components of the Natural Environment

- Transient
  - Galactic Cosmic Rays
    - Hydrogen & Heavier Ions
  - Solar Particle Events
    - Protons & Heavier Ions
- Trapped
  - Electrons, Protons, & Heavier Ions
- Atmospheric & Terrestrial Secondaries
  - Neutrons

Barth, MAPLD '98

GCRs: Integral LET Spectra

CREME 96, Solar Minimum, 100 mils (2.54 mm) Al



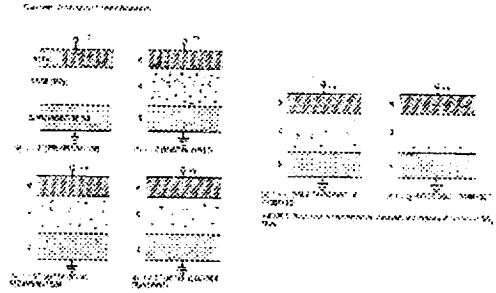
Barth, MAPLD '98

Types of Single Event Effects

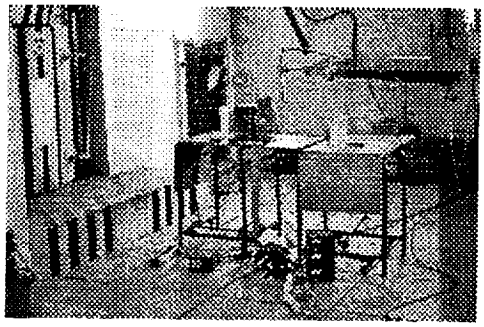
Acronym	Definition	Description
SEU	Single Event Upset	Change of information stored
SED	Single Event Disturb	Momentary disturb of information stored in memory bit
SET	Single Event Transient	Current transient induced by passage of a particle, can propagate to cause output error in combinational logic
SEDR	Single Event Dielectric Rupture	Essentially antifuse rupture
SEGR	Single Event Gate Rupture	Rupture of gate dielectric caused by a high current flow
SEL	Single Event Latchup	High current regenerative state induced in 4-layer device (latchup)
SES	Single Event Snapback	High current regenerative state induced in NMOS device (snapback)
MBU	Multiple Bit Upset	Several memory bits upset by passage of the same particle
SEFI	Single Event Functional Interrupt	Corruption of control path by an upset

Total Dose

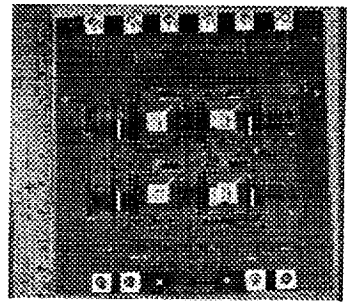
Recombination, Transport, and Trapping of Carries



GSFC Total Dose Facility



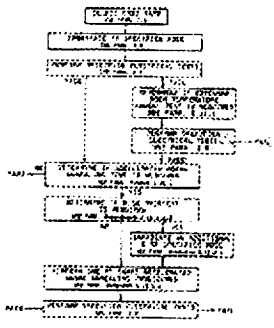
Example TID Static Bias Board Supports In Situ Testing

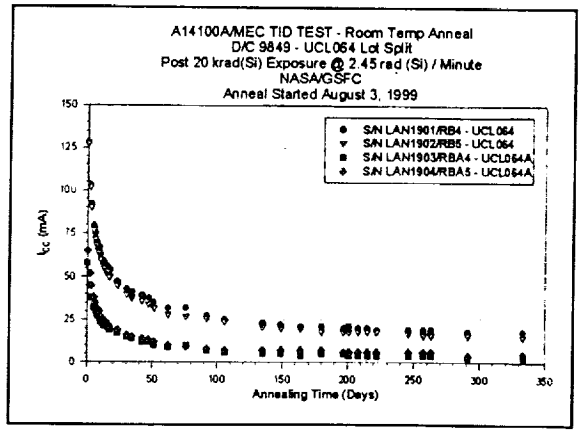


MIL-Std-883 Method 1019.5

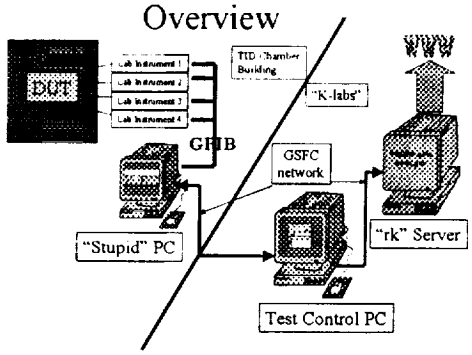
Annealing allowed for parametric failures; not for functional failures.

1019.5 also allows for low dose rate testing.

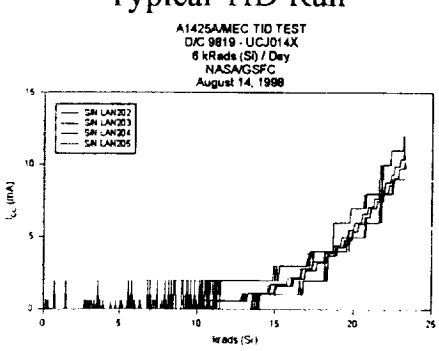




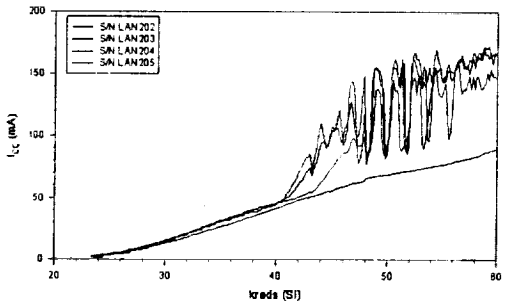
Second Generation System - Overview



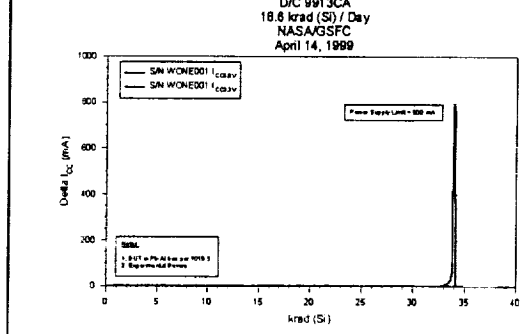
Typical TID Run



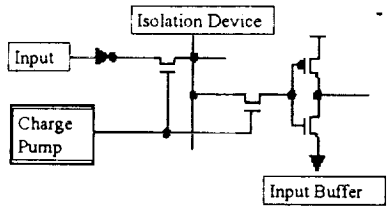
TID Run - Extended



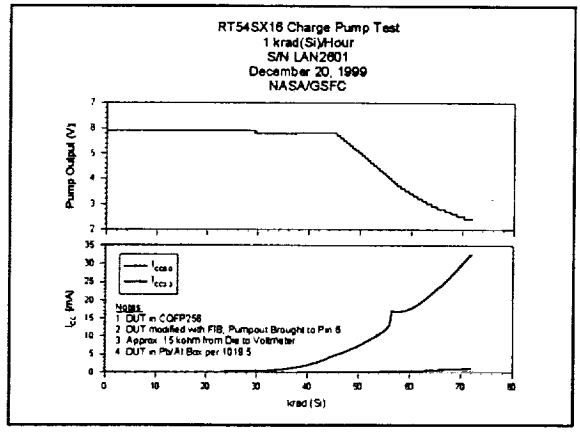
TID Run - Runaway



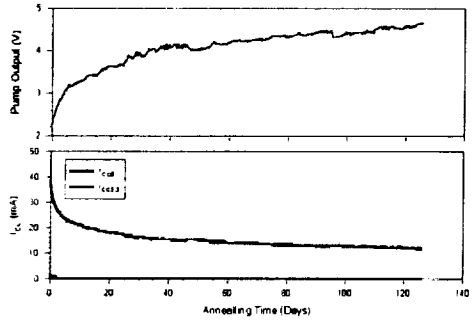
Charge Pump and Isolation FETs



from Wang, et. al

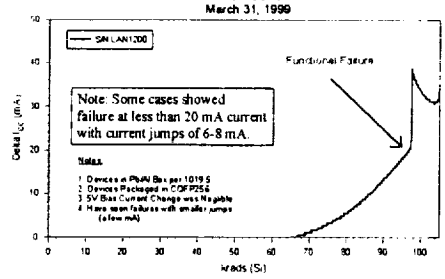


RT54SX16 Charge Pump Test
Annealing After 72 krad(Si)
S/N LAN2601
May 21, 2000
NASA/GSFC



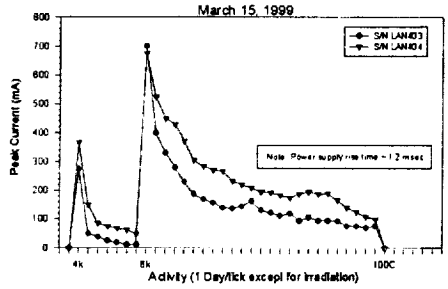
In Situ Functional Testing

RT54SX16/MEC TID TEST
D/C 9849 - P05
12.95 rad (Si) / minute
NASA/GSFC
March 31, 1999



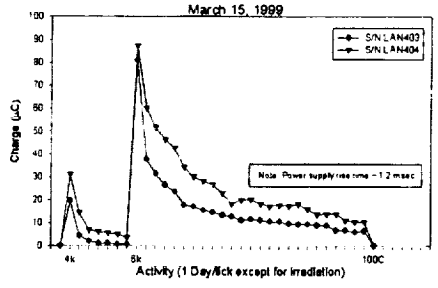
I_{CC} Transient - Peak Current

A1280A/MEC I_{CC} Transient Test
D/C 9826 - U1H466 - LAN400
1 krad(Si) / Hour
NASA/GSFC
March 15, 1999

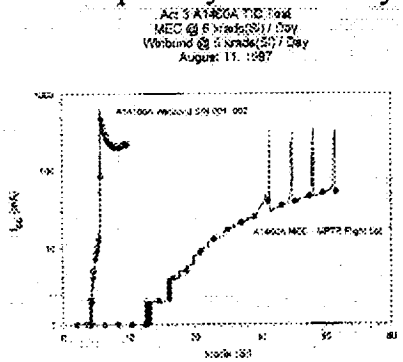


I_{CC} Transient - Charge

A1280A/MEC I_{CC} Transient Test
D/C 9826 - U1H466 - LAN400
1 krad(Si) / Hour
NASA/GSFC
March 15, 1999



TID Capability vs. Foundry



TID vs. Product Lifetime

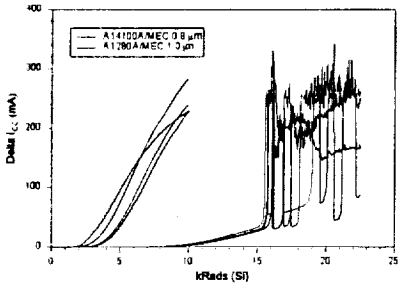
Device	Technology (µm)	Total Dose	Lifetime
A1020	2.0	> 100 krad(Si)	1988-92
A1020A	1.2	~ 100 krad(Si)*	1991-95
A1020B	1.0/0.9	< 20 krad(Si)	since '93
A1020DX	0.5	N/A	-

* Variable -some lots higher, some lower

from Wang, et al

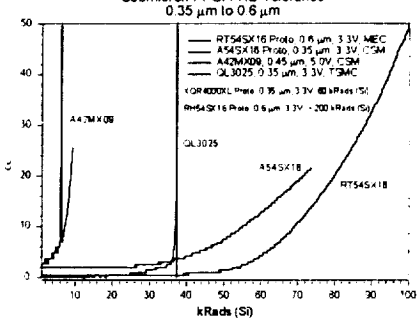
TID Capability vs. Feature Size

Recent 0.8 and 1.0 µm TID Results



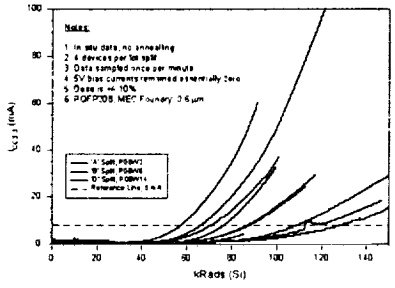
TID Capability vs. Feature Size

Submicron FPGA TID Tolerance
0.35 µm to 0.6 µm



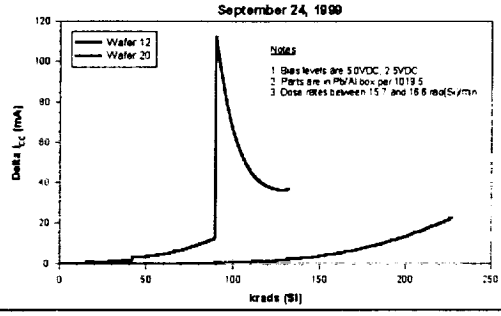
Process Mods - 0.6 µm

RT54SX16 Prototype
Lot Split TID Test
NASA/GSFC - Actel
July 3, 1998
1 kRad (Si) / Hour

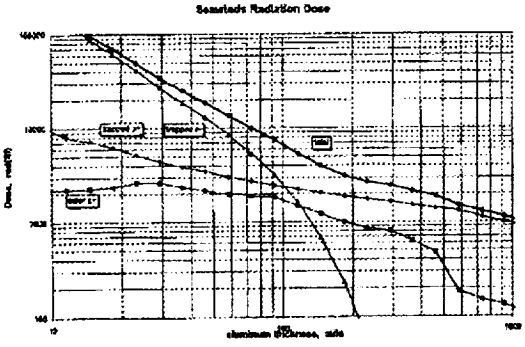


Process Mods - 0.25 µm

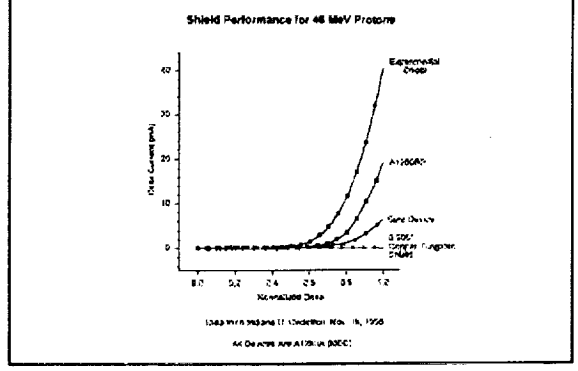
A54SX32A (Prototype) TID TEST
D/C 9924
P04 Wafer 12 and 20
NASA/GSFC
September 24, 1999



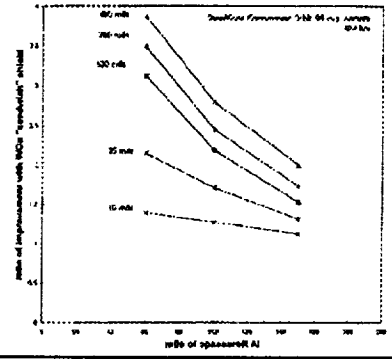
Dose Depth Curves



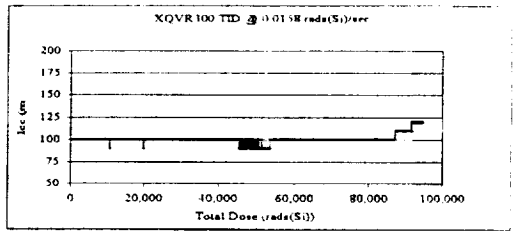
Shield of 46 MeV Protons



Shielding Effectiveness



Dose Rate Effects on Xilinx 0.25µm Technology



Total Ionizing Dose Effect on 0.18µM Technology

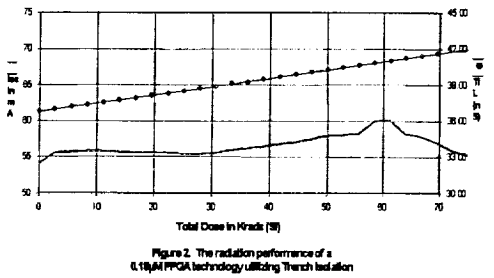
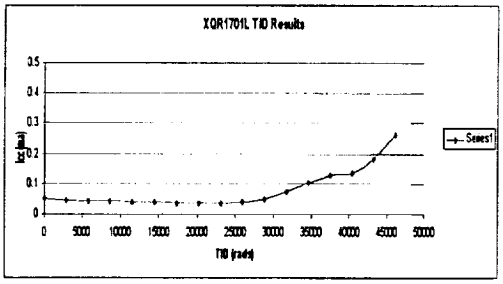


Figure 2. The radiation performance of a 0.18µM FPGA technology utilizing Trench Isolation

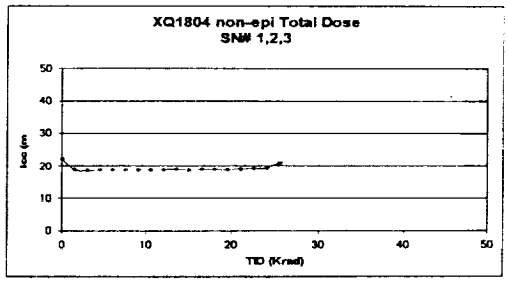
TID Testing Results

- 0.60µM OTP PROM Technology
  - TID evaluation performed on XQR1701L
  - device parametric shifts affected decoder speed
  - field oxide leakage determined TID of 60krads
  - device fully functional at end of dose
  - no data loss/gain as a result of TID
  - 100°C anneal fully restored device
  - room temp anneal showed no rebound

Xilinx PROM Response to TID



Xilinx PROM Response to TID

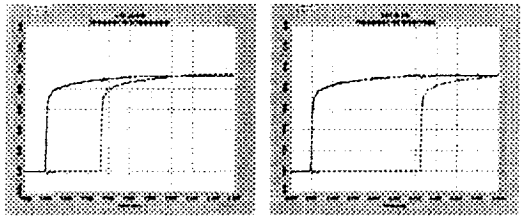


In Situ measurement of Propagation Delay

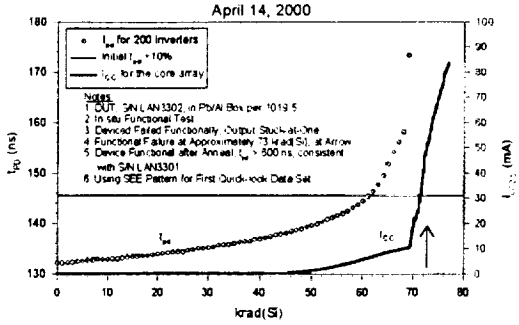
Real-time Digitized Input and Output Waveforms

Before irradiation t_{PD} = 135ns

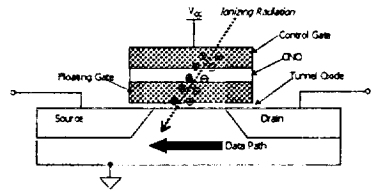
After accumulating 90 krad : t_{PD} = 260ns



A500K050 TID Test
Prototype Test
1 krad(Si) / Hour
NASA GSFC
April 14, 2000

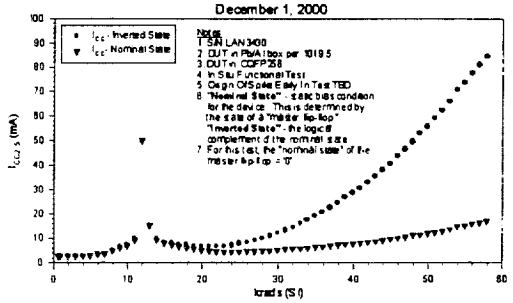


Total Dose Effects on FLASH Switch

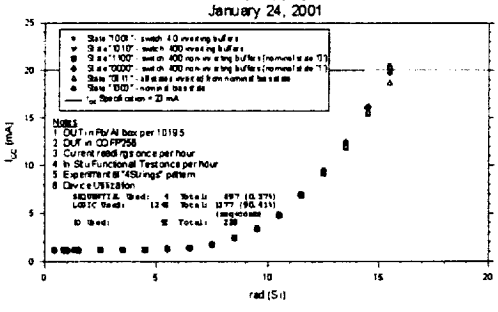


- Ionizing radiation discharge the floating gate
  - Increase ON-state NMOS transistor resistance, increase RC delay in the data path
  - Increase OFF-state NMOS sub-threshold leakage, increase I_{CC}

RT54SX32S (Prototype) TID TEST
0.25 µm, MEC
D/C 0019 - L/C T25JP01 001
1 krad (Si) / Hour
NASA/GSFC
December 1, 2000



A14100A TID TEST
0.8 µm, MEC
L/C UCL055 - LAN 171
1 krad (Si) / Hour
NASA/GSFC
January 24, 2001



Single Event Upset (SEU)

Definitions

Single Event Upset (SEU) is a change of state or transient induced by an ionizing particle such as a cosmic ray or proton in a device. This may occur in digital, analog, and optical components or may have effects in surrounding circuitry. These are "soft" bit errors in that a reset or rewriting of the device causes normal behavior thereafter. A full SEU analysis considers the system effects of an upset. For example, a single bit flip, while not damaging to the circuitry involved, may damage the subsystem or system (i.e., initiating a pyrotechnic event).

Definitions

Linear Energy Transfer (LET) is a measure of the energy transferred to the device per unit length as an ionizing particle travels through a material. The common unit is MeV-cm^2/mg of material (Si for MOS devices).

LET threshold (LET_{TH}) is the minimum LET to cause an effect. The JEDEC recommended definition is the first effect when the particle fluence = 10^7 ions/cm^2.

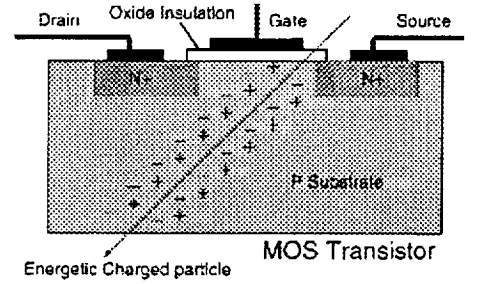
Definitions

Cross section (sigma) is the device SEE response to ionizing radiation. For an experimental test for a specific LET, sigma = #errors/(ion fluence). The units for cross section are cm^2 per device or per bit.

Asymptotic or saturation cross section (sigmasat) is the value that the cross section approaches as LET gets very large.

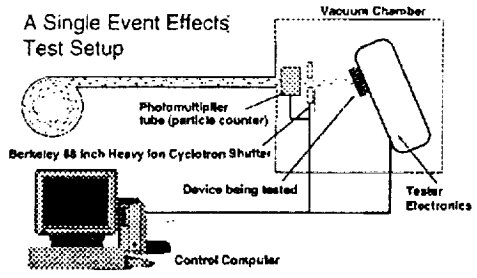
Sensitive volume refers to the device volume affected by SEE-inducing radiation. The geometry of the sensitive volume is not easily known, but some information is gained from test cross section data.

Interaction of a Cosmic Ray and Silicon

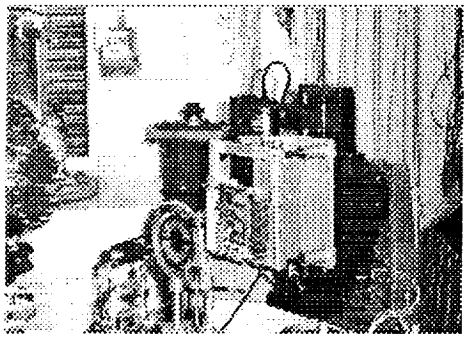


From Aerospace

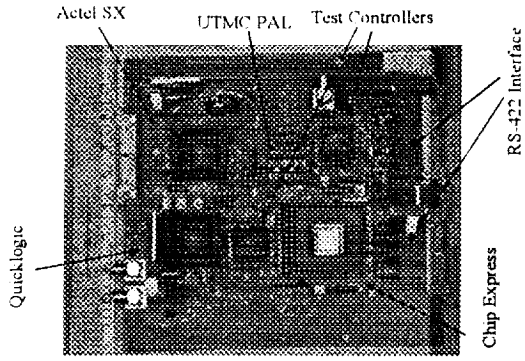
SEE Test Setup



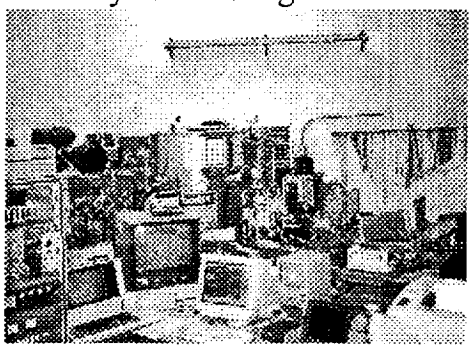
Heavy Ion Testing at BNL



Example SEE DUT Card

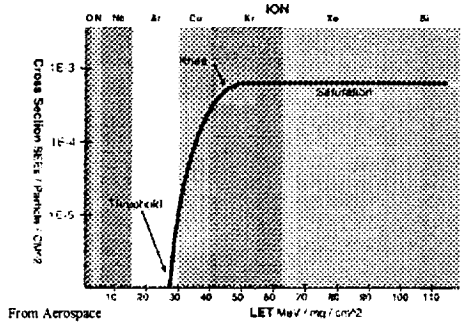


Heavy Ion Testing at BNL



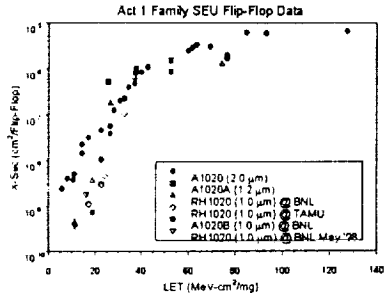
Heavy Ion Testing at BNL

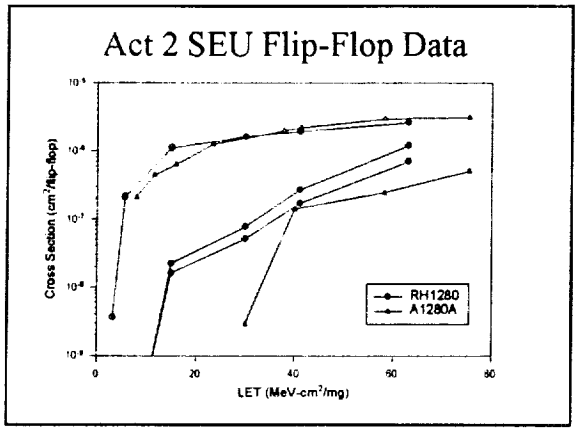
Cross Section versus LET Curve

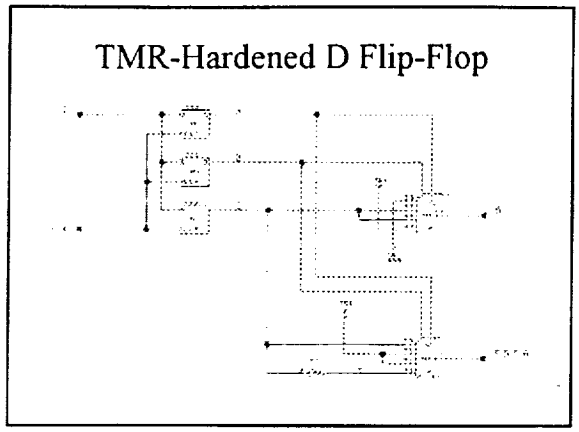


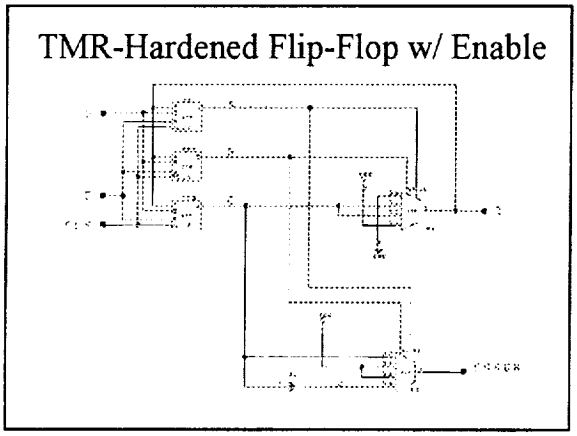
From Aerospace

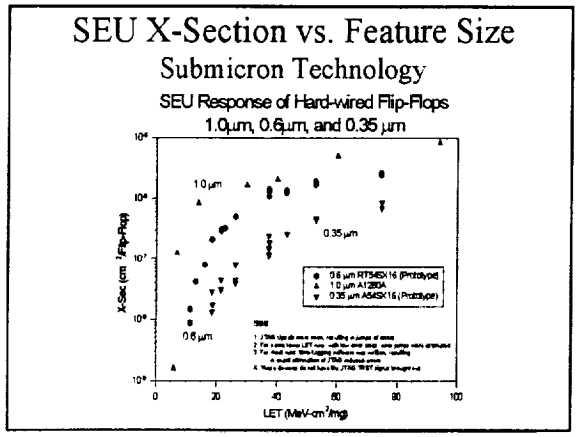
SEU X-Section vs. Feature Size Old Technology











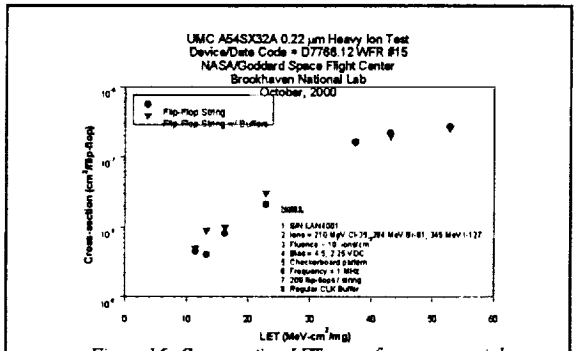


Figure 16. Cross section-LET curve for a commercial A54SX32-A. Few SEUs were detected for the hardened device at an LET ≥ 60 MeV-cm²/mg.

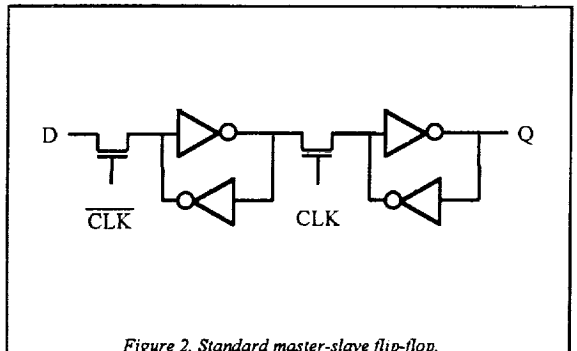


Figure 2. Standard master-slave flip-flop.

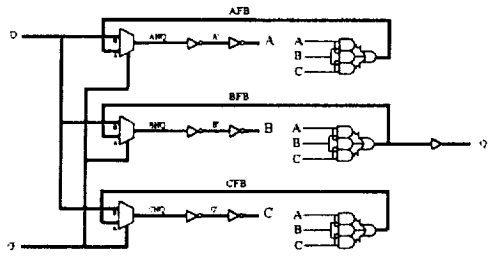


Figure 3. K-Latch schematic, simplified. The asynchronous structure and interlocks eliminate the need for a free running clock to scrub SEUs.

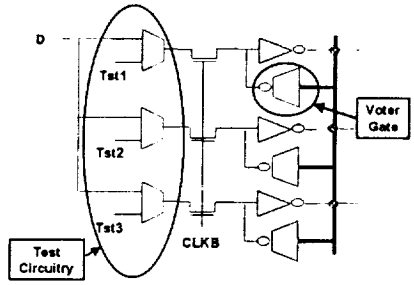
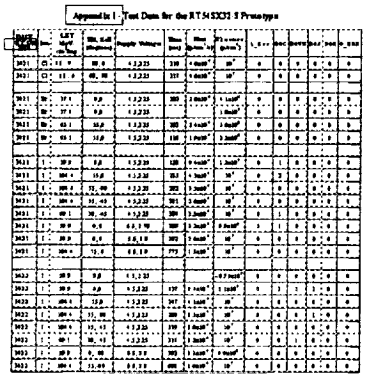
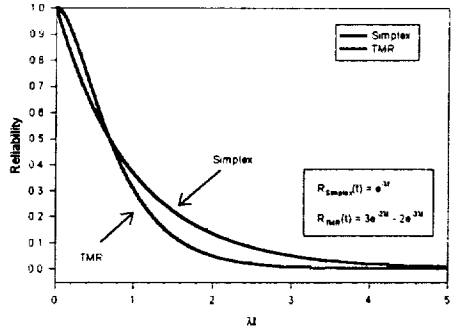


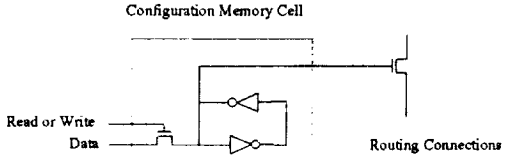
Figure 5. Simplified test circuitry logic.



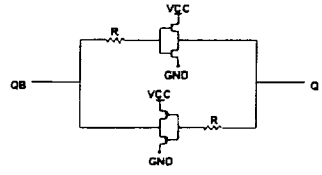
Simplex vs. TMR Reliability



SRAM Switch Technology

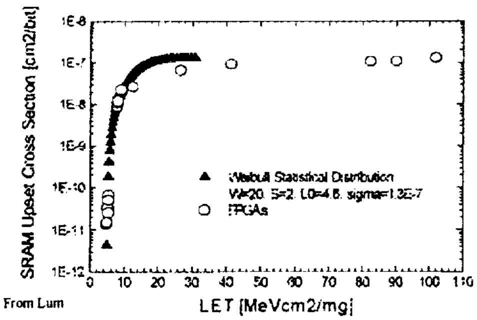


Resistor De-coupling Hardened SRAM



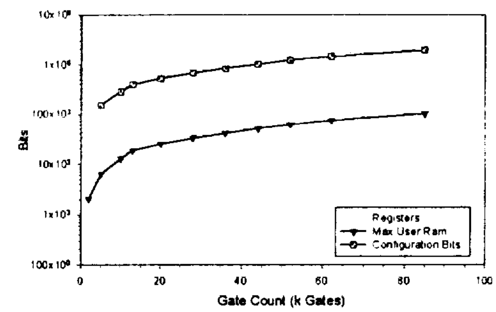
- Increase internal latch delay.
- no upset when response time > recovery time.
- Poly- resistor has high temperature coefficient.
- Poly-resistance has large process variation

XQR4036XL SEU Cross Section



From Lum

SRAM Memory Sizes



XQR4036XL SEU Rates

Table 2. Upset rates for several orbital environments

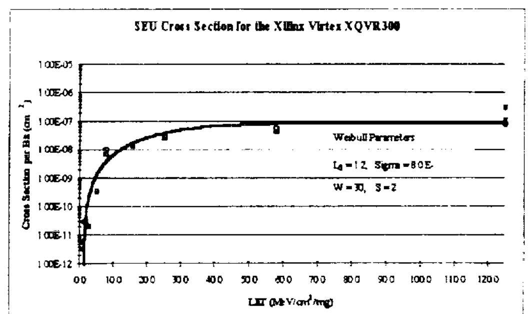
[illegible]						
Trapped p+	Galactic p+	90% w/c p+	ALSF p+	Galactic HI	90% w/c HI	ALSF HI
(ups/bit-day)	(ups/bit-day)	(ups/bit)	(ups/bit)	(ups/bit-day)	(ups/bit)	(ups/bit)
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Launch vehicle from Vandenberg, 100 mil Al shielding						
[illegible]	[illegible]	-	-	[illegible]		-

Table 3. Probability of success and total upsets predicted for a LEO 5 year mission

[illegible]						
Trapped p+	Galactic p+	90% w/c p+	ALSF p+	Galactic HI	90% w/c HI	ALSF HI
[illegible]	[illegible]	[illegible]	0	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]						
[illegible]	[illegible]	-	-	[illegible]	-	-
[illegible]	[illegible]	-	-	[illegible]	-	-

From Lum

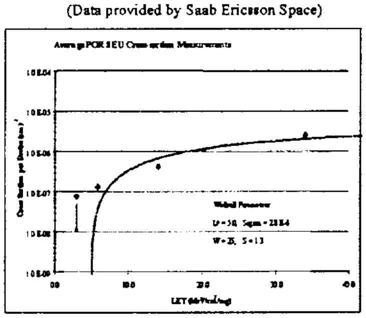
Virtex FPGA Static Heavy Ion SEU Sensitivity



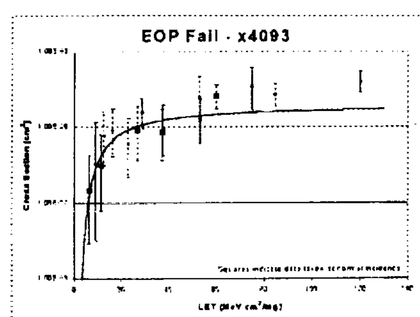
An upset in configuration control logic register was observed

Weibull Curve for Average POR Heavy Ion Cross-section

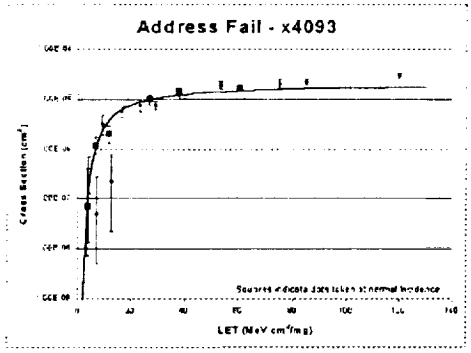
(Data provided by Saab Ericsson Space)



XQR1701L PROM



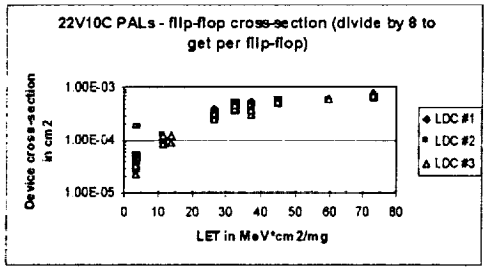
XQR1701L PROM



UT4090

- User flip-flops hardened
- I/O flip-flops not hardened
- RAM blocks not hardened

SEU in PAL - Large X-Section

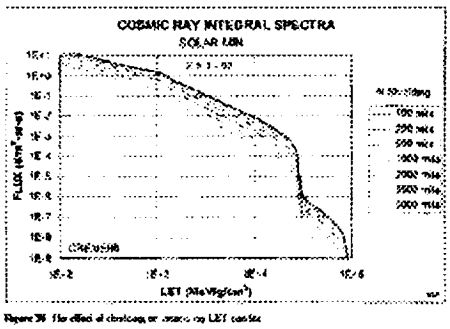


Solar Flare and SEU Rates

# of modules	input pattern	module design	LET threshold	sigma	upsets/ 1000 b-d's cosmic ray	upsets/ 1000 b-d's solar flare
102	0*S	C	25	1E-6	2.32E-4	1.32
40	0*S	S	25	4E-7	4.2E-5	0.16
360	0*S	S (H)	25	4E-7		
60	0*S	S (VH)	25	4E-7		
102	1*S	C	55	1E-7	4.46E-10	1.86E-6
40	1*S	S	5	6E-6	0.77	1.284
360	1*S	S (H)	5	6E-6		
60	1*S	S (VH)	5	6E-6		

Note effect of logic state on SEU Rate.

Shielding Cosmic Rays



Software Support for SEU-Hardening

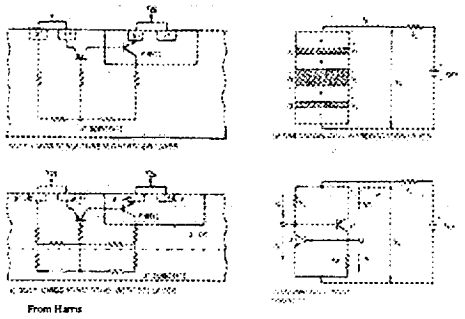
- Synopsis Design Compiler
- Synplicity Synplify
- NASA-GSFC 'Macro Substitution'
- Actmap & Actgen

Single Event Latchup (SEL)

Definitions

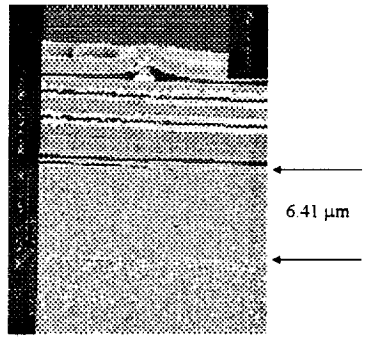
Single Event Latchup (SEL) is a potentially destructive condition involving parasitic circuit elements forming a silicon controlled rectifier (SCR). In traditional SEL, the device current may destroy the device if not current limited and removed "in time." A "microlatch" is a subset of SEL where the device current remains below the maximum specified for the device. A removal of power to the device is required in all non-catastrophic SEL conditions in order to recover device operations.

Latchup Basics

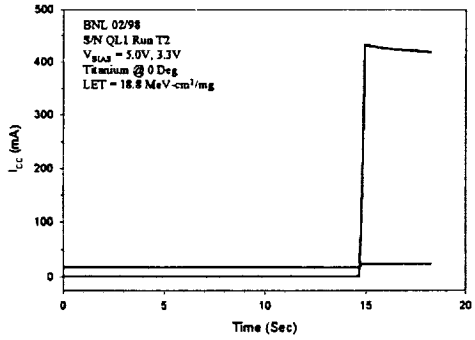


From Harris

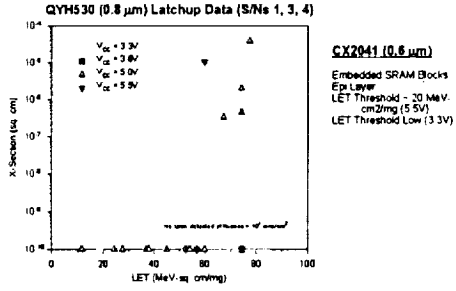
EPI Layer, Latchup, and Ion Range



SEL - QL3025 0.35 µm



Chip Express Latchup Comparison

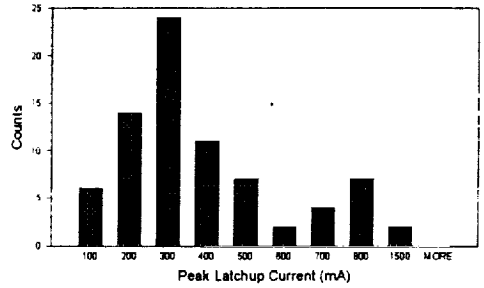


SEL_{TH} Variability

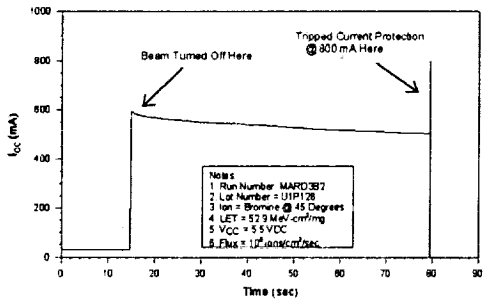
S/N	Lot No.	D/C	Threshold	X-Sec	Prolonged Latchup Allowed?
A1	U1P126	9646	52.9	1.5E-06	no
A4	U1P061	9402	52.9	4.50E-06	no
B1	U1P054	9851	52.9	3.4E-07	no
B2	U1P054	9851	43.2	2.0E-06	no
B3	U1P054	9851	52.9	3.0E-06	yes
B4	U1P054	9851	52.9	1.5E-06	yes
B5	U1P054	9851	> 74.7	no latchup	-
B6	U1P054	9851	< 74.7	no latchup	-
C1	U1P054	9844	52.9	3.0E-06	no
C2	U1P054	9844	43.2	no data @75	yes
C3	U1P054	9844	74.7	no data @75	no
D1	U1P126	9704	43.2	6.7E-06	no
D2	U1P126	9704	43.2	9.4E-06	no
D3	U1P126	9704	43.2	no data @75	yes
D4	U1P126	9704	< 37.4	no data @75	yes
D5	U1P126	9704	< 43.2	no data @75	yes

SEL Summary for A1020B. A large set of parts from multiple lots were tested, showing a wide range of SEL LET_{TH} and latchup currents. Some latchups were destructive with either higher I_{CC} or functional failure.

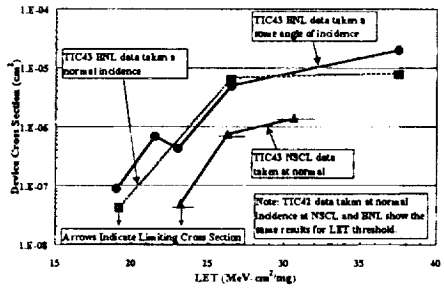
Distribution of Peak Latchup Currents for the A1020B (MEC)



Single Event Latchup

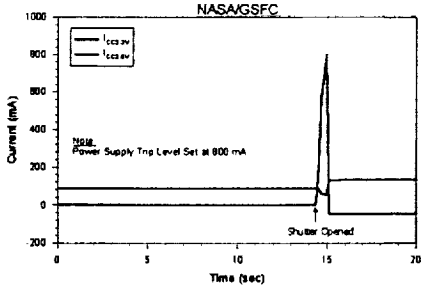


Single Event Latchup Ion Energy Dependence



SEL Test Results

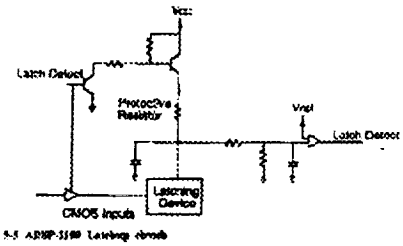
A500K050 (Prototype) SEE Test
BNL, September 2000
S/N LAN3303, Run B2
Bromine
NASA/GSFC



Latchup Summary

Device Type * Pre-prod.	Size/Voltage (nominal core)	Threshold (MeV-cm²/mg)	Comments
RH1020	1.0 µm / 5.0	> 74	
QL24X32B	0.65 µm / 5.0	< 18	Destructive
RT54SX16/32*	0.8 µm / 3.3	> 120	
A54SX32A*	0.25 µm / 2.5	High	
QYH530	0.8 µm / 5.0	52	One-Mask
CX2041	0.6 µm / 2.5	> 37	LPGA
CX3001	0.35 µm / 3.3	Low	
A54SX16*	0.35 µm / 3.3	> 74	
QL3025	0.35 µm / 3.3	< 11	Destructive
XQR4062XL*	0.35 µm / 3.3	> 100	

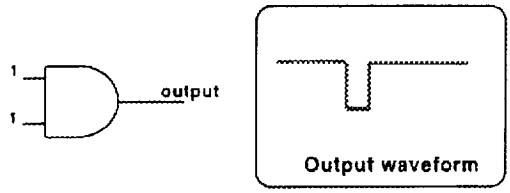
Ex. SEL Detection and Clearing



Note that FPGA have high I/O count with diodes to V_{CC} and GND in most cases.

Single Event Transient (SET)

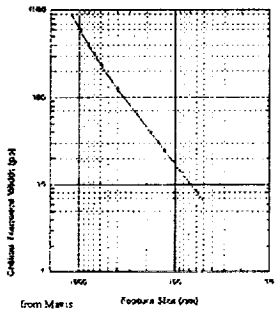
Single Event Transient (SET)



Fraction of a nanosecond to several nanoseconds.

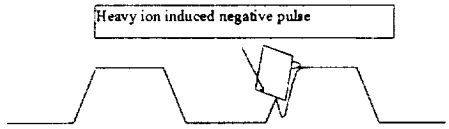
From Aerospace

Critical Transient Width vs Feature Size for Unattenuated Propagation



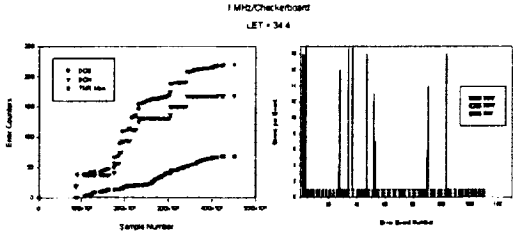
From Maris

Double Clocking As a Result of Heavy Ion Induced Pulse



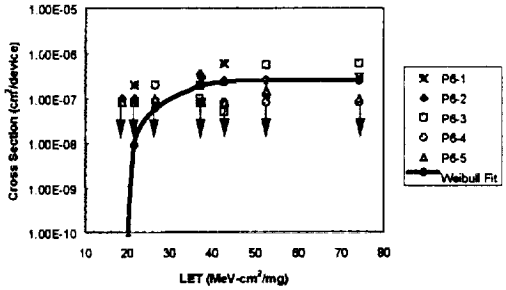
Cartoon of clock/logic upset. The device is most sensitive during the transition.

Clock Upset Instrumentation

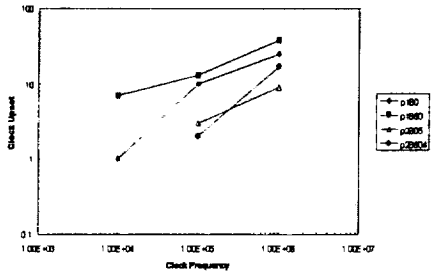


Cumulative Error Counts Differential Error Counts

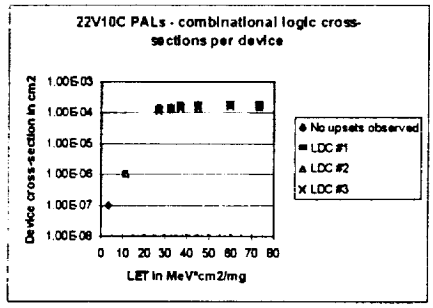
Clock Upset Cross Section RH1020



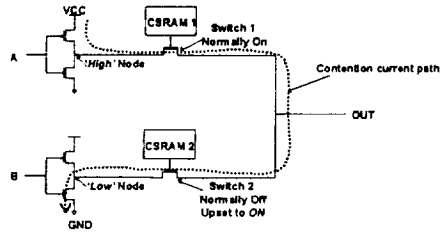
Frequency Dependence of Clock Upset



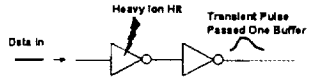
SET in PAL



Driver Contention Due to CSRAM Upset



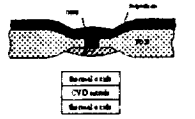
Mode 1 Transient Upset

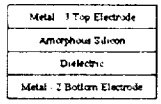


- Transient pulse higher than half VDC will propagate
- Q_{crit} ~ 0.02pC, or LET_{th} ~ 2MeV-cm²/mg for the worst case

Antifuse and Rupture

Antifuse Technology



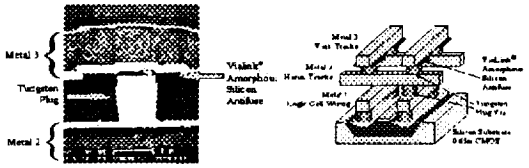


ONO Antifuse
Poly/ONO/N++
Heavy as doped Poly/N++
Thickness controlled by
CVD nitride
Programs ~ 18V
Typical Toxono ~ 85 Å
RH1280 Toxono = 99 Å
R = 200 - 500 ohms

TD Amorphous Silicon Antifuse
'Pancake' Stack Between Metal 2 and 3
Designed for 3.6V Operation in Sea Of Gates FPGA

'Logic' Devices Program at ~ 10V
'Substrate' Devices Program at ~ 30V
Thickness ~ 500 - 1000 Å
R = 20 - 100 ohms

Quicklogic ViaLink Antifuse



Antifuse Construction

Antifuse Radiation Effects

- Unprogrammed Reliability is the Key Concern
  - ONO
  - Amorphous Silicon (AS)
- Manufacturers:
  - Actel (ONO, Silicon) FPGA
  - L-M (ONO) PROM
  - Pico Systems (AS) Programmable Substrate
  - Quick Logic (AS) FPGA
  - UTMC (AS) PAL, PROM

Gate Rupture

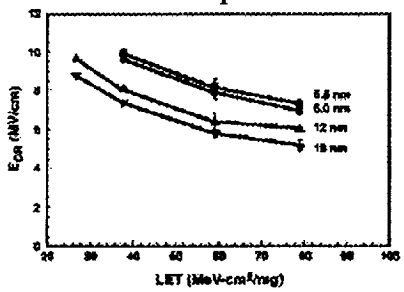
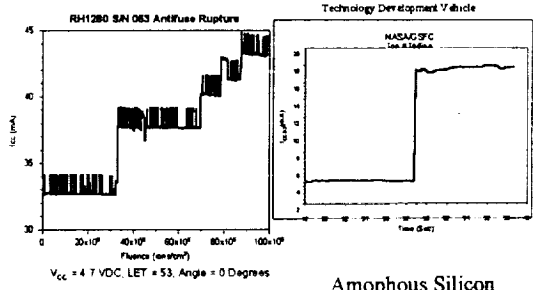


Figure 5.4. Critical oxide field for SEGR as a function of ion LET for various gate oxide thicknesses. In this data the breakdown field increases significantly for the thin oxides (After [Scot-97]).

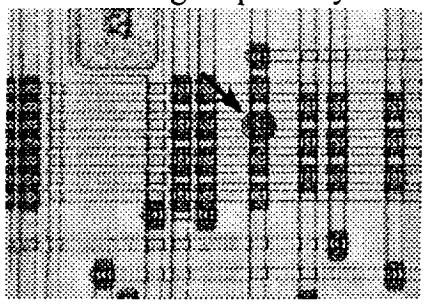
Comparison of Rupture Currents



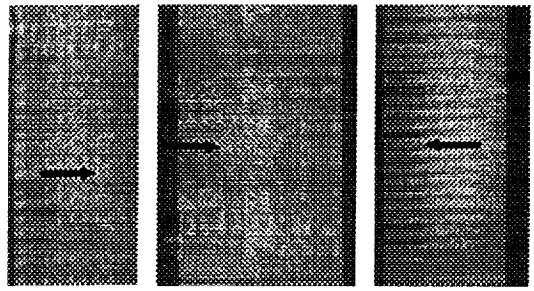
ONO Antifuse

Amophous Silicon Antifuse Rupture

Substrate α-Silicon Antifuse F/A Using Liquid Crystal

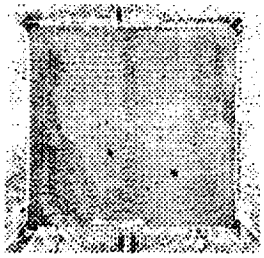


ONO Antifuse Breakdown - FA

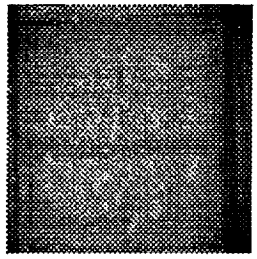


Mag = 5X Mag = 20X Mag = 100X

Heavy Ion Damage and Failure Analysis

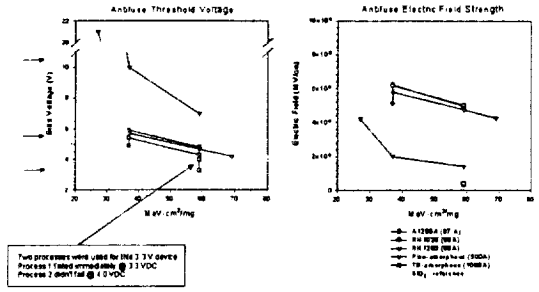


M2M Antifuse Device

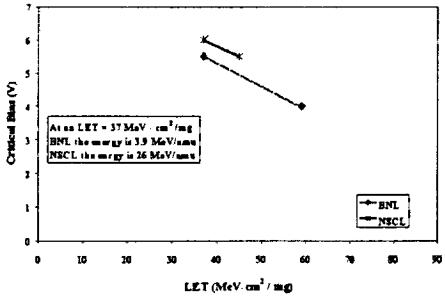


ONO Antifuse Device

Antifuse Failure Thresholds



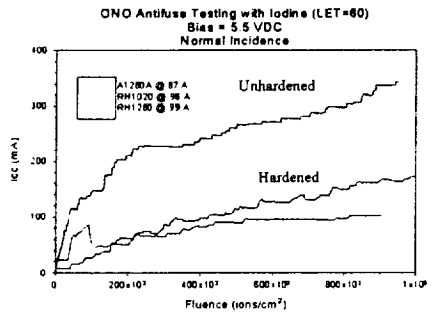
Antifuse Rupture Ion Energy Dependence



Antifuse Improvements

- Decrease Electric Field Strength
  - Thicker Antifuses (RH1020, RH1280)
  - Low Bias Voltage (L-M PROM)
- Antifuse "Recipe"
  - (RT54SX16, RH54SX16, RT54SX32)
- Minimize Bias Time
  - (UTMC PROM)
- Reduce Sensitivity
  - Differential Measurements (UTMC PROM)

Dielectric Antifuse Cross Sections



Antifuse Rupture

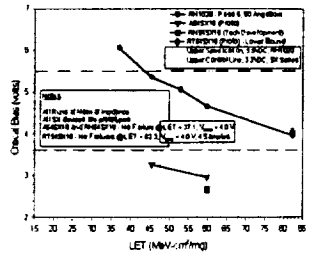
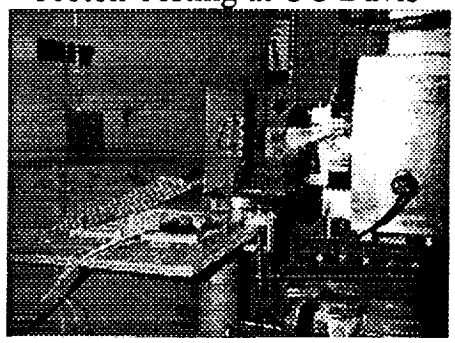


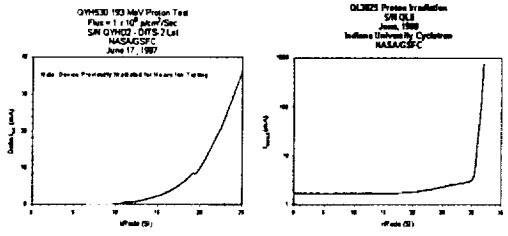
Figure 1. Summary of antifuse rupture data. Positive margin at LET = 37 MeV-cm2/mg is shown for production RH1020 with a hardened ONO antifuse. One "recipe" of an M2M antifuse did not fail at LET = 82 MeV-cm2/mg, V_{BIAS} = 400 mV.

Protons

Proton Testing at UC Davis

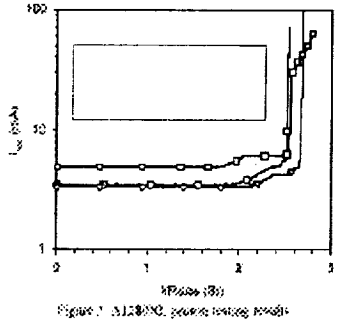


I_{CC} Damage During Proton Testing ASIC and Antifuse FPGA



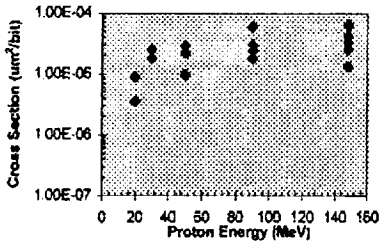
Note: Different scales for each run.

A1280XL Proton Results



from Wang, et. al

RH1280 Proton Upsets



From Lockheed-Martin/Actel

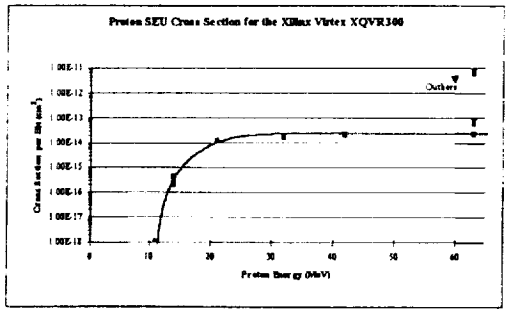
- S module threshold = 36 MeV
- C and Modified S > 148 MeV

A1280A Proton Upsets

Proton Sensitivities - 195 MeV

Device Type	Size/Voltage (nominal core)	Est. X-Sec (cm^2 / f-f)	Comments
A1280A	1.0 µm / 5.0	~ 137 x 10^{-15}	19 Parts Tested
RH1020	1.0 µm / 5.0	< 2 x 10^{-15}	
RH1280	0.8 µm / 5.0	~ 400 x 10^{-15}	S-Module
QYH500	0.8 µm / 3.3	< 0.5 x 10^{-15}	No upsets det.
RT54SX16	0.6 µm / 3.3	~ 6 x 10^{-15}	
QL3025	0.35 µm / 3.3	< 4 x 10^{-15}	No upsets det.
A54SX16	0.35 µm / 3.3	~ 3 x 10^{-15}	
JT22VP10	? µm / 5.0	~ 2 x 10^{-11}	Cypress die

Virtex FPGA Static Proton SEU Sensitivity



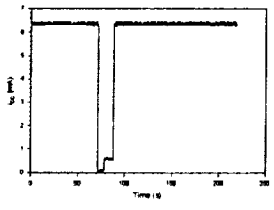
Configuration control logic register upset noted at 63MeV

Loss of Functionality

Definitions

Single Event Functional Interrupt (SEFI) is a condition where the device stops operating in its normal mode, and usually requires a power reset or other special sequence to resume normal operations. It is a special case of SEU changing an internal control signal. One example would be a DRAM entering the test mode defined by JEDEC. Another example is a microcircuit with IEEE 1149.1 JTAG circuitry leaving the TEST_LOGIC_RESET state and loading an unintended instruction into the instruction register (IR). Like other SEUs, the system effects must be properly analyzed. For example, a JTAG upset can cause the device to draw high currents or turn inputs into an output. The latter could, for example, drive a clock line to ground; thus, an independent clock signal should be used for the TCLK pin on devices without the optional TRST* pin.

FRAM Memory Functionality Loss During Heavy Ion Test



Strip chart of FM1608 (research fab) current during heavy ion irradiation. The device lost functionality during the test while the current decreased from it's normal dynamic levels of approximately 6.3 mA to it's quiescent value, near zero. The device recovered functionally and operated normally throughout the latter part of the test. This effect was seen at least three times during the limited testing of this device.

DRAM Modes

DRAM Special Test and Operational Modes

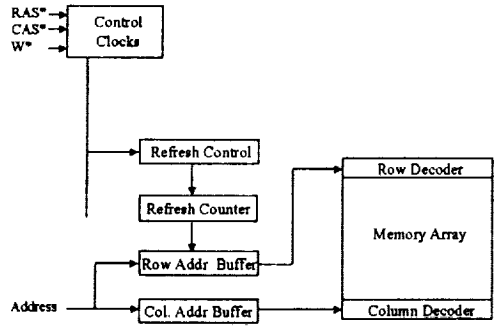
This standard defines a scheme for controlling a series of special modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control, and exit from the special modes. In addition, it defines a basic special test mode plus a series of other special test and operational modes.

TEST MODES are those that implement some special test of measurement function or algorithm designed to enhance the ability of the Vendor or User to determine the integrity of, or to characterize, the part.

OPERATIONAL MODES are those that alter the operational characteristics of the part but do not interfere with its function as a storage device and are intended to be used in system operation.

JEDEC Standard No. 21-C, page 3.9.5-7, Release 4

DRAM Refresh



Adapted from: http://www.techchannel.de/hardware/173/6.html

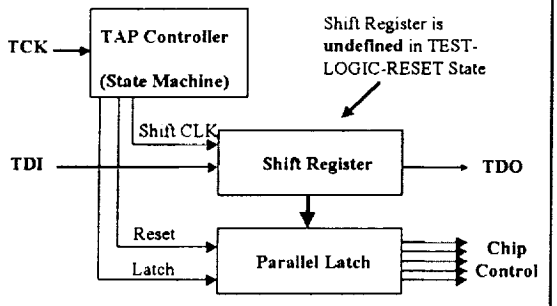
DRAM Refresh

CAS#-BEFORE-RAS# REFRESH is a frequently used method of refresh because it is easy to use and offers the advantage of a power savings. Here's how CBR REFRESH works. The die contains an internal counter which is initialized to a random count when the device is powered up. Each time a CBR REFRESH is performed, the device refreshes a row based on the counter, and then the counter is incremented. When CBR REFRESH is performed again, the next row is refreshed and the counter is incremented. The counter will automatically wrap and continue when it reaches the end of its count. There is no way to reset the counter. The user does not have to supply or keep track of row addresses.

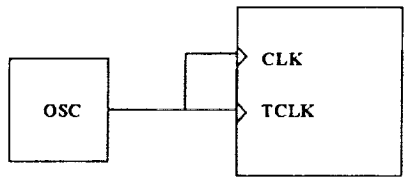
Since CBR REFRESH uses the internal counter and not an external address, the address buffers are powered down. For power-sensitive applications, this can be a benefit because there is no additional current used in switching address lines on a bus, nor will the DRAMs pull extra power if the address voltage is at an intermediate state.

Adapted from: Micron Technical Note TN-04-30: "Various Methods of DRAM Refresh."

IEEE JTAG 1149.1

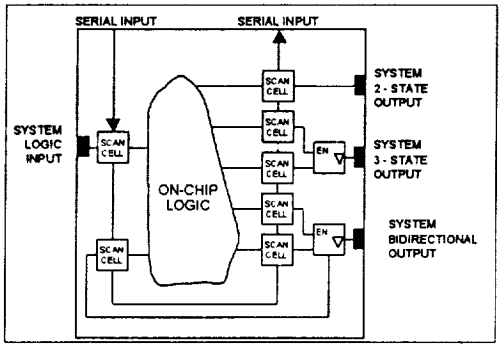


IEEE JTAG 1149.1 TCLK

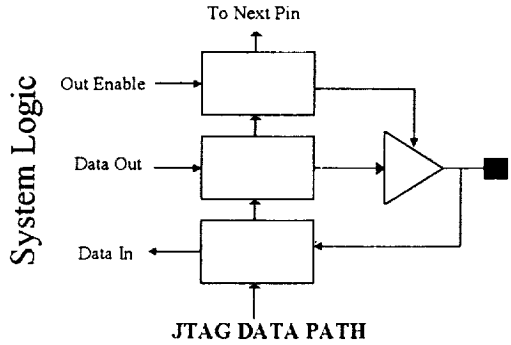


The CLK pin may turn into an output driving low, clamping the oscillator's output at a logic '0'. The TAP controller can not reset and restore I/O operation. Most FPGAs do not have the optional TRST* pin. Note TRST*, when present, has a pull-up

IEEE JTAG 1149.1 - Scan Path

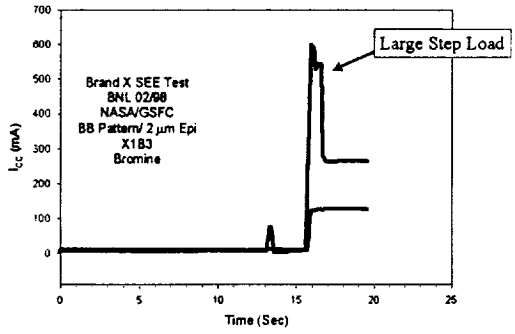


IEEE JTAG 1149.1 - Scan I/O Cell



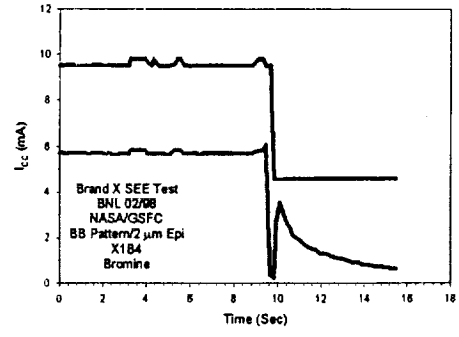
JTAG Upset Effect - Step Load

TCK and TMS=1 Not Guaranteed Solution

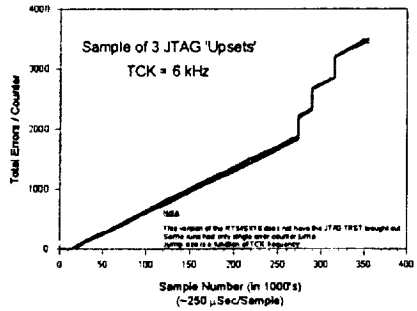


JTAG Upset Effect - Step Load

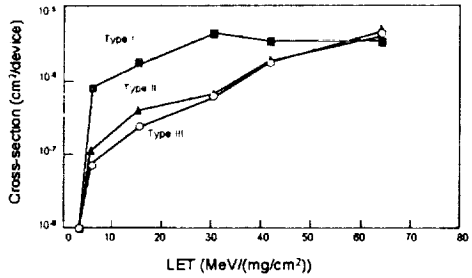
Second Distinct Failure Mode



JTAG Upset Effect - TCK On



SEE Results - Loss of Functionality
Atmel AT28C010 EEPROM, D/C 9706



"Single Event Functional Interrupt (SEFI) Sensitivity in EEPROMs," R. Koga, 1998 MAPLD International Conference, Greenbelt, MD.

Atmel AT28C010 EEPROM, D/C 9706
Type I Errors

- Manifested by the appearance of repeated errors, once the first error had been detected during ion irradiation. Here, the first error appeared at some point in time, which was tens of reading cycles ("cycle" is defined in Section II) after the exposure had started. Thereafter we observed one error every few cycles.
- Errors were altered bits in one word at various address locations.
- Simultaneously with the observation of the first error, the device bias current increased to 26 mA from 20 mA (normal, pre-error condition). The bias current continued to be 26 mA until the reading process stopped. At that time, the current became 0.2 mA (quiescent level).
- When the device was read again (without power-cycling), the bias current returned to 26 mA and errors appeared again (even without the beam).
- If the power to the device was shut off and re-started again (power-cycled), the device again functioned properly (i.e., no errors).
- In one instance we continued the irradiation without power-cycling for a long time, until the device no longer showed any errors. It appeared that the affected bit underwent additional upset, returning to the original polarity and thereby correcting the problem.

Atmel AT28C010 EEPROM, D/C 9706
Type II Errors

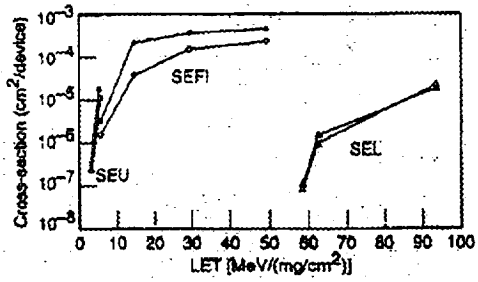
- Manifested by "00" in all address locations, once the first "00" was read.
- These errors could be removed only by power-cycling the device.

Atmel AT28C010 EEPROM, D/C 9706
Type III Errors

- Characterized by occasional errors in a byte, which appeared once in many cycles. There was no 'after-effect' for this type of error. In other words, one error appeared independently once in a while.
- Caused by an upset in the output buffer.

X28HC256 CMOS EEPROM
Xicore, D/C 9140

- Upset mode which also required the cycling of power to clear.

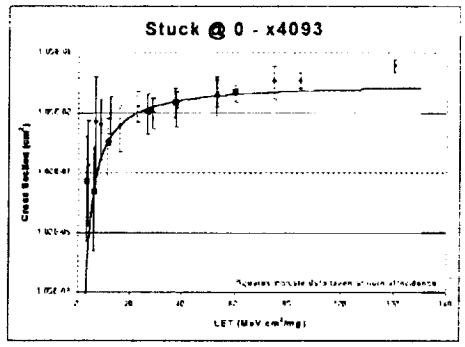


Loss of Functionality
Serial PROM

- Xilinx XQR1701L
  - 10% saturated intercept at LET=6 MeV-cm^2/mg, 1.2x10^{-5} cm^2/device

Reference: DS062 (v3.0) February 8, 2001.

XQR1701L

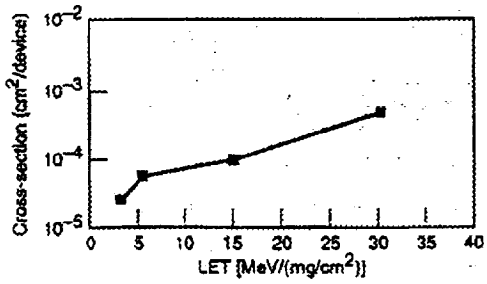


Loss of Functionality
Processors

- Processor simply stopped functioning without showing any observable bit errors.
- Noticed lockup in many microprocessors including MG80C186, MG80C286, and XC68302.
- Sensitivity to lockup was essentially independent of the test programs.

"Single Event Functional Interrupt (SEFI) Sensitivity in EEPROMs," R. Koga, 1998 MAPLD International Conference, Greenbelt, MD.

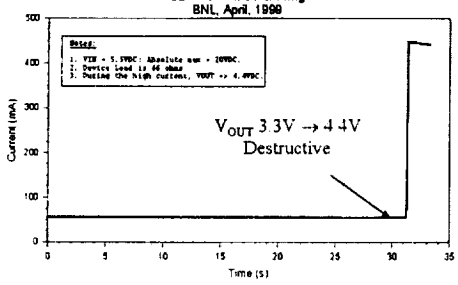
Loss of Functionality
Processors: XC68302 Example



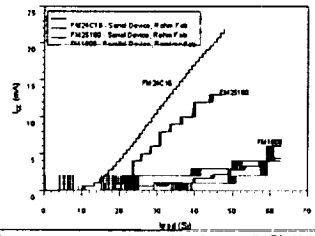
Miscellaneous

LVDO Regulator Failure

LM1117T-3.3 LVDO Heavy Ion Test
NASA/GSFC
S/N 3, Run I5
Iodine, 45 Degrees, 8.2 x 10^4 p/cm^2/sec
LET = 84.7 MeV-cm^2/mg
BNL, April, 1998



FRAM Memory Functionality Loss During Total Dose Test



In situ static current measurements of two serial and one parallel FRAM device types. This initial study showed that Rohm (serial) and Ramtron research fab (parallel) devices could withstand moderate doses without significant leakage currents. Post irradiation testing of the FM1608 showed that all devices catastrophically failed. Annealing did not help. In situ functional tests or a step irradiation method are needed for determination of the functional limit. The base CMOS process is not the limiting factor for the FM1608.

EDAC Techniques

EDAC Method	EDAC Capability
Parity	Single bit error detect
Cyclic Redundancy Check (CRC)	Detects if any errors have occurred in a given structure
Hamming Code	Single bit correct, double bit detect
Reed-Solomon Code	Corrects multiple and consecutive bytes in error
Convolutional Code	Corrects isolated burst noise in a communication stream
Overlying Protocol	Specific to each system. Example: retransmission protocol

From LaBel

Control-Error Protection Schemes

Protection Method	Capability
Watchdog Timer	If not reset within the designed interval, perform some function (usually a system reset).
Redundancy	Two equivalent systems operate on the same data. If the two systems disagree, a system reset is performed.
Lockstep	Two devices in a system are clocked simultaneously, and which are provided common inputs. If the devices disagree, perform a system reset.
Voting	Use three or more devices to perform the same function. If one device disagrees with the rest, use the remaining devices to determine the next system state.
Repetition	A system must provide the same data more than once to perform some action. Used, for instance, to lower the risk of an inadvertent spacecraft command being executed.

Definitions (1)

Single Event Upset (SEU) is a change of state or transient induced by an ionizing particle such as a cosmic ray or proton in a device. This may occur in digital, analog, and optical components or may have effects in surrounding circuitry. These are "soft" bit errors in that a reset or rewriting of the device causes normal behavior thereafter. A full SEU analysis considers the system effects of an upset. For example, a single bit flip, while not damaging to the circuitry involved, may damage the subsystem or system (i.e., initiating a pyrotechnic event).

Single Hard Error (SHE) is an SEU which causes a permanent change to the operation of a device. An example is a permanent stuck bit in a memory device.

Definitions (2)

Single Event Functional Interrupt (SEFI) is a condition where the device stops operating in its normal mode, and usually requires a power reset or other special sequence to resume normal operations. It is a special case of SEU changing an internal control signal. One example would be a DRAM entering the test mode defined by JEDEC. Another example is a microcircuit with IEEE 1149.1 JTAG circuitry leaving the TEST_LOGIC_RESET state and loading an unintended instruction into the instruction register (IR). Like other SEUs, the system effects must be properly analyzed. For example, a JTAG upset can cause the device to draw high currents or turn inputs into an output. The latter could, for example, drive a clock line to ground; thus, an independent clock signal should be used for the TCLK pin on devices without the optional TRST* pin.

Definitions (3)

Single Event Latchup (SEL) is a potentially destructive condition involving parasitic circuit elements forming a silicon controlled rectifier (SCR). In traditional SEL, the device current may destroy the device if not current limited and removed "in time." A "microlatch" is a subset of SEL where the device current remains below the maximum specified for the device. A removal of power to the device is required in all non-catastrophic SEL conditions in order to recover device operations.

Single Event Burnout (SEB) is a highly localized burnout of the drain-source in power MOSFETs. SEB is a destructive condition.

Definitions (4)

Single Event Gate Rupture (SEGR) is the burnout of a gate insulator in a power MOSFET. SEGR is a destructive condition.

Linear Energy Transfer (LET) is a measure of the energy transferred to the device per unit length as an ionizing particle travels through a material. The common unit is MeV-cm^2/mg of material (Si for MOS devices).

LET threshold (LET_{TH}) is the minimum LET to cause an effect. The JEDEC recommended definition is the first effect when the particle fluence = 10^7 ions/cm^2.

Definitions (5)

Cross section (sigma) is the device SEE response to ionizing radiation. For an experimental test for a specific LET, sigma = #errors/(ion fluence). The units for cross section are cm^2 per device or per bit.

Asymptotic or saturation cross section (sigmasat) is the value that the cross section approaches as LET gets very large.

Sensitive volume refers to the device volume affected by SEE-inducing radiation. The geometry of the sensitive volume is not easily known, but some information is gained from test cross section data.