ANALYSIS OF ALUMINUM-NITRIDE SOI FOR HIGH-TEMPERATURE ELECTRONICS

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Abstract

We use numerical simulation to investigate the high-temperature (up to 500K) operation of SOI MOSFETs with Aluminum-Nitride (AlN) buried insulators, rather than the conventional silicon-dioxide (SiO2). Because the thermal conductivity of AlN is about 100 times that of SiO2, AlN SOI should greatly reduce the often severe self-heating problem of conventional SOI, making SOI potentially suitable for high-temperature applications. A detailed electrothermal transport model is used in the simulations, and solved with a PDE solver called PROPHET. In this work, we compare the performance of AlN-based SOI with that of SiO2-based SOI and conventional MOSFETs. We find that AlN SOI does indeed remove the self-heating penalty of SOI. However, several device design trade-offs remain, which our simulations highlight.

1. Introduction

Silicon-on-insulator (SOI) technology has long promised to enable electronics operation at higher and lower temperatures than conventional MOSFETs, as well as lower power, smaller device sizes, and under much higher radiation exposure. Such "extreme" conditions can be common in spacecraft operation, making SOI a very interesting prospect for future spacecraft electronics. Considering high temperature requirements in particular, note that beyond the limitless thermal sink of Earth's atmosphere, spacecraft operation is a constant battle against temperature extremes to keep the onboard electronics (for control, communications, sensors, data storage, etc.) functioning. Figure 1 shows the temperature of a hypothetical black-body sphere versus distance from the Sun [1], indicating that high temperatures are inevitable for missions near the Sun. Even in Earth orbit, typical materials experience temperatures up to 400K. U.S. space shuttles leave their cargo bay doors open for the entire mission in order to vent heat.

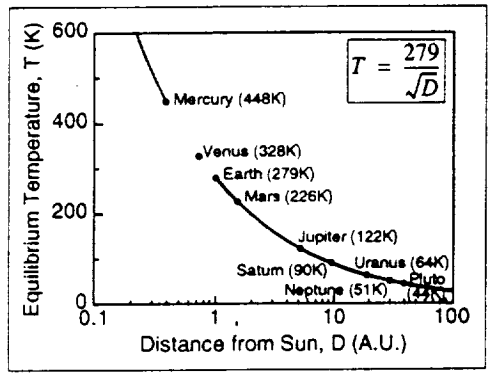

Figure 1. Equilibrium temperature of black-body sphere vs. distance from Sun [1]. Temperature increases rapidly inside orbit of Venus.

In spite of the promise of SOI to enable electronics operation at higher temperatures, the traditional buried insulator in SOI, silicon-dioxide (SiO2), traps heat from the operating device in the operating region (self-heating), degrading operation and reducing device lifetime (Figure 2b). Thus, in spite of its many potential advantages over conventional MOSFET electronics (Figure 2a), SOI has not been a serious contender for spacecraft electronics, which must be absolutely reliable. Recent experiments [2] indicate that aluminum-nitride (AlN) can be used for the SOI buried insulator. The thermal conductivity of AlN is about 100 times that of SiO2 (136 W/m·K versus 1.4 W/m·K) and roughly equal to that of silicon itself (145 W/m·K). Thus, using AlN as the buried insulator should essentially eliminate the self-heating penalty of SOI (Figure 2c). AlN SOI might be beneficial not only for general space mission electronics, but also for high-temperature missions.

To investigate AlN for high-temperature applications, we implemented a detailed electrothermal model of electronics operation in a PDE solver called PROPHET [3], as described in Section 2 of this paper.

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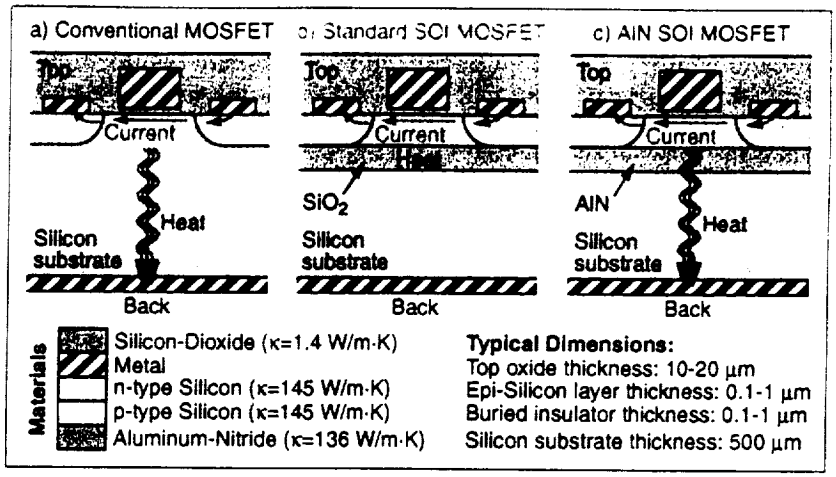

Figure 2. a) Conventional MOSFET. Silicon-dioxide (SiO_2) covers the top of the wafer as a dielectric between metal interconnect lines. Due to the low thermal conductivity of SiO_2, the back side of the integrated circuit is the main sink for heat generated by device operation. **b)** Conventional SOI, with SiO_2 buried insulator. Heat generated by device operation is trapped in the active region. **c)** Proposed SOI, with AlN buried insulator. The high thermal conductivity of AlN (roughly equal to that of silicon) allows heat to escape to the back-side heat sink.

Using this model, we performed extensive numerical simulations comparing the high-temperature (up to 500K) operation of conventional MOSFETs, standard SOI (with SiO_2 buried insulator), and AlN SOI. Results and discussion of these simulations are presented in Section 3. Section 4 summarizes our conclusions from this investigation about the suitability of AlN SOI for high-temperature electronics applications.

2. Electrothermal Model

The basic model of electronic device operation include the Poisson equation and the electron and hole continuity equations:

$$\nabla \cdot (\varepsilon \nabla \psi) = -q(p - n + N) \tag{1}$$

$$\frac{\partial n}{\partial t} = \nabla \cdot [D_n \nabla n - n\mu_n \nabla \psi] - R \tag{2}$$

$$\frac{\partial p}{\partial t} = \nabla \cdot [D_p \nabla p + p\mu_p \nabla \psi] - R \tag{3}$$

where ψ is the electrostatic potential, n and p are the electron and hole densities, N is the net fixed charge (ionized dopant) density, and R is the electron-hole recombination rate. Material and physical parameters include permittivity ε, electron charge q, electron and hole diffusivities D_n and D_p, and electron and hole mobilities μ_n and μ_p. For the recombination rate R, we included only Shockley-Reed-Hall recombination-generation, such that:

$$R = \frac{np - n_i^2}{\tau_p(n - n_i) + \tau_n(p - n_i)} \tag{4}$$

where n_i is the intrinsic carrier concentration of the material, and τ_n and τ_p are the electron and hole recombination lifetimes.

The full electrothermal model adds the thermal generation and diffusion equation to the basic device equations (1)-(3):

$$C_L \frac{\partial T_L}{\partial t} = \nabla \cdot (\kappa \nabla T_L) + \boldsymbol{J} \bullet \boldsymbol{E} \tag{5}$$

where T_L is the lattice temperature, $\boldsymbol{J}$ is the total (electron and hole) current density, $\boldsymbol{E}$ is the electrostatic field. Parameters include the specific heat C_L and the thermal conductivity κ of the material.

We used Scharfetter-Gummel discretization [4] for the continuity equations and Maxwell-Boltzmann statistics for the carrier energy distribution. [A few test simulations showed that Fermi-Dirac statistics, while quantitatively more accurate, gave qualitatively identical results in this case.] Our electrothermal model [5] includes temperature dependencies for all material parameters, including carrier diffusivities, mobilities, and lifetimes, thermal diffusivity, and intrinsic carrier concentration. Simulations reported in this paper were all for devices operating in the steady-state, so all time derivatives were zero. For this investigation, we ignored bandgap narrowing and carrier velocity saturation. However, the mobility model included impurity scattering (doping dependence).

Our electrothermal model was implemented in a partial differential equation solver called PROPHET [3]. The main feature of PROPHET is rapid prototyping: the ability to specify and modify a model at a high level, without ever writing, debugging, or modifying the low-level gridding, discretization, data handling, and solver code (Figure 3). [Relatively simple operator routines must sometimes be written, however.] The ability to modify a model without programming is especially important for complex models such as the electrothermal model used in this work, where investigation of variations of the model is a significant part of the research. In fact, PROPHET allows device models, material parameters, and arbitrarily complex simulation sequences to be defined *in the run-time input script*. Other benefits of PROPEHT include the ability to switch from simple to more complex models in order to concentrate computing power on operating regions of interest, and the ability to gradually phase in numerically problematic PDE terms in order to achieve solution convergence.

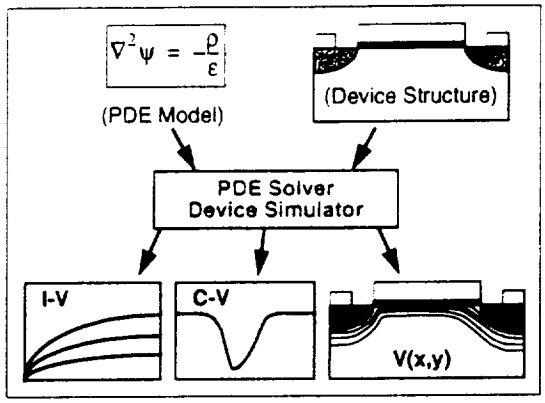

Figure 3. PDE-solver based electronic device simulator. Only the system of PDEs describing the device physics and the device structure need to be specified. Ideally no programming is required.

Before describing our simulation results, we need to quantify the device structures investigated. As indicated earlier, every simulation was repeated for three devices: a conventional MOSFET, an SiO_2 SOI MOSFET, and an AlN SOI MOSFET, as shown in Figure 2. These devices were identical except for the buried insulator, which was replaced with an equal thickness of silicon for the non-SOI simulations. Two device sizes were simulated, a long-channel MOSFET and a short-channel MOSFET, the details of which are given in Table 1. The source and drain had abrupt box doping profiles at $10^{20}/cm^3$ n-type, extending to the buried insulator in the SOI devices, while the substrate was doped at $5x10^{15}/cm^3$ p-type. Figure 4 shows the assumed device structures as well as the biasing arrangement.

Table 1: MOSFETs Simulated

Device Parameter	Long-Channel MOSFET	Short-Channel MOSFET
Channel Length	2500 nm (2.5 μm)	250 nm
Gate oxide thickness	10 nm	4 nm
SOI epitaxial silicon (epi-Si) thickness	200 nm	50 nm
SOI epitaxial layer doping	$10^{17}/cm^3$ p-type	$10^{17}/cm^3$ p-type
SOI buried insulator layer thickness	600 nm	200 nm
Total simulation region size	5 μm x 5 μm	5 μm x 5 μm
Maximum gate/drain voltage	10 V	3 V

Finally, some simulation details merit mention. SInce the simulation region was only 5 μm square, the thermal conductivity of the substrate layer was decreased by a factor of 100 to approximate the thermal resistance of a typical 500 μm thick silicon chip. In initial simulations, we found that the electrothermal model would not converge without a thermal contact on the top side of the simulation region. We therefore made the source and drain thermal (as well as electrical) contacts. Since the top side does pass

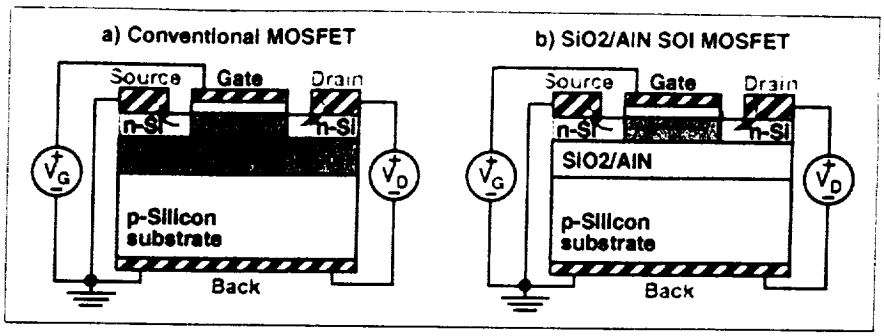

Figure 4. a) Conventional MOSFET and **b)** SOI MOSFET device structures simulated with biasing set-up. Thermal contacts are indicated by red lettering. Two device sizes were simulated: a 2.5 μm long-channel device, and a 250 nm short-channel device. To approximate a 500 μm thick wafer, the thermal conductivity of the substrate layer was specified as 0.01 times that of silicon.

some heat to the environment, having these top-side contacts seems reasonable anyway. We note that these simulations also predict the worst case thermal heating: steady-state. In a real circuit, spatial and temporal averaging would mitigate this heating extreme. Concerning solution grid sizes, we used about 3600 nodes for the long-channel devices and about 2600 for the short-channel devices. Typical computation times were 1-2 hours for a 200-point I-V curve simulation on a Sun Ultra II workstation.

3. Results and Discussion

Our investigation of the high-temperature AlN SOI (in comparison to conventional MOSFETs and SOI) involved the simulation of three operation regimes: OFF (drain leakage), turn-on (subthreshold), and ON (high-current). Results of these simulations are presented in the following three subsections. Throughout this section, the conventional MOSFET is indicated as "MOS" in text and with black curves in plots, the SiO_2 SOI device is indicated with "SiO_2" and red, and the AlN SOI device is indicated with "AlN" and green.

3.1. Drain Leakage Simulation

To simulate drain leakage current in the OFF state, gate bias V_G was held at 0V, and the drain bias was ramped up to full (10V for the long channel devices and 3V for the short-channel devices). This operating regime tests how well the device stays OFF (low drain current), in spite of a large drain bias. For this operating region, we can make a few predictions:

- Self-heating will be irrelevant, since current (and thus heat generation) will be very low. Thus, the SiO_2 and AlN SOI results should be virtually identical.
- Leakage current due to electron-hole pair (EHP) generation in the source and drain p-n junction depletion regions will be larger in the MOS device, since it has much larger depletion regions.
- Drain-induced barrier lowering (DIBL - drain depletion region extends near that of the source) should be the same for all the devices of a given size, since the doping profiles from source to drain are identical.Further, DIBL should be small, since channel doping is high enough to keep the drain depletion region from extending near the source.

Drain leakage current simulation results are shown in Figure 5. Figure 5a shows the long-channel results, which are exactly as predicted above. However, Figure 5b for the short-channel device seems to violate all of the above predictions - the SiO_2 and AlN results are widely different, MOS leakage is lower than SOI, and DIBL is different between the three devices and relatively high for the AlN device. The reason for these results is indicated in Figure 5c, which compares the 2-D potential profiles in the MOS and AlN devices at 300K and V_D=3V. [The 300K results were compared since they illuminate the cause of the short-channel results most clearly.] The potential plot shows that the barrier to electron flow between source and drain (indicated by blue), is much higher in the MOS device than in the AlN (and SiO_2) SOI device. A reduced channel barrier and higher leakage current are classic signs of the floating-body problem of fully-depleted (FD) SOI devices. We can now conclude the following:

- The long-channel SOI devices simulated are partially-depleted (PD). That is, the channel depletion layer extends only part way through the epi-Si layer towards the buried insulator. As a result, PD SOI devices operate in many respects like a conventional MOSFET. The leakage current predictions above only apply to this type of SOI device.

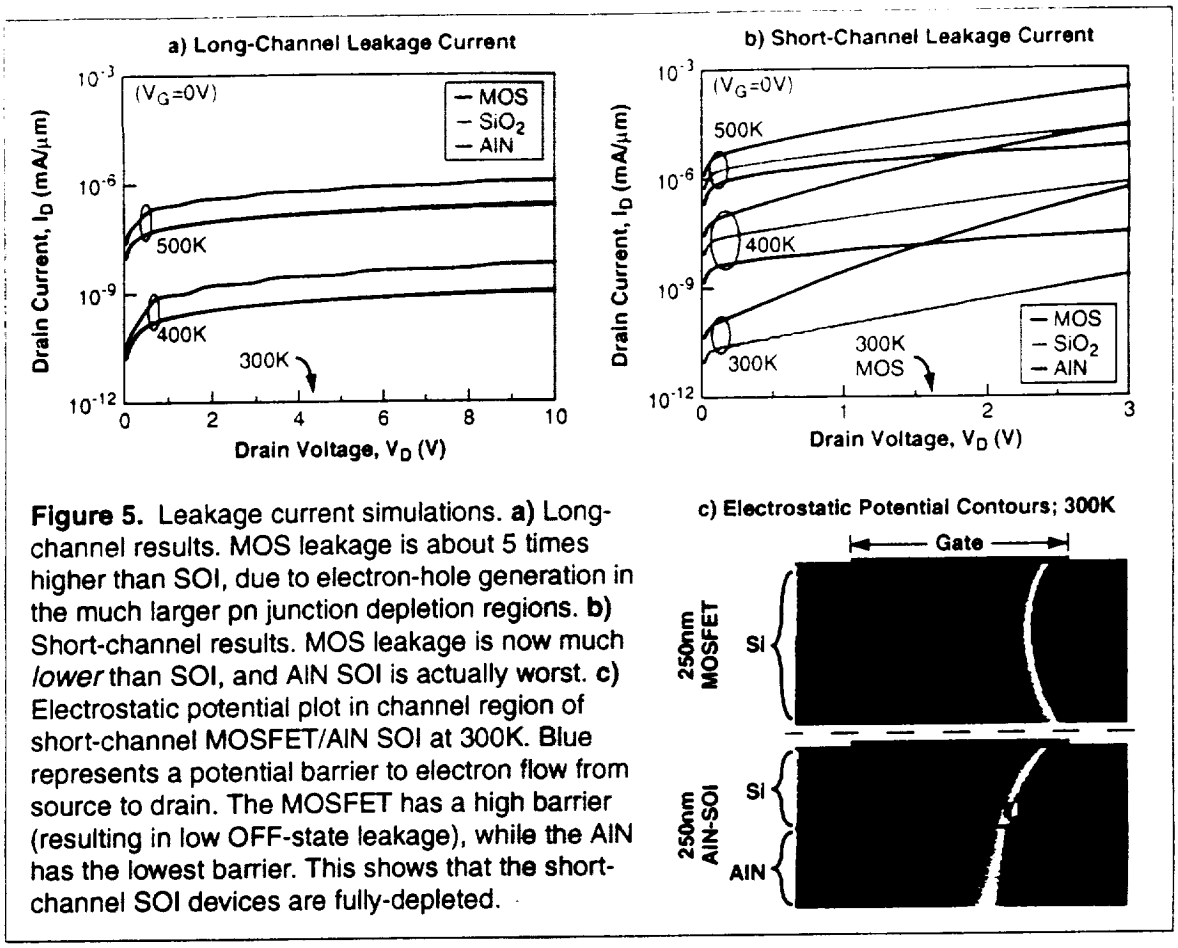

Figure 5. Leakage current simulations. **a)** Long-channel results. MOS leakage is about 5 times higher than SOI, due to electron-hole generation in the much larger pn junction depletion regions. **b)** Short-channel results. MOS leakage is now much *lower* than SOI, and AlN SOI is actually worst. **c)** Electrostatic potential plot in channel region of short-channel MOSFET/AlN SOI at 300K. Blue represents a potential barrier to electron flow from source to drain. The MOSFET has a high barrier (resulting in low OFF-state leakage), while the AlN has the lowest barrier. This shows that the short-channel SOI devices are fully-depleted.

- The epi-Si layer of the short-channel SOI devices is fully-depleted, even at V_G=0V. That means that the drain depletion region is able to punch through to affect the source-channel energy barrier, with the resulting observed DIBL. The lowest barrier, and most of the leakage current flow, are at the epi-Si/buried insulator interface, as indicated in Figure 5c.
- The higher leakage current of the AlN device results from a lower barrier to electron flow compared to that in the SiO_2 SOI device. The cause of the difference will be made clear in Section 3.2. We will evaluate at the end of Section 3.3 whether the leakage current of the AlN device at 500K is high enough to threaten proper operation of the device.

The results in this section show that there are potential advantages and disadvantages of fully-depleted SOI. However, there are advantages of properly-designed FD SOI over PD SOI, especially for sub-micron devices [6]. We have not attempted to in this work to optimize the design of either the long-channel PD SOI device or the short-channel FD SOI device.

3.2. Subthreshold Simulation

The subthreshold operating regime is simulated by ramping the gate voltage while holding the drain bias at a low value. For both long-channel and short-channel devices, we used V_D=0.1V. This operating regime tests how quickly the increasing gate bias turns on the device (increases drain current). Again, we make a few predictions of the expected device operation, although we now know that the operation of the FD short-channel SOI devices may be more complicated.

- Once again, self-heating will be irrelevant, in this case because drain bias (and thus heat generation) is small. Thus, the SiO2 and AlN SOI results should be virtually identical.
- For the PD SOI, the operation should be virtually identical to that of the MOSFET, since the buried insulator does not affect the activity in the surface inversion layer.

- For the FD SOI, it is difficult to predict the effect of the buried insulator on the electron inversion layer as the gate bias increases.

Subthreshold current simulation results are shown in Figure 6. Once again, the results for the long-channel devices are as predicted. Note that the higher current of the MOS device near V_G=0V is due to its higher leakage current, as found in Section 3.1. Once again, the short-channel results are surprising. This time, rather than both SOI devices being worse than MOS, one is worse (AlN SOI has a *higher* subthreshold slope), and the other is better (SiO_2 SOI has a *lower* subthreshold slope). These results are consistent over the full simulated temperature range from 300K to 500K.

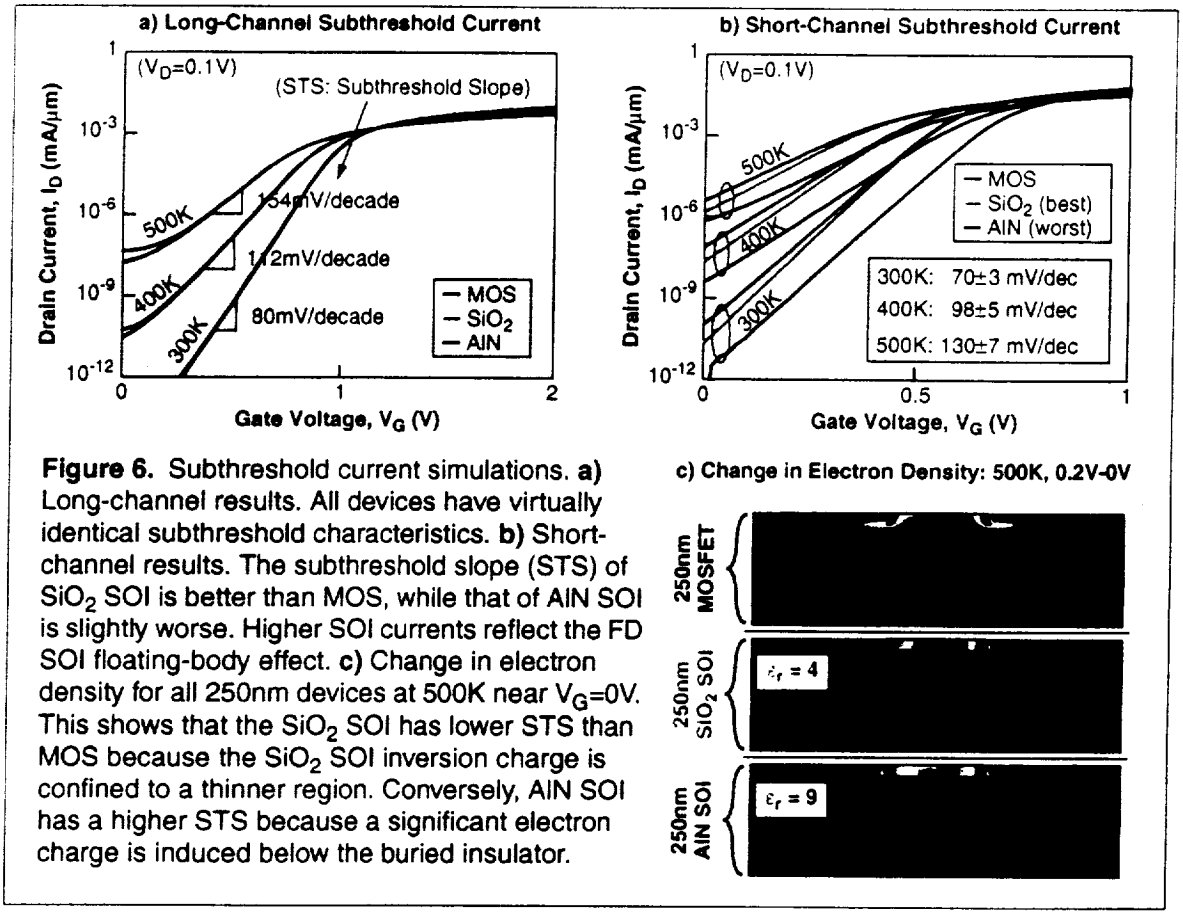

Figure 6. Subthreshold current simulations. **a)** Long-channel results. All devices have virtually identical subthreshold characteristics. **b)** Short-channel results. The subthreshold slope (STS) of SiO_2 SOI is better than MOS, while that of AlN SOI is slightly worse. Higher SOI currents reflect the FD SOI floating-body effect. **c)** Change in electron density for all 250nm devices at 500K near V_G=0V. This shows that the SiO_2 SOI has lower STS than MOS because the SiO_2 SOI inversion charge is confined to a thinner region. Conversely, AlN SOI has a higher STS because a significant electron charge is induced below the buried insulator.

To clarify the cause of these short-channel device results, note the in the subthreshold region, we are concerned about how effectively an increasing gate bias turns on the drain current. With drain bias fixed, the only thing the gate bias can do is increase the channel inversion charge. Thus, the definitive reason for differing subthreshold effects can be obtained by comparing where and how much the electron density increases in the channel for a given gate bias change. This is plotted in Figure 6c. Here we see that the SiO_2 SOI device improves on the MOS device because its inversion charge increase is confined to the epi-Si layer (with a small electron build-up below the buried insulator), while the MOS device inversion layer extends deeper into the substrate. The further from the gate that the inversion charge is, the less inversion charge will be needed to accommodate an increase in gate bias. In contrast, in the AlN SOI device, a significant portion of the gate bias is accommodated by charge beneath the buried insulator. Thus, there is less inversion charge in the epi-Si active layer to contribute to drain current.

What is the reason for the SiO_2/AlN SOI difference, when their device structures and doping densities are identical? As indicated in Figure 6c, the crucial difference, which manifests itself both in subthreshold and in the leakage current simulations of Figure 5b, is a result of the different dielectric constants of the two buried insulators. In particular, the higher permittivity of AlN as compared to SiO_2 means that electric fields penetrate the AlN layer with much less attenuation than for the same thickness of SiO_2. Thus,

more of any change gate potential is dropped in the substrate in AlN SOI than in SiO_2 SOI, with correspondingly less change in potential in the epi-Si layer where it would increase inversion charge. Alternatively, consider the SOI structure is as two parallel plate capacitors in series. To maximize the effectiveness of the gate bias to increase electron density in the epi-Si layer, the gate oxide capacitance should be much larger than the buried insulator capacitance. Since parallel plate capacitance is proportional to the dielectric constant of the intervening material, the capacitance of the AlN capacitor is greater than that of the SiO_2 buried insulator capacitor. The apparent solution for improving the performance of AlN SOI is now clear - increase the thickness of the AlN layer. This decreases the capacitance of this layer, forcing more of the gate potential to be felt in the epi-Si layer.

3.3. High Current Simulation

For the n-channel MOSFETs used in this study, high-current operation (device ON) is achieved with large positive gate and drain biases. For this simulation, the gate bias was held at its full ON value, while the drain bias was ramped from 0V to full bias. The predictions for device operation in this case are straight-forward:

- SInce both current and drain bias are high, thermal generation will be large in the device active layer. Thus, SiO_2 SOI should show significant self-heating effects, including high channel temperature, degraded current and mobility, and strong negative differential conductance (NDC).
- MOS and AlN SOI should have much lower self-heating effects, but similar to each other. They may still display moderate NDC.

Figure 7 shows the high-current simulation results. As shown in Figures 7a and 7b, both long-channel and short-channel simulation results were as expected, since self-heating is the dominant effect in these simulations. Note that self-heating was so strong in the SiO_2 SOI device that all but one of the simulations did not complete the current-voltage trace to full drain bias - NDC effects rendered the system of equations non-convergent. To demonstrate self-heating more clearly, Figures 7c, 7d, and 7e show, for the long-channel devices at T_{env}=500K and V_D=10V, the channel mobility, vertical temperature profile through the channel center, and a 2-D temperature plot of the channel region. Each of these show dramatically how strong self-heating effects are in the SIO_2 SOI device. The self-heating difference was even more dramatic in the short-channel devices: peak temperature of almost 1000K for SiO_2 SOI, but only device, while the maximum was under 630K for AlN. The SiO_2 device would surely melt itself before reaching such high temperatures. On the other hand, it is quite conceivable to use materials suitable for integrated circuit operation with internal temperatures just above 600K, as in the AlN devices operating in a 500K environment.

Before concluding, we return to a question raised in Section 3.1: Is the short-channel, AlN leakage current at 500K too high? The answer is yes if leakage is an appreciable fraction of the full ON current. Comparing the appropriate curves in Figures 5b and 7b, we see that even the highest leakage current is still almost 4 orders of magnitude smaller than the ON current, so the high AlN leakage is not a practical concern. We note that the leakage current is also too small to cause any appreciable self-heating.

4. Conclusions

With detailed electrothermal simulations, we showed the significant self-heating effects of conventional SOI, including high channel temperature, degraded current and mobility, and strong negative differential conductance (NDC). We showed that AlN SOI removes the self-heating penalty of SOI, allowing AlN SOI to function in a 500K environment. While partially-depleted SOI has lower drain leakage current than conventional MOSFETs, fully-depleted (FD) SOI has advantages for short-channel devices. However, FD SOI requires care is choosing the epitaxial silicon layer thickness and doping as well as the buried insulator thickness to maintain drain leakage at acceptable levels and to optimize turn-on characteristics. AlN-based SOI requires additional attention, due to the higher dielectric constant of this material compared to SiO_2. We expect that a thicker buried insulator, as compared to SiO_2-based SOI, will allow AlN SOI to maintain good operation in high-temperature applications and in general.

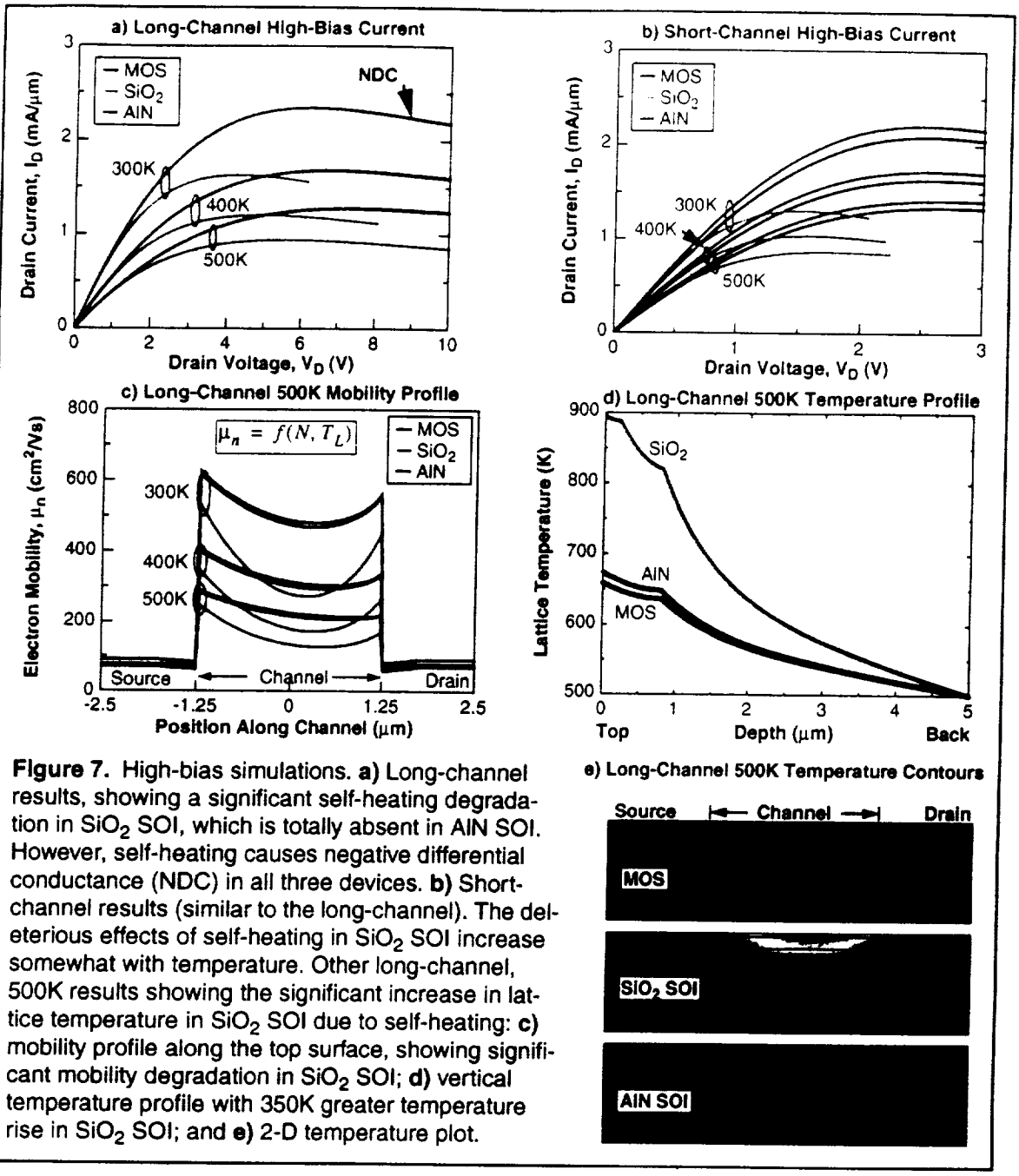

Figure 7. High-bias simulations. **a)** Long-channel results, showing a significant self-heating degradation in SiO_2 SOI, which is totally absent in AlN SOI. However, self-heating causes negative differential conductance (NDC) in all three devices. **b)** Short-channel results (similar to the long-channel). The deleterious effects of self-heating in SiO_2 SOI increase somewhat with temperature. Other long-channel, 500K results showing the significant increase in lattice temperature in SiO_2 SOI due to self-heating: **c)** mobility profile along the top surface, showing significant mobility degradation in SiO_2 SOI; **d)** vertical temperature profile with 350K greater temperature rise in SiO_2 SOI; and **e)** 2-D temperature plot.

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