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Low Temperature Testing of a Radiation Hardened CMOS 8-Bit Flash Analog-to-Digital (A/D) Converter

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ABSTRACT

Power processing electronic systems, data acquiring probes, and signal conditioning circuits are required to operate reliably under harsh environments in many of NASA's missions. The environment of the space mission as well as the operational requirements of some of the electronic systems, such as infrared-based satellite or telescopic observation stations where cryogenics are involved, dictate the utilization of electronics that can operate efficiently and reliably at low temperatures. In this work, radiation-hard CMOS 8-bit flash A/D converters were characterized in terms of voltage conversion and offset in the temperature range of +25 °C to –190 °C. Static and dynamic supply currents, ladder resistance, and gain and offset errors were also obtained in the temperature range of +125 °C to –190 °C. The effect of thermal cycling on these properties for a total of ten cycles between +80 °C and –150 °C was also determined. The experimental procedure along with the data obtained are reported and discussed in this paper.

INTRODUCTION

Certain NASA deep space missions may require electronic components that encounter temperatures well below their minimum manufacturer's specified operating temperature (–55°C for military parts). Presently, spacecraft operating in the cold environment of deep space carry radioisotope heating units to maintain the on-board electronics at a temperature of approximately 25 °C.[1] The radioisotope heating units, however, require active thermal control system management, are expensive, and require elaborate containment structures. In addition to the environment of deep space and planetary exploration, extreme low temperatures are encountered in applications such as infrared-based satellite systems and Next Generation Space Telescope (NGST).[2] In some of these systems, electronic sensors and detector arrays are required to operate at cryogenic temperatures in order to reduce background thermal noise. In addition to detectors and sensors, these electronic systems employ a vast variety of integrated circuits and devices such as A/D and D/A converters, multiplexing and de-multiplexing chips, and solar-based circuits. Electronics circuits and systems, which are capable of operation at cryogenic temperatures, are, therefore, needed in order to meet the requirements of NASA space missions and commercial ventures. Low temperature electronics will not only tolerate the hostile environment of deep space but also reduce system size and weight by eliminating radioisotope

heating units or any thermal control measures and associated structures; thereby reducing system development and launch costs, improving reliability and lifetime, and increasing energy densities.

A radiation hardened CMOS 8-bit flash A/D converter is an attractive candidate device for future NASA deep space missions that require a significant level of radiation tolerance. This particular device has been considered by the Jet Propulsion Laboratory (JPL) for potential use on the MUSES CN (Mu Space Engineering Spacecraft) NASA/Japanese mission to Asteroid Nereus.[3] The purpose of this investigation was to determine the A/D converter suitability for use in a low temperature environment. In this work, radiation-hard CMOS 8-bit flash A/D converters were characterized in terms of their performance in the temperature range of +25 °C to −190 °C. The testing activities were performed at the Low Temperature Electronics Facility at the NASA Glenn Research Center and at a contractor facility.

The in-house test activities included voltage conversion, offset voltage, and ladder resistance measurements as a function of temperature. The 8-bit flash A/D converter was tested at a clock rate of 1 MHz. For simplification, only DC values from 0 to 4V (test vector) were applied to the analog input of the converter. For each DC analog input value, the A/D converter produced an effective output bit pattern in binary format that was monitored by a logic analyzer. The experimental test setup and the device layout are shown in Figure 1. Testing of the A/D converter was performed in a chamber whose temperature was controlled using liquid nitrogen as the coolant at a ramp rate of 10 °C per minute. The test started at room temperature and was taken in steps down to −190 °C. At each temperature the device was allowed to soak for 20 minutes in order to reach thermal stability or equilibrium. At each temperature, a test vector was applied to the input of the A/D and the corresponding digital output was recorded.

The static and dynamic supply currents, ladder resistance, gain and offset error measurements were performed in the temperature range of +125 °C to −190 °C. Thermal cycling activities were also performed between +80 °C to −150 °C. All these tests, which comprised characterization of a total of four devices, were carried out at a contractor facility. The results are presented and discussed in this paper.

EXPERIMENTAL RESULTS

The CMOS 8-bit A/D converter was designed for space applications where relatively low power, exceptional accuracy, and very fast conversion speeds were necessary. This radiation-hard A/D converter was tested at a clock rate of 1 MHz. For simplification, the device's enable pins CE1 and CE2 were set for valid data on B8 through B1. In addition, only DC input values were applied to the input (Vin). For each DC input value, the converter produced an effective output pattern (B8 through B1) in binary format. Table I shows the corresponding binary value for each of the 8-bits. With a reference voltage of 4.012V, the A/D converter has a 15.3 mV per bit measurement resolution.

The output voltage of the converter was obtained as a function of the input voltage in the temperature range of +25 °C to −190 °C. The values of the output voltage, in binary as well as decimal format, corresponding to an input voltage variation from about zero to 4 volts are listed at the two extreme temperatures, i.e. +25 °C and −190 °C, in Tables II and III, respectively. In general, the measured output voltage tracked the input voltage quite well. For example, the average offset voltage at room temperature (25 °C) and at −190 °C was 34 and 24mV, respectively. This means that the 8-bit flash A/D converter is able to track the input voltage within about 2 bits. The offset voltage exhibited by the device over the temperature range is plotted in Figure 2. The deviations of about 20 to 40 mV within this temperature range are well within the overall error of the inaccuracies of the test setup. These errors can be attributed to factors inherent to the device, instrumentation error, and circuit layout. It is important to note that although the data presented in Tables II and III pertain to only the extreme test temperatures, the performance of the device was similar throughout the test temperature range of +25 °C to −190 °C.

The performance of four A/D converter devices was obtained over both hot and cold temperature ranges, i.e. from +25 °C to +125 °C and from +25 °C to −190 °C. The properties investigated included: dynamic supply current (IDDD), clock low static supply current (IDDS), clock high static

supply current (IDDH), ladder resistance (Lad Res), and gain and offset (Vos) errors.

Table IV lists the properties of the four devices investigated at temperatures of 25, 80, 100, and 125 °C. It can be seen that, at a given test temperature, all investigated properties of the four devices remained within their specifications.

Test results for six parameters measured at low temperatures from –55 °C to –190 °C are listed in Table V. The Vos and gain errors were measured only at –55 °C. Testing of the converter at lower temperatures necessitated the development of a special test fixture, which utilized long wires to provide connections between the instrumentation and the device under test. These wires introduced excessive noise that had detrimental effects on the accurate measurement of low-level signals, such as Vos, Gain Error, and to determine linearity behavior.

Table V shows that, while the dynamic supply current (IDDD) was the only parameter that remained within its specification to –190 °C even though its drift increased with decrease in temperature, the other parameters, i.e. IDDH and IDDS (static supply currents) and ladder resistance moved outside their specification limits at and below –120 °C. The out-of-specification values are shaded in Table V. Test results for four devices were slightly different, but they showed very similar trends with decrease in temperature.

A number of functional tests were performed in-house to determine if the drift in the parameters was real and whether the drift influenced the functionality of the converter. These tests involved measurement of the ladder resistance in the temperature range of +25 °C to –190 °C, while the voltage conversion was also monitored. As an example, the values obtained for the ladder resistance and the converted output for a 2.75 V input are listed in Table VI for this temperature range. It can be clearly seen that the trend of decreasing ladder resistance with temperature was similar to that obtained for devices evaluated at the contractor facilities (see Table V). As temperature was varied, the voltage conversion remained consistent. The 8-bit flash A/D converter functioned well even with a decrease in operating temperature, although ladder resistance drifted to values outside of manufacturer's specifications.

The effect of thermal cycling on the A/D converter was investigated by exposing the A/D converter to a total of ten thermal cycles. Two of the four devices were thermally cycled between –150 °C and +80 °C at a rate of 5 °C per minute with dwell times of 20 minutes. After completion of ten thermal cycles, parameters were measured at the two extreme cycling temperatures, i.e. –150 °C and +80 °C. The device parameter values at these two temperatures prior to and after ten cycles are shown in Table VII. As before, only four parameters were measured. At both low and high temperatures, the four parameters were in good agreement before and after ten thermal cycle exposures.

CONCLUSIONS

A radiation hardened CMOS 8-bit flash A/D converter, which is an attractive candidate device for future NASA deep space missions requiring a significant level of radiation tolerance, has been investigated for suitability for use in a low temperature environment. The A/D converters were characterized in terms of their performance in the temperature range of +125 °C to –190 °C. Properties investigated included static and dynamic supply currents, ladder resistance, and gain and offset errors. The effect of thermal cycling for a total of ten cycles on these properties was also determined.

Room temperature results have shown that the 8-bit flash A/D converter was able to track the input voltage with an average of 34 mV or about 2 bits. This error, which was well within the overall error of the inaccuracies of the test setup, was the largest error measured for the converter over the temperature range of +25 °C to –190 °C. These preliminary test results have also shown that the A/D converter may be considered as a potential candidate for operation at low temperatures down to –190 °C, well below the manufacturer's minimum specified operating temperature. Although, the converter survived and maintained good operation after a total of ten thermal cycles at extreme temperatures, more comprehensive testing is, however, required to fully-characterize its performance and to determine its suitability for low temperature space missions and commercial applications.

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[2]. R. Patterson, A. Hammoud, J. Dickman, S. Gerber and E. Overton, "Development of Electronics for Low Temperature Space Missions," 4th European Workshop on Low Temperature Electronics, Noordwijk, the Netherlands, 21-23 June 2000.

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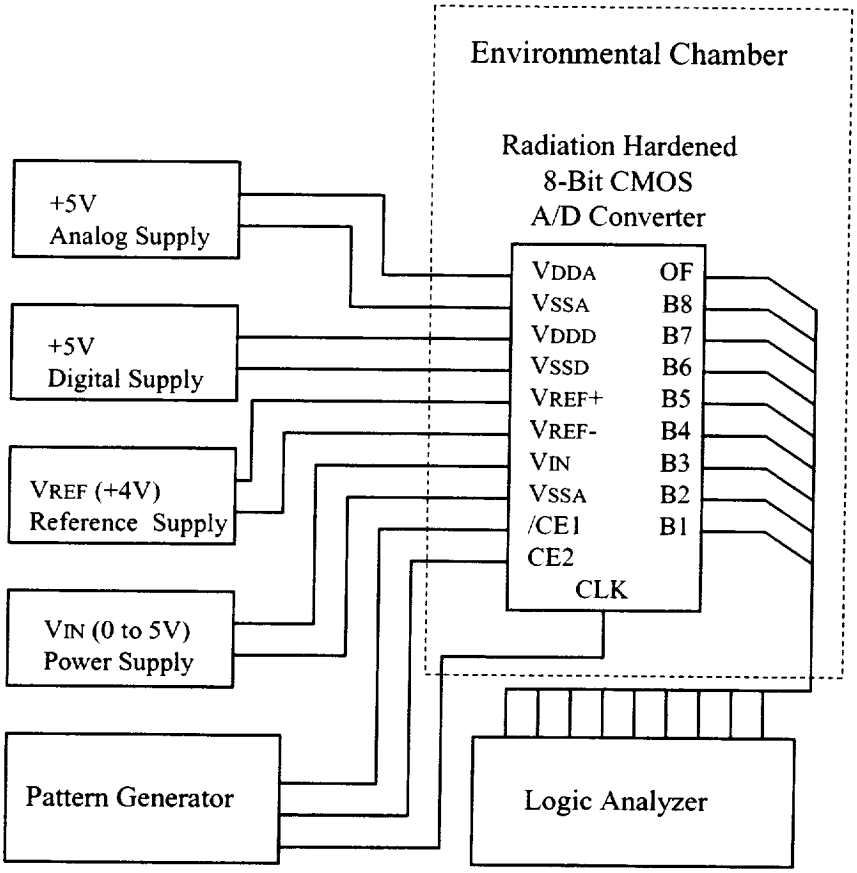

Figure 1. Test Setup for Radiation Hardened 8-Bit CMOS A/D Converter.

Table I. Binary coding.

A/D outputs	B8	B7	B6	B5	B4	B3	B2	B1	
Binary value	128	64	32	16	8	4	2	1	Total 255 bits

Table II. Voltage conversion at test temperature of 25 °C

Vin	OF	B8	B7	B6	B5	B4	B3	B2	B1	Binary Vout	Decimal Vout (V)	Δ Vout -Vin (offset) (V)
-0.06	0	0	0	0	0	0	0	0	0	0	0	0.06
1.00	0	0	1	0	0	0	0	0	1	65	1.02	0.02
2.00	0	1	0	0	0	0	0	0	1	129	2.03	0.03
2.50	0	1	0	1	0	0	0	0	1	161	2.53	0.03
2.75	0	1	0	1	1	0	0	0	1	177	2.78	0.03
2.99	0	1	1	0	0	0	0	0	0	192	3.02	0.03
3.97	0	1	1	1	1	1	1	1	1	255	4.01	0.04
4.00	1	1	1	1	1	1	1	1	1	overflow	overflow	average offset = 0.034

Table III. Voltage conversion at test temperature of -190 °C

Vin	OF	B8	B7	B6	B5	B4	B3	B2	B1	Binary Vout	Decimal Vout (V)	Δ Vout -Vin (offset) (V)
-0.04	0	0	0	0	0	0	0	0	0	0	0	0.00
0.21	0	0	0	0	0	1	1	1	0	14	0.22	0.01
1.00	0	0	1	0	0	0	0	0	1	65	1.02	0.02
2.00	0	1	0	0	0	0	0	0	1	129	2.03	0.03
2.41	0	1	0	0	1	1	0	1	1	155	2.44	0.03
2.42	0	1	0	0	1	1	1	0	0	156	2.45	0.03
2.75	0	1	0	1	1	0	0	0	1	177	2.78	0.03
2.99	0	1	1	0	0	0	0	0	0	192	3.02	0.03
3.97	0	1	1	1	1	1	1	1	1	255	4.01	0.04
3.99	1	1	1	1	1	1	1	1	1	overflow	overflow	average offset = 0.024

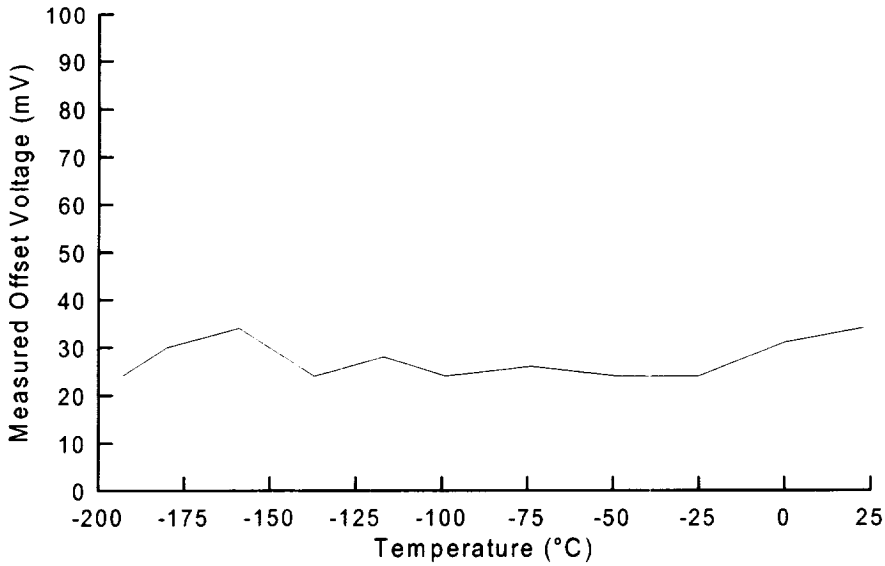

Figure 2. Converter offset voltage as a function of temperature

Table IV. Converter properties at high temperatures

Parameter	Specifications	25 °C	80 °C	100 °C	125 °C
Device #1					
IDDD	0.05 to 135 mA	61	55	53	51
IDDH	0.05 to 135 mA	87	78	74	71
IDDS	0.05 to 80 mA	34	37	35	33
Lad Res	300 to 900 Ohms	577	614	693	675
Vos	-1.25 to 1.25 LSB	0.06	-0.00	-0.04	-0.10
Gain Error	-2.25 to 2.25 LSB	0.16	0.12	0.09	0.09
Device #2					
IDDD	0.05 to 135 mA	62	62	53	51
IDDH	0.05 to 135 mA	90	90	75	71
IDDS	0.05 to 80 mA	34	34	34	33
Lad Res	300 to 900 Ohms	593	571	689	682
Vos	-1.25 to 1.25 LSB	0.08	0.07	0.01	-0.03
Gain Error	-2.25 to 2.25 LSB	0.27	0.05	0.15	0.11
Device #3					
IDDD	0.05 to 135 mA	62	55	53	50
IDDH	0.05 to 135 mA	90	79	75	70
IDDS	0.05 to 80 mA	34	37	36	33
Lad Res	300 to 900 Ohms	590	636	654	685
Vos	-1.25 to 1.25 LSB	0.11	0.10	0.04	-0.00
Gain Error	-2.25 to 2.25 LSB	0.38	0.13	0.09	0.17
Device #4					
IDDD	0.05 to 135 mA	60	53	51	49
IDDH	0.05 to 135 mA	87	76	73	69
IDDS	0.05 to 80 mA	34	34	32	31
Lad Res	300 to 900 Ohms	582	617	704	685
Vos	-1.25 to 1.25 LSB	-0.00	-0.07	-0.13	-0.11
Gain Error	-2.25 to 2.25 LSB	0.30	0.15	0.17	0.08

IDDD: Dynamic supply current
IDDH: Clock high static supply current
IDDS: Clock low static supply current
Lad Res: Ladder resistance
Vos: Offset voltage

Table V. Converter properties at low temperatures

Parameter	Specifications	-190 °C	-180 °C	-170 °C	-150 °C	-120 °C	-80 °C	-55 °C	25 °C
Device #1									
IDDD	0.05 to 135 mA	133	133	133	124	118	110	75	61
IDDH	0.05 to 135 mA	174	174	174	160	151	139	112	87
IDDS	0.05 to 80 mA	100	92	92	84	76	73	39	34
Lad Res	300 to 900 Ohms	199	204	204	284	312	363	466	577
Vos	-1.25 to 1.25 LSB							0.28	0.06
Gain Error	-2.25 to 2.25 LSB							0.23	0.16
Device #2									
IDDD	0.05 to 135 mA	131	128	125	122	113	102	76	62
IDDH	0.05 to 135 mA	171	166	161	156	142	129	113	90
IDDS	0.05 to 80 mA	91	88	84	83	74	68	39	34
Lad Res	300 to 900 Ohms	216	252	273	296	340	385	458	593
Vos	-1.25 to 1.25 LSB							0.28	0.08
Gain Error	-2.25 to 2.25 LSB							0.12	0.27
Device #3									
IDDD	0.05 to 135 mA	132	132	127	122	114	115	77	62
IDDH	0.05 to 135 mA	175	174	166	158	146	127	114	90
IDDS	0.05 to 80 mA	92	89	86	82	80	78	40	34
Lad Res	300 to 900 Ohms	199	207	254	298	328	328	438	590
Vos	-1.25 to 1.25 LSB							0.36	0.11
Gain Error	-2.25 to 2.25 LSB							0.11	0.38
Device #4									
IDDD	0.05 to 135 mA	124	120	120	115	107	97	74	60
IDDH	0.05 to 135 mA	169	160	159	152	140	125	110	87
IDDS	0.05 to 80 mA	83	79	81	75	70	63	38	34
Lad Res	300 to 900 Ohms	204	262	263	297	344	385	447	582
Vos	-1.25 to 1.25 LSB							0.13	-0.00
Gain Error	-2.25 to 2.25 LSB							0.19	0.30

Table VI. Converter output voltage and ladder resistance at low temperatures

Parameter	-190 °C	-180 °C	-170 °C	-150 °C	-120 °C	+25 °C
Ladder Resistance (Ω)	222	229	250	286	333	571
Vin (V)	2.75	2.75	2.75	2.75	2.75	2.75
Converted Vout (V)	2.78	2.79	2.79	2.78	2.78	2.78

Table VII. Summary of Thermal Cycling Data (10 Cycles from +80 °C to -150 °C)

			Before Thermal Cycling	After Thermal Cycling	Before Thermal Cycling	After Thermal Cycling
Device #	Parameter	Specifications	-150 °C	-150 °C	80 °C	80 °C
1	IDDD	0.05 to 135 mA	124	123	55	55
	IDDH	0.05 to 135 mA	160	156	78	78
	IDDS	0.05 to 80 mA	84	78	37	37
	Lad Res	300 to 900 Ohms	284	298	614	617
	Vos	-1.25 to 1.25 LSB			-0.00	-0.00
	Gain Error	-2.25 to 2.25 LSB			0.12	0.03
2	IDDD	0.05 to 135 mA	115	113	53	53
	IDDH	0.05 to 135 mA	152	150	76	76
	IDDS	0.05 to 80 mA	75	71	34	34
	Lad Res	300 to 900 Ohms	297	302	617	623
	Vos	-1.25 to 1.25 LSB			-0.07	-0.09
	Gain Error	-2.25 to 2.25 LSB			0.15	0.09

Shaded areas are outside of specifications. Blank cells: invalid/questionable data (not reported).

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13. ABSTRACT ***(Maximum 200 words)***

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