Fabrication of Very High Efficiency 5.8GHz Power Amplifiers Using AlGaN HFETs on SiC Substrates for Wireless Power Transmission

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For wireless power transmission using microwave energy, very efficient conversion of the DC power into microwave power is extremely important. Class E amplifiers have the attractive feature that they can, in theory, be 100% efficient at converting DC power to RF power.

Aluminum gallium nitride (AlGaN) semiconductor material has many advantageous properties, relative to silicon (Si), gallium arsenide (GaAs), and silicon carbide (SiC), such as a much larger bandgap, and the ability to form AlGaN/GaN heterojunctions.

The large bandgap of AlGaN also allows for device operation at higher temperatures than could be tolerated by a smaller bandgap transistor. This could reduce the cooling requirements. While it is unlikely that the AlGaN transistors in a 5.8 GHz class E amplifier can operate efficiently at temperatures in excess of 300 or 400°C, AlGaN based amplifiers could operate at temperatures that are higher than a GaAs or Si based amplifier could tolerate.

Under this program, AlGaN microwave power HFETs have been fabricated and characterized. Hybrid class E amplifiers were designed and modeled. Unfortunately, within the time frame of this program, good quality HFETs were not available from either the RSC laboratories or commercially, and so the class E amplifiers were not constructed.

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EXECUTIVE SUMMARY

For wireless power transmission using microwave energy, very efficient conversion of the DC power into microwave power is extremely important. Class E amplifiers have the attractive feature that they can, in theory, be 100% efficient at converting DC power to RF power.

Aluminum gallium nitride (AlGaN) semiconductor material has many advantageous properties, relative to silicon (Si), gallium arsenide (GaAs), and silicon carbide (SiC). One significant advantage of AlGaN, relative to Si and GaAs, is a much larger bandgap. This allows for operation at higher voltages. This higher voltage capability is very important in class E amplifiers, because the maximum voltage developed across the transistor is about three times larger than the supply voltage. A high breakdown voltage transistor enables high power generation by the amplifier. AlGaN HFETs have demonstrated breakdown voltages more than an order of magnitude larger than that for similar geometry GaAs HFETs. An advantage of AlGaN relative to SiC, both of which have similarly large bandgaps, is the ability to form AlGaN/GaN heterojunctions, thus making possible AlGaN/GaN heterojunction field effect transistors (HFETs). A similar heterojunction capability has not been demonstrated for SiC.

Efficient operation of the class E amplifier requires that the transistor switch between on and off states of conduction in a small fraction of the time required for one cycle of the RF output. The rapid switching requirement is equivalent to requiring that the high frequency figures of merit for the transistor, f_t (unity short circuit current gain frequency) and f_{max} (unity unilateral gain frequency), be many times higher than the frequency of the output. Again, AlGaN offers excellent high frequency performance, in addition to the high breakdown voltage.

The large bandgap of AlGaN also allows for device operation at much higher temperatures than could be tolerated by a smaller bandgap transistor, such as a silicon device. This could be valuable, in that it reduces the cooling requirements. Unfortunately, some very fundamental properties of the semiconductor material, such as the electron mobility and maximum electron velocity, decrease with increasing temperature. These changes result in decreased RF performance with increasing temperature. At low frequencies, this decreased RF performance is less of a problem, and nice DC characteristics have been measured at 600°C. If the goal is to operate the transistor at elevated temperature, there are aspects of the device design that can be

adjusted for improved operation at elevated temperatures. While it is unlikely that the AlGaN transistors in a 5.8 GHz class E amplifier can operate efficiently at heat sink temperatures in excess of 300 or 400°C, AlGaN based amplifiers could operate at temperatures that are higher than a GaAs or Si based amplifier could tolerate.

Under this program, AlGaN microwave power HFETs have been fabricated and characterized. Hybrid class E amplifiers were designed and modeled. Unfortunately, within the time frame of this program, good quality HFETs were not available from either the RSC laboratories or commercially, and so the class E amplifiers were not constructed and characterized.

1 What Is a Class E Amplifier?

One of the most common modes of operation for an amplifiers is a class A mode of operation. The class A amplifier is a very linear amplifier, with the output being a higher power replica of the input signal. Unfortunately, the maximum possible drain efficiency is only 50%, where drain efficiency is defined to be RF power out divided by DC power in. The bias point of class A amplifiers is discussed in more detail in section 5, and illustrated in Figure 5.3.

Class E amplifiers have the attractive feature that they can, in theory, be 100% efficient at converting DC power into RF power. This makes them attractive for wireless power transmission (WPT) using a microwave beam, where high efficiency at converting DC to microwave power is extremely important. Class E amplifiers are very non-linear, with the output signal having a significantly different shape, compared to the input signal. This non-linearity limits the applicability of class E amplifiers in many audio and RF communications applications, but the non-linearity is not an issue for WPT applications. The frequency of the output matches that of the input signal.

Class E amplifiers are typically classified as a switching amplifier, in that the transistor is operated as a switch, rather than as a variable resistor. A standard schematic diagram for a class E amplifier is shown in Figure 1.1. The HFET is driven with a gate signal that either turns the HFET completely on, or turns it completely off. For high efficiency, it is important that the HFET not be partially on for any significant length of time. The ideal gate drive signal is a suitable amplitude square wave.

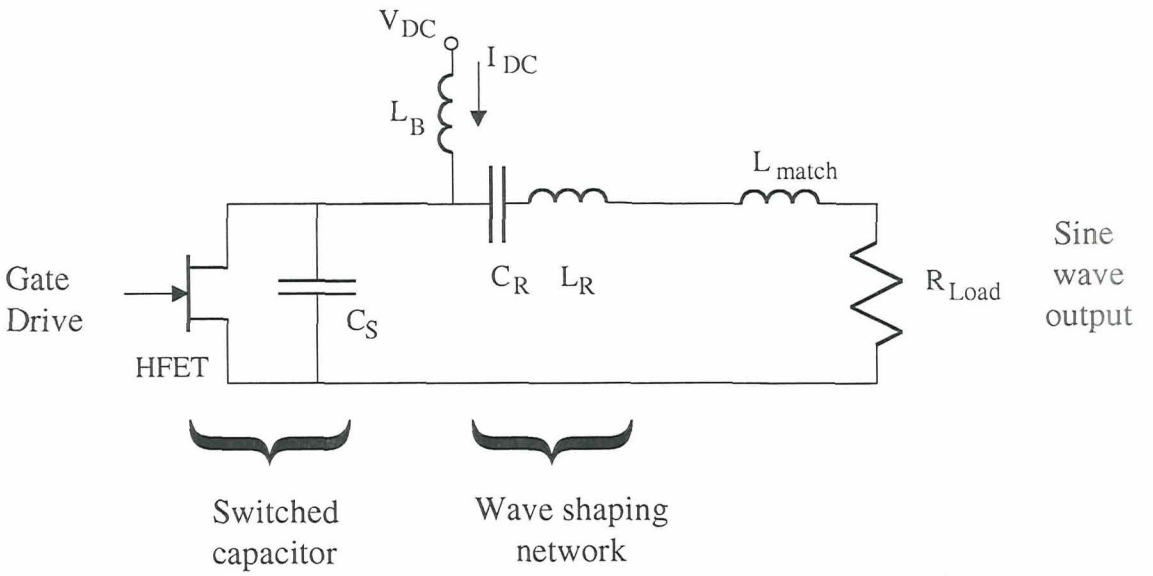

Figure 1.1: Schematic diagram of a Class E Amplifier

In the standard simple analysis of the class E amplifier [1], several simplifying assumptions are made. The transistor is assumed to be a switch that takes zero power to switch, has infinite resistance when open, and zero resistance when closed. It is assumed that the inductor in the DC supply connection, L_B, is sufficiently large that no RF power gets through L_B. The series connected C_R and L_R are resonant at the gate drive frequency, and assumed to have a sufficiently high Q that they suppress all harmonics from reaching the load resistor, R_{Load}. The value of the matching inductor, L_{match}, is chosen such that the current and voltage are in-phase across the load resistor.

The requirements on the circuit's wave forms that essentially define class E operation are that the switch open and close when there is no voltage across it, or therefore across the shunt capacitor, C_S, which is in parallel with the switch. If the switch were to close when there was a voltage across it and the shunt capacitor, the energy stored in the shunt capacitor would be discharged by the switch, and lost. The efficiency would be reduced. Because all of the other components (except for the load resistor) in the class E amplifier are assumed to be purely reactive (no dissipation), as long as the switch opens and closes when there is no voltage across it, the class E amplifier will be 100% efficient at converting DC power to RF power delivered to the load, R_{Load}.

Another constraint on the operation of the circuit that is typically imposed is that the first time derivative of the voltage across the switch be zero when the switch closes. Although this is not required for 100% efficiency, it makes the circuit more tolerant of the switch closure taking a small but finite length of time. These requirements on the voltage waveform, coupled with a few extra constraints, such as the magnitude of the shunt capacitance and the maximum voltage on the transistor, uniquely determines the other components in the circuit.

Figure 1.2 shows the calculated voltage across the switch and a current through the switch for this simplified circuit, where the switching frequency equals 5.8 GHz, C_S equals 0.145 pF, C_R equals 0.058 pF, L_R equals 13 nH, L_{match} equals1.4 nH, R_{Load} equals 40 Ohms, V_{DC} equals 10 Volts and L_B equals 200 nH. As can be seen in the figure, the voltage is zero when the switch opens or closes. Also, the peak voltage across the switch is about 3.5 times larger than the supply voltage. The peak current is more than twice as large as the steady-state supply current. These high peak currents and voltages in the class E amplifier are one of the limitations of this amplifier topology. While the class E amplifier can be very efficient, the maximum power that can be generated from a specific transistor is much lower in class E operation, relative to class A, B or C operation. Equivalently, for a specified output power, a class E amplifier requires a larger transistor than does a class A amplifier. The calculated efficiency for this idealized class E amplifier for converting DC power into RF power at the fundamental frequency is 97%. The 3% of power not being converted into power at the fundamental frequency is being converted into higher harmonics. This calculated efficiency could be increased closer to 100% by increasing the Q of the series resonant L-C circuit. The disadvantage of making the Q of the resonant circuit too large is that the voltages developed at the middle node become very large, and corona discharges and arcing can occur.

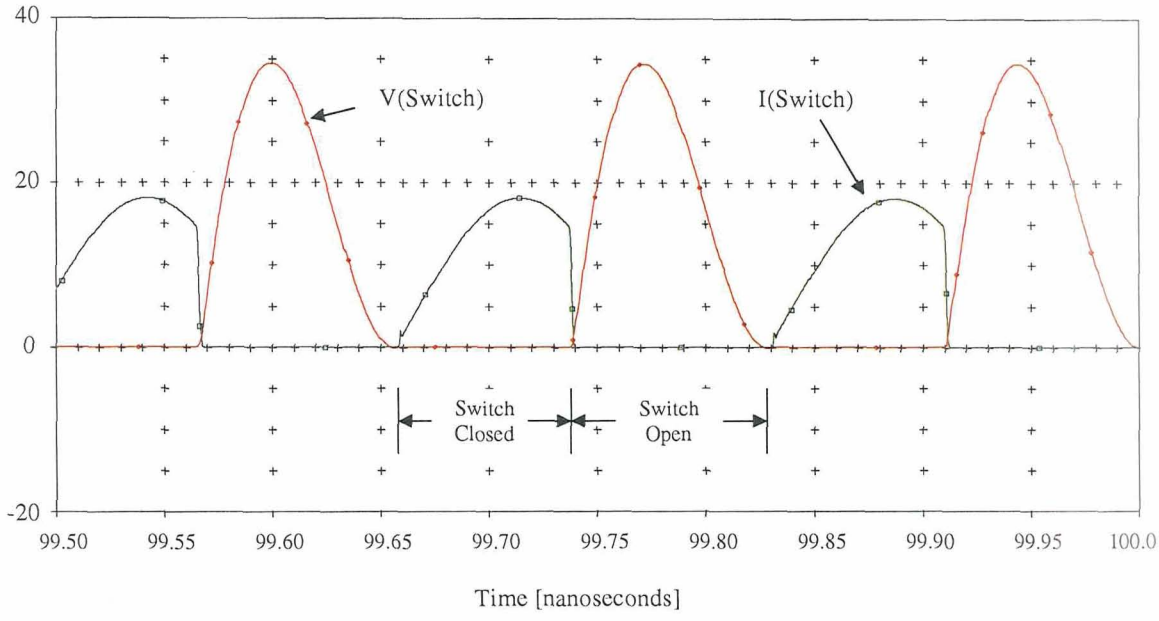

Figure 1.2: The voltage across and current through the switch in a class E amplifier operating at 5.8 GHz, with the component values listed in Table 1.1.

With increasing frequency, the magnitude of the shunt capacitance, C_S, must decrease in order to operate the circuit in the class E mode. HFETs have a drain capacitance that is associated with the intrinsic transistor. This capacitance can be included as part of the shunt capacitance, and therefore does not degrade operation of the class E amplifier. In fact, this intrinsic drain capacitance sets the minimum shunt capacitance that can be achieved. At GHz frequencies, this junction capacitance can supply all of the shunt capacitance needed for class E operation. It also prevents operation of class E amplifiers at arbitrarily high frequencies.

Excellent efficiencies have been demonstrated in class E amplifiers at low frequencies. Sokal and Sokal [1] demonstrated 96% power added efficiency at 4 MHz using a silicon transistor. Recently, there has been significant interest in class E amplifiers for wireless battery-powered communications applications, where high efficiency of the power amplifier is important for long battery life. A collection of recently published papers on class E amplifiers is listed in Table 1.1. While the efficiencies are good, they are not approaching 100%. These published results are aimed at low voltage battery-powered applications. The low supply voltages limit the maximum efficiency that could be achieved. Significantly higher efficiencies should be achievable with an optimized AlGaN HFET-based class E amplifier operating at higher supply voltages.

Table 1.1: Published characteristics of class E amplifiers using various types of transistors.

Frequency [GHz]	Efficiency [PAE]	Power [Watts]	Technology	Reference
0.004	96%	26	silicon bipolar	N.O. Sokal and A.D. Sokal, IEEE JSSC, SC-10, no. 3, p. 168 (1975).
0.50	80%	0.55	GaAs MESFET	T.B. Mader and Z.B. Popovic, IEEE M&GWL, vol. 5, p. 290 (1995).
0.80	74%	0.13	GaAs HBT	G.K. Wong and S.I. Long; 1999 GaAs IC Symposium, p. 299.
0.9	79%	1.5	silicon bipolar	F.J. Ortega-Gonzalez et al., IEEE M&GWL, vol. 8, p. 348 (1998).
1.0	73%	0.94	GaAs MESFET	T.B. Mader and Z.B. Popovic, IEEE M&GWL, vol. 5, p. 290 (1995).
8.3	60%	0.68	GaAs MESFET	Z.B. Popovic and E. Bryerton, ARO MURI review, Aug. 1999.

2 Why Use AlGaN?

Most transistors are made from silicon. However, for some applications, other semiconductors offer important advantages. As shown in Table 2.1, GaAs has a much higher electron mobility than silicon. This higher mobility, coupled with several other advantages, results in much better high frequency performance for GaAs transistors. Both SiC and GaN have much larger bandgaps than silicon or GaAs. The larger bandgaps allow SiC and GaN to support larger electric fields before suffering breakdown. The electron mobility in lightly doped bulk samples of SiC and GaN are very similar. An important distinction between these two wide bandgap materials is that high quality heterojunctions can be formed on GaN using AlGaN. There is no similar lattice-matched, wider bandgap semiconductor that has been grown on SiC. The AlGaN/GaN heterojunction has the desirable property that the electrons in the channel formed at the heterojunction can have mobilities that are much larger than the mobility in bulk GaN. This improved mobility, coupled with the better RF performance of an HFET structure relative to a MESFET structure, as discussed in section 3, results in AlGaN HFETs having significantly better RF performance than SiC MESFETs. Good RF performance is important for efficient operation of class E amplifiers at high frequencies.

Table 2.1: Materials properties for several semiconductors.
The electron mobilities listed for GaN are for: a- bulk electron mobility in lightly doped GaN; b- electron mobility in the channel of an AlGaN/GaN HEMT structure.

Property \ Material	Si	GaAs	4H-SiC	GaN
Bandgap (eV)	1.1	1.4	3.3	3.4
Breakdown field [$x10^5$ V/cm]	2	4	20	33
Electron mobility [cm^2/Vs]	1400	8500	800	900 [a] **2000** [b]
Maximum velocity [$x10^7$ cm/s] (E= 8 E5 V/cm)	0.5	0.7	1.0	1.4
Thermal conductivity [W/cm K]	1.5	0.5	4.9	1.3

Another important difference between SiC and GaN is the thermal conductivity. High thermal conductivity is needed to remove the waste heat generated during high power operation, and thereby keep the intrinsic transistor cool. The SiC has a much higher thermal conductivity than does GaN. Unfortunately, bulk GaN substrates are not yet available commercially. The most common substrate for growth of GaN epitaxial layers is sapphire, which has a very poor thermal conductivity (0.30 W/cm•K). The very poor thermal conductivity of sapphire causes the performance of power AlGaN/GaN HFETs fabricated on sapphire substrates to be severely degraded in performance, as discussed in section 5. Fortunately, GaN can be grown epitaxially on SiC substrates. This combines the high electron mobility at an AlGaN/GaN heterojunction with the high thermal conductivity of SiC substrates. This is the device structure used in this project.

3 What Is an HFET?

There are many kinds of transistors. As illustrated in Figure 3.1, metal-semiconductor field effect transistors (MESFETs) have a doped layer at the surface to which the source and drain make Ohmic contact. The gate forms a Schottky diode on this doped layer, and the depletion layer under the gate modulates the carrier concentration in the doped layer under the gate, which modulates the current flowing from the source to the drain.

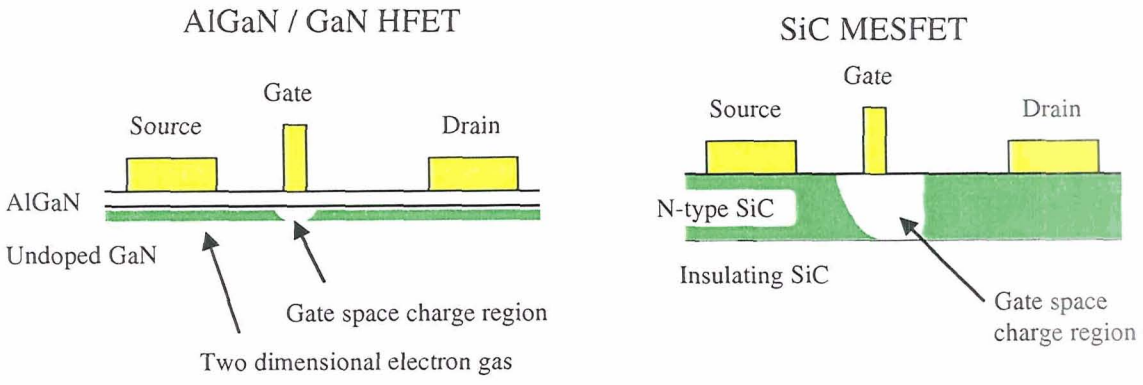

Figure 3.1: Comparison of the structure of an HFET and a MESFET.

Getting good high frequency performance in a MESFET requires compromises of some of the other MESFET characteristics. The product of the doping density in the channel and the thickness determine the number of mobile electrons, or sheet charge density, available to conduct current. This sheet charge density can be held constant while the doped layer is reduced in thickness, by increasing the doping density. However, as the doping density increases, the mobility of the electrons decreases, so the current decreases. Also, with increasing doping density, the reverse breakdown voltage of the Schottky gate decreases. It is essential that the Schottky diode be able to tolerate a reverse bias sufficient to completely deplete the doped channel under the gate, so that the current through the MESFET can be pinched off. For good RF performance, the thickness of the doped channel must be reduced, so that the width of the gate space charge region along the channel can be made small. The maximum doping in this thinner channel is constrained by the need to maintain a good reverse breakdown characteristic for the

Schottky gate diode. As the structure of the MESFET is optimized for operation at higher frequencies, their power handling capability must be sacrificed.

Heterojunction field effect transistors (HFETs) have several important advantages for high frequency applications, relative to MESFETs. The donors responsible for the mobile electrons in the channel can be placed in the wider band gap AlGaN, where they are spatially separated from the electrons. The electrons do not suffer as much from scattering by the remotely located ionized donors, so the mobility of the carriers in the channel of an HFET can be much higher than that in a MESFET, as shown in Table 2.1. The wide bandgap of the AlGaN, and the fact that the top region of the AlGaN which is immediately under the gate can be undoped, increases the gate reverse breakdown voltage. As a result of these various differences between MESFETs and HFETs, HFETs are expected to have better high frequency performance than MESFETs. This is experimentally confirmed for GaAs HFETs relative to GaAs MESFETs, and is true for reported performance of AlGaN HFETs relative to SiC MESFETs.

4 Fabrication of the AlGaN HFETs

The AlGaN and GaN epitaxial layers were grown on electrically insulating (0001) oriented SiC substrates by MOCVD. The thicknesses of the layers for the HFETs are listed in Table 4.1. The epitaxial layer structure results in an electron sheet charge density of about 1 $x10^{13}$ cm^{-2}, and a Hall mobility of about 1300 $cm^2/V \cdot s$. This results in a sheet resistance for the HFET structure of 480 Ohms/square.

Table 4.1: The layer structure of the AlGaN/GaN HFETs

Layer	**Thickness** [Angstroms]	**Alloy Comp.** [%]	**Doping** [cm^{-3}]
Cap	50	25% AlGaN	Undoped
Donors	100	25% AlGaN	5E18
Spacer	50	25% AlGaN	Undoped
(Channel)			
Buffer	1 um	GaN	Undoped
Nucleation	1000	AlGaN	Undoped
Substrate	14 mils	SiC	Insulating

The AlGaN HFETs have been fabricated using our standard process [2, 3]. Shown in Figure 4.1 is an SEM image of the source, gate and drain region of a fabricated AlGaN/GaN power HFET. The gate lead connects to two gates, which are on either side of the drain. A metallic air bridge goes over the gates and the drain, and connects the sources together. Figure 4.2 shows an entire AlGaN/GaN power HFET. This HFET has a total of 16 gates, each of which is 80 microns long, resulting in a total gate width of 1280 microns. An HFET similar to this one was planned for use in the class E amplifiers.

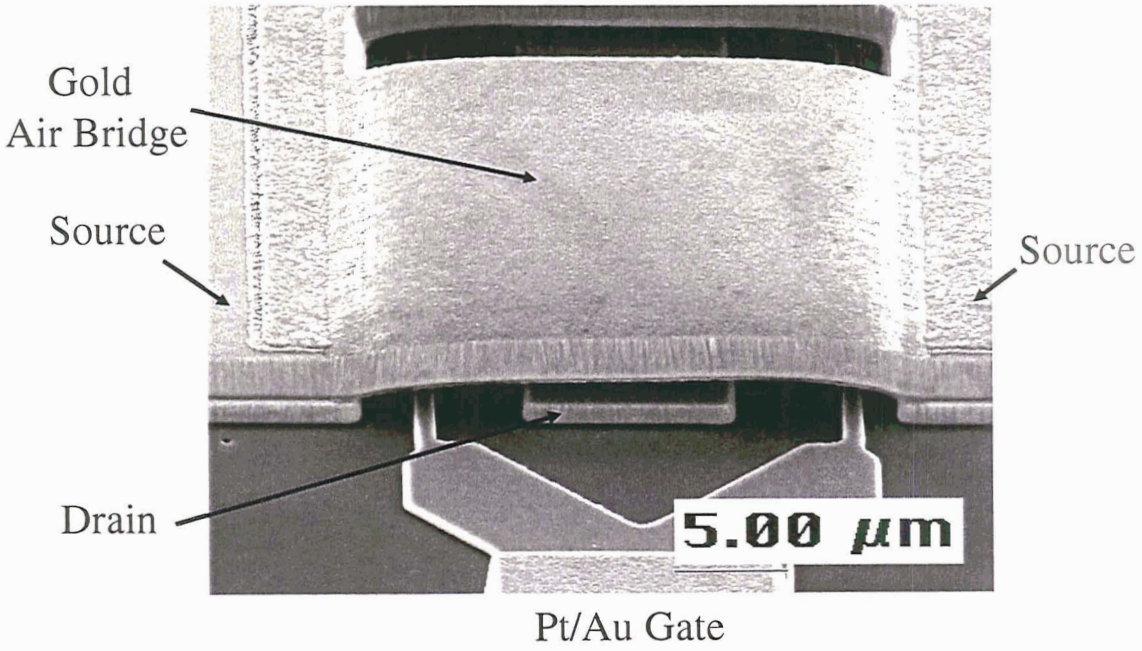

Figure 4.1: SEM image showing the details of the source and drain regions of an AlGaN/GaN power HFET.

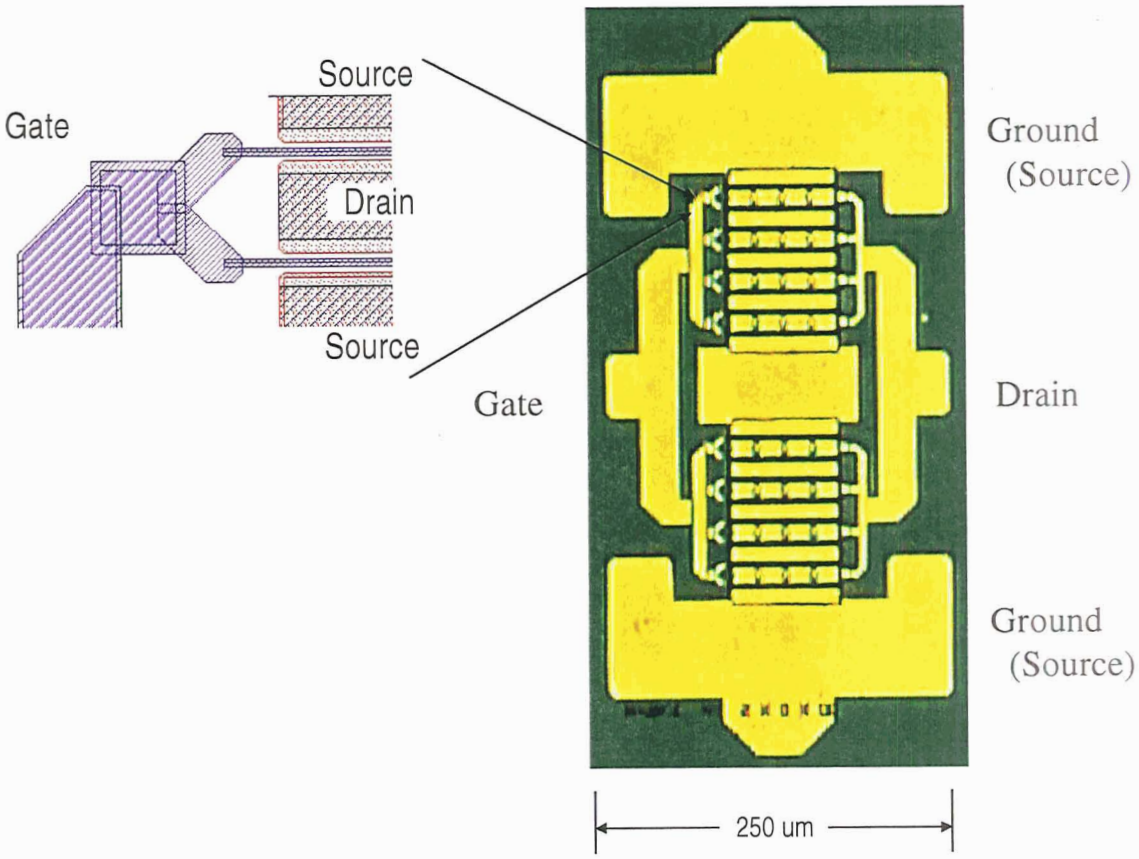

Figure 4.2: Optical micrograph of an AlGaN/GaN power HFET.

5 Electrical Characteristics of AlGaN HFETs.

The typical electrical characteristics of an AlGaN/GaN power HFET are shown in Figure 5.1. This shows the HFET I-V characteristics of a fairly small device, measured to 40 volts of drain bias. Larger devices have similar characteristics, but are more difficult to measure using on-wafer probes due the undesirable heating in the large devices which are not packaged with efficient thermal management. The transconductance in these devices is in excess of 200 mS/mm. The f_t (unity short circuit current gain frequency) for these HFETs is about 20 GHz, and the f_{max} (unity unilateral gain frequency) is about 45 GHz. Shorter gate lengths will improve the high frequency performance, but these values are adequate for this 5.8 GHz class E amplifier.

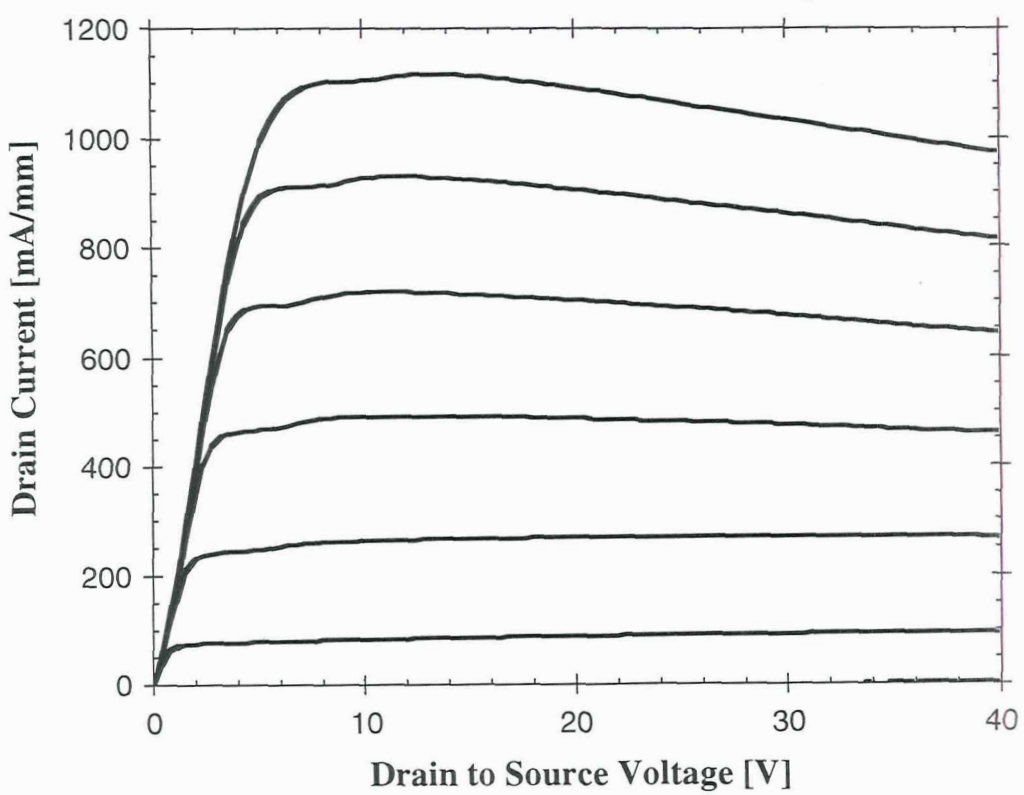

Figure 5.1: HFET I-V characteristics for a 20 micron wide AlGaN/GaN HFET. The device is on an electrically insulating SiC substrate, and has an optically defined 0.7 micron long gate. The gate to source voltage ranges from -5 to +1 volts. (Device 9-4 / 1-B / 4-K)

If the HFET is on a lower thermal conductivity sapphire substrate, rather than being on a high thermal conductivity SiC substrate, the electrical characteristics are severely degraded.

Shown in Figure 5.2 are the electrical characteristics of another fairly small HFET similar in layout to the HFET measured in Figure 5.1, but grown on a sapphire substrate. As can be seen, with increasing power being dissipated in the device, the current is decreasing. This current decrease is due to the device getting hot, which causes the electron mobility to decrease. In large area devices, this current decrease is much more severe.

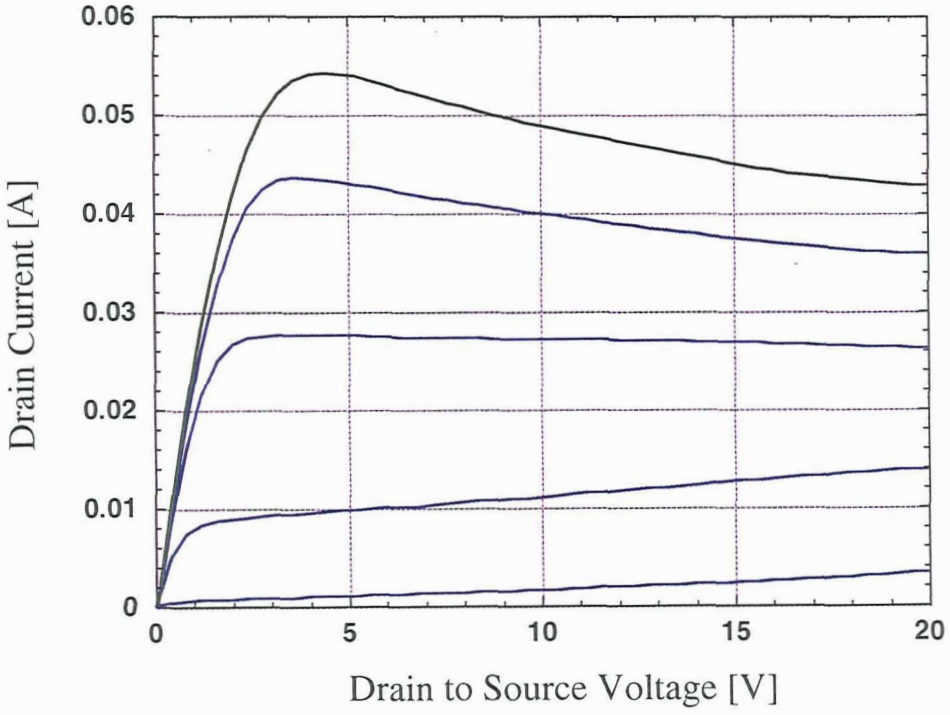

Figure 5.2: HFET I-V characteristics for an 80 micron wide AlGaN/GaN HFET. The device is on a sapphire substrate, has an optically defined 0.7 micron long gate, and 3 micron source to drain spacing. The gate to source voltage ranges from -3 to +1 volts. (Lot 12, wafer 6)

Very good RF power performance has been measured on these HFETs. On-wafer probing at 10 GHz of moderately large devices (320 microns wide) has yielded an RF power density of 2.8 Watts/mm with a gain of 6.5 dB [2]. This power density is several times larger than can be achieved in comparably sized GaAs devices. In larger devices (1280 microns wide), a total power of 2.3 Watts at 10 GHz has been measured [3]. Pulsed testing of these 1280 micron wide HFETs, which reduces the thermal limitations on these unpackaged devices, has produced 3.9 Watts at 8 GHz [4].

The difference between class A and class E modes of operation is illustrated in Figure 5.3. For high power class A operation, the device is biased at approximately half of the maximum current and half of the maximum voltage. This bias condition results in power being dissipated even if no RF signal is applied, resulting in a maximum possible efficiency of 50%. The RF voltage swings the operating point along a load line. In contrast, for class E operation, the transistor is either fully off or fully on. When the transistor is pinched off, very little current flows, and the transistor resembles a good switch. When the transistor is turned on, there remains some series resistance, which is undesirable. An ideal switch has no series resistance. The on-resistance in the transistor dissipates power in the class E amplifier, and can result in a significant loss in efficiency. Minimizing this series resistance is important.

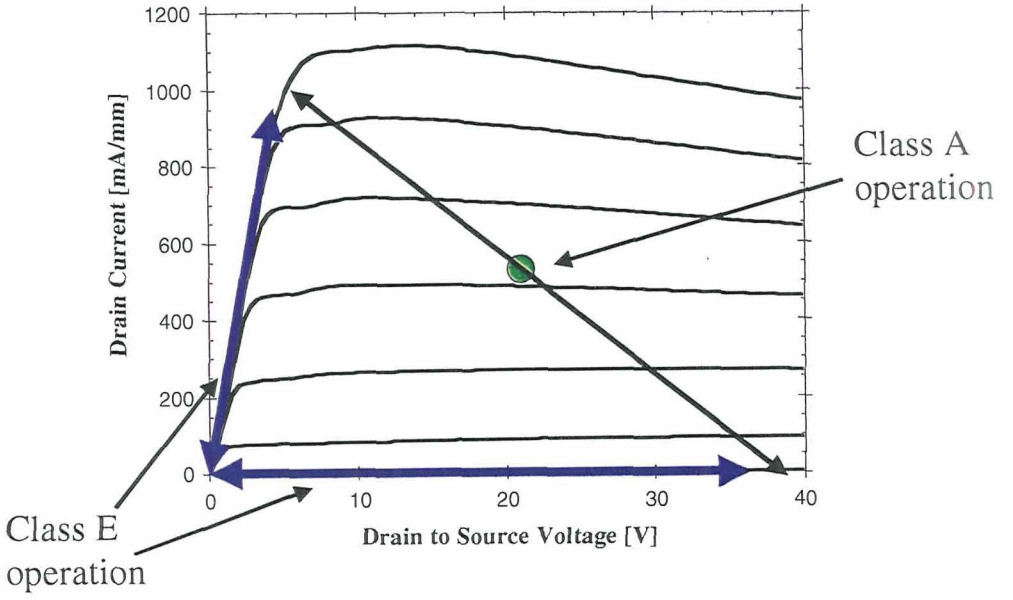

Figure 5.3: Illustration of the difference between the operation of class A and class E amplifiers. (Device 9-4 / 1-B / 4-K)

The sources of this on-resistance can be identified. Illustrated in Figure 5.4 is an estimation of the on-resistance in the HFET. The on-resistance is about 5.0 Ohm*mm (R= 6V / 1.2 A/mm). The expected resistance can be divided into two parts, one part associated with the source and drain Ohmic contacts, and a second part associated with the semiconductor channel resistance. The contact resistance on this wafer, measured on transmission line test structures, is about 2.5 Ohm*mm. The expected contribution to the on-resistance due to the two contacts (source and

drain) is, therefore, 5 Ohm*mm. The measured sheet resistance of the AlGaN/GaN channel is about 350 Ohms/square. For a 2 micron source to drain spacing in a HFET, there would be 500 squares of channel in a 1 mm wide HFET (1000 microns wide / 2 microns), so the intrinsic channel resistance is only 0.7 Ohm•mm (350 Ohms/square / 500 squares). The Ohmic contacts are the dominant contributor to the on-resistance in this HFET. It should be possible to dramatically reduce this resistance with a more optimal Ohmic contact process.

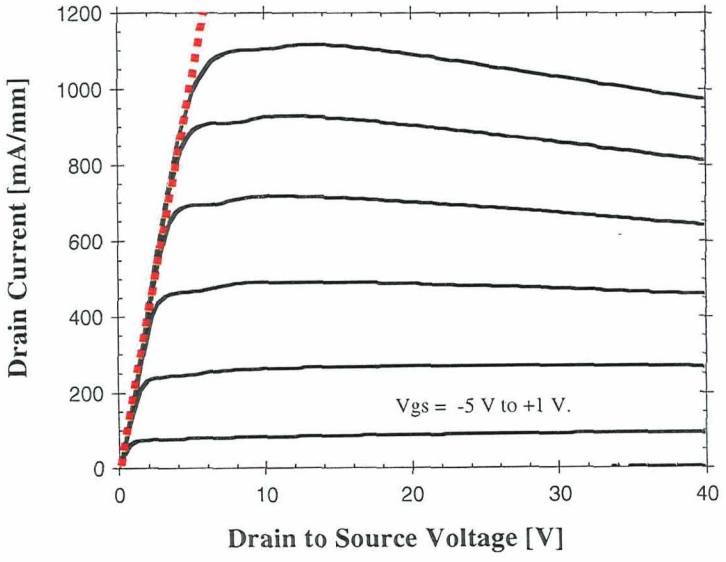

Figure 5.4: Estimation of the on-resistance of the AlGaN/GaN HFET. (Device 9-4 / 1-B / 4-K)

Attempts were made to reduce this on-resistance in the HFETs. A process demonstrated by a group at the University of California at San Diego [5] was examined in our laboratory. The process modifies the layer thicknesses in the titanium and aluminum metal stack that forms the Ohmic contact, and modifies the thermal alloying cycle which forms the contact. In the standard Ohmic contact process, 35 nm of titanium followed by 70 nm of aluminum are deposited, and annealed at 950°C for 30 seconds. The improved contact ("Advancing Ohmic" [5]) increases the percentage of titanium (150 nm of titanium followed by 20 nm of aluminum), and anneals the contact more aggressively.

As shown in Figure 5.5, our attempts to reduce the contact resistance were not very successful. It is believed that this is partially due to the differences in the starting wafers used at UCSD and in our experiments. We have demonstrated reductions in the contact resistance by other standard techniques, such as implanting silicon donors in the contact region, annealing to activate the donors, and then depositing the metallic contacts. It should be possible to make the

contact resistance a small fraction of the on-resistance. The details of this process have not been worked out yet.

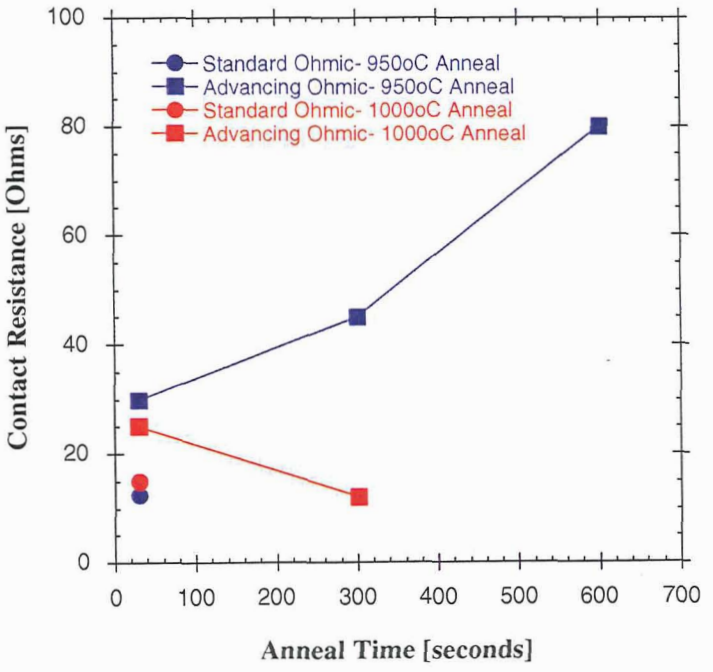

Figure 5.5: Ohmic contact resistance of the standard and "advancing" [5] Ohmic contact, as a function of annealing time and temperature.

6 Measurement of the HFET Drain Capacitance

A critical aspect for the design of the class E amplifiers is a measurement of the drain capacitance in the HFETs. To measure this drain capacitance, microwave S parameter measurements were taken on an assortment of the AlGaN HFETs that were to used for construction of the amplifiers. The S parameters were measured using an HP 8510 network analyzer at frequencies from 0.1 GHz to 50 GHz. To extract the capacitance, the S parameters were converted to admittance (Y) parameters. At low and moderate frequencies, the imaginary part of Y_{22} should be equal to the drain capacitance. The manipulation of the S parameter data to extract this capacitance was done using the MathCAD software package. The MathCAD routine to extract the drain capacitance is listed in Appendix 1.

This analysis for the capacitance assumes that the drain port of the HFET can be modeled as a parallel combination of a capacitor and a resistor. At low and moderate frequencies, this is certainly true. At high frequencies, the parasitic inductance of the metallic interconnects will become important, and this simplifying assumption (parallel capacitor and resistor) will no longer be valid. Shown in Figure 6.1 is a representative plot of the calculated drain capacitance for one of the HFETs. As can be seen in the figure, at lower frequencies, the calculated capacitance is fairly frequency independent, indicating that modeling the drain port as a parallel capacitor and resistor is reasonable. At 5.8 GHz, the assumptions in this capacitance analysis are well satisfied.

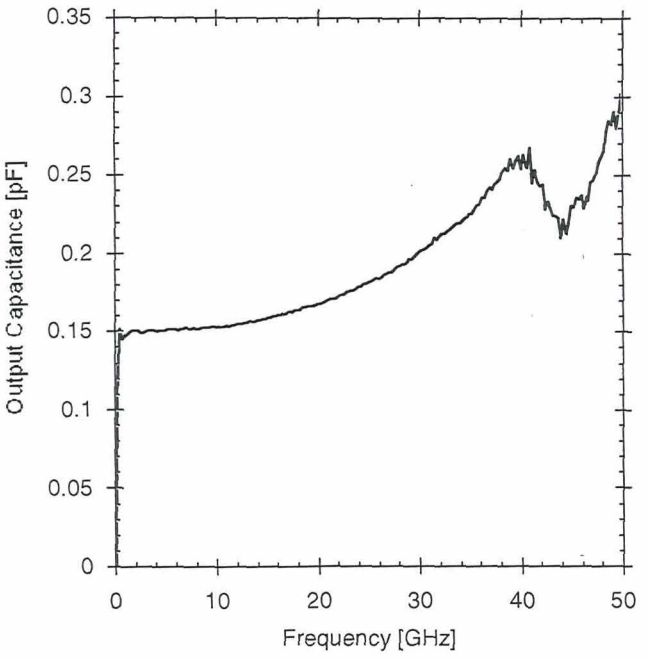

Figure 6.1: Drain capacitance versus frequency for a 640 micron wide AlGaN/GaN HFET, extracted from S parameter measurements. For this measurement, the drain to source voltage was 5 volts, and the gate to source voltage was -4 Volts (Pinched off). (Device 9-2_1-C_1-F)

Using this analysis, the measured capacitance at 5.8 GHz was extracted for an assortment of 640 micron wide HFETs, under a variety of bias conditions. This capacitance is plotted in Figure 6.2. As can be seen, the capacitance decreases slightly with increasing bias. This decrease in capacitance with increasing bias is due to the depletion width under the gate increasing with increasing bias. From this data, a drain capacitance of 0.145 picoFarads was chosen for the design of the class E amplifiers.

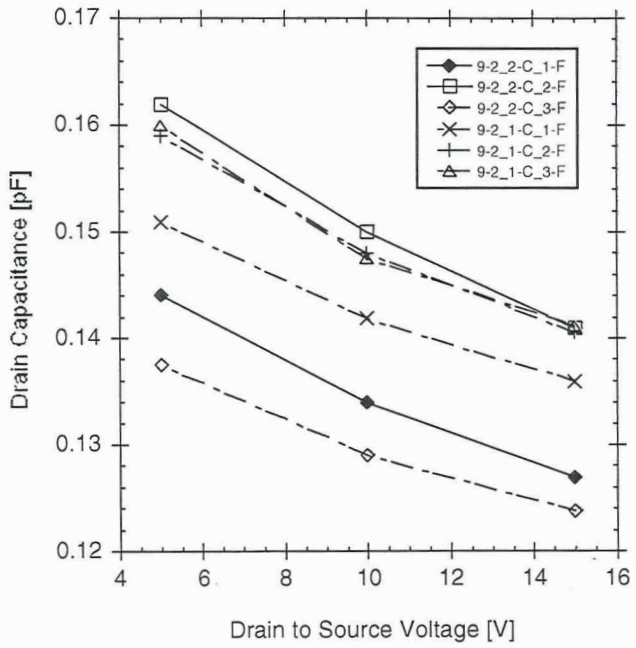

Figure 6.2: Drain capacitance at 5.8 GHz versus drain to source voltage, for some 640 micron wide HFETs. The HFETs were pinched off in these measurements (V_{gs}= -4V)

7 Design of the Class E Amplifier

Shown in Figure 7.1 is the schematic for the class E circuit which was modeled. The measured value of the transistor's shunt capacitance (C_S= 0.145 pF), and the specified frequency of operation (5.8 GHz) do not uniquely determine all of the parameters in the class E circuit. One more parameter is needed. This is typically related to the breakdown voltage of the transistor. If we assume that these transistors can safely operate at a peak drain bias of 40 Volts, then the maximum supply voltage becomes 12 Volts. The Q of the series LC circuit is chosen to be about 5, which results in the value of the capacitance being a convenient size. The series resistance for the 640 micron wide HFETs is measured to be 12 Ohms. The switch is toggled at 5.8 GHz with a 50% duty cycle.

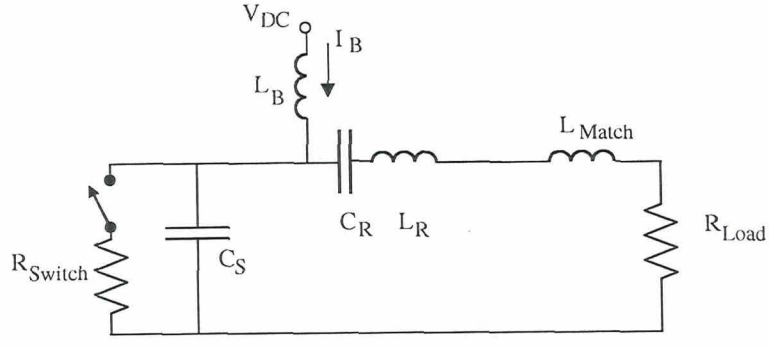

Figure 7.1: Class E amplifier circuit used in the circuit simulations.

With these assumed parameters, the values of the matching inductor (L_{Match}) and the load resistance (R_{Load}) can be adjusted to give a class E amplifier waveform, based on modeled performance using PSpice. The values for the circuit elements are listed in Table 7.1. The resulting wave forms are shown in Figure 7.2. The analysis was done using the PSpice file listed in Appendix 2. The peak switch voltage is 35.7 Volts, and the peak switch current is 0.327 Amperes. The DC power flowing into the amplifier is 1.25 Watts, and the RF power at the fundamental frequency in the load resistor is 0.895 Watts, resulting in an efficiency of 71%. This comparatively low efficiency is due almost entirely to the significant on-resistance of the transistor.

Table 7.1- Values of the optimized circuit elements for the class E amplifier.

V_{DC}	12.0 Volts
L_B	200 nH
R_{switch}	12.0 Ohms
C_S	0.145 pF
C_R	0.058 pF
L_R	13.0 nH
L_{match}	1.6 nH
R_{load}	34.0 Ohms

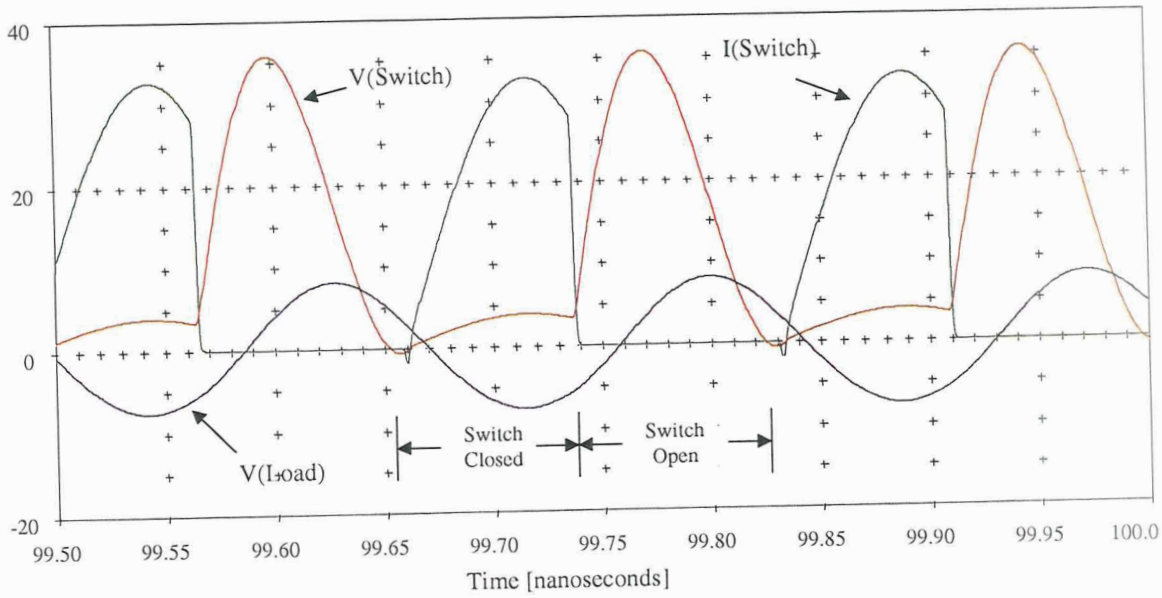

Figure 7.2: Calculated steady-state voltage and current through the switch, and the voltage across the load resistor. The switch current, in Amperes, has been multiplied by 100 to make it a convenient size in the plot.

8 Fabrication of the Class E Amplifier

The class E amplifier was to be fabricated using hybrid construction techniques. Discrete transistors would be soldered to a base plate, and wire bonded into the circuit. For the series capacitor, a high Q surface mount device would be used. It would be necessary to match the 50 Ohm input into the gate of the transistor, and to match the 34 Ohm output impedance of the amplifier to 50 Ohm impedance. This would be done using standard microstrip matching techniques. Figure 8.1 shows what the completed amplifier would look like.

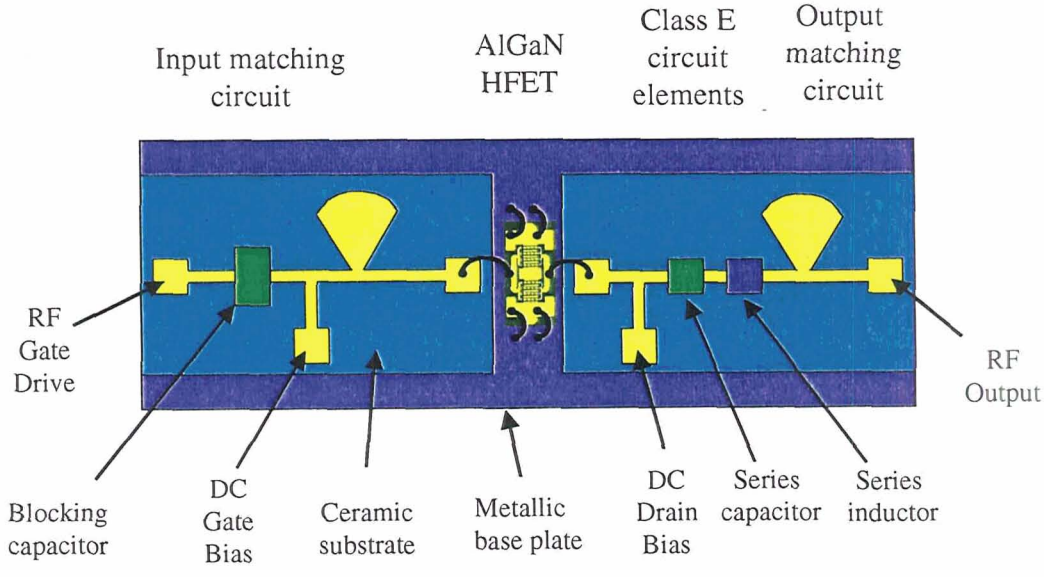

Figure 8.1: Schematic representation of what the class E amplifier will look like.

Unfortunately, transistors with good electrical characteristics were not available within the time frame needed for this project. The limited number of HFETs fabricated at RSC suffered from significant electrical trapping effects that dramatically degraded the I-V curves and caused the characteristics to change with time. AlGaN HFETs are not commercially available. The lack of transistors made construction of the amplifiers impossible.

9 Planned Testing of the Class E Amplifier

For testing, the class E amplifier would have been mounted into our standard test fixture. A representative fixture is shown in Figure 9.1. This well understood fixture brings the RF signal from coaxial connectors to microstrip lines that connect to the circuit under test. The power and harmonic content of the output sine wave will be easy to measure using RF power meters and spectrum analyzers.

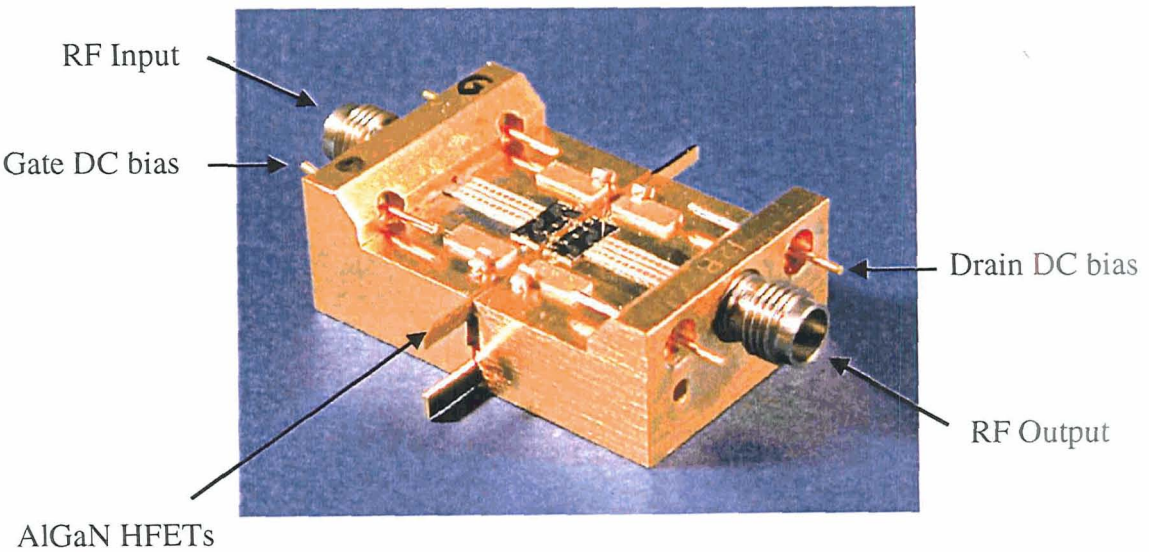

Figure 9.1: Standard test fixture for RF testing of circuits.

A difficulty involved in the testing is the generation of the required gate signal to drive the HFET. Ideally, for class E operation, the gate signal should alternately turn the transistor on and off, with minimal time in the transition between states. If the transistor is a MOSFET, this gate drive can be approximated using a very large amplitude sine way. In a MOSFET, a dielectric layer between the gate and the channel prevents DC conduction from the gate into the channel. If the gate signal increases beyond that bias needed to turn the MOSFET on, no DC gate current flows.

The gate in the AlGaN HFET is a Schottky diode. The gate Schottky diode is reverse biased to pinch the HFET off. If the gate Schottky diode is forward biased by more than a few volts, large gate currents flow into the channel, which is undesirable. Driving the gate of an AlGaN

HFET based class E amplifier with a large amplitude sine wave will result in large gate currents during a portion of the cycle, which would make evaluation of the performance difficult.

The preferred gate drive signal for the AlGaN HFET is a square wave which drives the transistor from pinched-off to completely on. For a real system application, this gate drive signal could be generated using a small circuit to generate the needed wave form. This gate drive circuit could be fabricated monolithically with the class E amplifier, using AlGaN HFETs to make the drive circuit. Generating the 5.8 GHz square wave for this testing is more difficult.

The Fourier representation of a square wave signals consists of a sum of the fundamental sinusoid and odd harmonics of the fundamental frequency. While square wave signal generators with adjustable amplitude are available at low frequencies, they are not a simple commercially available box at 5.8 GHz. While the fixed amplitude square wave generator is available, as a signal generator for the high speed digital electronics industry, amplifying the 5.8 GHz square wave to get the +1 volt and -4 volts needed to switch the transistor is difficult. The amplifier would need to be able to operate at the fundamental 5.8 GHz, as well as at several odd harmonics (17.4 GHz, 29.0 GHz, 40.6 GHz), in order to get a nice large amplitude square wave. Amplifiers do not normally have band widths that are this wide.

To generate the needed signal for testing, our plan was to clip a large amplitude sine wave, resulting in a wave form approximating a square wave. The circuit which was to accomplish this is shown in Figure 9.2. The gate bias pad, V_{gs}, would be used to set the average DC level of the gate wave form, while the positive and negative clipping bias pads would be used to determine the clipping voltages.

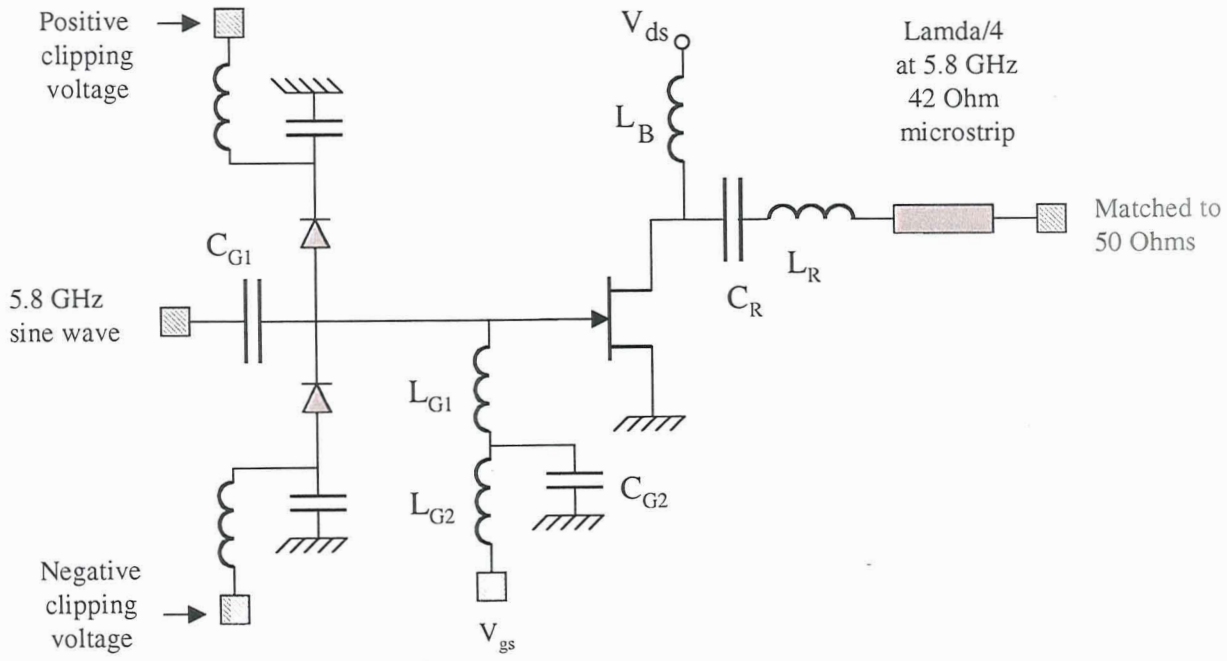

Figure 9.2: Schematic illustrating the use of clipping diodes to generate the gate drive signal.

10 High Temperature Operation of AlGaN HFETs

One of the potential advantages of wide bandgap materials is the option of operating at elevated temperatures. The larger bandgap increases the temperature at which carrier generation across the bandgap degrades device performance. Silicon's comparatively small 1.1 eV bandgap limits the maximum temperature of operation for silicon devices to fairly low temperatures (~150°C). Because thermal generation processes are exponentially related to temperature, the 3.4 eV bandgap of GaN should allow operation at temperatures twenty time higher ($e^{(3.4 / 1.1)} = 22$) than silicon devices, if GaN device operation is limited by thermal carrier generation across the bandgap. Unfortunately, the process limiting high temperature operation for GaN devices is almost never thermal generation across the bandgap.

There have been several reports of the high temperature operation of AlGaN/GaN HFETs. In 1995, Khan et al. [6] reported that AlGaN HFETs, which operated nicely at 25°C, developed significant output conductance at 200°C, and were very leaky at 300°C. The leakage was behaving like a series resistor connecting the drain to the source, in parallel with the HFET channel. The leakage is attributed to leakage through the substrate.

In 1997, Binari et al. [7] reported dramatically better high temperature performance. These devices had minimally increased output conductance at 400°C, but were showing significantly increased leakage at 500°C. The significant improvement is probably due to the rapidly improving material quality.

In 1999, Daumiller et al. [8] reported low leakage HFET operation at 600°C. These high temperature results have all been low frequency (DC) measurements. Unfortunately, while there is minimal DC leakage at these elevated temperatures, there are other changes that affect device operation, particularly at high frequencies. While the measured charge density in the channel does not increase significantly with increasing temperature, the mobility is rapidly decreasing [8]. The mobility is decreasing at the predicted rate, based on phonon scattering (thermally induced lattice vibrations) being the mobility limiting process. This phonon scattering is a fundamental process, which would be very difficult to eliminate. This reduced mobility reduces the maximum channel current, and increases the channel resistance. Another undesirable effect

of increased temperature is a predicted decrease in the electron peak velocity [9]. These effects reduce the RF performance of the transistor.

While transistor operation at 600°C has been demonstrated at low frequency, the rapid decrease in RF performance will limit the useful operating temperature for RF applications to much lower temperatures. This useful temperature limit will depend on the frequency, and on the needed RF performance. For class E amplifiers operating at 5.8 GHz using currently available HFETs, this temperature limit is probably only a few hundred degrees Centigrade. It is possible to design the HFET so that it could operate with acceptable RF performance at higher temperatures. Fabricating much shorter gate lengths would result in better RF performance at room temperature, and degraded but still superior performance at elevated temperature. Also, the AlGaN material quality continues to improve, so that device performance is continuing to improve. It is difficult to predict what the maximum useful operating temperature for an AlGaN RF transistor might be in the future. It is unlikely to be 600°C, but a temperature of 300°C is not unreasonable. The maximum operating temperature for GaN is greater than that for Si or GaAs, and will remain larger. Issues related to the long term reliability of the metallurgical contacts will need to be addressed.

11 Optimization of the Class E Amplifier for WPT Applications

For WPT systems applications, some support circuitry in addition to the class E amplifier will be needed. Specifically, a circuit to generate the signal to drive the gate will be needed. As discussed above, the optimal gate signal for a class E amplifier is a square wave signal which quickly switches the transistor from on to off, and visa versa. This gate drive circuit could be packaged along with the class E amplifier, as illustrated in Figure 11.1. It may be possible to have the same power supply voltages for the gate pulse shaping circuit and the class E amplifier. This would reduce the DC connections to the package from four to two, at the potential penalty of increased complexity in the circuit and the package.

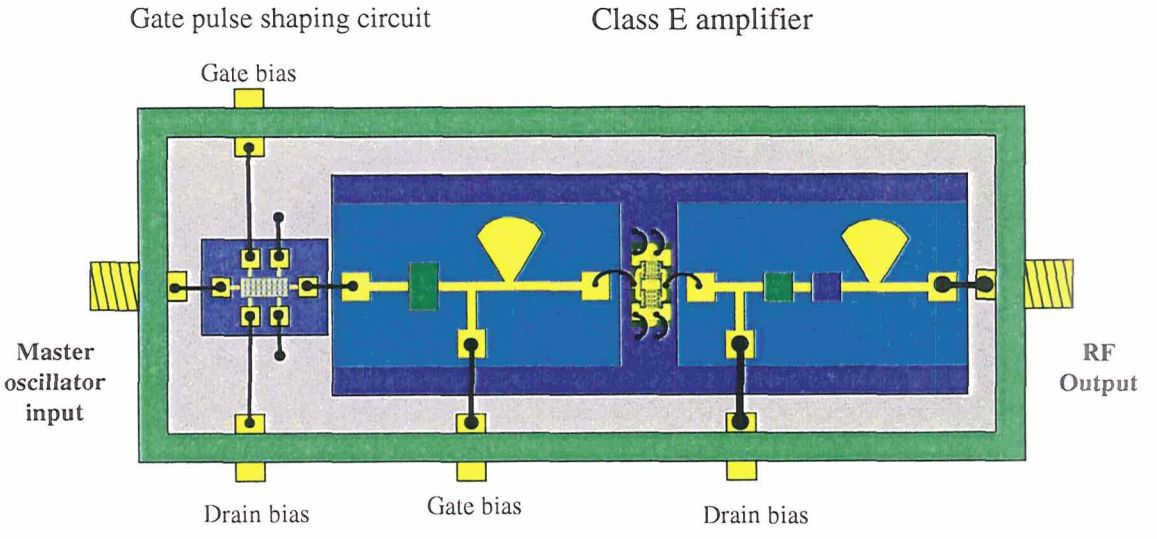

Figure 11.1: Schematic representation of a complete power conversion module might look like.

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1. N.O. Sokal and A.D. Sokal, IEEE JSSC, SC-10, no. 3, p. 168 (1975).

2. "High-power 10-GHz operation of AlGaN HFET's on insulating SiC", Sullivan, G.J.; Chen, M.Y.; Higgins, J.A.; Yang, J.W.; Chen, Q.; Pierson, R.L.; McDermott, B.T., IEEE Electron Device Letters, vol. 19, no. 6, pp. 198-200, (June 1998).

3. "High power RF operation of AlGaN/GaN HEMTs grown on insulating silicon carbide substrates", G.J. Sullivan, J.A. Higgins, M.Y. Chen, J.W. Yang, Q. Chen, R.L. Pierson, B.T. McDermott, J.W. Yang, Q. Chen, Electronic Letters; Vol. 34, No. 9, p. 922, (1998).

4. Pulsed testing done by R.P. Smith and J. Perez at JPL:
   Highest Power: 3.9W (3W/mm) with 7.7 dB gain and 26% P.A.E.
   At Vds=25V: 3.3W (2.6W/mm) with 8.5 dB gain and 30% P.A.E.
   RSC wafer 9-2, cell 1c, device 4e.
   0.7 x 1280 mm gate width.
   10 msec DC pulse; 0.1% duty, 20 msec RF pulse.
   Vds = 32V, Vgs = -1.5V, 8 GHz

5. "Low resistance Ohmic contacts on AlGaN/GaN structures using implantation and the "advancing" Al/Ti metallization", Qiao, D.; Guan, Z.F.; Carlton, J.; Lau, S.S.; Sullivan, G.J., Applied Physics Letters, vol. 74, no. 18 , pp. 2652-4, (May 1999).

6. M.A. Khan, M.S. Shur, J.N. Kuznia, Q. Chen, J. Burm and W. Schaff; *Appl. Phys. Lett.*, Vol. 66, No. 9, p. 1083, (1995).

7. S.C. Binari, K. Doverspike, G. Kelner, H.B. Dietrich, and A.E. Wickenden, Solid-State Electronics, Vol. 41, No. 2, pp. 177-180 (1997).

8. I. Daumiller, C. Kirchner, M. Kamp, K.J. Ebling, and E. Kohn, IEEE EDL, Vol. 20. No. 9, p. 448 (1999).

9. M.S. Shur et. al., Inst. Phys. Conf. Ser. No. 141, Chap. 4, p. 419 (1994).

Appendix 1

MathCAD Analysis for the Extraction of the Drain Capacitance of the HFETs from Measured S Parameters.

AlGaN Transistor Capacitance Analysis

[Uses MathCAD 8]

[Read S parameter file from HP 8510]

data :=

F:\..\922b2h00.s2p.txt

freq := data$^{\langle 0 \rangle}$

s11m := data$^{\langle 1 \rangle}$ s21m := data$^{\langle 3 \rangle}$ s12m := data$^{\langle 5 \rangle}$ s22m := data$^{\langle 7 \rangle}$

s11a := data$^{\langle 2 \rangle}$ s21a := data$^{\langle 4 \rangle}$ s12a := data$^{\langle 6 \rangle}$ s22a := data$^{\langle 8 \rangle}$

n := 0 .. rows(s11m) –

[Convert magnitude and angle to complex number

$$s11c_n := s11m_n \cdot \left(\cos\left(s11a_n \cdot \frac{\pi}{180}\right)\right) + \left[s11m_n \cdot \left(\sin\left(s11a_n \cdot \frac{\pi}{180}\right)\right)\right]$$

$$s21c_n := s21m_n \cdot \left(\cos\left(s21a_n \cdot \frac{\pi}{180}\right)\right) + \left[s21m_n \cdot \left(\sin\left(s21a_n \cdot \frac{\pi}{180}\right)\right)\right]$$

$$s12c_n := s12m_n \cdot \left(\cos\left(s12a_n \cdot \frac{\pi}{180}\right)\right) + \left[s12m_n \cdot \left(\sin\left(s12a_n \cdot \frac{\pi}{180}\right)\right)\right] \cdot i$$

$$s22c_n := s22m_n \cdot \left(\cos\left(s22a_n \cdot \frac{\pi}{180}\right)\right) + \left[s22m_n \cdot \left(\sin\left(s22a_n \cdot \frac{\pi}{180}\right)\right)\right]$$

freq =

	0
0	0.1
1	0.898
2	1.696
3	2.494
4	3.292
5	4.09
6	4.888
7	5.686
8	6.484
9	7.282
10	8.08
11	8.878
12	9.676
13	10.474
14	11.272
15	12.07

[Convert to normalized admittance representation]

Go := 0.02 mho [1/(50 Ohms)]

$$y11c_n := \frac{\left[\left(1 - s11c_n\right)\cdot\left(1 + s22c_n\right) + s12c_n\cdot s21c_n\right]}{\left[\left(1 + s11c_n\right)\cdot\left(1 + s22c_n\right) - s12c_n\cdot s21c_n\right]} \qquad y12c_n := \frac{\left(-2\cdot s12c_n\right)}{\left[\left(1 + s11c_n\right)\cdot\left(1 + s22c_n\right) - s12c_n\cdot s21c_n\right]}$$

$$y21c_n := \frac{\left(-2\cdot s21c_n\right)}{\left[\left(1 + s11c_n\right)\cdot\left(1 + s22c_n\right) - s12c_n\cdot s21c_n\right]} \qquad y22c_n := \frac{\left[\left(1 + s11c_n\right)\cdot\left(1 - s22c_n\right) + s12c_n\cdot s21c_n\right]}{\left[\left(1 + s11c_n\right)\cdot\left(1 + s22c_n\right) - s12c_n\cdot s21c_n\right]}$$

[Conversion formulas from P.J. VanWijnen book "On the Characterization and Optimization of High Speed Silicon Bipolar Transistors", Cacade Microtech, page 40, (1995)]

$$OutputSusceptance_n := Im\left(y22c_n\right)\cdot Go \quad \text{[mhos]}$$

$$OutputCapacitance_n := \frac{\left(OutputSusceptance_n\cdot 10^{12}\right)}{\left(2\cdot\pi\cdot freq_n\cdot 10^{9}\right)} \quad \text{[picoFarads]}$$

$$OutputConductance_n := Re\left(y22c_n\right)\cdot Go \quad \text{[mhos]}$$

$$OutputResistance_n := \frac{1}{OutputConductance_n} \quad \text{[Ohms]}$$

$$InputSusceptance_n := Im\left(y11c_n\right)\cdot Go \quad \text{[mhos]}$$

$$InputCapacitance_n := \frac{\left(InputSusceptance_n\cdot 10^{12}\right)}{\left(2\cdot\pi\cdot freq_n\cdot 10^{9}\right)} \quad \text{[picoFarads]}$$

$$InputConductance_n := Re\left(y11c_n\right)\cdot Go \quad \text{[mhos]}$$

$$InputResistance_n = \frac{1}{InputConductance_n} \quad \text{[Ohms]}$$

[Assemble output data file]

$Characteristics_{n,0} := freq_n$

$Characteristics_{n,1} := InputSusceptance_n$

$Characteristics_{n,2} := InputCapacitance_n$

$Characteristics_{n,3} := InputConductance_n$

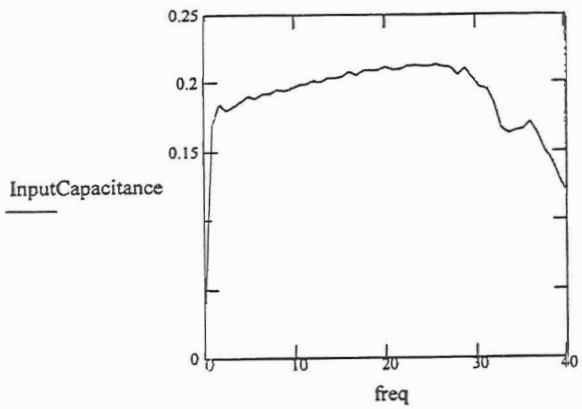
$Characteristics_{n,4} := InputResistance_n$

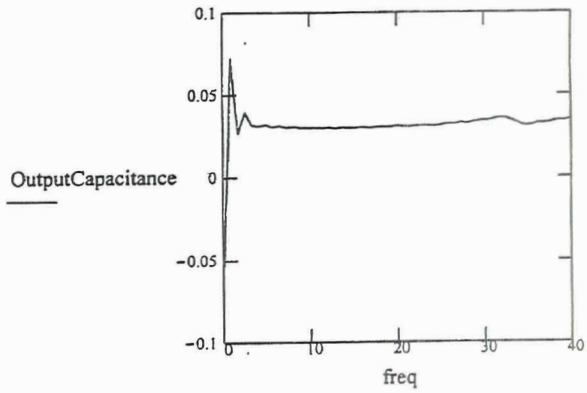
$Characteristics_{n,5} := OutputSusceptance_n$

$Characteristics_{n,6} := OutputCapacitance_n$

$Characteristics_{n,7} := OutputConductance_n$

$Characteristics_{n,8} := OutputResistance_n$





$$U_n := \frac{(y21c_n - y12c_n)^2}{4\cdot(Re(y11c_n)\cdot Re(y22c_n) - Re(y12c_n)\cdot Re(y21c_n))}$$

[W. Liu's book, "Handbook of III-V HBTs"; eqn 8_257, (1998)]

$$UMAG_n := 10\cdot\log\left(\sqrt{Re(U_n)^2 + Im(U_n)^2}\right) \cdot dB$$

$$h21_n := \frac{\left[-\left(2 \cdot s21c_n\right)\right]}{\left(1 - s11c_n\right) \cdot \left(1 + s22c_n\right) + s12c_n \cdot s21c_n}$$

(VanWijnen, page_40)

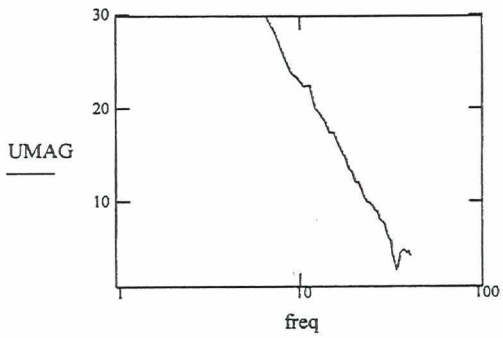
$$h21MAG_n := 20 \cdot \log\left(\sqrt{Re\left(h21_n\right)^2 + Im\left(h21_n\right)^2}\right) \text{ dB}$$

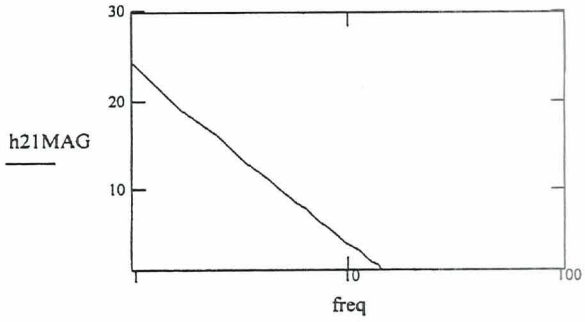
h21MAG =

	0
0	47.284
1	25.499
2	19.079
3	16.184
4	13.29
5	11.64
6	9.981
7	8.605
8	7.779
9	6.455
10	5.746
11	4.879
12	4.069
13	3.591
14	3.191
15	2.412

UMAG =

	0
0	30.599
1	33.951
2	43.87
3	35.182
4	34.494
5	39.71
6	40.32
7	38.321
8	29.975
9	28.212
10	25.93
11	23.999
12	23.37
13	22.465
14	22.592
15	20.232





$Characteristics_{n,9} := h21MAG_n$

$Characteristics_{n,10} := UMAG_n$

[Write data file to disk]

F:\..\Characteristics

Characteristics

Appendix 2
PSpice Deck Used for the Analysis of the Class E Amplifier

```
* Class E, with a switch. 15 Dec. 2000

.TRAN 0.5PS 100NS 99.5NS 0.5PS
.OPT ITL5=0
SW 3 0 21 0 SWITCH
VSIG 21 0 SIN 0 5.0 5.8GHZ
LDC 3 4 200NH
CP 3 0 0.145PF
CS 3 5 0.058PF
LS 5 7 13.0NH
Lmatch 7 6 1.6NH
RLOAD 6 0 34.0
VDC 4 0 12.0V
CBYP 4 0 100PF

.MODEL SWITCH VSWITCH (RON=12.0 ROFF=100000)

.PROBE
.END
```