Development of low-noise high value chromium silicide resistors for cryogenic detector applications

Murzy Jhabvala [a], NASA/Goddard Space Flight Center, Greenbelt, Maryland 20771
Sachi Babu, Ball Aerospace Technologies Corp.,Greenbelt, Maryland 20771
Carlos Monroy, Raytheon ITSS, 4500 Forbes Blvd., Lanham, Maryland 20706
C. Darren. Dowell, California Institute of Technology, 320-47, Pasadena, California 91125

Extremely high sensitivity detectors, such as silicon bolometers are required in many NASA missions for detection of photons from the x-ray to the far infrared regions. Typically, these detectors are cooled to well below the liquid helium (LHe) temperature (4.2K) to achieve the maximum detection performance. As photoconductors, they are generally operated with a load resistor and a pre-set bias voltage, which is then coupled to the input gate of a source-follower Field Effect Transistor (FET) circuit. It is imperative that the detector system signal to noise performance be limited by the noise of the detector and not by the noise of the external components. The load resistor value is selected to optimize the detector performance. These two criteria tend to be contradictory in that these detectors require load resistors in the hundreds of megaohms, which leads to a higher Johnson noise. Additionally, the physical size of the resistor must be small for device integration as required by such missions as the NASA High Resolution Airborne Wide-Band Camera (HAWC) instrument and the Submillimeter High-Angular Resolution Camera (SHARC) for the Caltech Submillimeter Observatory (CSO). We have designed, fabricated and characterized thin film resistors using a CrSi/TiW/Al metal system on optical quality quartz substrates. The resistor values range from 100MΩ to over 650MΩ and are Johnson noise limited at LHe temperatures. The resistor film is sputtered with a sheet resistance ranging from 300Ω/□ to 1600Ω/□ and the processing sequence developed for these devices allows for chemically fine tuning the sheet resistance in-situ. The wafer fabrication process was of sufficiently high yield (>80%) providing clusters of good resistors for integrated multiple detector channels, a very important feature in the assembly of these two instruments.

[a] Electronic mail: murzy.jhabvala@gsfc.nasa.gov

I. INTRODUCTION

NASA, the Department of Defense and the international astronomy community has extensively relied on highly sensitive infrared (IR) detectors for more than three decades. Over the years, the detectors have evolved in both sensitivity and technology, from germanium bolometers to composite silicon bolometers, to extrinsic photoconductors, to micromachined silicon membranes and recently to 2-dimensional "pop-up" bolometer arrays [1] (not to mention the proliferation of large format arrays). However, the basic methodology for operating these discrete photoconductors has remained essentially unchanged. The detector is cooled, the most sensitive detectors being cooled the most, a load resistor is connected in series, a bias voltage is applied and the signal is extracted, as shown in figure 1 below. This method has been used in the Infrared Astronomical Satellite (IRAS), NASA's Cosmic Background Explorer (COBE), numerous DoD missions, many ground-based astronomy telescopes and is

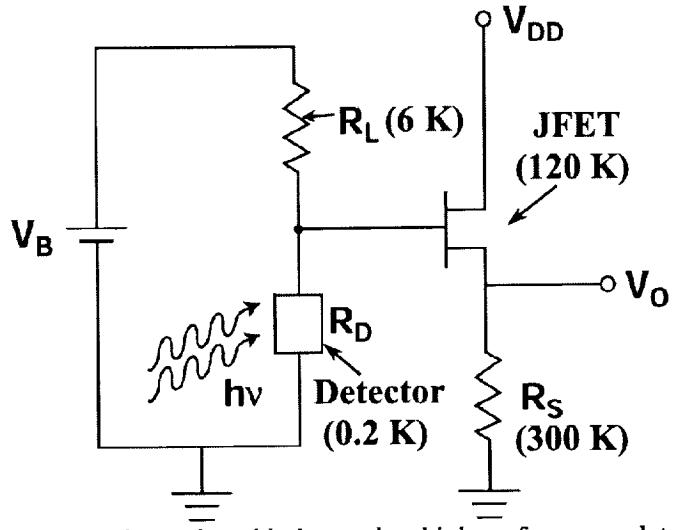

FIG 1. Source-follower JFET circuit employed in low noise, high performance detector systems.

currently the method to be employed by the future High Resolution Airborne Wide-Band Camera (HAWC) to be installed on the SOFIA (Stratospheric Observatory for Infrared Astronomy) Boeing 747 aircraft astronomy platform and by the ground based Submillimeter High-Angular Resolution Camera (SHARC) to be installed on the Caltech (California Institute of Technology) Submillimeter Observatory (CSO). ASTRO-E is a future NASA mission, which

has similar load resistor-preamp requirements. HAWC will be a facility instrument providing users with the best angular resolution in the 40-300 micrometer IR spectral region. It is intended to provide data on a wide range of astronomical phenomenon, such a, star formation in our own and in distant galaxies[2]. The HAWC instrument development is a highly collaborative effort between the University of Chicago, California Institute of Technology and NASA's Goddard Space Flight Center (GSFC). The SHARC instrument is a collaborative effort between Caltech and GSFC also intended to search for and provide data about extragalactic source emissions [3]. Both instruments are based on the recently developed "pop-up" bolometer MEMS technology developed by H. Moselely and C. Allen of the Goddard Space Flight Center[1]. The circuit in Figure 1 is simple in principle but extracting the maximum performance from the detector can be quite challenging. During operation, incident radiation is absorbed by the detector, which responds by undergoing a change (decrease) in impedance. The instantaneous detector voltage, $V_{D,}$ is simply:

$$V_D = \left[\frac{R_D}{R_D + R_L}\right] V_B$$

and the output voltage V_O, is

$$V_O = G\, V_D,$$

where G is the gain of the source-follower and generally ranges from 0.8–0.98. To obtain the maximum sensitivity, the detector signal-to-noise ratio must be limited by the detector noise and not by the noise from other system components. The most egregious noise offenders tend to be the load resistors and the JFET and to minimize this effect extraordinary designs are implemented. The JFETs are carefully evaluated to locate their optimum operating temperature. The resistors are designed so that their value (typically 10-20 times the detector dark resistance) optimizes the detector responsivity and must be fabricated to be Johnson noise limited. For the HAWC an SHARC instruments this translates to individually screened JFETs operating at 110K, resistors of 350-450MΩ for HAWC and 100-200MΩ for SHARC operating near 4.2K. Both instruments are baselining a focal plane array of 12 x 32 (384) detector elements, each detector requiring a load resistor and JFET. This paper will describe the development of the load

resistors for these projects at NASA's Goddard Space Flight Center. We will describe the design, fabrication, assembly and present test results of resistors we fabricated.

II. DESIGN AND FABRICATION

A custom resistor pattern was developed to bracket the desired resistance values of 100-200MΩ for SHARC and 350-450MΩ for HAWC. However, the critical performance metric is the noise of the device at its operating temperature and should be Johnson noise limited. Experiments were conducted to determine the minimum CrSi film thickness we were confident would not introduce excess noise as the resistors were processed (dicing, for example), assembled and cryogenically cycled. This film thickness would then drive the resistor design. The minimum CrSi thickness we implemented was nominally around 570Å yielding a resistivity of 1.06-1.16KΩ/□. Another constraint was the yield consideration. Each instrument requires 384 individual load resistors, which is further complicated by the various operating temperatures required of the three components (detector, load resistor and JFET). The detectors are located at the focal plane and operate at T<0.06K. The JFETs will be operated at 110K and the load resistors will operate near the liquid helium bath temperature of 4.2K. The three components are electrically connected but must be kept thermally isolated yet remains in close proximity to each other. To accomplish this, the load resistors and JFETs are mounted on their own ceramic carrier boards and then interconnected using the Goddard developed silicon bridge chip technology [4]. Each instrument contains 384 detectors electrically divided into three groups of 128 channels. The 384 JFETs are individually "hand" mounted onto a ceramic board and then cryogenically rescreened and replaced, if necessary. The resistors can be mounted in groups of up to 32 (depending on the contiguous yield) so conceivably one board can be populated with just four resistor segments as opposed to 128 individual die. Therefore one of the resistor design considerations is selecting an appropriate geometry which achieves the desired resistance value in the allotted real estate but keeps the line width large enough to maximize the yield. These two constraints lead to a serpentine structure in a rectangular area of 25 mils by 1100 mils. The lines and spaces are drawn at 4.0 microns and each resistor has 3,425 segments for a total of approximately 425,000□s. The 25-mil width was an instrument constraint to meet a 25-mil channel-to-channel pitch. Each resistor was designed to have a single bond pad at one end and

three bond pads at the other end to provide for resistance tapping at the full value, 2/3 full value and 1/3 full value to bracket the required values for both the SHARC and HAWC instruments. Additionally, each resistor is assigned a unique identification number, which is absolutely critical during wafer probing, dicing and assembly. A photomicrograph of one such resistor is shown in figure 2.

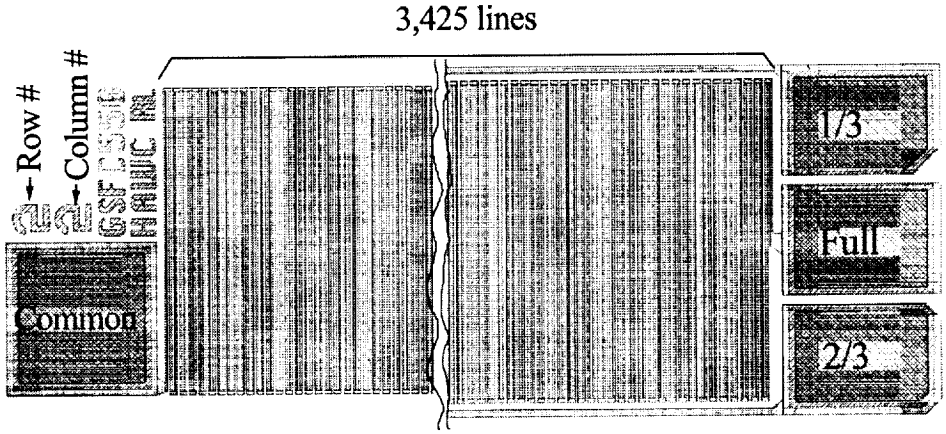

FIG 2. Computer-aided drawing of the resistor illustrating some of the design attributes.

Since the resistor consumes such a vast stretch of substrate and the value is so large, the substrate capacitance is a concern. Depositing the film on a standard SiO_2/Si system proved to be to capacitive. However, had we used very high resistivity silicon (operating at 4.2K) the capacitance would be greatly reduced. We chose instead to use 4-inch diameter quartz wafers, since we have used this substrate for other high value resistor developments (NiCr/quartz) with excellent results. CrSi is sputter deposited on the quartz substrate from a 60:40 ratio of silicon to chromium target. The approximate deposition time is 60 minutes with the wafers rotating at 5rpm. At this stage, the film resistivity is 800-900Ω/□. After depositing the CrSi 500Å, of TiW followed by 10KÅ of Al with 1% silicon are deposited. The first mask and etching defines the bond pads and removes the overlaying metals from the CrSi film. A second mask defines the resistor pattern. After the photoresist is removed, the wafers are probed and if the resistor value is too low (i.e., the CrSi film is too thick) the entire resistor pattern can be further etched and monitored until the desired resistivity is achieved. We have typically adjusted the resistivity to between 1000 and 1200Ω/□ at this stage. Finally, 2000Å of low temperature oxide is deposited

and the bond pad areas opened. The etchant for the CrSi film is a mixture [5] of H_3PO_4, HNO_3 and HF in a ratio of 60:5:1.

III. RESULTS

Since these devices are to be integrated into a flight detector assembly, there are additional screening criteria other than just functional performance. The additional criteria include:

1. Johnson noise limit performance at cryogenic temperatures
2. Voltage and temperature coefficients (R vs. V and R vs. T)
3. Contiguous device yield
4. Device to device matching
5. Cryogenic cycling

A. Temperature, voltage and noise performance

The test resistors were mounted in a large 1.5"x.75" Kovar header. Although directly mounted on the LHe cold surface, there was a substantial thermal rise to the resistors and temperature sensor, which was mounted, on the topside of the package. The dewar used for these tests is multipurpose and the wiring harness posed a substantial thermal load The lowest temperature we were able to achieve during the actual noise measurements was 10K. Our noise measurement system is in an isolated screen room, which prevents LHe transfer. However, the DC resistance measurements were taken in proximity to our helium source and therefore we were able to refresh the reservoir as necessary. These DC measurements were made at 5K.

After assessing functionality at room temperature, 77K and 5K, the noise performance of the resistors was evaluated. In the past, we have encountered excess noise (from otherwise good resistors) as a result of wafer processing methods. Some problems have been the noise generated when an interface oxide layer is inadvertently introduced between the metal films and a second problem has been the introduction of microcracks in the resistor film from wafer dicing, thermal stresses and improper handling. Drawing on our past experience with thin film NiCr resistors we had previously fabricated, we encountered no excess noise in these CrSi resistors at the test temperatures of 300K, 77K and 10K. We also did not see additional noise as a function of

resistor bias voltage. We did observe a voltage and temperature coefficient (at 5K) which will be described. The resistors and JFETs were mounted inside a liquid helium cryostat. A series of DC electrical tests were first performed. Measurements of the JFET gain (>.95), resistance and resistance vs. bias were made at room temperature (T=295K), 77K and 5K. The plots of figure 3 show the resistance as a function of temperature and bias. Three resistors (arbitrarily R1, R2 and R3), each nominally 280MΩ at 295K were measured. The resistors R1 and R2 were measured as a combined series pair and R3 was measured as a single 280MΩ resistor. The measurement method used a voltage source in series with a nanoammeter to measure the resistor current.

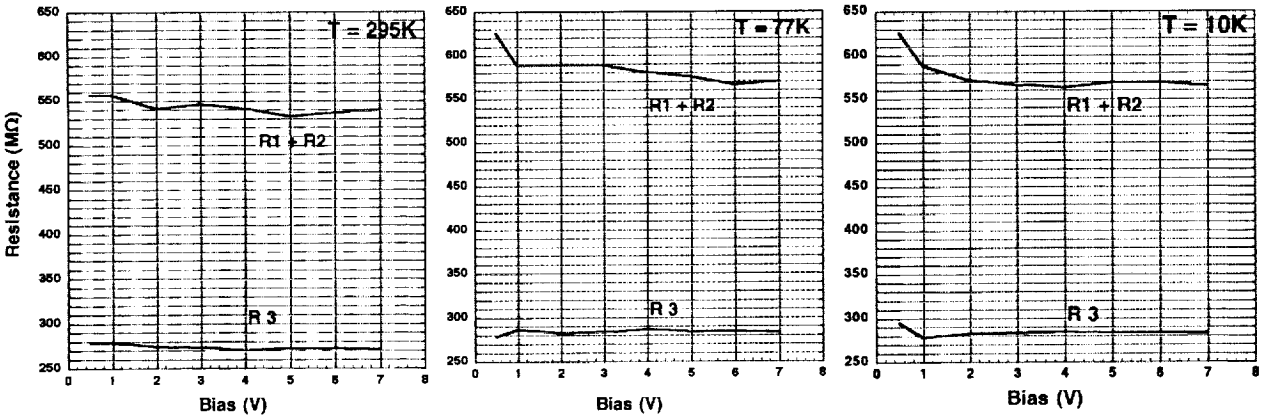

FIG 3. Resistance as a function of voltage at T=295K, 77K and 10K for a single 280 MΩ resistor and two resistors in series totaling 560 MΩ.

The thermal coefficient of resistance (TCR) for these devices is calculated from

$$a = \frac{1}{R_0}\left(\frac{dR}{dT}\right)$$

For R_0 equal to the room temperature resistance, α ranges from $-1\text{x}10^{-4}$/K to $-4\text{x}10^{-4}$/K. However, the resistance was highest at 77K and therefore the TCR from 77K to 5K is positive ($\approx 4\text{x}10^{-4}$/K).

The voltage coefficient, VCR, at a specific temperature is similarly defined as

$$a = \frac{1}{R_0}\left(\frac{dR}{dT}\right) = \frac{R(V_2) - R(V_1)}{R(V_1)(V_2 - V_1)}$$

The accuracy of the ammeter at very low bias voltage levels made it difficult to obtain a near zero bias resistance. However, over the 1-7 voltage range the VCR was typically $\approx 5\text{x}10^{-3}$/V. Over the range of the detector operation where the current through the resistor is almost constant

this represents an insignificant variation. Upon completion of these DC tests, noise spectra were obtained. The Johnson noise voltage, V_n, is given by

$$V_n = \sqrt{4kTBR}$$

where,

k=Boltzmann's constant, 1.38×10^{-23} W-sec/K

T =temperature (K)

B = measurement bandwidth

R = resistor value

The frequency spectrum of concern is that below 200 Hz and of particular concern is the low frequency performance below 30 Hz. In the first test one end of the 280MΩ was grounded inside the dewar and the noise was measured with the JFET source-follower connected to an Ithaco 1201 amplifier (gain set to 20) and an HP 35670A signal analyzer. Figure 4 shows the noise spectrum at three temperatures normalized to unity bandwidth and gain.

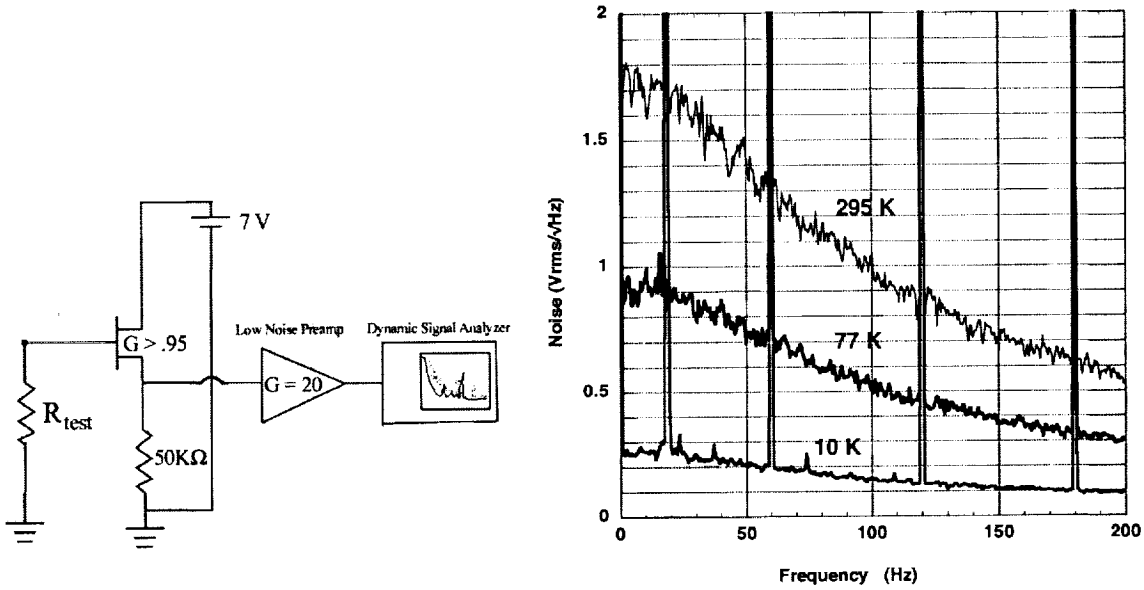

FIG 4. The test configuration and noise spectra for a single 280 MΩ CrSi resistor at T=295K, 77K and 10K.

The calculated values are listed below for the single 280MΩ resistor.

T(K)	Vn(μV/Hz$^{1/2}$)
295	2.13
77	1.09
10	0.4

These values are in excellent agreement with the acquired data at frequencies below ≈20Hz. The noise voltage attenuation as a function of frequency is a result of the shunting capacitance across the 280 MΩ resistor. The condition where RC= 1/2πf occurs at the frequency where the voltage is reduced to .707 of the DC or low frequency value. From the noise spectra this frequency is between 60-80Hz corresponding to a capacitive load of 5.6pF-7.5pF. This is essentially the parasitic capacitance of the resistor-JFET combination.

Evaluation of the effect of bias voltage on the resistor noise was performed using the second circuit configuration shown below in fig 5.

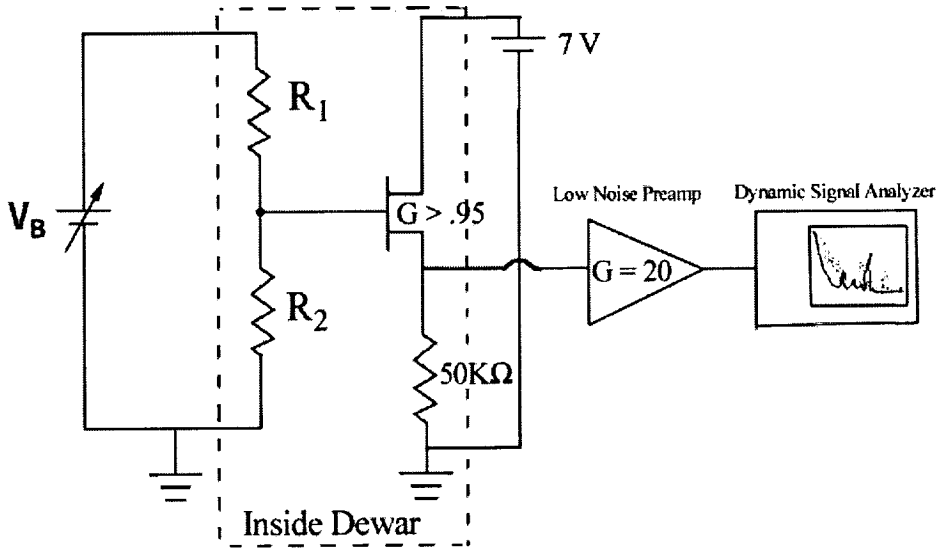

FIG 5. JFET source-follower configuration with dual resistors each 280 MΩ used for evaluating the effect of bias voltage on the resistor noise.

Two resistors on the same quartz die were connected to a battery source and the noise spectra were obtained for three bias voltages; 0.5, 1.0 and 5.0 volts. Since the resistors were of equal value 1/2 of the bias was dropped across each element. This test was performed at room temperature, 77k and 10K. The effective noise voltage is now determined from the parallel resistance value of 140 MΩ. The calculated noise voltages for the 140 MΩ resistor combination for the three test temperatures are:

T(K)	Vn(μV/Hz$^{1/2}$)
295	1.5
77	0.77
10	0.28

The noise spectral plots are shown below in figure 6.

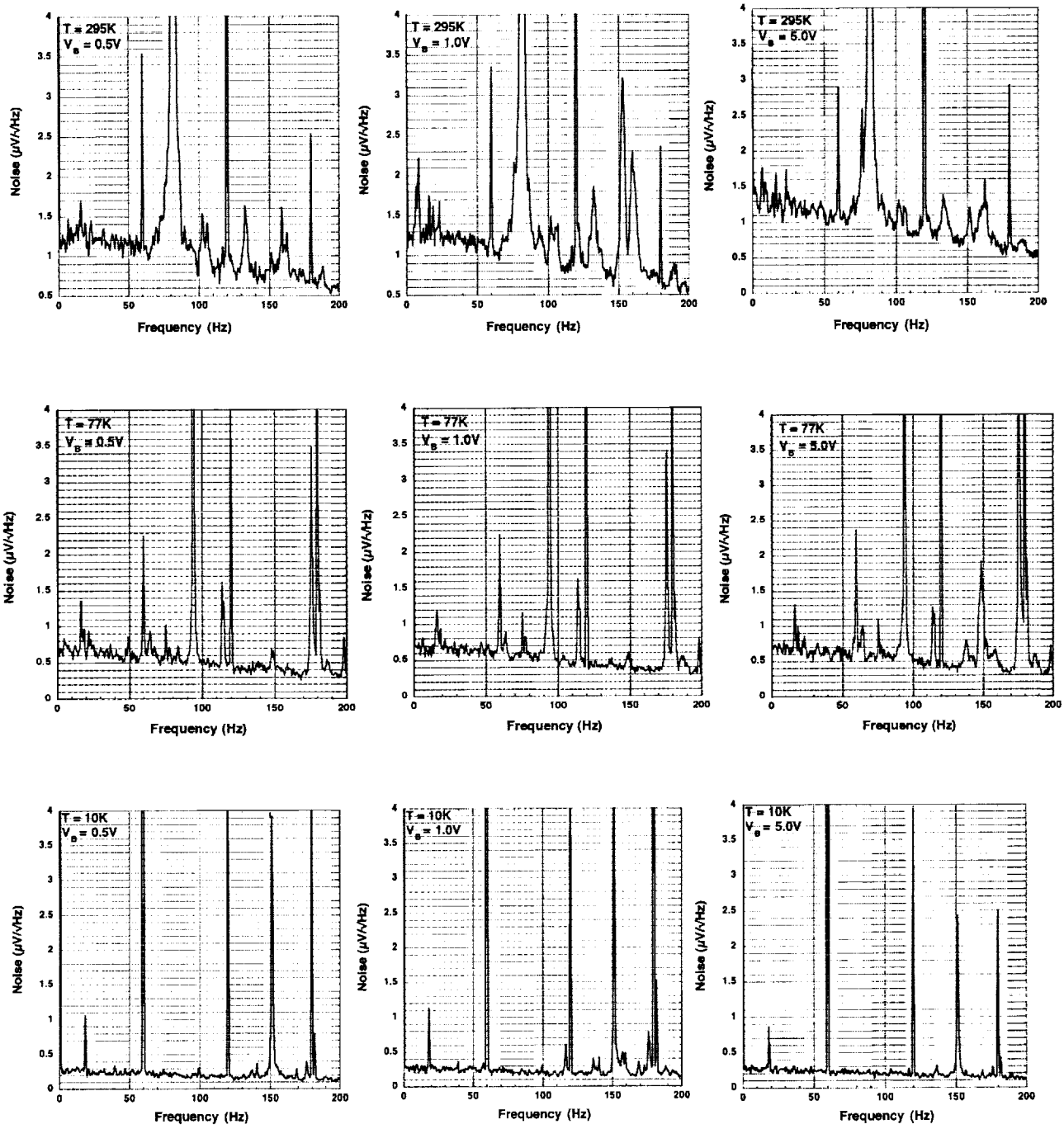

FIG 6. The noise spectra as a function of resistor bias (VB=0.5, 1 and 5 volts) at T= 295K, 77K and 10K.

Of particular note is the invariance of the spectra amplitude with increasing bias voltage from 0 to 5.0 volts (2.5 volts across each resistor). The acquired data is in excellent agreement with the calculated data at low frequencies. Most of the large spikes are the 60 Hz and harmonics which are omnipresent in terrestrial test configurations. There are other spurious noise spikes that result from the dewar microphonics and external electrical equipment emissions.

B. Device yield and uniformity

Six different runs were processed in addition to the test lots needed to establish a baseline process. The wafers were entirely processed in the Detector Development Laboratory at NASA's Goddard Space Flight Center. Each lot contained between 2 and 6 quartz wafers. As mentioned, there are three taps on each resistor and in the case of the SHARC instrument, which required resistors of 100 -200MΩ, the 1/3 tap was used. Since the quartz substrate is a 4-inch diameter wafer there are three rows of resistors. The top and bottom rows each contained an average of about 70 potential candidates. The central row had 140 candidates for a total of 280 potentially good die per wafer. As an example of functional yield the table below lists values of four wafers from the sixth lot.

Lot M6	**Good/Bad Die**	**(R_{avg} = 125MΩ)**	
Wafer	**Top Row**	**Center Row**	**Bottom Row**
1	74/5	133/7	44/9
2	77/1	134/6	57/2
3	75/4	137/4	55/2
4	74/4	137/4	56/4

The average yield of these wafers was 1053/1105 or 95.3. From these numbers it is apparent that there were numerous groups where there were 30 or more contiguous good die. In the design of the instruments each group of 64 channels share the same bias. The uniformity requirement was ±5% around a nominal value for these groups of 64 resistors. We did have several contiguous segments of 30 or more die and plenty of smaller segments meeting this specification.

A nominal value of 350-450MΩ is required for the HAWC and therefore the full resistance is required. In this case, the yield, although not quite as high as the 1/3 tap (which is to be expected) was still excellent as shown in the table below.

Lot M5 **Good/Bad Die** **R_{avg} = 417MΩ**

Wafer	Top Row	Center Row	Bottom Row
1	52/18	106/10	32/15
2	57/15	108/15	53/6
3	63/15	118/21	53/7
4	77/9	122/18	61/6

The average yield of these wafers was 902/1057 or 85.3%. Referring to Lot M6, wafer 2 (the highest yielding wafer) a breakdown of the contiguous die yield is given below. The table identifies the number of segments that contained only good die.

Top Row (78 die)

# of Good Die/Segment	# of Segments
39	1
38	1
<38	0

In other words, one die midway in the top row was the only rejection in this row.

Middle Row (140 die)

# of Good Die/Segment	# of Segments
60	1
26	1
10 – 12	4
<10	0

Bottom Row (59 die)

# of Good Die/Segment	# of Segments
28	2

On this wafer the resistance values ranged from 109MΩ to 166 MΩ. In a given row, however, the variation amongst any contiguous 12 die was a maximum of 6% between the high and low value and in some cases less than 0.5%.

C. Cryogenic cycling

During the course of an instrument build, many components of a cryogenic system will be subjected to numerous cooling cycles throughout its mission lifetime. In some cases, many dozens of thermal cycles may be encountered, in more extreme cases only a few cycles may be permitted. In any case, the devices will experience some number of thermal cycles and it is expected and generally required that not only will the devices survive mechanically but that their stability also remain unchanged or at the very least highly predictable. To this end two quartz strips containing nine resistors were epoxy mounted to a HAWC load resistor ceramic board. After a 100C epoxy cure and cool the resistors were directly immersed into LN2, thermally equilibrated to 77K and then removed. The resistors were then rapidly brought to room temperature with the help of a heat gun. This process was repeated for a total of 10 LN2 soaks. Generally, the cooldown from room temperature to 77K will manifest any failures due to thermal

shocks. If a device survives this test we have high confidence that the device will remain mechanically stable throughout cryogenic cycling. The resistance of all nine devices was measured initially in June, 2000, then again immediately before the first LN2 immersion on October 26, 2000 and again after the tenth immersion in LN2 also on October 26, 2000. All nine resistors were within .5% of their initial value, the variability of the measurement system. In March of 2001 we again measured the value of each resistor and then immersed the sample into LHe, allowed time for equilibration then removed and brought the device to room temperature (with the aid of the heat gun). We repeated this sequence for five LHe soaks and then remeasured the resistors. To within our measuring accuracy each of the nine resistors was exactly the value we had measured in June, 2000.

III. SUMMARY

The need for high value, integrated resistors capable of operating at liquid helium temperatures has been a nagging issue for decades in the astronomy and low temperature physics communities. Although resistors are technologically one of the least complex electronic components their evolution has not kept pace with advanced detector technology. We have presented results indicating we have breached the gap between resistor technology and detector technology. The CrSi resistors we have fabricated can easily exceed 250 MΩ, operate at low temperatures, can be integrated on silicon, quartz or sapphire substrates and can be manufactured with high yield using relatively standard IC photolithograhic processes.

As part of our future efforts to improve detector performance we will be integrating these resistors directly with silicon microbolometer arrays not only improving system performance by Locating the resistors in close proximity to the detector but by also reducing the wire interconnects that are sources of microphonic noise generation. The overall resistor production is relatively inexpensive and the manufacturing time relatively short.

Acknowledgement

The authors would like to express their appreciation to Harvey Moseley, Dave Franz, Frank Peters, Carol Sappington, Peter Shu, Wayne Smith, George Voellmer and Arlin Bartels...

[1] S. H. Moseley, Jr., C.D. Dowell, C. A Allen and T.G Phillips, ASP Conference Series **217**, 140, edited by J. G. Mangum and S. J. E. Radford (2000).

[2] A. Harper et al, Proceedings of SPIE, **4014**, 43 (2000).

[3] D. Dowell, S. H. Moseley and T. Phillips, ASP Conference Series **217**, 105, edited by J. G. Mangum and S. J. E. Radford (2000).

[4] C. Allen, S. H. Moseley, D. S. Schwinger and D.E. Franz, presented at Nanospace 1998, Houston, Texas.

[5] L. Maissel and R. Glang, *Handbook of Thin Film Technology* (McGraw-Hill 1970).