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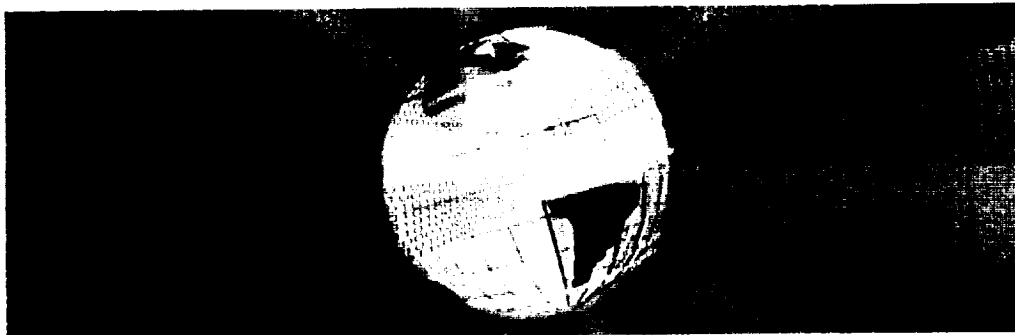
Proceedings

# Non-Volatile Memory Technology Symposium 2001

<http://nvm.jpl.nasa.gov>

*Humphrey's Half Moon Inn  
2303 Shelter Island Dr., San Diego, California*

*November 7-8, 2001*



**National Aeronautics and  
Space Administration**

**Jet Propulsion Laboratory  
California Institute of Technology  
Pasadena, California**

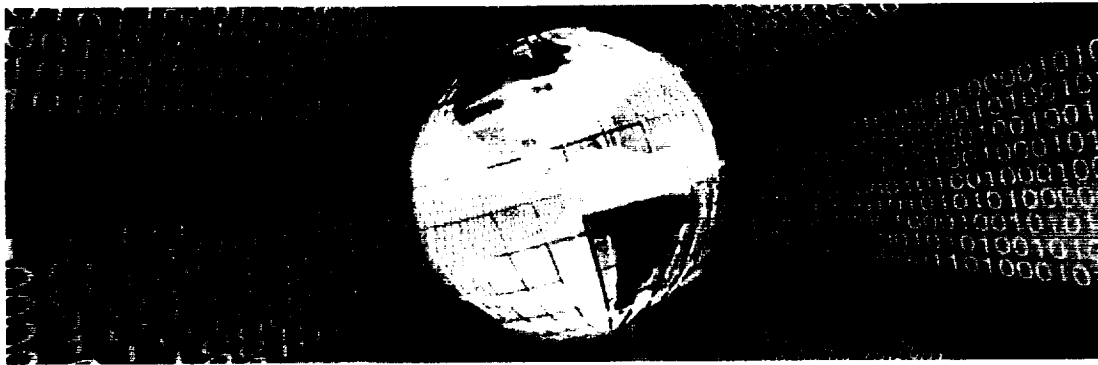




## Proceedings

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**November 7-8, 2001**

**Humphrey's Half Moon Inn  
2303 Shelter Island Dr., San Diego, California**

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# **Non-Volatile Memory Technology Symposium 2001**

**November 7-8, 2001**

**Humphrey's Half Moon Inn  
2303 Shelter Island Dr., San Diego, California**

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## WELCOME

On behalf of NASA's Jet Propulsion Laboratory, the Center for Integrated Space Microsystems, the Remote Exploration and Experimentation Project, and all who worked so hard to make this Symposium happen, we bid you Welcome to the Second Annual Non-Volatile Memory Technology Symposium.

Our first Symposium, held last year in the Washington, DC area was a resounding success. In those 28 papers and talks presented by two keynote speakers, our audience learned about many new and exciting things: developments, processes, applications, and problems.

This year's meeting promises to be even better.

Just months ago we received notification from not one, but two, IEEE Societies, of their recognition and co-sponsorship of this event. What this brings to us is an acknowledgment by our peers that Symposia such as this do, indeed, carry to the forefront all the hard work that our Speakers present to you today.

This Symposium was founded on the basis of being open to all Non-Volatile Memory technologies, not just focusing on one or the other ñ cross-pollination, from Process to Design, Discipline to Implementer, and all places in between, will occur. We hope that the talks we have selected for you over these next two days are both informative and compelling: that they have the right mixture of detail and brevity, interest and applicability.

A copy of the Program follows.

For such a young undertaking, this is our second year, we are indeed flattered of the interest we have received by journals, academia, and industry. We begin each day with a Keynote address by leaders renowned for the vision: Leon Alkalai of JPL, and Lew Cohn of DTRA. Each day also includes four specially invited talks: ideas that we find fascinating, clearly in the forefront of technology, and of benefit to all.

We have broken the Symposium into 6 sessions, each chaired by a person well-regarded in Academia and Industry. We begin with *Innovative Concepts*, chaired by Jimmy Zhu of Carnegie-Mellon University, followed by *Environment, Reliability & Characterization*, chaired by Alan Johnston of the Jet Propulsion Laboratory. We conclude Day 1 with *Processing*, chaired by Marvin White of Lehigh University.

We commence Day 2 with *Applications*, chaired by Scott Anderson of SEAKR Engineering, and *Emerging Technologies* chaired by Scott Tyson of the Air Force Research Laboratory. We conclude the day and the Symposium with *Magnetic Memories* chaired by Jimmy Zhu.

As with all Symposia or Conferences, it is important to pay tribute to the Authors and Contributors of these fine papers; if it were not for the hard work of these fine folk, we would not be here today.

Like any fledgling enterprise, certain bumps will occur on the road to success. We encourage your thoughts and comments, please see anyone of us to help us make your stay pleasant and informative. At the back of this publication, you will find a short survey, please complete and return it at your leisure.

Please take a moment to visit our Industrial Exhibitors.

See you next year at IEEE NVMTS2002.

Taher Daud  
General Chair

Nazeeh Aranki  
Publications Chair

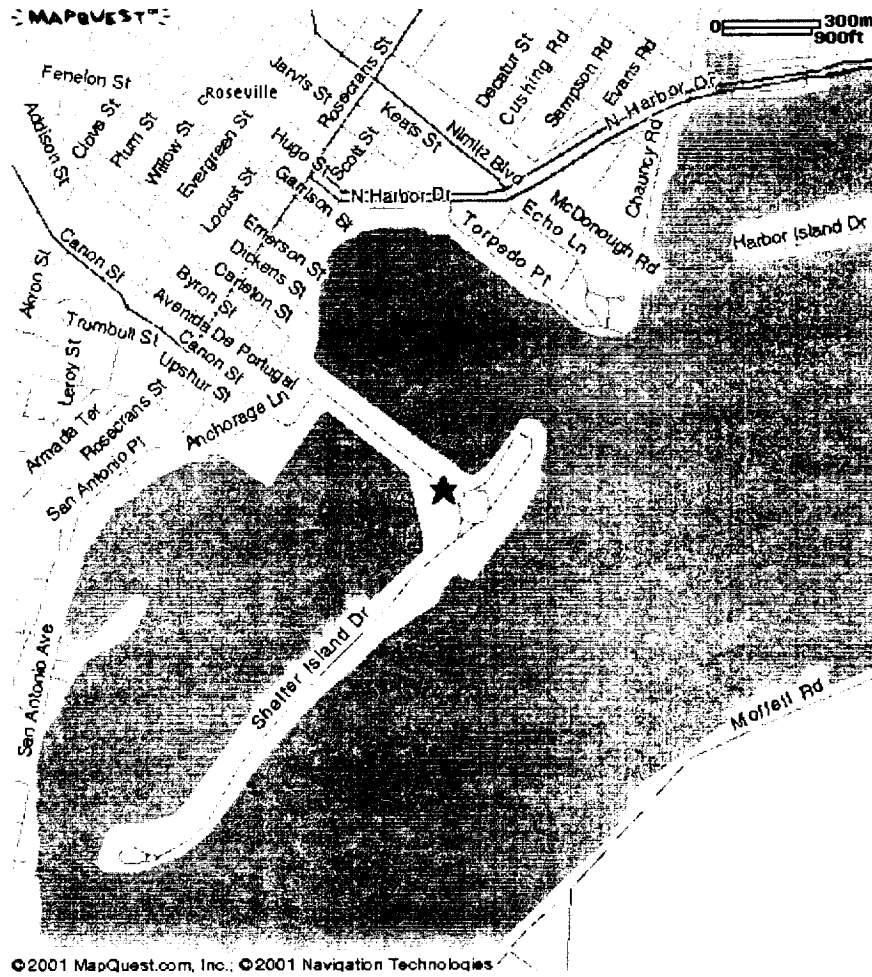
Karl Strauss  
Program and Technical Chair

**TUESDAY Nov 6**  
 6:00pm to 8:00pm **REGISTRATION RECEPTION**

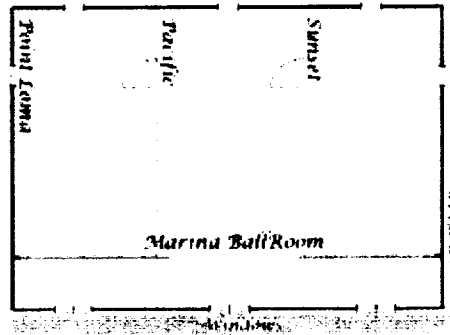
<b>WEDNESDAY Nov. 7</b>	
8:45	Introduction & Welcoming Address
9:00	[1] Keynote Address: Developments from the Center for Integrated Space Microsystems; <i>L Alkalai, Jet Propulsion Laboratory</i>
9:40	[2] Invited Talk: MEMS Memory Elements; <i>R Carley, Carnegie-Mellon University</i>
10:10	[3] Invited Talk: Integrating EEPROM, Resistor, Capacitor, PIN Diode, Schottky Diode and Bipolar Modules into a 0.35 micron CMOS process optimised for Low Voltage Applications; <i>J Ellis, Zarlink Semiconductor</i>
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	<i>INNOVATIVE CONCEPTS, J Zhu, Carnegie-Mellon University, Chair</i>
10:50	[4] Nonvolatile Rad-Hard Holographic Memory; <i>T-H Chao, JPL</i>
11:10	[5] A New Concept for Non-Volatile Memory: The Electric-Pulse Induced Resistive Change Effect in Colossal Magnetoresistive Thin Films; <i>A Ignatiev, Univ. of Houston</i>
11:30	[6] High-Density Ferroelectric Memories Using a One-Transistor Cell; <i>D Kamp, Cells Semiconductor</i>
12:00	<b>LUNCH</b>
1:00	[7] Invited Talk: Requirements and Usage of NVM in Advanced Onboard Data Processing Systems; <i>R Some, Jet Propulsion Laboratory</i>
1:20	[8] Invited Talk: Europa Orbiter Mass Memory Requirements and Status; <i>D Karmon, Jet Propulsion Laboratory</i>
	<i>ENVIRONMENT, RELIABILITY &amp; CHARACTERIZATION, A Johnston, Jet Propulsion Laboratory, Chair</i>
1:40	[9] Space Radiation Effects in Advanced Flash Memories; <i>A Johnston, Jet Propulsion Laboratory</i>
2:00	[10] Reliability and Radiation Characterization of an SOI EEPROM/Flash Memory Cell; <i>C Tabbert, Peregrine Semiconductor</i>
2:20	[11] Evaluation of Data Retention Characteristics for Ferroelectric Random Access Memories; <i>A Teverovsky, Goddard Space Flight Center</i>
2:40	<b>BREAK</b>
3:00	[12] Radiation Response of Emerging FeRAM Technology; <i>I Schmalz, Jet Propulsion Laboratory</i>
3:20	[13] Characterization of Scaled SONOS NVSM Devices for Space and Military Applications; <i>S Wrazien, Lehigh University</i>
3:40	[14] Overview of Non-Volatile Testing and Screening Methods; <i>F Iron, Jet Propulsion Laboratory</i>
4:00	[15] An FPGA-based Test-bed for Reliability and Endurance Characterization of Non-Volatile Memory; <i>J Patel, Jet Propulsion Laboratory</i>
	<i>PROCESSING, M White, Jet Propulsion Laboratory, Chair</i>
4:20	[16] Copper Wire Interconnect Integration into 1um single poly EEPROM technology; <i>Shelton, Alantec Corporation</i>
4:40	[17] Process Optimization for MOCVD of SrBi2Ta2O9 for Non-Volatile Memory Applications; <i>D Burgess, Alantec Corporation</i>
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9:40	[20] Invited Talk: Drivers, Accelerators and Inhibitors for Solid State Drive Markets; <i>R Andrei, Web-Foot Research</i>
10:10	[21] Invited Talk: NonVolatile Memory Systems Design: Concept-to-Reality & Trades Along the Way; <i>S Anderson, SEAKR Engineering</i>
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11:10	[23] Neo-Stacking of Packaged Flash Memory; <i>K Gann, Irvine Sensors</i>
11:30	[24] High Speed MRAM Buffer for High Capacity Nonvolatile Shock Recorders; <i>R Sinclair, NVE Corporation</i>
12:00	<b>LUNCH</b>
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1:20	[27] <i>Phase Development of Dense, Non-Volatile Memories for Space Applications; [REDACTED] Semiconductor</i>
1:40	[28] <i>Commercialization of 1T-Cell Ferroelectric Memories for Space Applications; [REDACTED] Semiconductor</i>
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2:40	[30] Vertical Magnetoresistive Random Access Memory: Promises and Challenges; <i>J Zhu, Carnegie-Mellon</i>
3:00	[31] Criteria for Magnetic Tunnel Junctions; <i>B Jonsson-Akerman, University of California at San Diego</i>
3:20	[32] A Modified MRAM Cell Architecture without a Current Rectifier per Cell; <i>F Wang, University of North London</i>
3:40	<b>END of SYMPOSIUM</b>

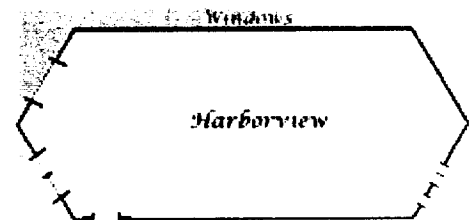
## Map of Surrounding Area



## Conference Facilities



NVMT 2001  
Symposium  
Site



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## *Keynote Addresses*

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*L. Alkalai, JPL*

Thursday, November 8

9:00 AM      Non-Volatile Memory Technology for Space and Missile System  
Application: Past, Present, and Future; *L Cohn, DTRA*

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# MEMS Memory Elements

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Department of Electrical and Computer Engineering, Carnegie Mellon Univ., Pittsburgh PA 15213 USA

**Abstract**— This paper presents a design example that illustrates the potential of microelectromechanical systems (MEMS) to perform the mechanical positioning required for addressing stored data and to enable an entirely new mechanism for reading and writing magnetic data. Specifically, MEMS sensors and actuators can be used to achieve active servo control of the separation between magnetic probe tips and a media surface with sub-nanometer accuracy. This allows mechanical position to be used to selectively write magnetic marks in a continuous thin-film magnetic media. In addition, MEMS sensors can be used to measure the separation between a magnetic probe tip and the media with a noise floor of roughly 22 picometers, allowing them to be used as position sensors in a magnetic force microscope (MFM) style data detection system.

MEMS-based mass storage devices could enable many new applications capable of exploiting the low entry cost and extremely small size of these new hybrid devices; e.g., “intelligent” appliances, sophisticated teaching toys, biomedical monitoring devices, civil infrastructure monitoring devices, micro- and nano-satellites, highly-integrated archival storage systems, highly-secure storage systems, etc.. For many of these applications the needed computing power is already available at low cost. What has kept many of them from becoming a reality is the lack of low cost mass data storage device storing a few gigabytes of data and costing only \$10-\$20.

The technologies needed to build these hybrid devices are already emerging, making it likely that a broad market for MEMS-positioned nonvolatile rewritable **mass** storage devices will develop within the next five years. This paper examines one approach to creating a MEMS-based data storage technology being developed in the Center for Highly Integrated Information Processing and Storage Systems (CHIPS) at Carnegie Mellon University.

In this paper, we will first describe the design of a MEMS media positioning system. Next, we will describe a MEMS probe tip positioning system that can control the spacing between the probe tip and the media. We will discuss the feasibility and performance of using electrostatic actuation and capacitive sensing to actively control the height of each probe tip with respect to the media. Then, we will describe an approach to creating a large array of permanent magnet nanometer size probe tips. Finally, we will describe results of computer simulation of both the writing and reading processes for this type of MEMS-positioned permanent magnet probe based mass storage device.

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3. PROBE HEAD POSITIONING
4. MAGNETIC PROBE RECORDING HEADS
5. SYSTEM PERFORMANCE SIMULATION
6. CONCLUSIONS
7. ACKNOWLEDGMENTS

## 1. INTRODUCTION

Mass data storage devices in which data is addressed by positioning some form of storage media with respect to an array of sharp probe tips using microelectromechanical systems (MEMS) have the potential to create a whole new storage technology capable of achieving a quantum decrease in entry cost, access time, volume, mass, power dissipation, failure rate, and shock sensitivity when compared with today’s hard disk drives. At the same time, MEMS-based mass storage devices have the potential to achieve a cost / bit stored that is one to two orders of magnitude cheaper than that of patterned nonvolatile storage technologies; e.g., EEPROM, MRAM, FeRAM, etc. This is because they do not rely on lithography to precisely define a data storage cell – they rely on mechanical positioning for addressing.

## 2. MEDIA POSITIONING

Microelectromechanical systems (MEMS) are being developed as actuators for positioning the media in new mass-manufactured silicon-based non-volatile storage devices at a number of companies and research universities; e.g., IBM [1], HP [2][3], Kionix [4][5] and CMU [6]. In general, all of these approaches include

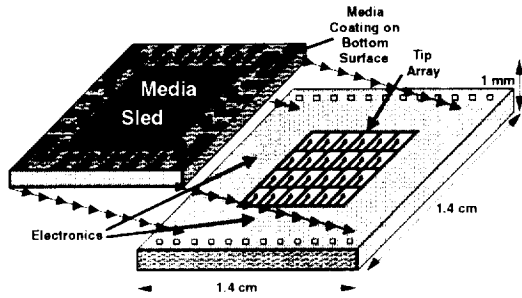


Fig. 1: Conceptual diagram MEMS-Actuated data storage devices with X-Y motion of the media and Z motion of the Probe Tip for a 4x5 array of Probe Tips with electrostatic actuators.

some form of storage media on the surface of a large nearly flat micromachined plate that is suspended by springs and moved in X and Y as a result of the force generated by electrostatic, piezoelectric, or magnetic actuators. The micromachined plate has the potential to move with nanometer resolution because there are no rubbing mechanical contacts between components and hence, there are no stiction problems. For structures with micrometer dimensions, the surface area to volume ratio is high; therefore, stiction forces between any two surfaces that touch (e.g., the surfaces in any mechanical bearing) are extremely large and make precise positioning nearly impossible.

Unfortunately, most MEMS spring suspension systems exhibit repeatable linear motion only for deflections that are a small fraction of their length (typically 10%). In order to scan data stored on the entire media plate, a large array of probe tip read / write heads is necessary. As long as the pitch of the array in X and Y is smaller than the peak motion of the media plate in X and Y, then the complete media area can be used for data storage. Fig. 1 illustrates a simplified diagram of a MEMS-actuated probe-based storage device constructed from two silicon wafers that are bonded together.

Because the cost to manufacture devices using a VLSIC photolithographic fabrication process is roughly proportional to the total area of the device, one important figure of merit for MEMS-actuated data storage devices is the percentage swept area, which we define to be the fraction of the total area of the die containing the probe tip array that can be addressed by all of the tips. For a fixed minimum line width used to define the springs, the maximum deflection achievable in an electrostatically actuated media positioning system rises roughly as the square of the X or Y dimension of the overall structure. Therefore, bigger actuators and bigger media plates result in higher percentage swept areas.

A simplified conceptual layout of one proposed media actuator is shown in Fig. 2. The anchors (black squares) in the four corners are all connected to the media sled. They are held near electrical ground and a high-frequency

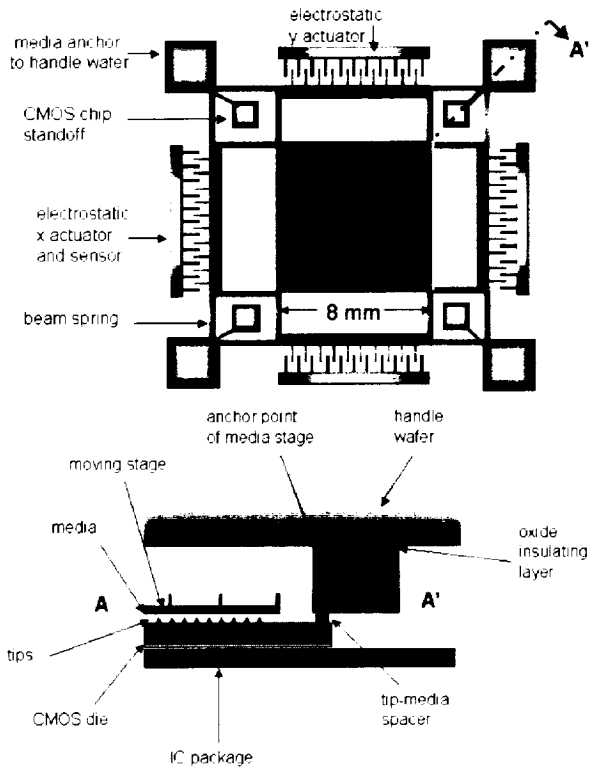


Fig. 2: Simplified pictorial diagram of the MEMS media actuator. Below is a cross-section illustrating how the single crystal silicon actuator wafer can be assembled onto an IC with an array of probe tips.

excitation signal is applied in order to allow capacitance measurements to be made. The comb-like structures on the four sides are the actuator stators. Both the media anchors and the actuator stators are bonded to the underlying silicon wafer that holds the probe tip array and the CMOS electronics in a wafer-to-wafer bonding process. This avoids hand assembly of individual devices. X and Y positioning will be performed by a closed-loop control system that senses the position of the stage by measuring the capacitance of each actuator using high frequencies and controlling the force of each actuator by applying a low frequency signal.

This design for the media actuator is based on a decoupled-mode X-Y microstage originally conceived for use as a vibratory-rate gyroscope [12]. A box-spring suspension is used to decouple the two in-plane directions of actuation so that comb fingers can be used for X and Y actuation without mechanical interference. High-aspect-ratio silicon structures allow the actuator to remain extremely flat even though it is a large structure. In addition, in order to decrease the mass of the media plate, much of the mass is etched away leaving only stiffening beams to maintain flatness. The high aspect ratio also greatly diminishes the vertical motion resulting from external accelerations of the device. Note that the fabrication and operation of the media actuator have been described further by Carley et al [6].

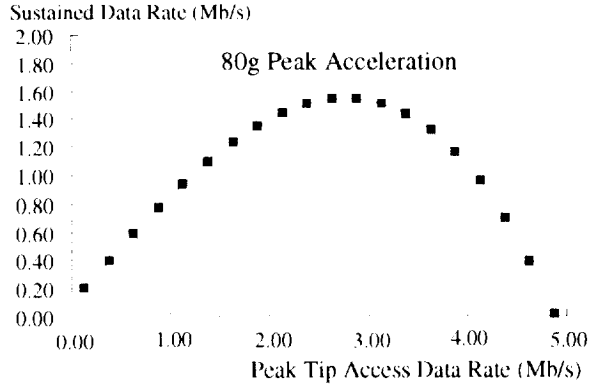


Fig. 3: Overall sustained data rate as a function of the actual probe tip reading and writing data rate (assumes probe makes no limit on data rate).

Because there is a maximum voltage that can be applied to the actuator, there is also a maximum acceleration that can be imparted to the media plate. In this design, peak operating voltages for the actuators are 120V which generates a peak acceleration of roughly 80g's. It is important to realize that there is an optimum individual probe tip data rate for any Cartesian storage device subject to a maximum acceleration limit (see Fig. 3). For a 100 $\mu$ m-stroke Cartesian media plate and an 80g acceleration limit, probe tip data rates above 3Mb/s actually result in a lower average data rate. This is because the media plate spends a disproportionate time decelerating and turning around after reading an individual track, and, because higher probe tip data rates require higher linear velocity for a given data bit size (see [13]).

### 3. PROBE HEAD POSITIONING

Most mechanisms for reading and writing data bits require the probe tip to be extremely close to the media (typically much closer than the mark size). Therefore, some mechanism must be provided to allow all of the large array of probe tips to come into near contact with the media simultaneously. Most approaches to this problem place each probe tip on the end of a mechanical beam that can move in the  $Z$  direction. Passive schemes simply bring the array of probe tips and the media together until there is contact between all of the probe tips and the media [1]. Wear of the probe tips and the media is minimized by keeping the spring constant of the cantilevers low and keeping the difference between tip heights small.

One major advantage of magnetic recording as a storage mechanism is that physical contact between the probe tip and the media is not required – a soft or hard magnetic probe tip need only be brought to within a fraction of the recorded mark size to allow reading and writing [7]. In this section we describe a methodology for precisely

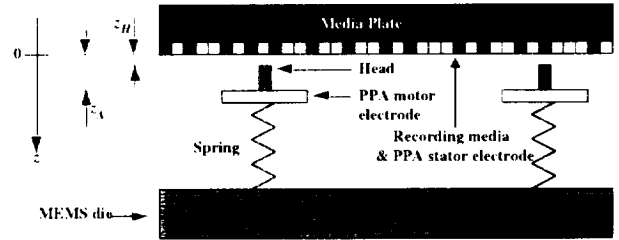


Fig. 4: General approach of using a parallel plate capacitor for both  $Z$  position sensing and  $Z$  actuation.

controlling the probe-tip to media spacing with sub-nanometer accuracy.

Our approach to MEMS-based probe-tip height control is shown conceptually in Fig. 4. Each permanent magnetic probe recording head is carried by an independent  $Z$  actuator which controls its head-to-media spacing. Each actuator consists of a spring and an electrostatic parallel-plate electrostatic actuator (PPA) [10]. The recording media acts as the PPA's stator electrode. It is common to all head actuators. The PPA electrodes can also be used to capacitively sense the distance from the media to the motor electrode. This is an extremely nonlinear feedback control system, and providing stable feedback control can be difficult. See [11] and [14] for a discussion of the control system design.

One implementation of a simple head actuator structure is shown in Fig. 5. This figure also shows an SEM of such a device fabricated using the "poly-release" CMOS MEMS process developed at Carnegie Mellon University [8]. The PPA motor electrode is 40 $\mu$ m by 40 $\mu$ m, and the feedback loop is designed to hold the plate to media spacing at a value of approximately 230nm. In this head actuator design, the spring is implemented by a pair of cantilever beams in order to provide sufficient stiffness against lateral and rotational motion. Each beam is 200 $\mu$ m long, 1.8 $\mu$ m across, and 4.1 $\mu$ m high. Note that the laminated structural material fabricated in the CMU CMOS MEMS process [9] has an intrinsic vertical stress gradient which cause the spring to curl out of plane by several microns (curl is visible in Fig. 5).

Writing with a permanent magnetic probe tip at the end of this cantilever can be achieved by simply modulating the spacing between the magnetic probe tip and the media. This suggests that we want a  $Z$  suspension that has a high resonant frequency in order to allow writing at a high data rate. In our initial prototype device (see Section 5), we find that a probe-tip to media spacing of 2nm results in highly reliable written marks while a height of 11nm results in good reading resolution with an extremely low probability of causing any change in the stored pattern in the media. Note, one disadvantage of this scheme is that a separate permanent magnetic probe tip of slightly larger diameter must be used to erase a given track before it can

be rewritten. Therefore, two separate  $Z$  mechanical

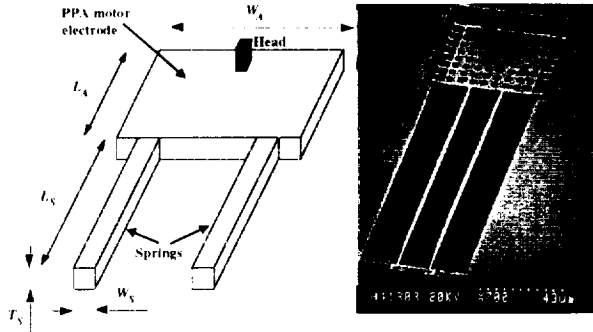


Fig. 5: MEMS implementation of parallel plate capacitor for both  $Z$  position sensing and  $Z$  actuation. Note, an SEM of such a structure is shown at right without a head in place

suspensions must be able to access the same data area – one for reading/writing and one for erasing. In essence, a stripe of data on this devices (approximately 1000 bit positions long) is like a sector on a hard disk drive. It must all be read or written at once.

When we are reading the data, we create what amounts to a magnetic force microscope. The RMS equivalent disturbance force noise due to the front end electronics noise is approximately  $38 \text{ fN}/\sqrt{\text{Hz}}$ , which gives an RMS input referred force noise floor that is about  $12 \text{ pN}$  assuming a  $50 \text{ KHz}$  bandwidth. For more details on the noise floor for this sensor, see [14]. Since the interaction force between a permanent magnetic tip and a thin-film magnetic media can be hundreds of  $\text{pN}$ , this means that we can actually read the magnetic state of the media by simply sensing the force the media exerts on the permanent magnet read/write head. Note, one other source of disturbance is the Brownian noise associated with the air between the actuator plate and the media. In this case, we are assuming that we are operating in a near vacuum and can neglect the Brownian noise contribution.

#### 4. MAGNETIC PROBE RECORDING HEADS

Optimization of the design of permanent magnetic probe heads interacting with a thin-film magnetic media would lead to an extremely high aspect ratio cylinder of permanent magnetic material. Fortunately, dropping the aspect ratio down to 4:1 causes only a small drop in the magnetic field at the tip of the probe.

In manufacturing, deposition of an array of permanent magnet probe tips could be done using the Spindt tip process [15] widely used in making field emission displays with minimum effect on the other parts of the structure. In this case we would have probe tips in the shape of a cone. Alternatively, a combination of wide area optical lithography with small area e-beam lithography can be used to cost effectively manufacture an array of photoresist dots where tips are desired down to

$50 \text{ nm}$  in diameter [16]. By using this combination of optical lithography and e-beam lithography to pattern a magnetic thin film,  $50 \text{ nm}$  diameter cylinders of a permanent magnetic material with a height of  $100 \text{ nm}$  can be created cost effectively [11].

#### 5. SYSTEM PERFORMANCE SIMULATION

In order to assess the viability of the proposed storage system, we created a detailed simulation that includes the effects of media noise, electronics noise, Brownian noise, and manufacturing variations. We generate a distribution of magnetic grain size, and orientation to match that of today's commercial vertically oriented magnetic media. Optimizing the selection of the magnetic probe tip geometry for the best signal-to-noise ratio (SNR) resulted in a cylindrical magnetic probe tip  $40 \text{ nm}$  in diameter and  $100 \text{ nm}$  in height. The track pitch was  $68 \text{ nm}$  and the bit length (with run length coding) was  $100 \text{ nm}$ . For these parameters, the simulation of 4000 recorded bits, including the up and down movement of the probe tip during writing and then a second pass scan for reading, resulted in an RMS-to-RMS SNR of  $13 \text{ dB}$  which is quite sufficient for reliable signal detection.

#### 6. CONCLUSIONS

Assuming a 20% overhead for error correction coding, the track pitch and bit pitch determined for the initial demonstration system results in approximately 1.5 million user bits being addressed by an individual magnetic probe tip that scans over a  $100 \mu\text{m}$  by  $100 \mu\text{m}$  media area. The overall system would consist of 6,400 of these individual probe tip elements, resulting in a total storage capacity of approximately 1Gbyte of user data on a  $1.4 \text{ cm} \times 1.4 \text{ cm} \times 1 \text{ mm}$  2 wafer silicon sandwich. The density of the magnetic data stored on this media is limited by thermal decay of the smaller magnetic grains over time. In our simulations, we are assuming that a 10 year lifetime is required when we set the grain size. Fortunately, researchers at companies that manufacture hard disk drives are working hard to develop thermally stable media with smaller grain sizes and as these developments become available, we would expect to be able to increase the density of data stored on MEMS-positioned magnetic-probe-based mass storage devices.

#### 7. ACKNOWLEDGEMENTS

We wish to specifically thank John Griffin, Arthur Davidson, Suresh Santhanam, Dr. Leon Abelmann, Dr. Tamal Mukherjee, and the students and staff of both CHIPS and the CMU MEMS research group who have made many contributions to the work presented in this

paper. This research was sponsored in part by the NSF under grant no. ECD-8907068, in part by DARPA under the AFRL, Air Force Materiel Command, USAF, under agreement F30602-97-2-0323, in part by the National Aeronautics and Space Administration, and in part by an NSF Graduate Student Fellowship. The United States government has certain rights to this material. In addition, we would like to acknowledge the equipment donations by INTEL and IBM that helped to support this research. More information on this project can be found at <http://www.chips.ece.cmu.edu>.

## 8. REFERENCES

- [1] M. I. Lutwyck, G. Cross, M. Despont, U. Drechsler, U. Durig, W. Haberle, H. Rothuizen, R. Shutz, R. Widmer, G. K. Binnig, P. Vettiger, "Millipede – A highly-parallel dense scanning-probe-based data-storage system," *Digest of Technical Papers, IEEE International Solid-State Circuits Conference*, pp. 126-127, Feb. 2000.
- [2] S. Hoen, P. Merchant, G. Koke, and J. Williams, "Electrostatic Surface Drives: theoretical considerations and fabrication," *Proceedings of the 9th Int. Conf. on Solid-State Sensors and Actuators (Transducers '97)*, Chicago, IL, pp 41-44, June 1997.
- [3] C. Morehouse, "A decade away: atomic resolution storage," sidebar in J. W. Toigo, "Avoiding a Data Crunch," *Scientific American*, May 2000.
- [4] J.J. Yao, S.C. Arney, and N.C. MacDonald, "Fabrication of high frequency two-dimensional nanoactuators for scanned probe devices", *J. Microelectromechanical Systems*, vol. 1, no. 1, pp. 14-22, March 1992.
- [5] T. Davis, "Realizing a completely micromechanical data storage system," *Proceedings of the IDEMA DISKCON*, Session 1, pp. 1-14, Santa Clara, CA, 21 Sept. 1999.
- [6] L. R. Carley, J. A. Bain, G. K. Fedder, D W Greve, D. F. Guillo, M. S. C. Lu, T. Mukherjee, S. Santhanam, I. Abelman, and S. Min, "Single-chip computers with microelectromechanical systems-based magnetic memory," *J. of Applied Phys.*, vol. 87, no. 9, pp. 6680-85, 1 May 2000.
- [7] I. Abelman, S. K. Khizroev, D. Litvinov, J.-G. Zhu, J. A. Bain, M. H. Kryder, K. Ramstock, and C. Lotter, "Micromagnetic simulation of an ultrasmlal single-pole perpendicular write head," *Journal of Applied Physics*, vol. 87, no. 9, pp. 6636-38, May 2000.
- [8] D.F. Guillo, S. Santhanam and L.R. Carley, "Laminated, sacrificial-poly MEMS technology in standard CMOS," *Proc. Eurosensors XIII*, The Hague, NL, pp. 339-340, Sept. 12-15, 1999.
- [9] G. K. Fedder, S. Santhanam, M.L. Reed, S.C. Eagle, D.F. Guillo, M.S.-C. Lu and L.R. Carley, "Laminated high-aspect-ratio microstructures in a conventional CMOS process," *Sensors and Actuators A*, vol. 57 pp. 103-110, 1996.
- [10] G. T. A. Kovaacs, *Micromachined Transducers Sourcebook*, New York, NY: McGraw-Hill, 1998.
- [11] D. F. Guillo, *Design of a MEMS-Based Data Storage System*. Ph.D. Thesis, Dept. of Electrical and Comp. Eng, Carnegie Mellon Univ., Pittsburgh, PA, Dec. 2001.
- [12] M. S. Kranz and G. K. Fedder, "Micromechanical Vibratory Rate Gyroscopes Fabricated in Conventional CMOS," *Proc. of the Symp. on Gyro Technology*, Stuttgart, Germany, pp. 3.0-3.8, Sept. 16-17, 1997.
- [13] Griffin, J. et. al. Modeling and Performance of MEMS-Based Storage Devices, in *Proceedings of ACM SIGMETRICS '2000*, ACM, New York, N.Y. June 2000.
- [14] L. R. Carley, Greg Ganger, David Guillo, and David Nagle, "System Design Considerations for MEMS-Actuated Magnetic Probe Based Mass Storage", *IEEE Transactions on Magnetics*, vol. 37, no. 2, pp. 657-662, March 2001.
- [15] C. A. Spindt, C. E. Holland, A. Rosengreen, and I. Brodie, Field-emitter arrays for vacuum microelectronics *IEEE Trans. Electron Devices*, vol. 38, no. 10, Oct. 1991.
- [16] Y. Kondoh, J. Seeger, and P. Merchant, Fabrication of nanoscale tungsten tip arrays for scanning probe microscopy-based devices *Journal of Microelectromechanical Systems*, Vol. 7, No. 4, pp. 428-434, Dec. 1998.

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# **Integrating EEPROM, Resistor, Capacitor, PIN Diode, Schottky Diode and Bipolar Modules into a 0.35 micron CMOS process optimised for Low Voltage Applications.**

John Ellis

Zarlink Semiconductor, Plymouth, Devon, U.K.

## **Abstract**

*We have integrated EEPROMs, resistors, capacitors, PIN diodes, Schottky diodes, an isolated NPN bipolar transistor and dual-poly gate CMOS transistors into a 0.35 micron technology. This provides low threshold voltage transistors for 1-3V battery operation, high voltage transistors for EEPROM programming and a number of passive components for mixed-signal functions. Applications for this technology include Zarlink's medical products where programmability enables complex circuits to be optimised for individual customer requirements.*

## **1. Introduction**

The integration of non-volatile memory with passive components, transistors with a low threshold voltage, PIN diodes, Schottky diodes, high voltage transistors and bipolar transistors offers a very diverse range of options for custom, mixed-signal products. We have integrated these into a new 0.35 micron CMOS technology, called ANV™\* for analogue, non-volatile, which is compatible with our core 0.35 micron digital process. It is intended for mixed signal products in a range of low power applications.

## **2. Quadruple Wells**

The core 0.35  $\mu\text{m}$  digital technology begins with the field oxide formation. The wells are implanted through the field oxide using high energy implantation, but give junction breakdown voltages of around 10-12V, for circuitry operating at 3.3V. The gate electrode on the core process is n-type polysilicon. Two key requirements for the new process were a low leakage, low threshold voltage transistor, and secondly, high voltage transistors for EEPROM programming. We incorporated high voltage wells in front of the field oxide, which also use high energy allowing a moderate thermal cycle to be used to drive them. This has enabled us to provide transistors with >18V breakdown voltage for EEPROM programming. The low voltage transistors retain their normal well implants post-field oxide. In this way the new process steps are fully modular and do not impact the core transistors.

To provide low threshold voltage transistors we used N+ and P+ poly gates for the NMOS and PMOS transistors respectively. The NMOS transistor is identical to the one on the core digital process but the PMOS is able to operate

\* ANV is a trademark of Zarlink Semiconductor Inc

with 500 mV threshold, some 200 mV lower than the partially-buried channel, digital transistor. In addition, lower leakage currents have been obtained. At longer channels the P+ gate maintains a lower threshold whereas the earlier N+ gate exhibits an increase. Fig. 1 illustrates the new transistors. The PMOS device has improved on the sub-threshold characteristics compared with the NMOS.

Fig. 2 compares the sub-threshold characteristics of the high voltage transistors.

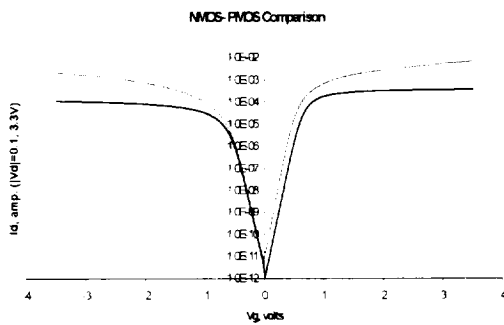


Fig. 1: Low Voltage Transistors  
Vd=0.1, 3.3V; Vg=0... 3.3V

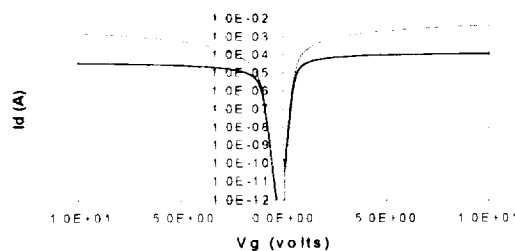


Fig. 2: High voltage transistors  
Vd=0.1, 10V; Vg=0 ... 10V

### 3. EEPROM module

The EEPROM cell we integrated into the low voltage process is a single-poly type using a tunnel oxide window for Fowler-Nordheim tunnelling for both writing and erasing. This is an ideal solution for low power non-volatile applications, and can be

supported from low current, on-chip programming voltages. The single poly process enables the EEPROM to be built as a module and fully supports the Company's double poly capacitor for analogue applications.

The cell operates with 12-14V programming voltage, typical write-erase characteristics are shown in fig. 3.

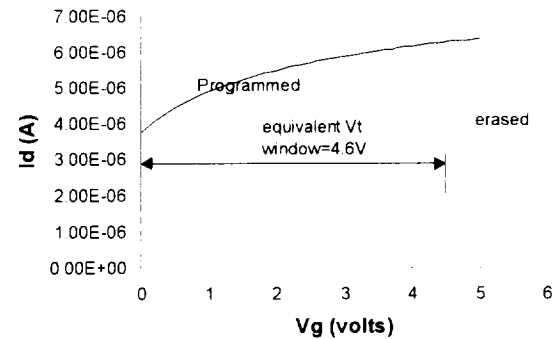


Fig. 3: EEPROM Erase and Programming Characteristics

### 4. Passive components

The number of resistors possible are so extensive we only support a sub-set. For battery operation from 1 to 3 V, and analogue circuitry, a high value resistor is desirable. We developed a 10 kohm/sq resistor in polysilicon to meet this need. Fig. 4 shows a typical resistor spread.

The resistor has a negative temperature coefficient. At high voltages, above the normal 3.3 V operating voltage, self-heating can cause the resistance to drop. For use in high voltage applications the power must be limited to avoid this effect. However, it may also serve as a temperature indicator for sensor applications.

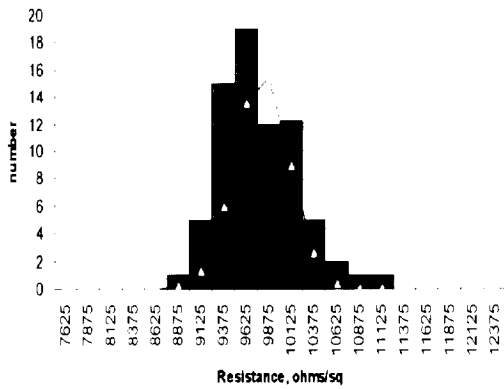


Fig. 4: High Value Resistor Distribution

In addition, several process resistors arising from the P+ poly, N+ poly, buried N layer and two sets of Nwells are supported for designers to use. The high voltage, silicide-protected LDD regions are not supported for design. Most resistors are also available silicided, which tends to give a similar value of about 3 ohms/sq. for all. These are summarised in table 1.

P+ poly	320
N+ poly	50
P+ diffusion	90
N+ diffusion	90
Nwell	1 kohm
Poly 1 HiRes	10 kohm
Silicided (all)	3 (typ.)

Table 1: Supported Resistors (ohms/sq unless stated otherwise)

Capacitors are available using the gate oxide ( $4.5 \text{ fF}/\mu\text{m}^2$ ), high voltage gate oxide

( $1.2 \text{ fF}/\mu\text{m}^2$ ) and a low parasitic, double poly component ( $0.8 \text{ fF}/\mu\text{m}^2$ ).

## 5. Bipolar transistor

For some applications bipolar transistors have advantages over MOS. Utilising the deep, retrograde, high voltage Nwell as a collector a reasonable quality isolated NPN transistor can be provided with the addition of one base implant.

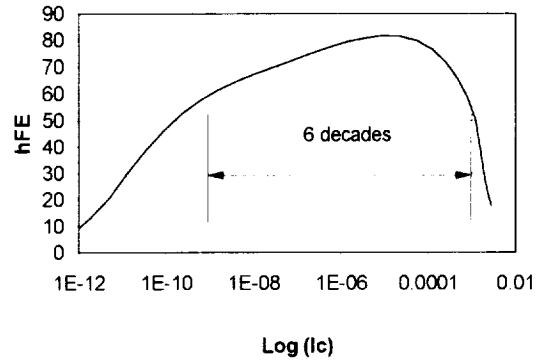


Fig. 5: Bipolar gain characteristics (Emitter  $0.6 \times 0.6$ , poly defined)

## 6. Diodes

A fully isolated "P-I-N" diode in polysilicon is available which uses the high value resistor implant for the lightly doped region, and has N+ and P+ end contact diffusions. The breakdown voltage is limited to approximately 7V but several devices can be operated in series for higher voltages.

A Schottky barrier diode is provided using the titanium barrier metallisation available in the process Fig. 6 shows typical characteristics.



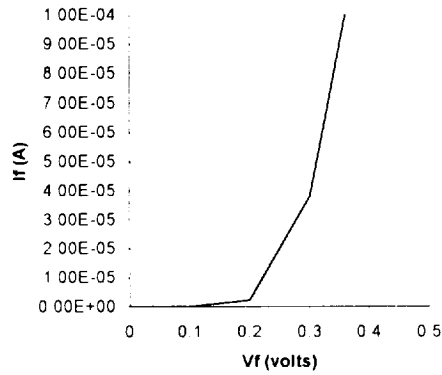
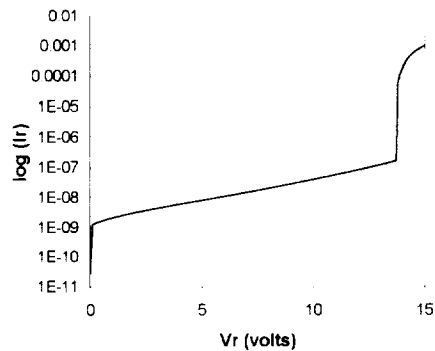


Fig. 6: Schottky Barrier Diode (top: forward; bottom: reverse) (minimum geometry)



## 7. Modular Flow

The ANV™ process is built using Zarlink's 0.35 micron core digital technology but has a number of fully modular additions to form the new components. The flow is illustrated in fig. 6, showing how the new modules may be used flexibly.

Prior to growing the field oxide, high voltage wells are implanted and driven. After growing the field oxide, the standard low-voltage (digital) wells are implanted. A number of masking stages are used to define the EEPROM coupling diffusion, dual gate oxides, bipolar and poly gate material. After poly 1 the only additional

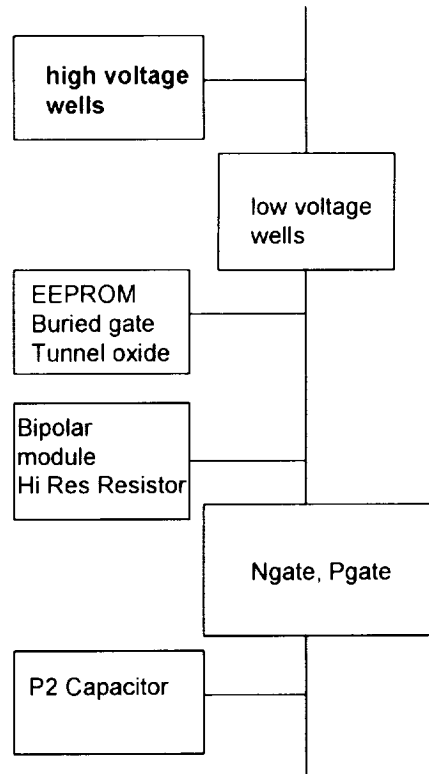


Fig. 7: Modularised Flow

module is for high voltage LDD regions. Poly 2 and low voltage LDDs are standard.

## 8. Applications

This technology is suitable for many low power applications. Test chips for logic/DSP and memory are shown in fig. 8 (a) and (b). Some applications operate from single cells and low power is key to extending the battery life.

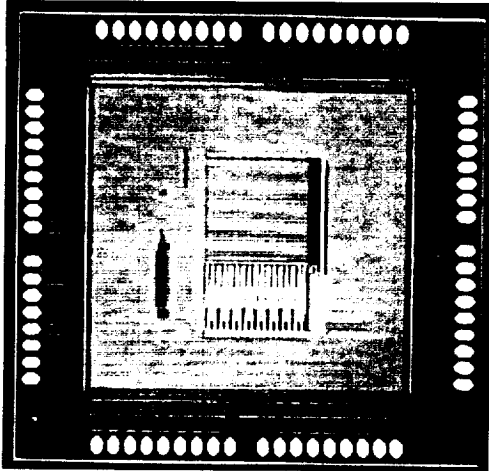


Fig 8(a) Memory Test Chip

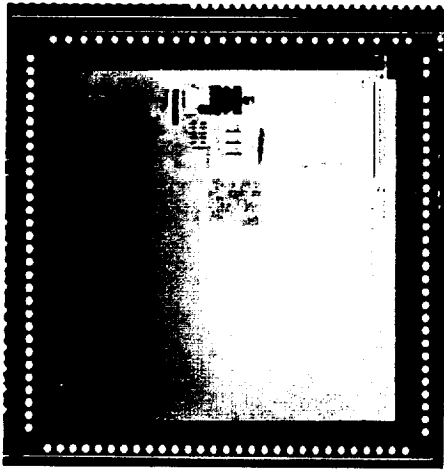


Fig.8 (b): DSP and Logic Test Chip

This represents one of the most comprehensive process extensions Zarlink has produced and is targeted to a range of consumer and industrial products in specialist areas. The high voltage components also enable the technology to be used to interface to higher rails than the nominal 3.3V core supply voltage.

#### Acknowledgement

This technology could not have been developed without the enthusiastic contributions from the team members: Clive Beech, Paul Stribley, Mark Beeley, Gary Day, Ian Macpherson, Ian Daniels and Goran Alestig, and of course the Fab personnel for processing the wafers.

## 9. Summary and Conclusions

We have described a process flow for integrating high voltage transistors, EEPROMs, dual gated MOS transistors for low threshold voltages with low leakage currents, PIN diodes, Schottky barrier diodes, bipolar transistors, high value resistor and poly 1- poly 2 capacitors for a modular technology suited to mixed signal, analogue functions.

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## ***SESSION #1: Innovative Concepts***

Wednesday, November 7, 2001

10:50 AM–12:00 Noon

Chair: *J. Zhu*, Carnegie-Mellon University

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- 10:50 AM      Non-Volatile Rad-Hard Holographic Memory; *T-H Chao, H. Zhou, G. Reyes, D. Dragoi, and J. Hanna*, JPL
- 11:10 AM      A New Concept for Non-Volatile Memory: The Electric-Pulse Induced Resistive Change Effect in Colossal Magnetoresistive Thin Films; *S. Liu, N. Wu, and A. Ignatiev*; University of Houston
- 11:30 AM      High-Density Ferroelectric Memories Using a One-Transistor Cell; *D. Kamp, A. DeVibiss, and G. Derbenwick*, Celis Semiconductor Corporation, *F. Gnadinger and G. Huebner*, COVA Technologies Incorporated

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## Nonvolatile Rad-Hard Holographic Memory

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### ABSTRACT

We are investigating a nonvolatile radiation-hardened (rad-hard) holographic memory technology. Recently, a compact holographic data storage (CHDS) breadboard utilizing an innovative Electro-optic scanner has been built and demonstrated for high-speed holographic data storage and retrieval. The successful integration of this holographic memory breadboard has paved the way for follow-on radiation resistance test of the photorefractive (PR) crystal, Fe:LiNbO<sub>3</sub>. We have also started the investigation of using 2-photon PR crystals that are doubly doped with atoms of iron group (Ti, Cr, Mn, Cu) and of rare-earth group (Nd, Tb) for nonvolatile holographic recordings.

### I. INTRODUCTION

NASA's future missions would require massive high-speed onboard data storage capability [1]. This is a particularly challenging technology issue for long-life, deep space missions. The memory technology required to support these missions have to be rad-hard and nonvolatile (i.e. no loss of stored data after power switched off). Nonvolatile memory is critical to spacecraft's ability to survive fault conditions (i.e. no loss in stored science data when spacecraft enters the "safe mode") and autonomously recover from them. In addition, this nonvolatile memory has to be rad-hard to survive the stringent space environment (e.g. very high radiation around Europa where radiation exceeding 1 Mrad). It should also operate effectively and efficiently for a very long time (10 years), and sustain at least a billion ( $10^{12}$ ) write cycles

Current technology, as driven by the personal computer and commercial electronics market, is focusing on the development of various incarnations of Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM), and Flash memories [2, 3]. Both DRAM and SRAM are *volatile*. The Flash memory, being nonvolatile, is rapidly gaining popularity. Densities of flash memory of 512 Mbits per die exist today. However, Flash memory is presently faced with two insurmountable limitations: 1) poor radiation-resistance (due to simplification in power circuitry for ultra-high density package); and 2) Limited endurance (breakdown after repeated read/write cycles).

JPL, under sponsorship from NASA Earth Science Technology Office, is currently developing a high-density, nonvolatile and rad-hard Compact Holographic Data Storage (CHDS) system to enable large-capacity, high-speed, low power consumption, and read/write of data for potential commercial and NASA space applications [4,5]. The CHDS stores data in the form of holograms inside a photorefractive (PR) crystal. In operation, pages of holograms would be recorded and retrieved with random access and high-speed. Since these holographically recorded images are stored in three dimensions and uniformly spread out throughout the entire recording volume, massive redundancy is built into the holograms, and the stored data would not suffer from imperfections in the media or point defects. This massive redundancy forms the basis for

radiation-resistance. On the other hand, recent advances in new photorefractive material research make it possible to extend the lifetime of the holograms recorded in PR crystals from months to decades or longer [6]. The nonvolatile, rad-hard characteristics of the holographic memory will provide a revolutionary memory technology to enhance the data storage capability for all NASA's Earth Science Missions.

In this paper, we will first briefly report the most recent progress in developing this CHDS at JPL. Ongoing and future research effort in developing nonvolatile rad-hard photorefractive recording materials will then be discussed in detail.

## II. CHDS BREADBOARD DEVELOPMENT AND EXPERIMENTAL DEMONSTRATION

JPL has recently built a fully functional book-size CHDS breadboard using liquid crystal SLM as beam steering device [4,5]. Figure 1a shows the CHDS architecture, and Fig. 1b is a photograph of the CHDS breadboard. In this breadboard we have implemented a 1-D scanning scheme using a single beam steering SLM (from Boulder Nonlinear System, Inc.) which is capable of recording 128 resolvable holograms to date. A LabView based system controller has been developed to perform holographic data recording/retrieval in an autonomous manner.

We have successfully performed hologram recording/retrieval demonstrations using this breadboard. During this experiment, we have utilized a sequence of grayscale images of the near earth asteroid, Toutatis, as the input. A few retrieved images from the holograms recorded in the  $\text{LiNbO}_3$ , presenting the Toutatis viewed in several aspect angles, are shown in Figure 2.

In the next step, a pair of this BSSLM will be cascaded to enable 2-D scanning of the reference beam to increase the number of stored holograms. This 2-D beam multiplexing would result in a total of 11,520 resolvable scanning angles. Thus it will enable the storage of more than 11,000 pages of holographic data within a  $1\text{-cm}^3$  volume of a PR crystal. The total storage capacity, when using a  $1000 \times 1000$  pixel size SLM as input device, would exceed 10 Gbs. Further increase the input frame size (e.g.  $5000 \times 5000$  pixels) would further increase the memory size to 250 Gbs.

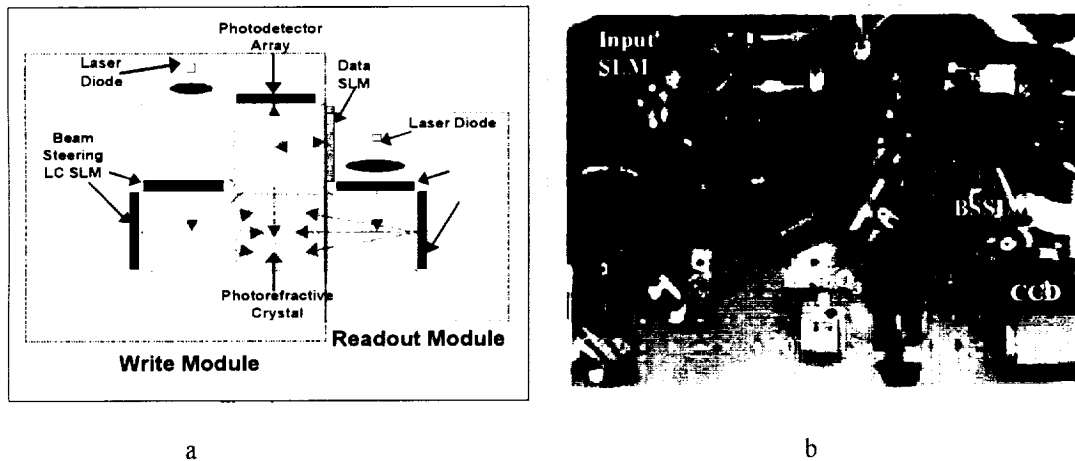


Figure 1a. System schematic architecture of an Advanced Holographic Memory  
 1b. A book-sized CHDS breadboard under development at JPL.

The potential of stacking a multiple of very compact holographic memory cubes on a memory card (e.g. 10 x 10 cubes on each card) will provide up to 1 terabits storage capacity per card. The transfer rate ranges from 200 Gbs/sec (with nematic liquid crystal BSSLM) to 2000 Sec/sec (with ferroelectric liquid crystal BSSLM). In summary, primary advantages of this holographic memory system include: high storage density, high transfer rate via randomly accessible E-O beam steering, compact and ruggedness, low voltage and low power consumption.

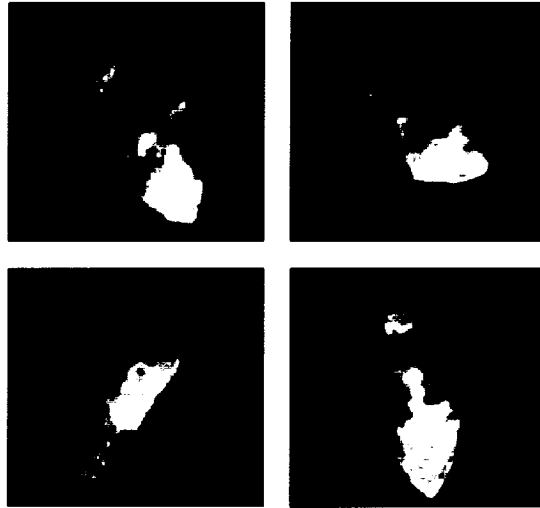


Figure 2 Experimental results showing retrieved holographic images of asteroid Toutatis.

### III. NONVOLATILE PHOTOREFRACTIVE MATERIAL

Recently, technology breakthrough in extending storage lifetime of photorefractive memory from months to decades or longer have been reported by researchers at Caltech and elsewhere. A new type of two-photon recording material, doubly doped  $\text{Fe:Mn:LiNbO}_3$ , has been developed. This material possesses a deep traps partially filled with electronics and a shallow (intermediate) traps to trap photo-generated electrons with very long lifetime. Doubly doped extrinsic dopants ( $\text{Fe}^{2+}$ ,  $\text{Mn}^{2+}$ ) would provide this intermediate state. As illustrated in Figure 3: During recording, a first photon (from an ultraviolet light source) is used to excite an electron from the Valence band to an intermediate state. A hologram writing photon is then used to bring the electron up to the Conduction band. The electron will then migrate and get trapped to record the interference pattern. During readout, the readout beam will readout the hologram but is with insufficient energy to elevate the electron to the conduction band. Hence the stored hologram will not be erased during readout.

More recently, more doping ions from the iron group ions (Ti, Cr, Mn, Cu) [6] and the rare-earth group ions (Nd, Tb) [7] have been investigated for nonvolatile performance in a  $\text{LiNbO}_3$  crystal. To date, it has been reported that doubly doped  $\text{Cr:Cu:LiNbO}_3$  as well as  $\text{Fe:Tb:LiNbO}_3$  are effective in nonvolatile holographic recordings.

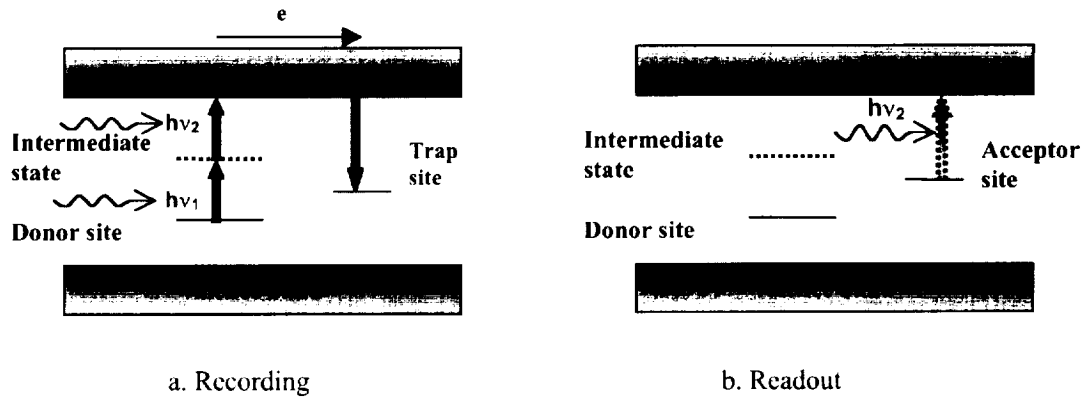


Figure 3. Two-photon nonvolatile hologram a) recording and b) readout

We have recently started the investigation of the holographic performance of new two-photon PR  $\text{LiNbO}_3$ . We are in the process of acquiring  $\text{LiNbO}_3$  crystals doped with various 2-photon dopants and concentration (e.g.,  $\text{Fe:Mn:LiNbO}_3$ ,  $\text{Cr:Cu:LiNbO}_3$ ,  $\text{Fe:Tb:LiNbO}_3$ , and  $\text{Ce:Mn:LiNbO}_3$ ). Once acquired we will insert them into a holographic memory testbed for nonvolatile data storage performance evaluation. The holographic memory testbed under assembling for testing the nonvolatile data storage capability of candidate 2-photon PR crystals is shown in Figure 4. An iterative test procedure will be developed during the test of the doubly doped  $\text{LiNbO}_3$  PR crystal. The dopant type and concentration of the PR crystal will be altered for maximum nonvolatile memory performance. The selected PR crystal will then go through radiation tests until the optimum combination is identified.

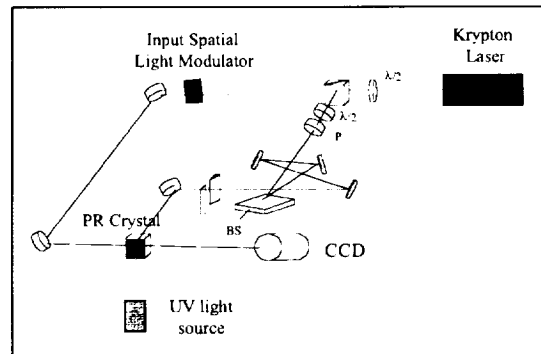


Figure 4. Experimental set up for holographic recording using 2-photon PR crystal (Krypton laser for holographic recording and readout, UV light source for flood gating)

#### IV. EVALUATION OF RAD-HARDNESS OF PHOTOREFRACTIVE CRYSTAL

The radiation environment in space depends strongly on location, and is composed of a variety of particles with widely varying energies and states of ionization [8-11]. The major types of radiation that are potentially hazardous to memory systems (electronic and holographic) include high-energy photons (X-ray, gammas), neutrons, and charged particles (electrons, protons, alpha particles, heavy ions). The parameters, which determine the amount of damage introduced by a particle, are the rest mass (e.g. zero for protons), the energy and the charge state (e.g. electronics are negative, protons and alphas are positive. Ions can even be multiply charged).

The radiation in space has a degrading effect on the microelectronic devices. For example, neutrons bombardments of Si atoms will convert them into Phosphorous (Neutron Transmutation Effect) that will adversely affected the performance of electronics. The radiation effect on the LiNbO<sub>3</sub>, the most important PR material, has been partially investigated in literature. In general the degrading effect of radiation on Lithium Niobate is a function of the type of the dopants and of the radiation dose [8-11].

The primary radiation effects on PR crystals due to all types of aforementioned radiation sources include variations in refraction index, spectral absorption (coloring), and change of density (volume expansion and striation). A summary of the previous study of the radiation effects on the doped LiNbO<sub>3</sub> is shown in Table II

**Table I. Radiation types and their damages to doped LiNbO<sub>3</sub> holographic material**

<b>Types of damages</b>	Refractive index ( $\Delta n_o$ ) changes	Density changes	Spectral absorption
<b>Source of Radiation</b>			
X-rays, $\gamma$ -rays	$\Delta(n_o)$ increases with dose	None	Spectral absorption in blue spectral region observed
Neutrons/charged particles	Decrease with dose	Volume increases at very high nuclear deposited energy	None

The preliminary results of radiation test of doped LiNbO<sub>3</sub> crystal have shown encouraging results that those damages occurred in orders of magnitude higher dose than that of the electronics. These tests indicated that rad-hard holographic memory could be developed using iron(s) doped LiNbO<sub>3</sub> PR crystal.

We will conduct a comprehensive radiation test of several doubly doped LiNbO<sub>3</sub> PR crystals. Specifically, we will measure the following key PR material parameters before and after the radiation tests: photorefractive sensitivity, recording time-constant, and material dynamic range (or maximum refractive index change). In addition, other material properties, such as optical uniformity, scattering noise, etc. would also be measured to evaluate the quality of the retrieved holographic data

### CONCLUSION

In summary, we have built a fully functional book-size CHDS breadboard using liquid crystal SLM as beam steering device and demonstrated the recording and retrieval of holograms with high quality. Radiation resistance test of the PR crystal LiNbO<sub>3</sub> is under way. In addition, we have also started the investigation of new 2-photon PR crystals for nonvolatile holographic recording

### ACKNOWLEDGMENT

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## REFERENCES

- 1 K. F. Strauss, T. Daud, "Overview of radiation tolerant unlimited write cycle nonvolatile memory", Proceeding of IEEE Aerospace Conference 2000.
- 2 W. Schober, F. Lansing, K. Wilson, and E. Webb, "High Data Rate Instrument Study", JPL publication 99-4.
- 3 A. K. Sharma, Semiconductor memories, IEEE Press, 1996.
- 4 T. H. Chao, H. Zhou, and G. Reyes, "High-density holographic memory and its applications to optical pattern recognition," proceedings of SPIE on ISOM/ODS'99, VOL. 3864, pp 181-183 July, 1999.
- 5 T. H. Chao, H. Zhou, and G. Reyes, "Advanced compact holographic data storage system," Proceedings of Non-volatile memory technology symposium 2000, pp. 100-105, November, 2000
- 6 K. Buse, A. Adibi, and D. Psaltis, "Non-Volatile Holographic Storage in Doubly Doped Lithium Niobate Crystals," *Nature* **393**, 665668 (1998)
- 7 M. Lee, S. Takekawa, Y. Furukawa, K. Kitamura, and H. Hatano, "Nonvolatile and quasi-nonvolatile holographic recording in near-stoichiometric lithium niobate doubly-doped with Tb and Fe", EMRS 2000 International Conference on Electronic Materials, Strasbourg, France (May 2000)
- 8 R. Yu. Azimzade, A. Kh. Zeinally, I. S. Kogan, and A. I. Timofeev, "Effect of gamma radiation on hologram recording", *Sov. Phys. Tech. Phys.* 24(9), p.1143, 1979
- 9 T. R. Volk, S. A. Shramchenko, and L. A. Shuvalov, "Changes in birefringence of LiNbO<sub>3</sub> crystals under the influence of x-rays (x-ray refraction effect)" *Sov Phys Solid State*, 28(12), p.2135-2138, 1984.
- 10 S. B. Ubizskii, A. O. Matkovskii, N. A. Mironova-Ulmane, V. Skvortsova, A. Suchocki, Y. A. Zhydachevskii, P. Potera, "Radiation displacement defect formation in some complex oxide crystals", *J. Nucl. Instr. and Meth. in Phys. Res. B* 166-167 (2000) 40-46.
- 11 G. Gotz, "Radiation effects in optoelectronic materials", *Radiation Effects*, 98, pp 189-210, 1986

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# A New Concept for Non-Volatile Memory: The Electric-Pulse Induced Resistive Change Effect in Colossal Magnetoresistive Thin Films

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## I. Abstract

A novel electric pulse-induced resistive change (EPIR) effect has been found in thin film colossal magnetoresistive (CMR) materials, and has shown promise for the development of resistive, nonvolatile memory. The EPIR effect is induced by the application of low voltage (< 4V) and short duration (< 20ns) electrical pulses across a thin film sample of a CMR material at room temperature and under no applied magnetic field. The pulse can directly either increase or decrease the resistance of the thin film sample depending on pulse polarity. The sample resistance change has been shown to be over two orders of magnitude, and is nonvolatile after pulsing. The sample resistance can also be changed through multiple levels - as many as 50 have been shown. Such a device can provide a way for the development of a new kind of nonvolatile multiple-valued memory with high density, fast write/read speed, low power-consumption and potential high radiation-hardness.

## II. Introduction

A great amount of effort is being applied to the development of nonvolatile memories (NVM) in response to a huge demand for non-powered high-density data storage [1,2]. Recently more and more interest

has moved to two-terminal resistive-type devices, including the utilization of crystalline-amorphous phase transition effect [3], ferroelectric diode effect [2], the dielectric dispersion effect [4], and magnetoresistive memories [5]. Although NVM innovation and technology are experiencing great growth, new memory concept and technologies are needed to support the rigid challenges to the requirements: low power and low voltage for reading and writing, non-volatility with infinite retentivity, fast, inexpensive, radiation-hard, and infinitely rewritable.

The hysteretic behavior of the resistivity of the colossal magnetoresistance (CMR) materials under high magnetic fields and low temperatures has incited interest to develop new nonvolatile memory devices in this materials system [6,7]. However, the high magnetic fields and the low operating temperatures are hindrances to applications. Much effort has been expended to overcome these difficulties including utilizing the extrinsic effects of grain boundaries [8], field focusing [9], and the intrinsic effect of tunneling [10,11]. However, only small changes in resistance of from 2 to 20% were obtained.

We have recently found that an electric field can also induce resistance change in CMR materials at room temperature and under no

applied magnetic field [12]. By applying short electrical pulses with moderate voltage to the magnetoresistive thin films, a new resistive effect with a large room-temperature nonvolatile resistance change ratio (>20,000%) has been achieved. Based on this electrically variable and reversible resistance change effect, we report here a new nonvolatile, rewritable binary and multi-valued memory elements driven by electrical field, and made of thin magnetoresistive material which can be read and written randomly at high speeds. More than 50 nonvolatile resistance levels (bit level) have been demonstrated in a simple two-terminal storage element with no requirement for initial forming or poling.

### III. Device Fabrication

$\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$  (PCMO) thin films of thickness range of 300nm-800nm were grown epitaxially by pulsed laser deposition (PLD) on atomically ordered  $\text{Yba}_2\text{Cu}_3\text{O}_{7-x}$  (YBCO) and platinum substrates. The YBCO and Pt films were epitaxially grown by pulse laser deposition (PLD) and e-beam vaporization respectively on the (100)  $\text{LaAlO}_3$  (LAO) substrates, and were used as the bottom electrodes and the atomic templates for PCMO epitaxial growth. The epitaxial PCMO films were nominally grown at 700°C-750°C in an atmosphere of ~200 mTorr of flowing oxygen, and then were cooled to room temperature under one atmosphere of oxygen. Patterned metal (Ag, Au or Pt) contacts were fabricated on top of the PCMO, YBCO and base-Pt layers by room temperature sputtering.

### IV. Results And Discussion

Write and erase electrical pulses were applied to the samples through the metal contact pads on the top PCMO and the bottom YBCO or Pt layers. Applied pulses with amplitude and duration values over a set of

values called “the start threshold values” resulted in change in sample resistance. The start threshold values depend on the film thickness and composition, and are nominally 1V-3V at pulse widths of ~ 10ns or less. Pulses with negative polarity (negative pulse applied to the top electrode on PCMO film) resulted in an increase in sample resistance to a high saturation value. Pulses of opposite polarity resulted in a decrease in sample resistance to a low saturation value. The high and low saturation values depend on the applied pulse amplitude and duration which must be below another set of values called “the break threshold values”, over which the sample will be damaged. When the amplitude and duration of the pulses are between the “start” and “break” threshold values and are selected suitably, the sample resistance can be switched between binary states by single pulse or multi-pulses, as well as can be changed in a gradual and stepwise manner resulting in multitudinous intermediate hysteresis resistance levels.

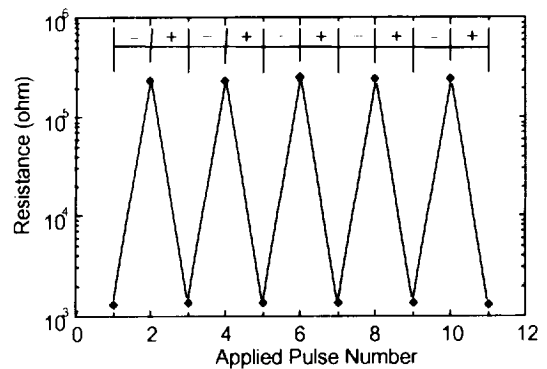


Fig. 1 Two-state non-volatile resistance switching performance of an Ag/PCMO/Pt EPIR device switched by applied electric pulses with alternative positive and negative polarities and pulse amplitude of 3.2V and pulse duration of 28 ns.

Switching performance by single pulse for an Ag/PCMO(100)/Pt(100) two-terminal device is shown in Fig. 1, where the thickness of the active PCMO layer is 300 nm, and the pulse amplitude is 3.2V with a duration of 28ns. At room temperature, the positive pulse induces a low nonvolatile resistance state, and the negative pulse induces a high nonvolatile resistance state indicating ideal two-state logic behavior. An EPIR ratio, defined as:  $\Delta R/R_{\text{MIN}} = (R_{\text{MAX}} - R_{\text{MIN}})/R_{\text{MIN}}$ , where  $R_{\text{MAX}}$  and  $R_{\text{MIN}}$  are the maximum and minimum nonvolatile resistances induced by write and erase pulses, can be used to describe the device resistance change. The induced EPIR ratio of this device is more than 20,000% at room temperature.

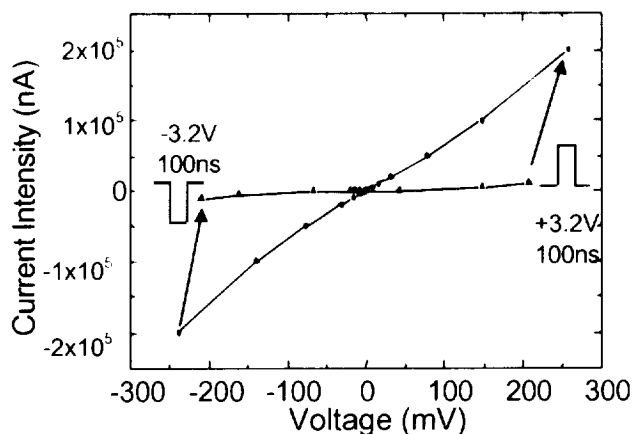


Fig. 2. I-V curves for a Ag/PCMO/Pt device showing high resistance state behavior (triangles), switching to the low resistance state at 250 mV by a +3.2 V, 100 ns pulse, low resistance behavior (diamonds), and switching back to the high resistance state at -250 mV with a -3.2 V, 100 ns pulse.

To help identify that the resistance change occurred intrinsically in the colossal magnetoresistive material and was not a contact problem, a single layer device: a PCMO layer grown directly on LAO with no bottom electrode was resistance characterized by the

standard four-point probe measuring technique. The write/erase pulses were initially applied to the device through the two inner electrodes. This was followed by a small, constant dc current being sent through the two outside electrodes with a voltage drop measured across the two inner electrodes. The measurements showed similar reversible resistance change behavior under electric pulsing, thus clarifying an intrinsic basis for the nonvolatile electrical-pulse-induced resistance (EPIR) effect.

A DC current-voltage (I-V) curve for a Ag/PCMO(100)/Pt device with a 600 nm thick epitaxial PCMO layer measured in low voltage and low current range and far away from the voltage for device switch is shown in Fig. 2. In the high resistance state the I-V curve shows a low slope from -250 mV to +250 mV. Upon applying a +3.2 V, 100 ns pulse the sample switches to the low resistance state with the I-V curve showing high slope from +250 mV to -250 mV where a -3.2 V, 100 ns pulse returns the sample back to the high resistance state. The I-V curves of the EPIR device are a symmetric about  $V=0$  for both low-resistance state and high resistance state in low voltage range. This symmetric character further shows that the EPIR effect is intrinsic, and is not caused by effects such as interface Schottky barriers.

It is important to note that multilevel switchable states can be obtained by the EPIR two terminal device, because of its large nonvolatile resistance dynamic change range and cumulative resistance change character. The actual value of the EPIR resistance state depends on the length and amplitude of the individual write/erase pulses and number of the applied pulse. Fig. 3 shows the device resistance with multiple intermediate levels depending on pulse number and pulse level for

a device with Ag/PCMO(100)/c-oriented YBCO structure. Each resistance level corresponds to a specific state of memory, and thus Fig. 3 clearly shows that more than 50 nonvolatile resistance levels can be stored in a simple two terminal storage element. The insert in Figure 3 also shows that with appropriate pulse numbers and pulse levels and polarities, any resistance state of the device is attainable. It is projected that a larger number of resistance levels will be able to be obtained upon optimization of the resistance element heterostructure and the pulsing and sampling process.

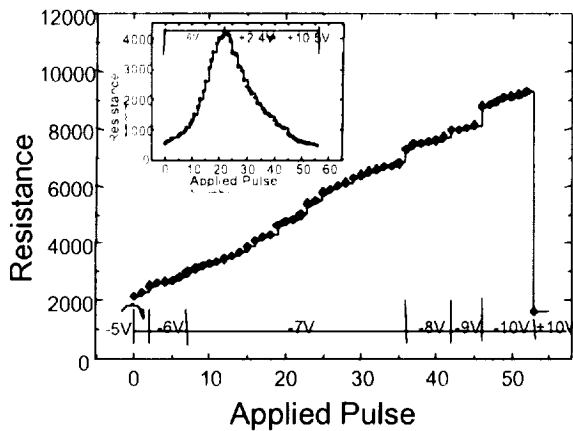


Fig. 3. The resistance change versus write pulse number for a  $\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3/\text{Yba}_2\text{Cu}_3\text{O}_7$  device. The write pulse duration was 100ns and the pulse amplitude was varied from -5V to -10V in increments of -1V. 53 discrete resistance steps can be seen for this sample. The insert shows the possibility of ramping sample resistance up and down with appropriate number of pulses and pulse heights.

An endurance test has shown that the present experimental devices, which have not yet been optimized for performance, can withstand much more than  $10^5$  resistance switches. Fig. 4 shows the results for a PCMO/YBCO device to which more than 100,000 pulses of 12V and 80ns were applied

at a frequency of 10Hz. The EPIR ratio approaches a non-zero saturation value of about 50% of the maximum value at high pulse numbers with this saturation behavior indicating the possibility of much higher pulse numbers. The changed resistance value, that is, a given resistance memory state, was also stable with time with a resistance shift of less than 1% over  $2.5 \times 10^5$  seconds

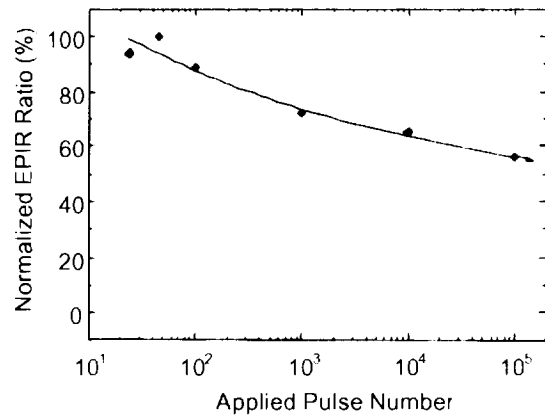


Fig. 4. A normalized EPIR ratio versus write and erase pulse number for a  $\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3/\text{Yba}_2\text{Cu}_3\text{O}_7$  device cycled at room temperature. Note the plateau behavior with pulse number projecting good resistance ratiion stability at much higher pulse numbers than shown.

As the present time devices are aimed at the experimental demonstration of the initial operation of an electrical-pulse-induced resistance change device, and thus they have not yet been fabricated in small size. The top electrode contacts for the devices were either  $200\mu\text{m}$  or  $500\mu\text{m}$  diameter. As a result, there are possibilities to improve device performance by decreasing device size to micron or submicron levels. For example, when the device becomes smaller the write energy is expected to be reduced. For a  $500\mu\text{m}$  device with write voltage of 5V and resistance of  $200\Omega$  the write energy is  $\sim 2\text{nJ}$ . This is already lower than some

present CMOS-related devices [1]. The reduction of device area for the EPIR device will increase its resistance resulting in a further decrease in write energy.

It is well to note that the EPIR device reported here is not seen to depend on the storing of charge as most semiconductor nonvolatile memories do [13]. The EPIR effect is believed to depend on ferromagnetic cluster arrangements of polarons and/or residual Jahn-Teller distorted  $Mn^{3+}O^6$  stripes (JTS) in the thin PCMO films which are accompanied by lattice distortions and phase separation [14-16]. Such cooperative phenomena are not expected to be greatly affected by high energy particles, and hence the EPIR devices should be radiation hard.

#### V. Conclusion

A novel kind of rewritable, non-volatile resistance memory has been demonstrated experimentally in perovskite oxide thin films, particularly CMR material films, based on electrically-induced resistance changes at room temperature. The electrically switched resistance devices have shown two-state behavior at switching voltages of  $<4V$ , and because of the large resistance change capability and cumulative behavior, an EPIR memory element with a simple two terminal structure has shown a storage ability of more than 50 discrete nonvolatile levels. The data write times are less than 20ns, and the write energy is lower than 2nJ. Preliminary endurance tests have shown that the devices can withstand much more than  $10^5$  resistance switching cycles.

The EPIR effect is very different from the previously known resistive memory effects such as the ferroelectric diode effect, the semiconductor crystalline-amorphous phase transition effect, and the dielectric dispersion effect, and is projected to be radiation hard. The mechanism responsible for the effect is

currently being investigated, however, it is clear that the EPIR effect is a new physical phenomenon which provides the possibility to built a solid state, electrically operated, directly overwritable, low excitation energy, very fast switching, nonvolatile, and multileveled high density resistive memory system.

#### VII. Acknowledgments

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#### VII. References

- [1] M. Dax, "The non-volatile memory challenge," Semiconductor International, p. 84. Sept. 1997.
- [2] M. Okano, and Y. Watanabe, "Nonvolatile programmable two-terminal diodes using a ferroelectric semiconductor," Appl. Phys. Lett., 76, 233 (2000).
- [3] W. D. Buckley, "Filament-type memory semiconductor device and method of making the same," U.S. Patent, No. 3886577, (1975).
- [4] M. J. Rose, J. Hajto, P. G. LeComber, S. M. Gage, W. K. Choi, A. J. Snell, and A. E. Owen, "Amorphous silicon analogue memory devices," J. Non-Cryst. Solids 115, 168 (1989).
- [5] G. A. Prinz, "Magnetoelectronics," Science, 282, 1660 (1998).
- [6] G. C. Xiong, Q. Li, H. L. Ju, S. M. Bhagat, S. E. Lofland, R. L. Greene, and T. Venkatesan, "Giant magnetoresistive memory effect in  $Nd_{0.7}Sr_{0.3}MnOz$  films," Appl. Phys. Lett., 67, 3031 (1995).
- [7] Y. Tomioka, A. Asamitsu, H. Kuwahara,

Y. Moritomo, and Y. Tokura, "Magnetic-field-induced metal-insulator phenomena in  $\text{Pr}_{1-x}\text{Ca}_x\text{MnO}_3$  with controlled charge-ordering instability," *Phys. Rev. B*, 51, R1689 (1996).

[8] S. P. Isaac, N. D. Mathur, J. E. Evetts, and M. G. Blamire, "Magnetoresistance of artificial  $\text{La}_{0.7}\text{Sr}_{0.3}\text{MnO}_3$  grain boundaries as a function of misorientation angle," *Appl. Phys. Lett.*, 72, 2038 (1998).

[9] H. Y. Hwang, S.-W. Cheong, and B. Batlogg, "Enhancing the low field magnetoresistive response in perovskite manganites," *Appl. Phys. Lett.*, 68, 3494 (1996).

[10] K.-I. Kobayashi, T. Kimura, H. Sawada, K. Terakura, and Y. Tokura, "Room-temperature magnetoresistance," *Nature* 395, 677 (1998).

[11] F. J. Cadieu, L. Chen, B. Li, and T. Theodoropoulos, "Room temperature  $\text{La}_{0.7}\text{Sr}_{0.3}\text{MnO}_3$  magnetoresistive prototype memory element," *Appl. Phys. Lett.*, 75, 3369 (1999).

[12] S. Q. Liu, N. J. Wu, and A. Ignatiev, "Electric-pulse-induced reversible resistance change effect in magnetoresistive films," *Appl. Phys. Lett.*, 76, 2749 (2000).

[13] *Nonvolatile Semiconductor Memory Technology*, Edited by W. D. Brown, and J. E. Brewer, (IEEE Press, New York, 1998).

[14] J. M. De Teresa, M. R. Ibarra, P. A. Algarabel, C. Ritter, C. Marquina, J. Blasco, J. Garcia, A. Del Moral, and Z. Arnold, "Evidence for magnetic polarons in the magnetoresistive perovskites," *Nature*, 386, 256 (1997).

[15] P. Littlewood, "Phases of resistance," *Nature*, 399, 529 (1999).

[16] A. J. Millis, "Lattice effects in magnetoresistive manganese perovskites," *Nature*, 392, 147 (1998).

## VII Biographies

**Shangqing Liu** received the Ph. D degree from Anhui Institute of Optics and Fine Mechanics of the Chinese Academy of Sciences, Hefei China, and did his postdoctoral work at the Institute of Physics of the Chinese Academy of Sciences, Beijing, China. He has spent over 15 years in optical information technology and devices. In 1997 he became a Member of Research Staff at the Space Vacuum Epitaxy Center at the University of Houston. His current research interests include oxide thin film growth, memory device design and colossal magnetoresistive material application.

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# High-Density Ferroelectric Memories Using a One-Transistor Cell

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**Abstract**—Discovery of new classes of ferroelectric materials that have low dielectric permittivities<sup>1</sup> allows nonvolatile ferroelectric random access memories that use a single ferroelectric transistor for the memory storage device to become practical, providing non-destructive read out and density comparable to a Flash memory cell. Ferroelectric memories using this new memory cell have programming times orders of magnitude faster than Flash memory and are capable of providing very dense non-volatile memory for space applications. Previous attempts to incorporate a ferroelectric material into the gate dielectric of a memory transistor have been hindered by the formation of an unwanted oxide interfacial layer between the ferroelectric material and the silicon that has made low voltage programming difficult and caused the devices to be unstable. These new ferroelectric materials allow the oxide interfacial layer to grow under the ferroelectric while maintaining low voltage programming characteristics because of the low permittivity. An underlying oxide is desirable because the low interface state density gives superior transistor channel characteristics. Memory window hysteresis of 2-3 volts on capacitor structures has been demonstrated and high-speed measurements of the ferroelectric switched charge correlate well with the observed memory window. Integrating the ferroelectric transistor into a memory array without the need for additional access devices is a challenge.

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4. SWITCHING CHARACTERISTICS
5. RETENTION and ENDURANCE
6. MEMORY ARRAY
7. CONCLUSIONS
8. REFERENCES

## 1. INTRODUCTION

The idea of using a ferroelectric transistor as a memory element is not new. In 1967, Fatuzzo and Merz<sup>2</sup> stated, "with a ferroelectric semiconductor combination one can build a field-effect device (similar to an MOS transistor) which has a memory and allows continuous, non-destructive read-out of information." However, attaining this goal has proven to be elusive. Attempts to incorporate a ferroelectric material into the gate dielectric of a transistor have been hindered by the formation of an unwanted oxide interfacial layer between the ferroelectric material and the silicon. Because of the high permittivity of most ferroelectric materials and low permittivity of this unwanted oxide layer, low voltage programming has been prevented and the devices have been unstable. Researchers have searched for a high permittivity dielectric layer to deposit under the ferroelectric materials that also inhibits SiO<sub>2</sub> formation on the silicon in the channel region without much success. Therefore, the densest ferroelectric memories currently available use larger one-transistor, one-capacitor memory cells and destructive read out schemes.

Recently, new classes of ferroelectric materials have been discovered that have low permittivities.<sup>1</sup> These materials also have low ferroelectric switched charge, but only approximately 1% of the switched charge needed to operate a conventional ferroelectric memory using a one-transistor, one-capacitor memory cell is required to operate the ferroelectric transistor. These new ferroelectric materials allow an oxide interfacial layer to grow under the ferroelectric material while maintaining low voltage programming characteristics. In fact, an underlying interfacial oxide layer is desirable in this case because a low interface state density gives superior transistor channel characteristics.

Nonvolatile memories using a single ferroelectric transistor memory cell of  $\sim 5F^2$ , where  $F$  is the lithographic feature size, are expected to have similar densities to Flash memories. However, ferroelectric memories have programming times and endurance orders of magnitude better than Flash memories. When combined with radiation hardened CMOS, dense ferroelectric memories can be used in space applications because the ferroelectric layer is radiation tolerant.

Adequate memory window hystereses of 2-3 volts are observed on silicon capacitor structures. High-speed measurements of the ferroelectric switched charge correlate well with the observed memory window. Major challenges are to integrate the memory cells into an array with small cell size and to obtain acceptable retention.

## 2. DEVICE STRUCTURE

For these studies, simple MOS-type capacitor structures were used. The ferroelectric material was deposited directly on the silicon and annealed in oxygen. During the oxygen anneal, an underlying interfacial oxide layer was grown. Top electrodes of platinum were then deposited and defined. Figure 1 shows a cross section of the test capacitor structure

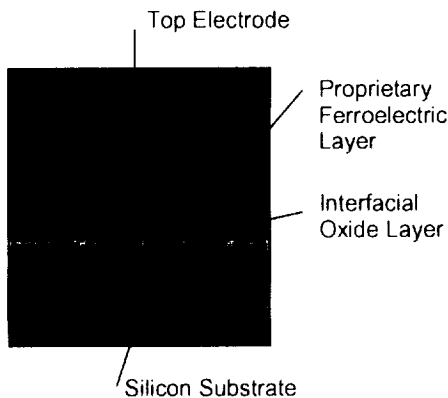


Figure 1. Cross Section of the capacitor test structure.

## 3. MEMORY HYSTERESIS

Hysteresis measurements were made by ramping the voltage applied to the gate of the test capacitor structure. A typical hysteresis plot is shown in Figure 2. The change in threshold voltage of a transistor similarly fabricated would be approximately the same as the shift in the C-V curve, or 2-3 volts. This is more than adequate for memory array sensing.

Using the capacitance value in accumulation, an effective dielectric permittivity for the dielectric stack is calculated to be approximately 13.

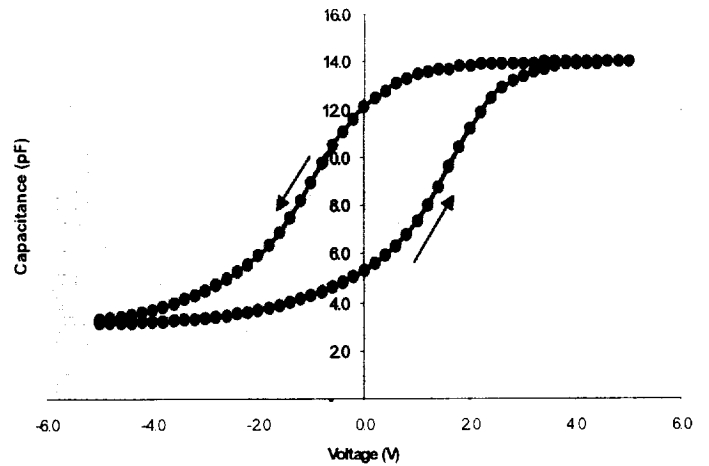


Figure 2. Hysteresis C-V plot on capacitor test structure for applied voltages from -6 to 6 volts.

## 4. SWITCHING CHARACTERISTICS

High-speed switching measurements were made on the test capacitor structures using special circuitry that assured impedance matching. This circuitry also provides a variable reference to assure that the full applied voltage was across the capacitor, unlike a Sawyer-Tower circuit where a variable portion of the applied voltage is dropped across a sensing device in series with the capacitor.

Because measurements using contact to the back of the silicon wafer is difficult at these high speeds, a large capacitor on the front of the wafer was used to couple to the silicon to obtain the measurements. This large capacitor in series with the test capacitor has a negligible effect on the measurements.

Figures 3 and 4 show the switched and non-switched current for applied voltages of 5V and 1V, respectively. The non-switching current is for an applied voltage pulse to keep the ferroelectric in the same polarization state and is comprised of the linear capacitive current and a small amount of switching. The switching current is for an applied voltage pulse that switches the ferroelectric polarization to the opposite state and is comprised of the linear capacitive current and image charge that flows between the electrodes of the capacitor because of the shift in charge centroid in the ferroelectric.

Figure 5 shows the switching charge as a function of time for the two applied voltages. For the rise time of 100 ns, the switching is complete within 200 ns. Figure 6 shows the switched charge resulting from a subtraction of the switched and non-switched charge measured for a 20 ns rise time. Integration of the area under this curve gives a switched polarization of approximately  $2 \text{ fC}/\mu\text{m}^2$  ( $0.2 \mu\text{C}/\text{cm}^2$ ). This switched charge is only approximately 1% of the switched charge needed in a one-transistor, one-capacitor ferroelectric memory cell. The switching time

is limited by the measurement and is less than 20 ns, consistent with ferroelectric behavior. Such fast switching times are not possible for ionic motion or charge injection and trapping.

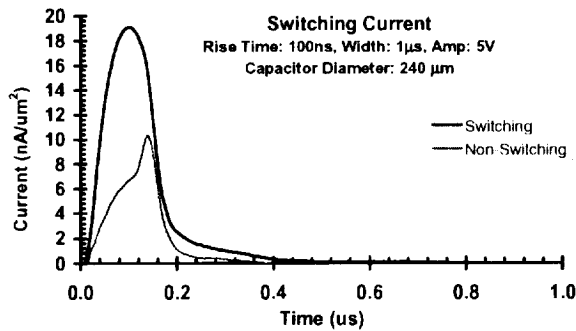


Figure 3. Switching current measurements at 5V.

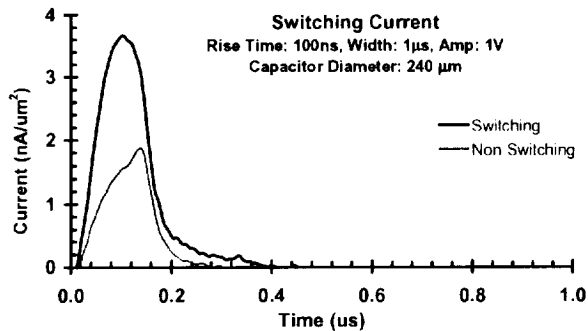


Figure 4. Switching current measurements at 1V.

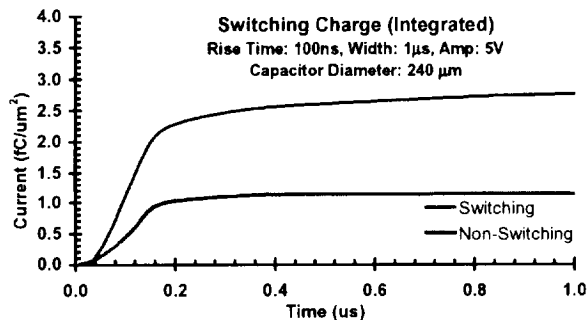


Figure 5. Switching time dependence.

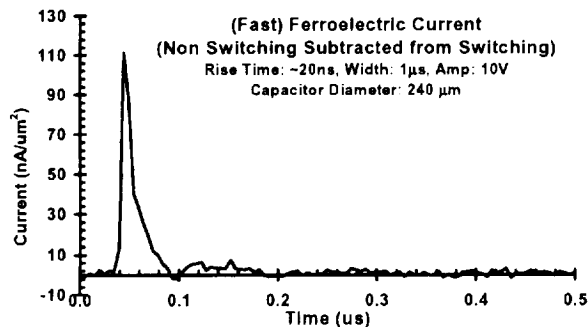


Figure 6. Switched charge for 20ns rise time.

Table 1 shows the measured electrical characteristics of the test capacitor structures.

Table 1. Electrical Characteristics

Parameter	Value
Non-switching permittivity (stack)	~ 7
Switching permittivity (stack)	~ 16
Switching speed	< 20 ns
Switching voltage	~ 1 V
Polarization	~ 2 fC/μm <sup>2</sup>
Memory window	2-3 V
Leakage current (@ ± 5 V)	± 5x10 <sup>-8</sup> A/cm <sup>2</sup>

## 5. RETENTION and ENDURANCE

With a nonvolatile ferroelectric transistor, care must be taken to avoid charge injection into the structure resulting in charge trapping and compensation of the electric field established by the polarization within the gate dielectric. This compensation effectively blocks control of the channel of the transistor by the polarization, shortening retention time. Reducing the charge injection or tunneling probability and the number of traps in the gate dielectric structure should lengthen the retention time.

To predict retention, charge injection and leakage current measurement conditions must correspond to the applied potentials during the passive storage condition of the memory cell and under worst case disturb conditions. For example, a current of 10<sup>-8</sup> A/cm<sup>2</sup> under storage or deselect conditions for the polarization shown in Table 1 may cause sufficient compensation of the polarization electric field to give unacceptably short retention times. Therefore, the circuit design must be such that the applied voltage across the dielectric structure under standby conditions is very small or zero and during read or deselected conditions is sufficiently small to allow long retention. Westinghouse investigators have shown ten year extrapolated retention on ferroelectric transistors incorporating PZT, as shown in Figure 7.<sup>3</sup>

Endurance has not yet been measured on the test capacitor structures. Ferroelectric endurance is typically at least 10<sup>8</sup> and sometimes virtually infinite, depending on the ferroelectric material and the electrodes. High endurance for the ferroelectric transistor is expected with the new ferroelectric materials.

Ten year retention and high ferroelectric endurance levels are key attributes for nonvolatile memories used in space applications, especially for deep space missions. It is expected that this new technology will meet the necessary nonvolatile memory requirements.

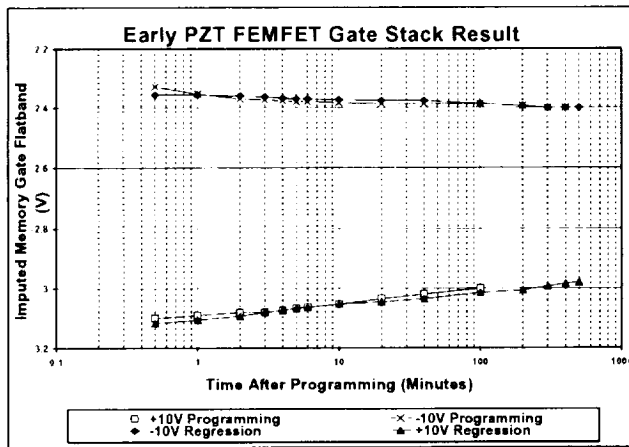


Figure 7. Retention measurements on a PZT ferroelectric transistor showing extrapolated ten year retention.

## 6. MEMORY ARRAY

Integrating a single transistor memory cell into a memory array without disturb of deselected memory cells during read and write operations is a challenge. This is because the gate and bulk are shared by adjacent memory cells and the programmed state of a memory transistor is determined by the gate to bulk voltage. A single access transistor with each memory cell can float the drain or source of the memory transistor but cannot isolate the gate and bulk. Addition of an access transistor to each memory cell increases the cell size above the  $5\text{-}6\text{ F}^2$  obtainable with just a single transistor memory cell, similar to Flash.

Ishiwara<sup>4</sup> and Ma<sup>5</sup> have both investigated ferroelectric transistors. Ren et. al. have suggested using depletion operation for both the access transistor and ferroelectric storage transistor to overcome the array architecture issues.<sup>6</sup> Ullman et. al. evaluated NAND, AND and NOR memory architectures and suggest the use of an AND architecture with single transistor memory cells.<sup>7</sup> However, this architecture requires decoding both the source and drain lines which increases the cell size. More work must be done investigating array architectures to solve these issues.

## 7. CONCLUSIONS

New classes of low dielectric permittivity ferroelectrics have enabled MOS-type capacitor test structures to be fabricated. Use of low permittivity ferroelectric materials allows a conventional oxide interfacial layer to form between the ferroelectric and the silicon bulk, solving the major problem for memories that use ferroelectric transistors for the memory storage element.

Electrical measurements on capacitor test structures give a memory window of approximately 2-3 V, switching

times less than 20 ns, the limit of the measurements, and switched charge of approximately  $2\text{ fC}/\mu\text{m}^2$ . Although two transistor memory cells using depletion access and depletion ferroelectric storage devices or AND memory arrays using single transistor ferroelectric storage devices have been shown theoretically to give acceptable array architectures, more work must be done in this area to realize memory cell sizes of the order of  $5\text{ F}^2$ .

When combined with radiation hardened CMOS, ferroelectric memories using the low permittivity ferroelectric materials may meet high-density nonvolatile memory requirements for space missions.

## 8. REFERENCES

- <sup>[1]</sup>Cova Technologies ferroelectric FET development supported by the Ballistic Missile Defense Organization under an SBIR grant administered by the U.S. Army Space and Missile Defense Command.
- <sup>[2]</sup>E. Fatuzzo and W. J. Merz, *Ferroelectricity*, North-Holland Publishing Co., Amsterdam, 1967, p. 272.
- <sup>[3]</sup>D. R. Lampe, H. Buhay, M. H. Francombe, D. A. Adams, J. W. Dzimianski and S. Sinharoy, "Ferroelectric Oxide Memory FET (FEMFET) Development," *Final Technical Report*, Office of Naval Research, DARPA Order No. 7503, DARPA Contract No. N00014-90-C-0159, 1994, p. 91.
- <sup>[4]</sup>E.K. Aizawa and H. Ishiwara, "Fabrication and Characterization of MFSFET Arrays using Al/BaMgF<sub>4</sub>/Si(111) Structures," *Integrated Ferroelectrics* **27**, 1999, p. 1045.
- <sup>[5]</sup>J-P. Han and T. P. Ma, *Ferroelectric Gate Transistor as a Capacitor-Less DRAM Cell (FEDRAM)*, *Integrated Ferroelectrics* **27**, 1999, p. 1053.
- <sup>[6]</sup>T. L. Ren, W-Q. Zhang, C-X Li, J. Zhu, "A Novel Cell and Array Architecture for FET-Type Ferroelectric Non-volatile Memories", *13<sup>th</sup> International Symposium on Integrated Ferroelectrics*, Colorado Springs, 2001, p. 190.
- <sup>[7]</sup>S.M. Ullmann, H. Goebe, T. Haneder and W. Hönlein, "A Nonvolatile Single Ferro FET Memory Concept with Disturb Free Operation Scheme," *13<sup>th</sup> International Symposium on Integrated Ferroelectrics*, Colorado Springs, 2001, p. 191.

## About the Author

David Kamp is the Chief Operating Officer and Executive Vice President of Celis Semiconductor Corporation. After receiving his BSEE degree from the University of Michigan in 1981, he joined Inmos Corporation where he worked on product engineering of semiconductor memories. In 1987 he joined Simtek Corporation and was responsible for design of nonvolatile memories. In 1994 and 1995 he designed nonvolatile ferroelectric memories for Ceram, Inc and Ramtron Corporation, respectively. Mr. Kamp holds several patents for memory design and has developed models for ferroelectric devices.

**Requirements and Usage of  
 NVM  
 in  
 Advanced  
 Onboard Data Processing Systems**

865021

R. Some  
 NVM Technology Symposium  
 11/7/01

This work was performed at the Jet Propulsion Laboratory, California Institute of Technology under a contract with the National Aeronautics and Space Administration. This project is part of NASA's High Performance Computing and Communications Program, and is funded through the NASA Office of Space Sciences.



## Spaceborne Computing:



- Past - Rad6000
  - Basic C&D H functions (1-10MOPS)
- Present - (well, almost) PPC-750 Rad (light)
  - Basic C&D H + simple data processing and task automation (10-100+ MOPS)
- Future - Supercomputing
  - Science data processing, autonomy, situational awareness, intelligent spacecraft and constellation control (100 - 10,000MOPS+)

## Why supercomputing in space?

- Only viable approach to the bandwidth problem - can't get the data down to earth
- Only viable approach to controlling constellations of cooperating satellites
- Only viable approach to reducing mission operations costs
- Only viable approach to real time intelligent decision making and science data gathering

### *The REE Vision:*

*• Move commercial scalable supercomputing technology into space, in a form which meets the demanding environmental requirements, to enable a new class of science investigation and discovery.*



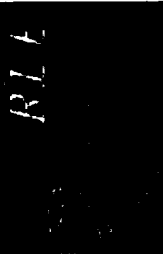
### *Background*

- Funded by Office of Space Science (Code S) as part of NASA's High Performance Computing and Communications Program
- Started in FY1996
- Guidelined at \$100M over 8 years

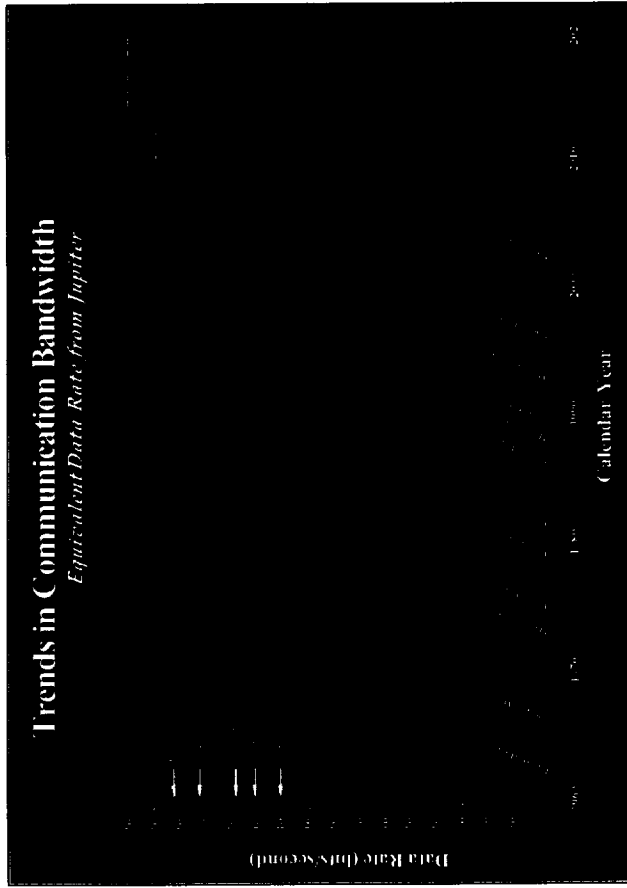
### *REE Impact on NASA and DOD Missions by FY05*

- Faster* - Fly State-of-the-Art Commercial Computing Technologies within 18 month of availability on the ground
- Better* - Onboard computer operating at > 300MOPS/watt scalable to mission requirements (> 100x Mars Pathfinder power performance)
- Cheaper* - No high cost radiation hardened processors or special purpose architectures





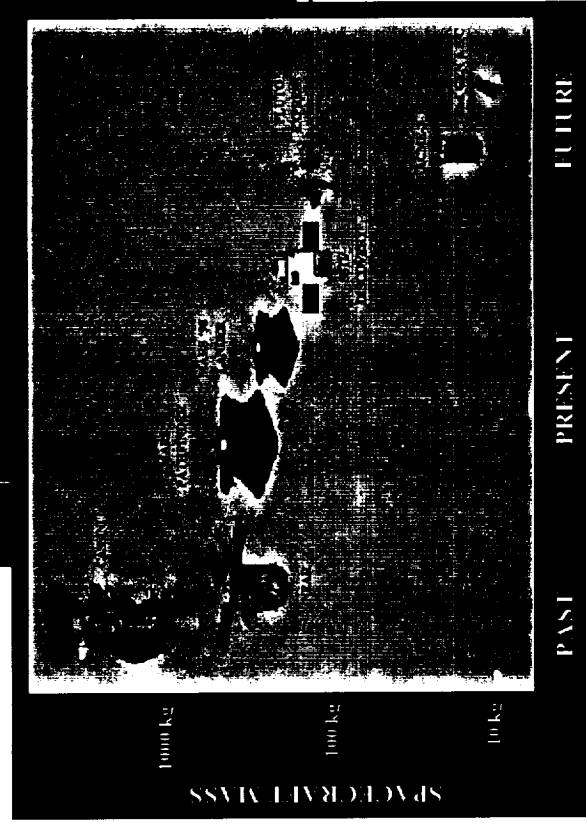
# The Problem Set



*bandwidth*

*Latency*

**Round Trip Delay**



*Power/Mass Volume*

**System Cost**

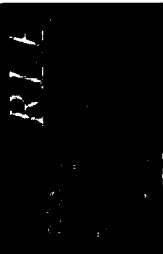
**Operational Cost**

**Development Time**

**Science Return**

# REE Objectives

- Demonstrate power efficiencies of 300 -1000 MOPS per watt in an architecture that can be scaled up to 100 watts, depending on mission needs.
- Demonstrate new spaceborne applications on embedded high-performance computing testbeds which return analysis results to the earth in addition to raw data.
- Develop fault-tolerant system software that will permit reliable operation for 10 years and more using commercially available or derived components.
- Explore ultra-low power onboard computer systems which will help open the entire Solar System to exploration without the need for nuclear technology.



# Science Teams



## *Five Science Application Teams Chosen to Drive Requirements and Demonstrate Benefits of HPC Onboard*

### **Next Generation Space Telescope - John Mather/GSFC**

- Onboard Cosmic Ray correction to the data
- Autonomous control and optimization of the adaptive optic



### **Gamma ray Large Area Space Telescope**

#### **• Peter Michelson/Stanford**

- Onboard cosmic ray rejection
- Real time gamma ray burst identification

### **Orbiting Thermal Imaging Spectrometer - Alan Gillespie/U Washington**

- Onboard Atmospheric corrections, Radiance calculations



### **Mars Rover Science - R. Steve Saunders/JPL**

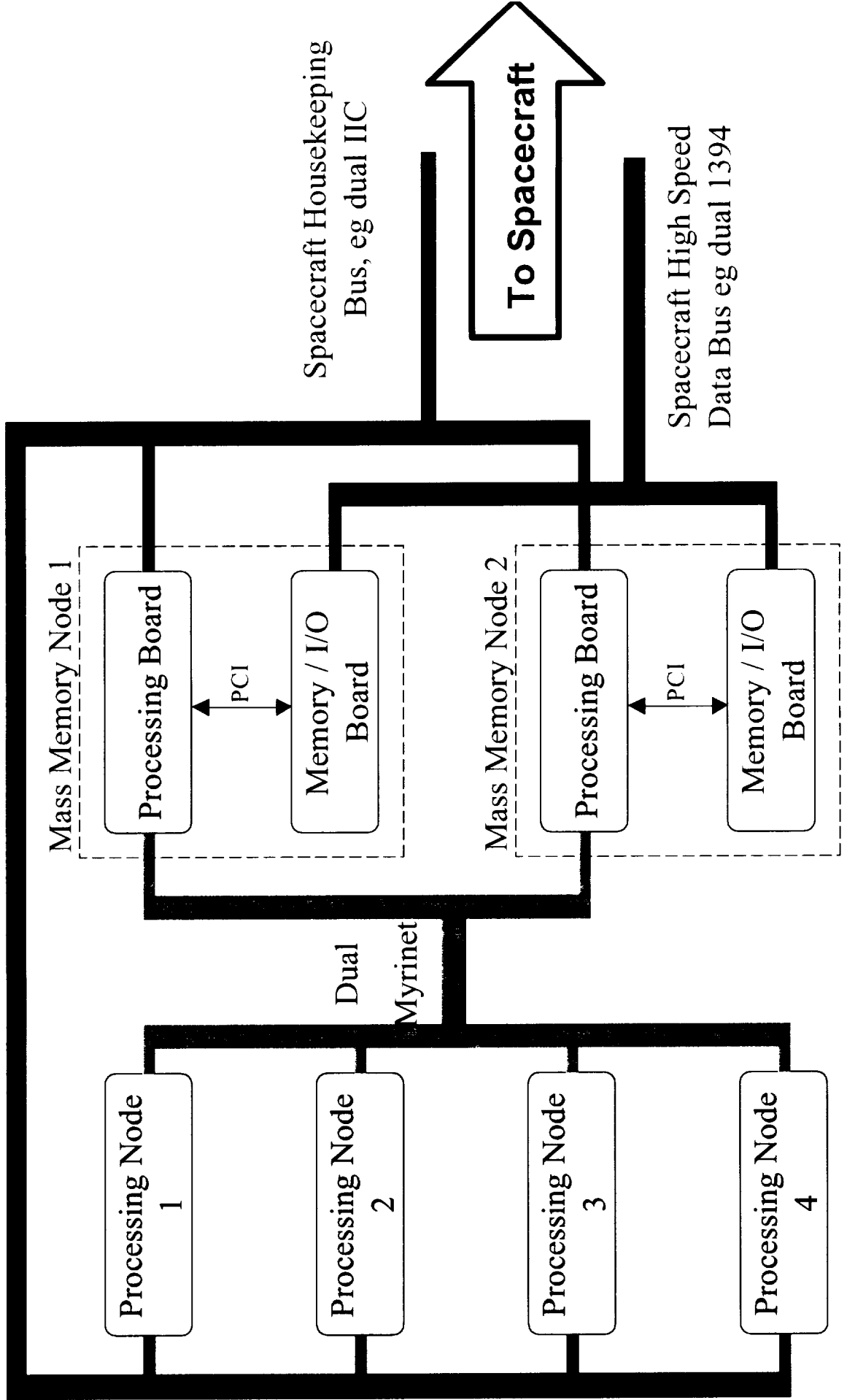
- Autonomous optimal terrain navigation
- Autonomous Field Geology



### **Solar Terrestrial Probe Program - Steve Curtis/GSFC**

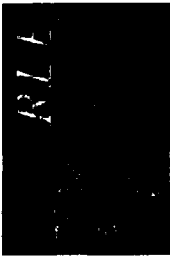
- Constellation/Formation Flying missions to probe the Sun-Earth Connection
- Onboard Plasma moment calculations, multi-instrument cross correlations, autonomous operation

# REE Baseline Architecture



# REE Issues

- COTS vs Rad Hard
  - It doesn't matter - NVMM is still required and (most of)
  - The requirements are the same
- GP Processors vs DSP's vs FPGA's
  - It doesn't matter - NVMM is still required and (most of)
  - The requirements are the same
- Application Domain - NGST vs OTIS vs Rover
  - It doesn't matter - NVMM is still require and (most of)
  - The requirements are the same

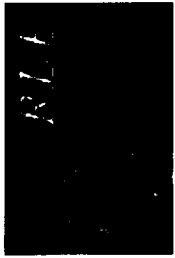


# NVM Usage/Requirements



- Mass Memory (Disk Emulator)
  - 1-10 GB per CPCI board
    - IC density
    - Packaging density
  - 10-20 Watts per CPCI board
  - Medium Speed
    - 2-5 Gbits/Sec bidirectional
    - Burst mode
    - File oriented
  - 50-100 krad Si (100 mil Al shield)
  - SEU Tolerance
    - SEL, SEFI, SEMU and Catastrophic Failure Immune

- Processing Node (OS & state storage)
  - High speed
    - Execute directly from NVM or,
    - High speed download from NVM to execution memory
    - High speed store of state variables
    - Typical processor throughput - 1-5 GWords/Sec
    - Typical DRAM speeds - moving towards
  - Low Power
    - Processor, Bridge, Net I/O and DRAM already eat up too much power
  - 50-100krad Si (100 mil Al shield)
  - SEU tolerance
    - SEE Hard



# NVM Usage/Requirements



- Processing Node (OS & state storage) cont.
  - Small memory, but high density
    - 1Mbyte will do, but more is better
    - 1 IC footprint
- General requirements/desirements
  - Low Cost
  - COTS/MOTS/SOTS



# Questions

- Can NVM replace DRAM (speed/density)?
- If not, how close will get and when?
- Will COTS NVM technologies be rad tolerant & SEU/SEL hard?
- Will NVM technologies experience catastrophic SEE's

565,820-2377



The 2nd Annual, Non-Volatile Memory Technology Symposium

7, 8 November 2001

## **Europa Orbiter Mass Memory Requirements & Status**

Study Contributors:

Wayne Arens

Taher Daud

Dan Karmon

Alan Nicholson

Karl Strauss

**Europa Orbiter – Mass Memory**

## Why am I here?

- Tell you about the Europa Orbiter Mass Memory requirements
- Tell you about our current status
- Challenge you to come and talk to us regarding alternative solutions.





## The challenge of the mission to Europa.

- Memory shall meet all performance specifications after being exposed to a radiation TID of:
  - 20 Mrad (10 Mrad environment, RDF = 2) inside the S/C bus, but not enclosed in an IFDP electronics chassis; **Of**,
  - 1 Mrad (500 Krad environment, RDF =2) if enclosed in the Avionics chassis
- 50 Krads (25 Krad environment, RDF = 2) if enclosed in an IFDP electronics chassis and shielded by the equivalent of an IFDP tungsten vault.

Memory shall be designed for a 15 year life

Need Dates.

EM TO JPL DEC. 2004

FLT to JPL March 2005

Europa Orbiter – Mass Memory

## **Other requirements on the list.**

Any device chosen shall not latch-up when exposed to the single events effects environments specified for EO.

The uncorrectable data error rate shall not exceed  $10^{-10}$  bit errors per day.

The memory shall be capable of operating at the continuous read or write rate of 20 Mbits/second.

The memory shall be capable of having data written into each storage location a minimum of 100,000 times.

Memory assembly mass shall not exceed 20 kg. As a goal, the mass shall be no greater than 11 kg.

Power consumption of the memory assembly shall not exceed 15 Watts. As a goal, the power required shall be no greater than 10 Watts.

If power is to be supplied by the spacecraft primary power bus, the memory shall operate nominally over an input voltage range of 22-36 VDC.



## Baseline Size Requirements

1/4/01 study identified the baseline memory requirements:  
 0.9 Gbits of non-volatile memory and 3.6 Gbits of volatile memory

Memory storage requirements (EDAC not included)

Data Type	Non-Volatile CBE	Non-Volatile Allocation	Volatile CBE	Volatile Allocation	Margin <sup>†</sup>
S/C Flight Software	0.268 Gb (32 MB)	0.670 Gb			60%
Sci. Instr. Flight Software			0.268 Gb (32 MB)	0.670 Gb	60%
Orbital Engineering Data	0.121 Gb <sup>2</sup>	0.173 Gb	0.518 Gb	0.741 Gb	30%
Orbital Science Data			1.496 Gb <sup>3</sup>	2.200 Gb	32%
S/C State Data	TBD [64 KB]	TBD [164 KB]			60%
Total <sup>†</sup>		0.843 Gb		3.611 Gb	
Write Cycles	15500, est. 12/99	Limit 100K Lifetime 150K			

**Notes:**

1. Margin = (allocation - CBE) ÷ allocation
2. 14 days of 100 bps data
3. 3 days of science data
4. If all storage is non-volatile, Total = 4.281 Gb because non-volatile engineering data (0.173 Gb) is a subset of the volatile engineering data allocation (0.741 Gb) (to simplify memory management).

## **Implementation Considered**

- Considered a divergent set of technologies:
  - DRAM, SRAM, Flash, Disk
  - FeRAM, MRAM, Chalcogenide
  - Cassini-style BAIL board
    - EEPROM, ROM



# Candidate Technologies Summary

Type	Cap'y	Volatile	Rad Tol (kRads)	Clamshell?	notes
DRAM	256 Mbit	Y	Lo (30-60)	N	
SRAM-RH	4 Mbit	Y	Very Hi	N	>1024 devices req'd
Flash	256 & 512 Mbits	N	Very Lo (7 - 30)	Y	
EEPROM	1Mbit	N	Hi (300)	N	
Disk	1 GByte	N	Lo ? (30?)	Y	In test
FeRAM	256K - 4 Mbit	N	Hi - Very Hi	N	Needs Development
GMRAM	1 Mbit	N	Very Hi	N	Needs Development
C-RAM	1 - 16 Mbit	N	Very Hi	N	Needs Development





## Prime Technologies & Methodology

- 5 Technologies were chosen for further study:  
DRAM, SRAM, EEPROM, Flash, Disk Microdrive
- Mass-power-volume-cost counterpoint analyses were generated for each.
  - Interfaces were studied. Ease of use determined. Cost and development schedule estimated. Risk of success qualified.
- At first, technologies were studied “stand alone.” Later, technologies were blended to see if a synergy developed. *It did*



## A quick Discussion of the Primes

- DRAM and SRAM offer ease of use, but also present inherent risk in that a Power Bus Fault could occur
- DRAM has remarkably high density, but can exhibit ‘SEFI’ conditions (Single Event Functional Interrupt: Single event mode change )
- Too little is currently known about the Microdrive to either Rule In or Rule Out
  - under Investigation
- Flash standalone is not currently considered viable for this mission, however, if Flash is blended with DRAM -- A Reasonable, Low Cost Solution Emerges

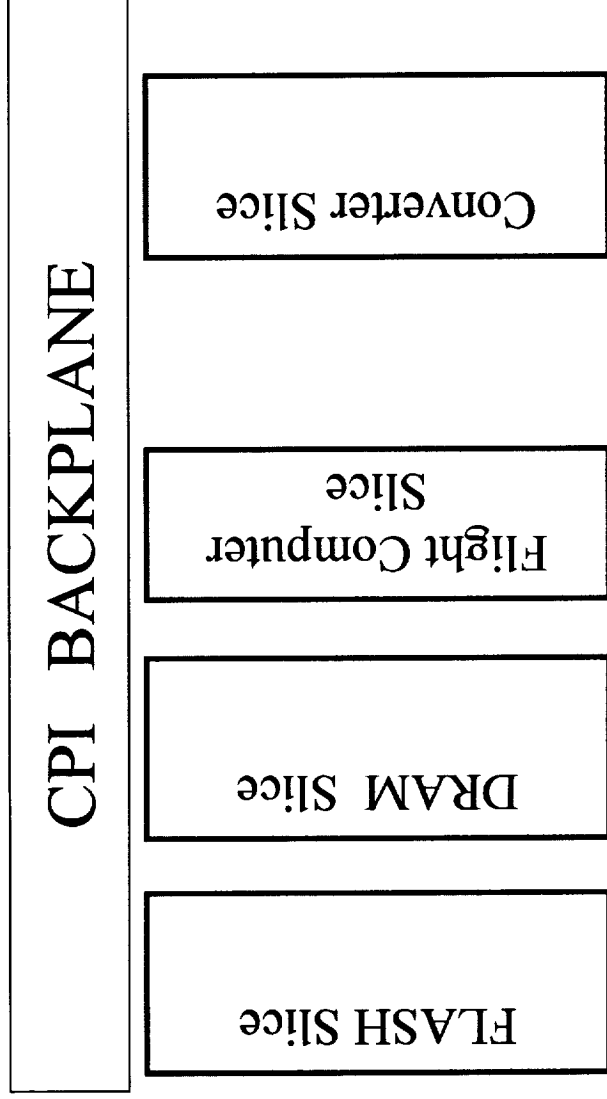
## **Proposed Solution (DRAM + Flash) Current Europa Baseline**

- A solution utilizing existing X2000 Flash Memory Cards (SEAKR) + developing a new DRAM card was considered
  - very low risk, lowest cost, fastest development



# Proposed Implementation (DRAM +Flash)

cCPI Backplane Implementation

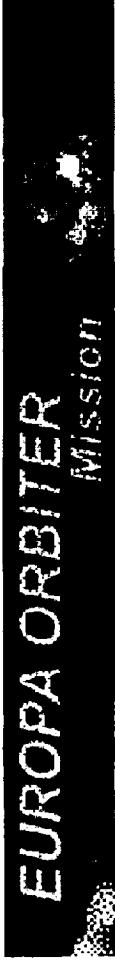


Europa Orbiter – Mass Memory

## The Flash Part

- Flash memory would be used for computer boot and FSW storage; OFF for >95% of the time.
- In this mode, the Flash devices achieve a Total Dose tolerance of ~ 30 kRads\* --- this is roughly equivalent to the TID for the DRAMs used on the SFC

\*(50 - 70 kRad regime if no writes occur past 10-12 kRad exposure)



## Non-Volatile Memory

**Contractor:** SEAKR

**Functionality:**

Bulk Data memory

**Specs:**

**Mass:** With Clamshell: 1.6 Kg; Without Clamshell: 0.34 Kg

**Power:** 2.3 W (max) @ 3.3V operating voltage

**Radiation:** With Clamshell: TID: 30 Krad, 1Mrad ASIC

SEE: 3.7 E -14 word errors/day

Without Clamshell: TID: 8-12 K Rad

SEE: No Latch Up

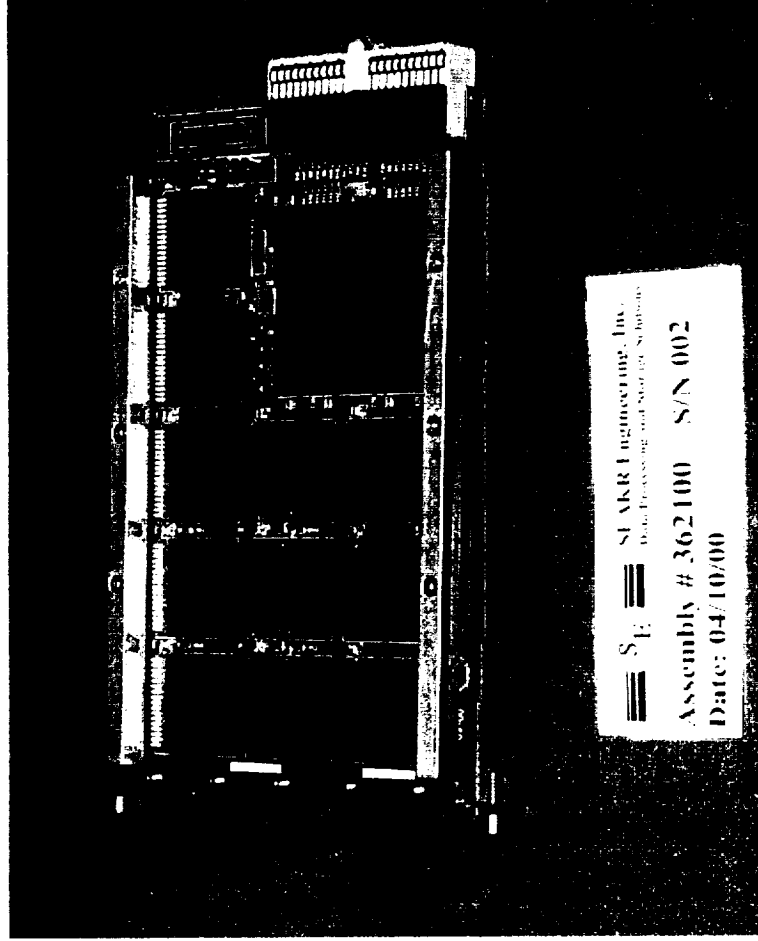
**Interfaces:** PCI Interface

**Mechanical Form:** Double Sided 3U Compact PCI Card

**Features:** 256 Mbytes Data capacity

Data Rate: 4 kb Burst Rate 200Mbit/sec

Option: Removable Clamshell



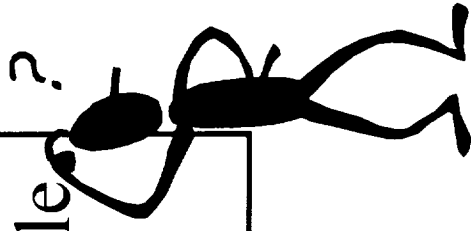
PT Non-Volatile Memory Slice

## The DRAM card

- A new DRAM card would be developed-- this card would be boot-loaded with active program(s), and/or science, engineering, and telemetry data
  - Very simple design

## Other Bits and Pieces- BUT not the end

- Additional variations on the subject where outlined-not reported here. The principle remains the same.
- IBM Microdrives are currently under test
- *We are still looking for a solution. A viable solution for mass memory, non-volatile and other, is needed by all missions.*
- Given that the Flash, DRAM, and Microdrive components are Commercial Off The Shelf, the very real possibility exists that parts tested and acceptable today may not be available tomorrow





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## ***SESSION #2: Environment, Reliability & Characterization***

Wednesday, November 7, 2001

1:40 AM–4:20 PM

Chair: *A. Johnston*, JPL

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- 1:40 PM      Space Radiation Effects in Advanced Flash Memories; *A. Johnston*, JPL
- 2:00 PM      Reliability and Radiation Characterization of an SOI EEPROM/Flash Memory Cell; *H. Peterson, C. Tabbert, F. Wright, H. Anthony, R. Reedy, and J. Cable*, Peregrine Semiconductor Corp.
- 2:20 PM      Evaluation of Data Retention Characteristics for Ferroelectric Random Access Memories; *A. Sharma and A. Teverovsky*, Goddard Space Flight Center (NASA),
- 2:40 PM      BREAK
- 3:00 PM      Radiation Response of Emerging FeRAM Technology; *D. Nguyen and L. Scheick*, JPL
- 3:20 PM      Characterization of Scaled SONOS NVSM Devices for Space and Military Applications; *S. Wrazien, J. Faul, Y. Zhao, and M. White*, Lehigh University, *D. Adams*, Northrop Grumman Corporation, *J. Murray*, Sandia National Laboratories
- 3:40 PM      Overview of Non-Volatile Testing and Screening Methods; *F. Irom*, JPL
- 4:00 PM      An FPGA-Based Test-bed for Reliability and Endurance Characterization of Non-Volatile Memory; *V. Rao and J. Patel*, University of Illinois, *J. Patel and J. Namkung*, JPL
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# Space Radiation Effects in Advanced Flash Memories†

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## I. INTRODUCTION

Memory storage requirements in space systems have steadily increased, much like storage requirements in terrestrial systems. Large arrays of dynamic memories (DRAMs) have been used in solid-state recorders, relying on a combination of shielding and error-detection-and correction (EDAC) to overcome the extreme sensitivity of DRAMs to space radiation. For example, a 2-Gbit memory (with 4-Mb DRAMs) used on the Clementine mission functioned perfectly during its moon mapping mission, in spite of an average of 71 memory bit flips per day from heavy ions.

Although EDAC worked well with older types of memory circuits, newer DRAMs use extremely complex internal architectures which has made it increasingly difficult to implement EDAC. Some newer DRAMs have also exhibited catastrophic latchup.

Flash memories are an intriguing alternative to DRAMs because of their nonvolatile storage and extremely high storage density, particularly for applications where writing is done relatively infrequently. This paper discusses radiation effects in advanced flash memories, including general observations on scaling and architecture as well as the specific experience obtained at the Jet Propulsion Laboratory in evaluating high-density flash memories for use on the NASA mission to Europa, one of Jupiter's moons. This particular mission must pass through the Jovian radiation belts, which imposes a very demanding radiation requirement.

The natural space radiation environment can affect flash memories in four basic ways:

- (1) Macroscopic ionization damage from the interaction of many electrons and protons, producing a buildup of charge in gate and isolation oxides;

- (2) Transient effects from the interaction of a single galactic cosmic ray or high-energy proton, causing upsets in the state machine, buffer or other digital regions of the flash memory (this is analogous to upset effects from alpha particles, but the particles in space produce far more intense track densities);
- (3) Microscopic *ionization* damage from the charge produced by a single cosmic-ray heavy-ion in the gate region; and
- (4) Microscopic *catastrophic* damage from high energy protons or galactic cosmic ray particles which can permanently increase the leakage current of the floating gate.

The first two mechanisms have been observed in older flash memory technologies [1-3], as well as in conventional memories and CMOS integrated circuits. Evidence for the last two mechanisms has been seen in evaluations of other memory technologies (particularly DRAMs), but they have not been examined in detail for flash memories

## II. FLASH TECHNOLOGY EVOLUTION

Flash memory applications can be divided into two basic categories: *code storage*, which requires fast, random access to all memory locations; and *file storage*, which mainly requires access to sequential data. Code storage flash memories usually use NOR architecture, with independent read access for each internal storage location. The cell size of a conventional NOR flash cell with LOCOS isolation is  $\approx 10-11 F^2$ , where  $F$  is the feature size of the technology. Modern NOR flash devices use multi-level storage (storing 3 different levels within each cell and providing 2 binary bits) in order to improve the effective storage density. This decreases the effective cell size to approximately  $6F^2$ , taking into account the requirement for additional circuitry. Multi-level storage reduces the margin between the threshold voltage of the various levels in the floating gate, and also requires a more sophisticated readout technology that can recognize the different charge levels within the floating gates.

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File storage flash memories use NAND architecture, which stacks  $n$  cells together to form a NAND logic array that can only be accessed sequentially. Sixteen or 32 cells are typically used, along with two control transistors [4]. The basic NAND cell occupies only about 50% of the area of a corresponding NOR cell (without considering multi-level storage) because the NAND cell does not require separate access to the source and drain regions of individual transistors in the NAND memory stack.

Scaling in both technologies is limited by the requirement for relatively high voltages for erase and write functions (12-20 V). An internal charge pump is nearly always used to provide those voltages. Special transistors with thicker gate oxides are required within the charge pump as well as in the control logic for writing and erasing.

NOR flash memories have been produced with multi-level storage since 1998. Currently 64-Mb devices are available, fabricated with a 0.25  $\mu\text{m}$  process, and higher density devices are in development using a process with a feature size of 0.18  $\mu\text{m}$  [5].

NAND flash memory trends are shown in Figure 1, adapted from Coi, et al. [6]. There are two "steps" in cell size trends that have reduced the cell size. The first is due to shallow trench isolation in 1998, the second is due to the anticipated use of multi-level cell technologies by mid-2001. NOR cell sizes are shown for comparison. Multi-level cell technology was introduced in the NOR technology in 1999. Dashed lines in the figure show anticipated trends during the next year.

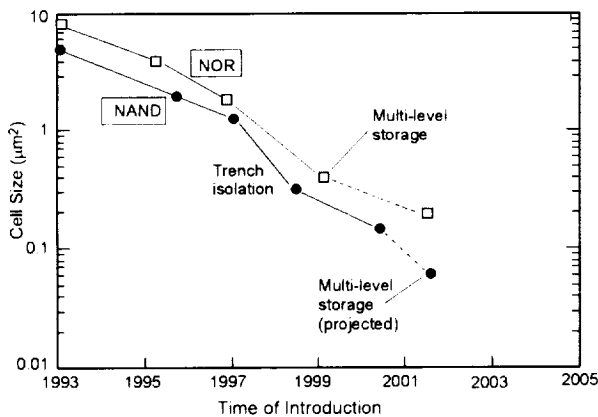


Figure 1 NAND flash memory evolution. The effective cell size decreases by a factor of four when multi-level cell structures are introduced. NOR flash trends are shown for general comparison.

### A. Basic Issues

Ionization from high-energy electrons and protons in space produces electron-hole pairs within gate and isolation oxides of MOS devices. Some of the excess charge is trapped at the interface region, changing the threshold voltage of the transistor. For basic MOS transistors the shift in threshold voltage scales with the square of the oxide thickness [7], which has generally reduced the importance of total dose damage in highly scaled devices.

Although this same scaling scenario applies to flash memories, the internal transistors used for the charge pump and erase/write control have much thicker oxides because of the requirement for high voltage. This causes flash devices to be considerably more sensitive to total dose damage compared to other ULSI technologies. It also implies that write and erase functions will be the first parameters to fail from total dose.

Figure 2 shows the results of probe measurements of the internal charge pump for a 128-Mb NAND flash device. The charge pump voltage starts to degrade at about 6 krad(Si), and falls rapidly at higher levels. At about 8 krad(Si) the device can no longer be erased. The shaded region in the figure shows the range of failure levels for different units from the same group of devices.

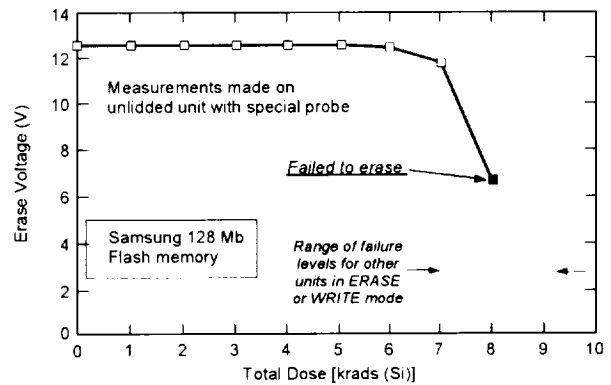


Figure 2 Degradation of the internal charge pump of a 128-Mb NAND flash memory after irradiation with gamma rays.

The gate oxide thickness of high-voltage transistors in this device is nominally 200 Å. At 8 krad(Si), the shift in threshold voltage is about 70 mV, assuming 50% hole trapping.

Flash memories will work at much higher radiation levels in the read mode. Figure 3 shows test results for an older NOR flash device that compares functional operation for biased and unbiased devices (charge trapping is reduced when no electric field is applied during exposure). When

the device is biased, field oxide inversion causes a highly nonlinear increase in power supply current at about 20 krad(Si).

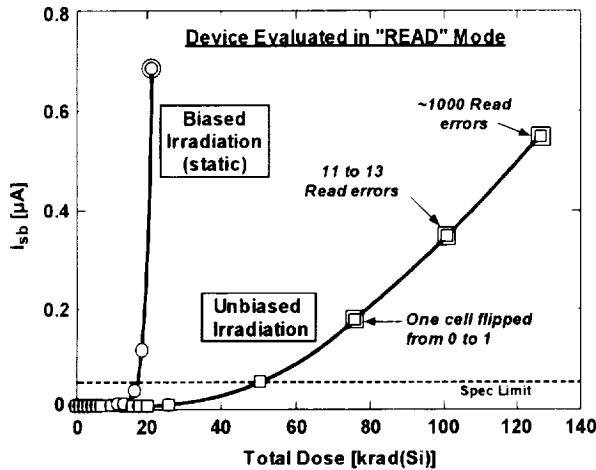


Figure 3 Effect of ionizing radiation on read mode operation of a 16-Mb NOR flash memory. The large increase in power supply current at low total dose levels is due to inversion of the LOCOS field oxide structure.

Trench isolation is used in more advanced flash devices. Similar isolation leakage effects can occur in trench isolation structures. Processing details play a large role in determining their sensitivity to radiation damage.

#### IV. SINGLE-EVENT UPSET EFFECTS

##### A. Basic Issues

Single-event upset sensitivity of flash memories is highly dependent upon the operating mode. If an ion strike causes the internal state machine to be altered, then the device will no longer work properly. This type of functional error is very difficult to categorize because of the limited information on the state machine that can be inferred from external pins. Read, write and erase functions can all be affected. In addition to the state machine, errors can also be introduced into buffers or other active internal memory regions.

Although many different operating conditions can be used for radiation testing, most tests are done with the device in the read mode after a specific pattern is loaded (this assumes that write operations are done infrequently, and that the probability of an ion strike hitting a sensitive node during write or erase operations is small). After the device is exposed to a flux of ions, the memory contents are read out to see if the data has been altered or if the device will still operate without being shut down and reinitialized.

##### B. Representative Test Results (Static Mode)

Tests on 16-Mb NAND flash technology with the device in a static mode during irradiation are shown in Figure 4. The ion used for these tests has an ionization track density that is slightly above the "iron threshold" in the distribution of galactic cosmic rays, and thus is a reasonable measure of the device sensitivity to galactic cosmic ray effects. The same fluence ( $10^6$  ions/cm<sup>2</sup>) was used for each of the four test runs.

Two points can be made concerning these data. First, functional operation was only affected during two of the four test runs. When functional errors occurred, they could either affect readout of the memory or other internal operation of the device in the read mode (such as page-mode errors). However, because the results are inconsistent from run to run, it is not possible to get the same statistical precision about error rates compared with tests that show less ambiguous results.

Second, during the test run there were abrupt increases and decreases in the power supply current. The current changes are likely due to upsets in control logic which cause conflicts in bidirectional logic. The presence of the current steps indicate that many internal regions are affected. However, upsets in regions of the device that affect write or erase functions will not be detected by post-irradiation tests in the read mode.

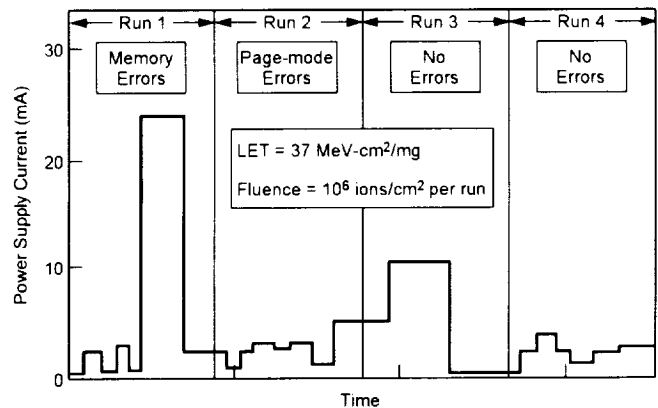


Figure 4 Steps in power supply current during a heavy ion test of a 16-Mb flash memory

Fortunately the cross section for upsets in the state machine is relatively small compared to the total device area. The lower curve in Figure 5 shows the upset cross section for a 16-Mb flash memory, dominated by upsets in the controller. Because of the small cross section, the error rate in space is relatively low, corresponding to one error in time periods of several days to weeks (depending on the particular orbit and other application details). The

upper curve in Figure 5 shows the upset cross section for the buffer in a more advanced 256-Mb flash memory [3]. Unlike the lower curve which was a total device cross section, this curve represents the error rate for a page buffer that stores 528 bits. Thus, the cross section is much larger than that of the older 16-Mbit device, and roughly scales with the size of the memory.

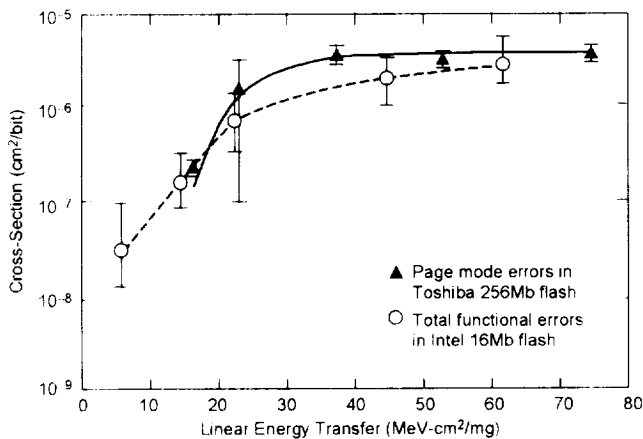


Figure 5 Upset cross section for an older 16-Mb and a more advanced 256-Mb flash memory. The lower curve is a total device cross section, whereas the upper curve for page-mode errors in the 256-Mb device represents errors per bit for a buffer that stores 528 bits

### C. Dealing with the Upset Problem

It is very difficult to detect whether internal errors have occurred in flash memory state machines and control logic because of the “closed” nature of flash memory designs. It is not possible to use address lines, status lines or operational flags that are used for conventional microcontrollers because those functions are buried internally within the flash memory device. Consequently, it is necessary to periodically reinitialize these devices as data is read out. It is also possible to incorporate error-detection techniques to aid in interpreting data validity providing data within a single word is distributed over different chips.

Some visibility can be obtained on internal errors by monitoring selected status lines, such as the page mode information that is present on larger flash devices. However, this does not provide information on overall operational errors, which are usually due to errors in the controller.

## V MICROSCOPIC IONIZATION EFFECTS

Microscopic ionization damage from heavy ions was analyzed by Oldham, et al. in DRAMs in 1993 [8], where it caused increases in cell leakage current that depends on operating conditions (including the refresh rate). The most straightforward way to study microscopic damage effects in DRAMs is to examine the threshold voltage distribution within a device before and after irradiation. Figure 6 shows an example for a dynamic memory where the retention time distribution was used to infer internal threshold voltage after total dose irradiation [9]. The mean value of the retention time changes, but there is a much larger effect on cells at the “tail” of the retention time distribution which have lower threshold voltage, causing the retention time to be more affected by radiation damage (processing variations, including the statistical distribution of dopant atoms in the channel, cause the threshold voltage to vary somewhat for different cell locations)

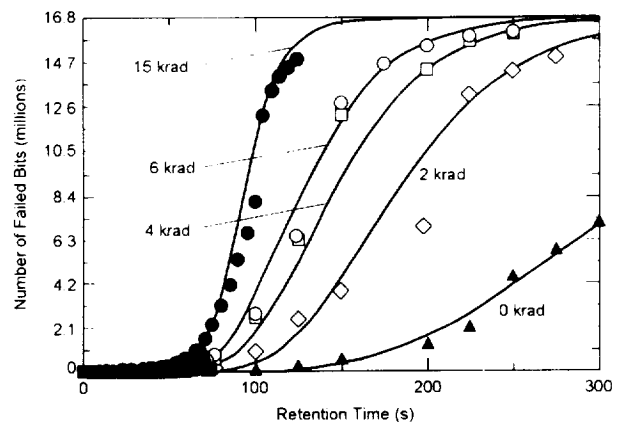


Figure 6 Change in retention time distribution for a DRAM caused by ionization damage. In this case all of the cells are irradiated, but the radiation has a much larger effect on marginal cells with low initial threshold voltage.

Retention time measurements after heavy ion irradiation also show that cells on the “tail” of the distribution are more sensitive to damage [10]. Thus, microdose damage from heavy ions can be investigated by examining threshold voltage distributions.

It is possible to measure threshold distributions on flash memories directly in an analogous manner to that of DRAMs. However, this usually requires special information from the manufacturer, using special probes to make tests on internal test points. Just as for the DRAMs, microscopic ionization damage will be apparent by a change in slope at the extremes of the threshold voltage distribution.

Microscopic ionization damage has been observed in multi-level flash devices after irradiation with heavy ions. The net effect was a shift of the internal state of some of the internal memory cells. This is shown schematically in Figure 7, where 18 cells with the highest internal storage level were shifted to the next level, 23 from the second highest to the third highest, and 2 from that level to the ground level. This is caused by ionization (microdose) that changes the storage level of the charge "packet" within the floating gate. Although this changes the stored information, it does not cause a permanent change in the device; rewriting the cell can be done to restore the information. These types of errors are expected to become more severe for future multi-level flash memories, particularly if larger numbers of bits are stored within each cell, because the internal margin for changes in threshold voltage is reduced.

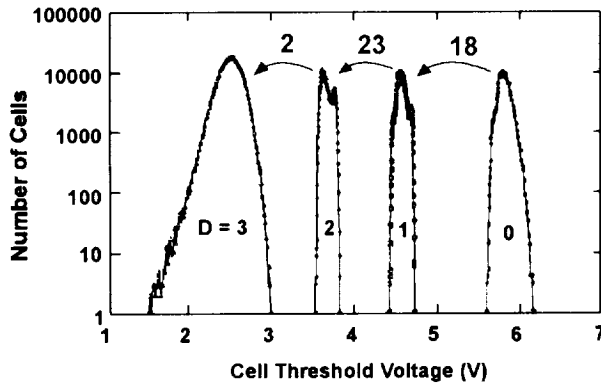


Figure 7 Change in higher-level storage locations in a multi-flash memory after irradiation with heavy ions

## VI. PERMANENT ERRORS CAUSED BY MICROSCOPIC DAMAGE

*Permanent* changes in thin oxide can occur due to the detailed interaction of the intense ionization track from a single heavy ion with the gate region, which produces localized damage in the structure of the gate [10]. The earlier work was done with 4-Mb DRAMs, and similar effects have been observed in 16 and 64-Mb DRAMs. This effect has been studied more recently in capacitor test structures [11], and can cause the leakage current to increase by several orders of magnitude. Figure 8 shows an example of this effect. Although the change in leakage current is small, it can affect the ability of the floating gate to store charge over long time periods. This is a permanent effect, and may limit the ability to use very advanced flash memories in space unless they

are refreshed periodically. The magnitude of the leakage current depends on the thickness of the gate region as well as the quality of the oxide.

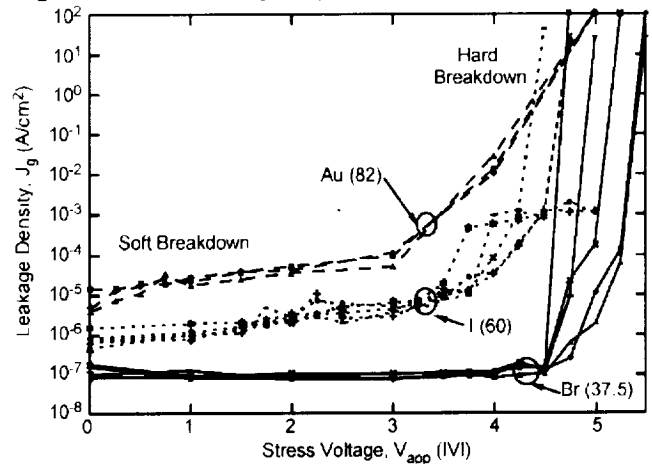


Figure 8 Increase in leakage current of a thin oxide after irradiation with heavy ions

Although high electric fields are required in order to get large current changes (hard breakdown), soft breakdown can occur at very low electric fields and required only a single ion strike. It is possible to deal with this issue by rewriting the memory periodically (similar to refresh in a DRAM, but on a much longer time scale), but this failure mode is clearly an important issue for applying advanced flash memories in space. It may become more important for flash memories in the near future because of the constant requirement to decrease cell size and increase erase/write efficiency.

Other microscopic damage mechanisms may also be important for more highly scaled devices, including microscopic displacement damage from protons. More work is required in order to determine how small cell geometries and more elaborate memory architectures are affected by space radiation.

## VII. CONCLUSIONS

Flash memories have unique design requirements that cause them to be more susceptible to radiation damage compared to more conventional microelectronic components. The high voltage required for the erase and write functions require that some of the internal transistors are designed with thicker gate oxides and more lightly doped channel regions compared to conventional digital logic transistors, making them far more susceptible to radiation damage. The charge pumps that are required to generate the high voltage for erasing and writing are usually the most sensitive circuit

functions, usually failing below 10 krad(Si). Some improvement can be realized by operating the flash memory devices without bias except during the time periods that they are required to operate, and that method has been proposed for possible implementation of advanced flash memories on the JPL Europa mission.

Single-event upset effects are far more difficult to deal with. The very complicated device architecture used in advanced flash devices causes their basic functionality to be affected by heavy ions and protons, and it is difficult to recognize and categorize these types of upsets because of the limited visibility about internal operating conditions. In some cases the device clearly does not function at all, but in others the errors may be difficult to detect -- such as errors in buffers or page address registers. Fortunately the overall error rate for those types of malfunctions is relatively small, allowing system mitigation with EDAC.

Permanent errors are a far more difficult problem for several reasons. First, tests of permanent errors are difficult and costly to perform. Second, some types of errors may occur even for devices that are not biased during the time that a heavy ion strike occurs. Error detection and correction may be a viable way to recognize this type of failure mechanism, but it is also necessary to understand how and why the errors are generated within the device, as well as whether internal errors in the memory controller will affect their operation in space.

#### REFERENCES

- [1] H. R. Schwartz, D. K. Nichols and A. H. Johnston, "Single-Event Upset in Flash Memories," *IEEE Trans. Nucl. Sci.*, **44**(6), 2315 (1997)
- [2] D. N. Nguyen, et al., "Radiation Effects in Advanced Flash Memories," *IEEE Trans. Nucl. Sci.*, **46**(6), 1744 (1999)
- [3] D. R. Roth, et al., "SEU and TID Testing of the Samsung 128 Mbit and the Toshiba 256 Mbit Flash Memory," 2000 IEEE Radiation Effects Data Workshop, p. 96
- [4] S. Antome, "Advanced Flash Memory Technology and Trends for File Storage Applications," 2000 IEDM Technical Digest, p. 763
- [5] A. Fazio, "A High-Density High-Performance 180 nm Generation ETOX Flash Memory Technology," 1999 IEDM Technical Digest, p. 267
- [6] J.-D. Coi, et al., "A 0.15  $\mu\text{m}$  NAND Flash Technology with 0.11  $\mu\text{m}^2$  Cell Size for 1-Gbit Flash Memory," 2000 IEDM Technical Digest, p. 767
- [7] N. S. Saks, M. G. Ancona and J. A. Modolo, "Radiation Effects in MOS Capacitors with Very Thin Oxides at 80 K," *IEEE Trans. Nucl. Sci.*, **31**(6), 1249 (1984)
- [8] T. Oldham, et al., "Total Dose Failures in Advanced Electronics from Single Ions," *IEEE Trans. Nucl. Sci.*, **40**(6), 1820 (1993)
- [9] L. Z. Scheick, S. M. Guertin and G. M. Swift, "Analysis of Radiation Effects on Individual DRAM Cells," *IEEE Trans. Nucl. Sci.*, **47**(6), 2534 (2000)
- [10] G. M. Swift, D. J. Padgett and A. H. Johnston, "A New Class of Single-Event Hard Errors," *IEEE Trans. Nucl. Sci.*, **41**(6), 2043 (1994)
- [11] J. F. Conley, et al., "Heavy Ion Induced Soft Breakdown of Thin Gate Oxides," presented at the 2001 IEEE Nuclear and Space Radiation Effects Conference, Vancouver, British Columbia, July 16-20, 2001, accepted for publication in the *IEEE Trans. Nucl. Sci.*, December, 2001

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## Reliability and Radiation Characterization of an SOI EEPROM/Flash Memory Cell

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### Abstract

This paper describes the on-going work, sponsored through the Defense Threat Reduction Agency (DTRA) SBIR program, at Peregrine Semiconductor Corp to characterize radiation and endurance behavior of the Peregrine's patented **PlusCell™** a new nonvolatile memory cell which utilizes a standard CMOS process on

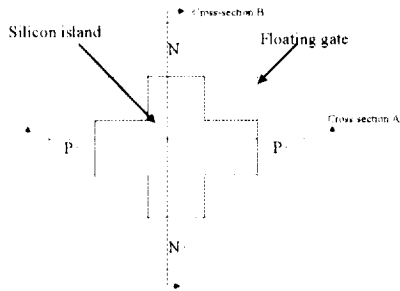
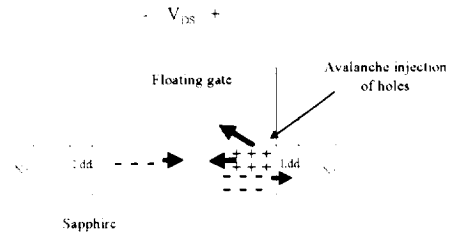


Figure 1 **PlusCell™** EEPROM basic cell

a silicon on insulator technology.

### Introduction

The Peregrine's patented **PlusCell™** shown in Figure 1 is one of several technologies

**Figure 3 Turning on the N-channel by avalanche injection of holes (Cross-section B)** currently under development which offer the potential for radiation hardness, good endurance and solid data retention. The **PlusCell™**, using both hole and electron injection (see Figures 2 and 3), has several key advantages, including elimination of any over-erase mechanism, a dense cell, availability of bi-directional read, and efficient block erase. The layout of the 1.2μm **PlusCell™** is shown in Figure 4.

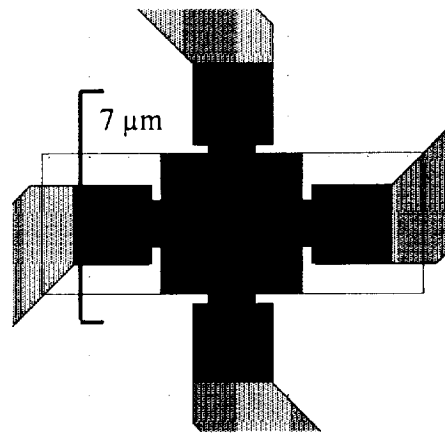


Figure 4 1.2x1.2 μm E<sup>2</sup> Cell for DTRA Characterization

Figure 2 Turning on P-channel transistor by avalanche injection of electrons (Cross-section A)



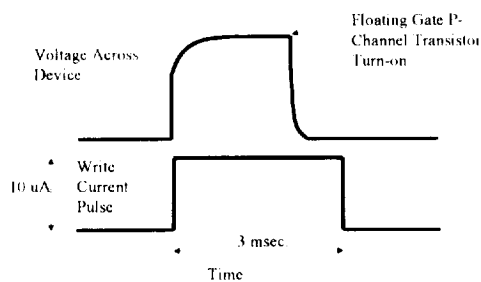
Three modes of operation are possible with the *PlusCell*<sup>TM</sup>

- 1) Write and erase the P-channel transistor
- 2) Write and erase the N-channel transistor
- 3) Write and erase both the P- and the N-channel

Each approach has its own strengths and weaknesses.

#### Writing and Erasing P-channel Transistors

The P-channel transistor is written by a controlled avalanche injection of hot electrons through the gate oxide to the floating gate. Although writing can be accomplished with either a constant voltage pulse or a constant current pulse, the cell endurance is greater with a constant current pulse and therefore this writing mode was



**Figure 5 Current-Voltage Characteristic of P-Channel Transistor**

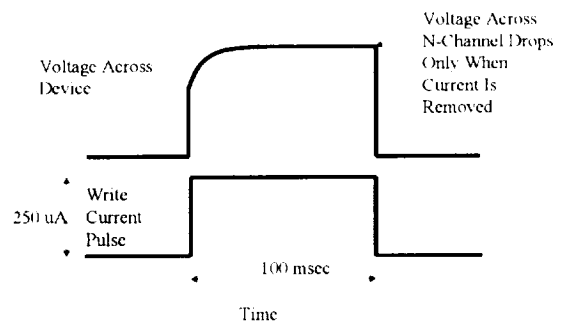
more extensively characterized. The typical write current for the P-channel transistor was 10  $\mu$ A for 3 msec. The voltage as a function of time is shown in Figure 5. As more electrons are injected into the gate oxide near the drain, the avalanche breakdown voltage increases. Ultimately, as charge is collected on the floating gate, the gate voltage exceeds the threshold voltage of the transistor, current is conducted through the channel, and the voltage across the drain junction drops below the voltage required to sustain the avalanche breakdown.

The P-channel transistor is erased by a controlled avalanche injection of holes

through the gate oxide of the N-channel transistor to the shared floating gate. Because of the lower injection efficiency of holes, a much higher current for a longer time is required to inject sufficient holes to erase the P-channel transistor, on the order of 150  $\mu$ A for 15 ms.

#### Writing and Erasing N-Channel Transistors

The N-channel transistor can be written by the same mechanism as the P-channel transistor was erased. However, either the write current or the write time must be increased to inject the necessary charge to turn on the transistor. The current required to write the N-channel exceeds the current carrying capacity of the transistor when the transistor is fully written. Therefore the current carried by the transistor does not exceed the write current and avalanche breakdown continues until the write current is externally removed. A typical voltage versus time plot for a constant current is shown in Figure 6. The N-channel transistor is erased by avalanche injection of electrons through the gate oxide of the P-channel transistor to the shared floating gate



**Figure 6 Current-Voltage Characteristics of N-channel transistor in write mode**

#### Data Retention as a Function of Write Cycles

We have previously reported retention over temperature for cells written with a fixed voltage. The initial endurance measurements suggested that the endurance would improve if the cells were written with

a fixed current, instead of a fixed voltage. Writing the P-channel transistor with a current pulse of 10  $\mu\text{A}$  for 3 ms and erasing the P-channel with a current pulse of 150  $\mu\text{A}$  for 15 ms, good retention was observed out to 200k cycles. Writing the P-channel with a current pulse of 10  $\mu\text{A}$  for 3 ms and then the N-channel transistor with a current pulse of 250  $\mu\text{A}$  for 100 ms in a single cycle, good endurance was observed out to 30k cycles.

#### Endurance and Retention Writing and Erasing P-Channel Transistors

To better understand the relationship between the number of write cycles and the retention over temperature, a matrix experiment was conducted, varying the number of write and erase cycles (1, 1k, 10k, 100k, 200k cycles) and the accelerated life retention temperature (85, 125 and 150C). Measurements were taken out to 168 hours to determine the rate of charge loss. An increase in the rate of charge loss with temperature was anticipated. For the samples written 1, 1k and 10k cycles the expected behavior was observed. However for samples written with 100k and 200k cycles, the rate of charge loss remained unchanged or decreased with increasing temperature. Some annealing of the oxide damage from writing and erasing may be occurring at the higher temperatures. Because the same samples were used at successively higher temperatures with only a single erase and write between successive temperatures, the annealing effect was cumulative. The limited sample size and some scatter in the measured data made it difficult to separate the effects of annealing from basic charge loss. A different set of experiments will be required to estimate the rate of annealing.

#### Endurance and Retention Writing P-Channels and N-Channel Transistors

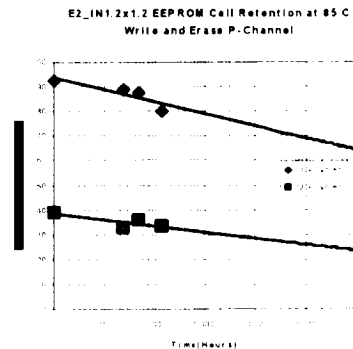
A series of measurements similar to those describe above were also performed while writing to both the P-channel and the N-channel transistors. For this case, retention with the P-channel written and retention

with the N-channel written were studied separately. The conditions for writing with holes were more stressful on the oxide than the conditions for writing with electrons and erasing with holes. 250  $\mu\text{A}$  for 100 ms was required to write with holes. This generates more oxide damage than 150  $\mu\text{A}$  for 15 ms required to erase the P-channel in the case above. The useful life of the cells written with holes is approximately 30k cycles, while the useful of cells written with electrons and erased with holes exceeds 200k cycles.

As expected, the retention of holes on the floating gate was worse at 125 C than at 85 C for all samples tested. However, between 125C and 150 C retention of holes on the floating gate improved, suggesting that annealing of damage to the gate oxide occurred at the higher temperatures. The retention of electrons on the floating gate exhibited less consistent behavior as a function of temperature. In general, the retention of electrons was worse at 125 C than at 85 C. Between 125 C and 150 C the retention of electrons generally improved, again suggesting that annealing at the higher temperature is improving the retention.

#### Implications for Device Use

The above results suggest that the predominant charge loss from the floating gate is different at 150 C than at 85 C and below, and that considerable care should be taken in extrapolating high temperature



**Figure 7 Read Current vs Time for P-Channel for Write and Erase Cycling**

results back to normal operating temperatures, particularly for devices which have seen a large number of write and erase cycles. In applications where the number of write and erase cycles is large, writing with electrons and erasing with holes will yield superior results. The retention for cells with 100k and 200k cycles is shown in Figure 7.

### Radiation Hardness

The EEPROM cell was tested for radiation hardness as a stand-alone element. The retention as a function of x-ray radiation dose is shown in Figures 8 and 9 in the two modes of operation.

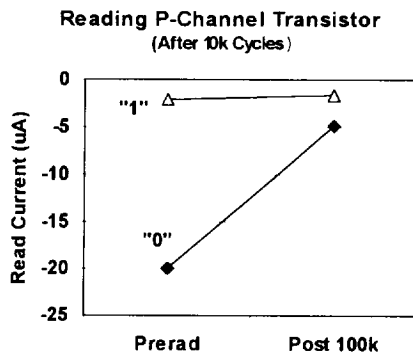


Figure 8 Radiation response of EEPROM cell for a P-Channel read

Reading the P-channel transistor is similar in operation to conventional EEPROM cells, i.e. the current from the P-channel transistor

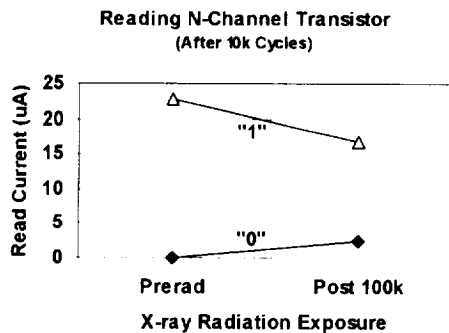


Figure 9 Radiation response of EEPROM cell for an N-channel read

is detected by a sense amp as a "1" or a "0". As can be seen in Figure 8, the current difference between a "1" and a "0" is greatly reduced after 100 krad. The N-channel transistor can be read in a similar manner. Note that at 100 krad the difference between a "1" and a "0" has not collapsed as much for the N-channel transistor (Figure 9) as for the P-channel transistor (Figure 8). The *PlusCell*<sup>TM</sup> can also be incorporated in a latch using a shared gate for both the EEPROM cell and an output inverter. By writing with the P-channel transistor (electron injection) and the N-channel transistor (hole injection), the inverter output will switch between the power supply rails. The performance of this cell is shown in Figure 10 for x-ray radiation doses up to 300 krad.

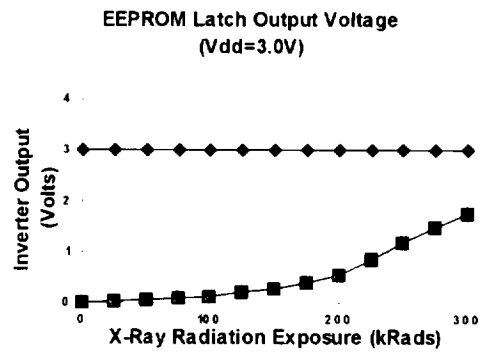


Figure 10 EEPROM latch output voltage as a function of x-ray dose

### Conclusions

The characterization data has shown that the *PlusCell*<sup>TM</sup> should become a viable memory cell for use in military and space applications. The *PlusCell*<sup>TM</sup> will be the basis for embedded EEPROM applications by the Space & Defense community along with introductions of high-density EEPROM devices. Peregrine Semiconductor Corp. is also using the *PlusCell*<sup>TM</sup> in its RF and photonics products for both trimming and tuning.

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# Evaluation of Data Retention Characteristics for Ferroelectric Random Access Memories (FRAMs).

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**Abstract.** Data retention and fatigue characteristics of 64 Kb PZT-based FRAM microcircuits manufactured by Ramtron were examined over temperature range from -85°C to +310 °C for ceramic packaged parts and from -85°C to +175 °C for plastic parts, during retention periods up to several thousand hours. Intrinsic failures, which were caused by a thermal degradation of the ferroelectric cells, occurred in ceramic parts after tens or hundreds hours of aging at temperatures above 200 °C. The activation energy of the retention test failures was 1.05 eV and the extrapolated mean-time-to-failure (MTTF) at room temperature was estimated to be more than 280 years. Multiple write-read cycling (up to  $3 \times 10^7$ ) during the fatigue testing of plastic and ceramic parts did not result in any parametric or functional failures. However, operational currents linearly decreased with the logarithm of number of cycles thus indicating fatigue process in PZT films. Plastic parts, that had more recent date code as compared to ceramic parts, appeared to be using die with improved process technology and showed significantly smaller changes in operational currents and data access times.

applications, especially for long-duration missions. The FRAMs have two orders of magnitude less write access time and require three orders of magnitude less energy per bit write compared to conventional nonvolatile memory devices (EEPROMs and/or Flash Memory). Driven by variety of commercial applications, the density of ferroelectric memories has improved dramatically over the last years. The first, 4 kb, commercially available FRAMs were manufactured by Ramtron less than ten years ago and now memory densities of 1 Gb based on 0.18 um technology appear to be technically feasible [1].

Ferroelectric memories have potentially high radiation tolerance. The ferroelectric capacitors, which are used as memory cells, had been shown to be tolerant to total ionization dose greater than 1 Mrad(Si) without loss of polarization [2], [3]. In many cases the radiation tolerance of the FRAM microcircuits is limited by CMOS circuit elements. By this reason the radiation response of commercial devices with and without ferroelectric films was similar for both parts [4].

One of the major reliability issues for all nonvolatile memory devices, FRAM including, is data retention, which is defined as the ability of a microcircuit to maintain stored data between the time of writing and subsequent reading of the stored information. Temperature significantly accelerates retention failures due to thermal depolarization of the poled state in the ferroelectric material and is commonly used to accelerate this failure mechanism. Experiments on low density Ramtron FRAM microcircuits have demonstrated the failure rate of less than 60 fits with a 60% confidence level for 10-year data storage at room temperature [5]. However, retention characteristics depend on multiple manufacturing and design factors and remain a major reliability concern for new generations of FRAM microcircuits.

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## 1.0 INTRODUCTION

Low power consumption and high operation speed make ferroelectric random access memory microcircuits (FRAM) very attractive for space

Another degradation mechanism, which is known to affect reliability of ferroelectric memory microcircuits is fatigue. Fatigue in ferroelectric materials is a decrease of switchable polarization with increased number of switching cycles or polarization reversals. This degradation process is related to the electrode interfacial areas of the memory cells and can be significantly decreased by using appropriate electrode materials, for example RuO<sub>2</sub>/PZT structures, instead of Pt/PZT structures [6]. The electric-field-assisted migration of charged species (most likely oxygen vacancies) within ferroelectric materials may be also responsible for the degradation/fatigue behavior [7], [8].

In addition to retention and fatigue failures, other failure modes and mechanisms, such as aging, imprint and reducing environment degradation are known to be specific to ferroelectric memory cells in microcircuits.

Aging is defined as a mechanism, which causes signal loss during a retention period which does not recover after a rewrite and immediate read. This differentiates it from the retention failures, where a signal recovers after rewrite and immediate read. Aging is considered as a gradual stabilization of the domain structure due to which the ferroelectric becomes less responsive to applied fields [9], [10].

Imprint is a phenomenon specific to the ferroelectric materials. Once a capacitor spent significant time in one polarity, it is reluctant to switch polarities [11]. This effect is due to accumulation with time of charges in the ferroelectric cell, which compensates the created polarization.

Annealing of Pt/PZT system in a hydrogen-containing ambient (e.g., forming gas) might cause severe degradation of PZT thin film [12]. Hydrogen that reaches the platinum-PZT interface is a strong enough reducing agent, with Pt as a catalyst, to take oxygen from the lead lattice of the PZT. This results in forming a water molecule, which reduces the adhesion between the PZT and platinum and degrades the signal from the ferroelectric cell. It was shown [13] that the hydrogen evolved from plastic packaging during molding and post mold cure can affect data retention reliability of FRAMs. Another mechanism of polarization suppression in PZT films is related to high temperature reducing treatments in dry nitrogen at 400 °C [14]. This treatment creates oxygen vacancies which might lock domains. The trapped charges are believed to inhibit the domain motion and cause failures of memory cells.

Ferroelectric memory is a relatively new, emerging technology, which requires in-deep understanding of the related reliability issues and extensive testing at

extreme conditions before it can be approved for space applications. The objective of this work was to evaluate reliability of commercial 64 kb FRAMs, available from Ramtron, over a wide temperature interval with a focus on data retention characteristics.

## 2.0 EXPERIMENTAL DETAILS

### 2.1 Parts Description.

Fifty FRAM microcircuits in ceramic 28-DIP packages (FM1608S-250CC) and fifty microcircuits in 28-DIP plastic packages (FM1608-P) manufactured by Ramtron were used for this evaluation. The FM1608 is a 64 Kbit, nonvolatile memory, organized as 8,192 x 8 bits. The complete address of 13-bits specifies each of the 8,192 bytes uniquely. The microcircuit is based on two-transistors, two-capacitors memory cells (2T2C), which had been proved to provide most robust data retention reliability [1].

### 2.2 Test Description.

A total of 100 parts, 50 each of ceramic 28-pin DIPs and plastic 28-pin DIPs were divided into various groups and subjected to high temperature storage aging tests at 150 °C, 175 °C, 200 °C\*, 225 °C\*, 250 °C\*, and 275 °C\* (\* ceramic packages only) for up to several thousand hours cumulative. The interim and final electrical measurements (EM) for each group were performed at room temperature. Low temperature testing was performed on a lot of parts at -85°C. Temperature cycling was performed between -65°C and +150°C for 425 cycles with interim and final EM. In addition, fatigue testing by extensive read-write cycling, and total dose ionizing radiation testing were performed on some lots of parts.

### 2.3. Electrical measurements.

Electrical measurements were performed using HP82000 digital tester and included parametric and functional measurements. The parametric measurements incorporated the measurements of input and output voltages and leakage currents (VOL, VOH, IIL, IIH, ILO\_L, ILO\_H), stand-by and active power supply currents (ICCSB\_cmos, ICCSB\_ttl, ICCOP) and chip enable access time, tCE. During the functional testing, six data patterns ("scan 1", "scan 0", "check error board" and three pseudo-random patterns) were consequently written and then read in each test sample. The functional test frequency was 1 MHz.

To evaluate retention characteristics, each sample was subjected to parametric measurements and then functionally tested with the pseudo-random pattern 1

(PRP1). Electrical measurements after the parts had been stressed for a specified period of time (retention period) at specified environmental conditions, began with reading the PRP1 and followed by the parametric measurements. A number of failed vectors obtained after the first PRP1 reading was used to estimate proportion of the failed cells. All parts passed radiography and PIND testing and then were preconditioned by 10,000 write-read cycles. No failures during preconditioning and/or initial electrical measurements were observed.

### 3.0 DATA RETENTION TEST RESULTS

The following sections summarize retention test results for high temperature aging, low temperature exposure testing, total dose radiation testing, and temperature cycling.

#### 3.1 High Temperature Step-Stress Test

The lead zirconate titanate (PZT) remains ferroelectric up to +350 °C (Curie temperature for PZT is about 670 K). However, thermal bakes at temperatures below the Curie point can degrade ferroelectric capacitors as a result of the relaxation phenomenon and aging [13]. Besides, it was not clear whether the CMOS circuits in the parts and the used packaging system can withstand temperatures above 150 °C.

To estimate the temperature range, which causes high rate of the retention failures, and to assure that the ceramic parts can withstand high temperature bakes without catastrophic failures, a high temperature step-stress was performed. Three ceramic parts were subjected to one-hour temperature bake in the range of 150 °C to 310 °C. Test results are summarized in Table 1. Two vectors failed in one of the parts after 175 °C, but then this part passed 200 °C test and no failures were observed up to the step-stress of 285 °C with only a few vectors failed at 310 °C. These results suggest a good thermal tolerance of the parts and indicate the possibility of performing high temperature storage testing.

#### 3.2 High Temperature Aging

Initial electrical testing (at 25°C) was performed on two lots of 5 ceramic and 5 plastic parts, with interim/final EM at 168, 273, 1000, and 5124 hours. All ceramic parts passed all EM. Two out of five plastic parts failed some test vectors on post-273 hours EM, but then passed post-1000 and 5124 hours tests. Test results are summarized in Table 2.

Table 1. Data Retention Results (failed vectors) for the Step-Stress Test.

T, °C	SN 77	SN 78	SN 79
150	0	0	0
175	0	0	2
200	0	0	0
225	0	0	0
240	0	0	0
255	0	0	0
270	0	0	0
285	0	0	1
300	1	0	1
310	1	2	1

Table 2 Data Retention Tests at Room Temperature (25°C).

RT, Hrs	Ceramic Parts		Plastic Parts	
	Failed parts	Failed vectors	Failed parts	Failed vectors
168	0/5	0	1/5	4
273	0/5	0	2/5	3
1000	0/5	0	0/5	0
5124	0/5	0	0/5	0

High temperature aging at 150 °C was performed on two lots of 5 ceramic and 5 plastic parts, with interim and final EM up to 6330 cumulative hours. The same vector in one out of five ceramic parts failed at retention time (RT) of more than 15 hours. A significant increase in failed vectors was observed in ceramic parts at RT > 1000 hours. Intermittent failures were observed for the plastic parts during some interim EM, which cleared up during the following EM, but then again reappeared. Test results are summarized in Table 3.

Table 3. Data Retention Tests at 150 °C.

Total time, hrs	RT, hrs	Ceramic Parts		Plastic Parts	
		Failed parts	Failed vectors	Failed parts	Failed vectors
3	3	0/5	0	1/5	1
18	15	1/5	1*	3/5	9
98	80	1/5	1*	0/5	0
268	170	1/5	1*	2/5	7
698	430	1/5	1*	2/5	3
1698	1000	1/5	5*	3/5	5
6330	4632	2/5	23*	2/5	5

\* same vectors

High temperature aging testing at 175°C was performed on two lots of 3 ceramic and 3 plastic parts, with interim and final EM during 6212 hours cumulative total. All three ceramic parts failed some test vectors during the interim and final EM. Intermittent failures were observed in plastic parts with one out of three failing during the interim EM at 30, 130 hours, which cleared up on post-303 and post-1303 EM. Test results are summarized in Table 4. Note, that the plastic parts had much less failures after 4908 hours of data retention period.

Table 4. Data Retention Tests at 175 °C

Total time, hrs	RT, hrs	Ceramic Parts		Plastic Parts	
		Failed parts	Failed vectors	Failed parts	Failed vectors
30	30	2/3	2*	1/3	4
130	100	2/3	2*	1/3	4
303	273	2/3	2*	0/3	0
1303	1000	3/3	34	0/3	0
6212	4908	3/3	671	2/3	28

\* same vectors

High temperature aging testing at 200 °C and above were carried out only with ceramic parts. At 200 °C interim and final EM were performed at 18, 98, 268, 678, 1678 and 6269 hours, cumulative total. One out of three parts failed interim and final EM with the same failed vector. Test results are summarized in Table 5.

Table 5. Data Retention Tests at 200 °C.

Total, hrs	RT, hrs	Failed parts	Failed vectors
1	1	1/3	1*
4	3	1/3	1*
24	20	1/3	1*
78	53	1/3	1*
248	170	1/3	1*
678	430	1/3	3*
1678	1000	2/3	125
6269	4592	2/3	5747

\* same vectors

High temperature aging testing at 225 °C was performed on 3 ceramic parts with interim and final EM at 1, 4, 19, 49, 149, 449, and 785 hours total cumulative. Two out of three parts failed due to 6

failed vectors. Test results are summarized in Table 6

Table 6. Data Retention Tests at 225 °C

Total, hrs	RT, hrs	Failed parts	Failed vectors
1	1	1/3	1*
4	3	1/3	1
19	15	1/3	1*
49	30	1/3	2*
149	100	2/3	2*
449	300	2/3	2*
785	336	2/3	6*

\* same vectors

Test results for 250 °C and 275 °C aging are displayed separately for each tested part in Tables 7 and 8

Table 7 Failed vectors during Data Retention Tests at 250 °C.

Total, hrs	RT, hrs	SN 87	SN 88	SN 89
1	1	11	5	1*
5	4	21	0	1*
19	14	33	1	1*
47	28	80	2	1*
147	100	144	4	1*

\* same vectors

Table 8. Failed Vectors during Data Retention Tests at 275 °C.

Total, hrs	RT, hrs	SN 95	SN 96	SN 97
6	6	40	0	35
7	0.66	36	0	35
57	50	1810	67	4707
58	1	348	1	1422

The observed data retention test failures can be divided in three categories:

I. Random failures, which are not related to the stress conditions. Plastic parts had approximately 15 times higher probability of similar failures (68 vectors failed during 702 part\*tests for plastic parts and only 7 vectors failed during 1155 part\*tests for ceramic parts). Inadequate writing or reading conditions could be one of the causes of these failures. In this case, a relatively fast relaxation of

the polarization is possible. It is known that significant amount of polarization in PZT films can be lost at times less than 1s [15]. The percentage of polarization loss within 1s after the write pulse applied to a ferroelectric capacitor was found to be only somewhat dependent on the number of read/write cycles and temperature. This degradation is believed to be due to the depolarization fields created in nonswitching interfacial regions.

II. Weak cell failures, which were also not related to stress conditions, but were reproducible from test to test. One-two failed vectors systematically appeared in some of the ceramic parts during the aging tests at 150, 175, 200, 225, and 250 °C. Similar failures were also observed in [16], where retention failures occurred instantaneously after the first thermal cycle and additional bake time did not yield additional failures. Implementing a retention test at elevated temperatures, may most likely screen out this type of failures.

III. Intrinsic failures, which were caused by a degradation of ferroelectric cells. Similar failures occurred in ceramic parts after tens or hundreds hours of aging at temperatures above 200 °C. The plastic parts were tested at temperatures below 200 °C; however, they had significantly less proportion of retention failures compared to the ceramic parts during aging at 150 °C and 175 °C.

### 3.3. Temperature Dependence of Retention Time to Failure.

Based on obtained data, a proportion of failed vectors was plotted with time of high temperature aging on a Weibull probability chart (see Figure 3). The data can be approximated with two lines: a low-slope line ( $\beta \ll 1$ ) at relatively low retention times and a high-slope line with  $\beta > 1$  at large retention times. The low-retention-time failures were due partially to the intermittent failures, whereas the high-retention-time failures (high-beta lines) were due to "intrinsic" failures of the FRAM cells caused by a thermally activated loss of polarization. An extrapolation of the high-beta lines allows for estimation of the median time-to-failure (MTTF) for a test vector. These data are plotted on the Arrhenius chart in Figure 4. It is seen, that the data retention medium time-to-failure follows the Arrhenius law, given by:

$$MTTF = A \times \exp(E/kT)$$

where A is a constant, T is the temperature, and E is the activation energy. Estimated activation energy of the retention test failures was 1.05 eV. This value is close to the 0.94 eV, which was obtained for Ramtron FM24C16, 16 kb microcircuits during testing of the

devices at temperatures of 150, 175, and 200 °C [17]. Activation energy of approximately 1 eV is probably typical for degradation of FRAM memory cells. Calculations based on the data reported for strontium bismuth tantalate (SBT) FRAMs manufactured by Celis Semiconductor [3], yielded activation energy of 1.15 eV.

Extrapolation of the data shown in Figure 4 to normal conditions shows that the MTTF for a vector exceeds  $10^4$  years at room temperature. The number of vectors in 64K FRAM is 8192, which corresponds to the MTTF for the microcircuit of more than 280 years at room temperature operation.

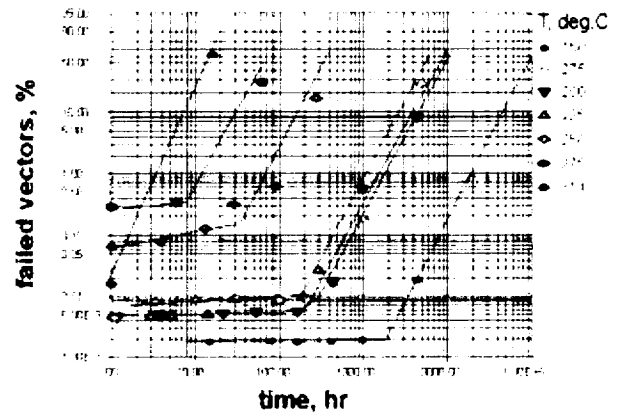


Figure 3. Cumulative proportion of failed vectors in ceramic parts.

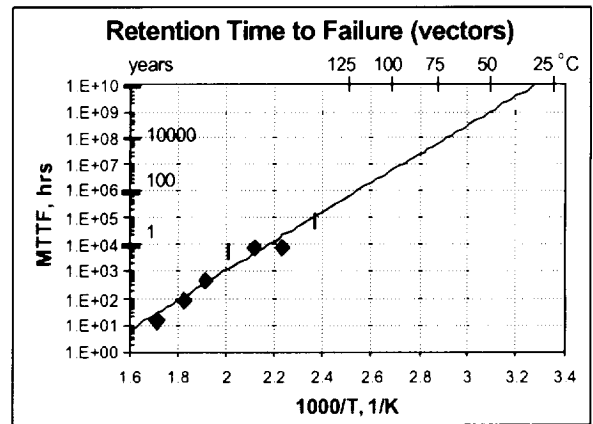


Figure 4. Temperature dependence of the medium time-to-failure.

### 3.4. Low Temperature Exposure Testing

Thermal relaxation of the polarized condition in a ferroelectric capacitor is very unlikely to occur at low temperatures. However, these conditions might create significant mechanical stress in FRAM chips.



These stresses can degrade the capacitors by altering the tetragonal structure of the perovskite lattice [13].

Low temperature exposure testing was performed at  $-85^{\circ}\text{C}$  on two lots of 5 ceramic and 5 plastic parts, with interim and final EM at 3, 28, 128, 373, 1373 and 6473 hours cumulative. Intermittent failures were observed in ceramic as well as in plastic parts with some failures appearing during interim EM that cleared up during following measurements. Test results are summarized in Table 9.

Table 9. Data Retention Tests at  $-85^{\circ}\text{C}$

Total time, hrs	RT, hrs	Ceramic Parts		Plastic parts	
		Failed parts	Failed vectors	Failed parts	Failed vectors
3	3	1/5	1	0/5	0
28	25	2/5	3	2/5	2
128	100	0/5	0	1/5	1
373	245	1/5	1	0/5	0
1373	1000	0/5	0	3/5	5
6473	5110	0/5	0	1/5	3

### 3.5 Temperature Cycling

Temperature cycling can significantly degrade the retention characteristics of FRAM microcircuits. A study [10] was performed to evaluate the effects of thermal excursions on the remnant polarization level in polycrystalline films in test capacitors. An excursion to elevated temperature was found to cause a reduction in retained polarization. Up to 60% of the initial polarization was lost when a device was cycled from  $-25^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . In another study [20], the thermal cycle dependent retentivity problem was attributed to pyroelectric charges that are developed during temperature cycling.

In our evaluation 5 ceramic and 5 plastic parts were subjected to temperature cycling from  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$  with dwell times of 10 minutes at each temperature extreme. Interim and final EM were performed at 10, 40, 140, and 425 cycles cumulative total. All ceramic parts passed all EM. Intermittent failures were observed in one out of five plastic parts that failed during two interim EM, but then passed final EM. Test results are summarized in Table 10.

These results show that the parts can sustain more than 285 temperature cycles, without losing stored information.

Table 10. Data Retention Test for Temperature Cycling ( $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ )

Total Cycles	RT, cycles	Ceramic Parts		Plastic parts	
		Failed parts	Failed vectors	Failed parts	Failed vectors
10	10	0/5	0	0/5	0
40	30	0/5	0	1/5	4
140	100	0/5	0	1/5	4
425	285	0/5	0	0/5	0

### 3.6 Total Dose Radiation Testing

Total dose radiation testing was performed on two lots of 4 ceramic parts and 4 plastic parts, using Co-60 irradiation source, at exposure level steps of 10, 50, and 90 krad(Si) cumulative total, in accordance with MIL-STD-883, Method 1019. Interim and final EM were performed at each of the steps and after final exposure. All four ceramic parts passed EM at all steps including final exposure level of 90 krad(Si). Intermittent failures were observed in plastic parts that failed at some intermediate step levels, but then passed at final exposure step level of 90 krad(Si). Test results are displayed in Table 11.

Table 11. Data Retention Results for Radiation Testing

Total dose (krad)	RT dose (krad)	Ceramic parts		Plastic parts	
		Failed parts	Failed vectors	Failed parts	Failed vectors
0	0	0/4	0	1/4	3
10	10	0/4	0	1/4	1
50	40	0/4	0	3/4	8
90	40	0/4	0	0/3	0

## 4.0 FATIGUE TESTING

One ceramic and one plastic part were subjected to  $3 \times 10^7$  write-read cycles to get preliminary evaluation of the fatigue tolerance of the parts. During the testing, parametric and functional measurements were performed with logarithmic increments in number of cycles to check for any parametric changes or functional anomalies. No failures occurred during the testing; however, some parametric degradation was observed.

Initial parametric measurements of the microcircuits revealed pattern dependence of the operational current (ICCOP). Figure 5 shows the effect of the "1"-to-"0" proportion in vector patterns on the operational current measured in two microcircuits. In both cases the current linearly increased with the proportion of bit "1" with the same slope of 0.0053 mA/%. The result can be explained, assuming that a significant proportion of the measured current is due to the sum of elementary switching currents in the ferroelectric cells. When a bit "1" is written, the elementary switching current is a sum of a linear (or nonswitching) response and a switching response of a cell. When a bit "0" is written, the cell current is due to only nonswitching response. The possibility to estimate switching current allows monitoring fatigue processes in ferroelectric cells by comparing operational currents with different patterns.

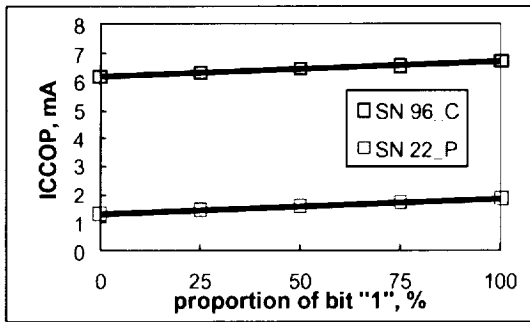
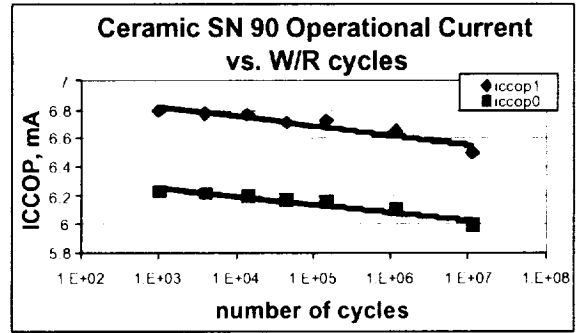


Figure 5. Effect of bits "1" to "0" ratio in the test pattern on operational current in a ceramic and a plastic part.

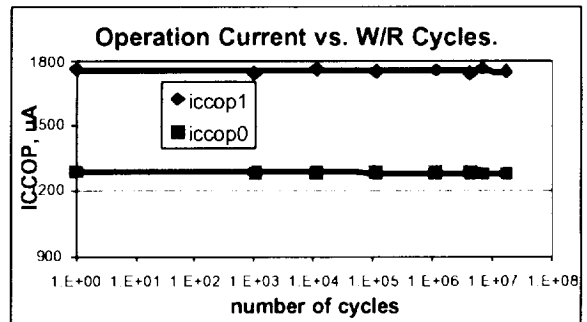
Test results shown in Figure 5 indicate that the operational currents decreased linearly with a logarithm of number of cycles:  $\log = \log(0) + \alpha * \lg(t)$ , where  $\log(0)$  is the initial current and  $\alpha$  is the slope. Results of calculations of the slope values are shown in Table 12.

Table 12. Operational current fatigue curve slope,  $\alpha$ , ( $\mu\text{A}/\text{decade}$ ).

Pattern	Ceramic part	Plastic part
ICCOp1	-67.16	-0.8234
ICCOp0	-56.12	-1.2972
$\Delta = \text{ICCOp1} - \text{ICCOp0}$	-11.27	0.4508



a)



b)

Figure 6. Fatigue test results for (a) ceramic, and (b) plastic parts.

For both patterns ("1" and "0"), the slope was negative, indicating a decrease in the nonswitching polarization. The plastic part had 50 to 80 times less slope than the ceramic part. This was probably due to some improvements in the process of wafer manufacturing of dice used in the plastic parts. Internal examination confirmed that the plastic and ceramic parts were manufactured using different processes. The die size, pattern size and layouts were different. The dice used in plastic parts were manufactured using 1998 photomasks and the dice, which were used in ceramic parts, were dated 1996. For the ceramic part the difference between ICCOp1 and ICCOp0 decreased with time, indicating some fatigue-related decrease of the switching polarization.

## 5.0 CONCLUSIONS

1. Data Retention characteristics of 64k FRAM microcircuits were characterized in temperature range from  $-85^{\circ}\text{C}$  to  $+310^{\circ}\text{C}$  during retention periods, up to several thousand hours with the following results:
  - 1.1. No parametric or functional failures, which would suggest aging degradation, had occurred during multiple ceramic and plastic

parts testing at aging temperatures below 250 °C

- 1.2. The observed retention test failures can be divided in three categories:
  - Random failures, which are not related to stress conditions. Plastic parts had approximately 15 times higher probability of similar failures.
  - Weak cell failures, which were also not related to a stress condition, but were reproducible from test to test. One-two failed vectors systematically appeared in some parts during the aging tests. Implementing a high temperature retention test most likely could screen out similar failures.
  - Intrinsic failures, which were caused by a thermal degradation of the ferroelectric cells. Similar failures occurred in ceramic parts after tens or hundreds hours of aging at temperatures above 200 °C. An estimated activation energy of the retention test failures was 1.05 eV and the extrapolated mean time to failure at room temperature is more than 280 years.
- 1.3. No parametric or functional failures of ceramic or plastic parts were detected during multiple (up to 425 cycles) temperature cycling from -65 °C to +150 °C. Both type of parts (ceramic and plastic) withstood data retention test with 285 temperature cycles between writing and reading.
- 1.4. Retention test at -85 °C did not reveal any intrinsic failures. However, some random failures occurred both in ceramic and in plastic parts. The long-term storage (more than 5000 hrs retention time) of the parts did not result in any parametric or functional degradation.
- 1.5. No retention, parametric, or functional failures occurred with ceramic parts during the radiation tests with cumulative total dose of 90 krad (Si). Plastic parts had some random retention test failures.
2. Operational current measurements with different patterns allow for estimation of the levels of switching and non-switching polarization in the ferroelectric cells. The difference between these two currents depends on the average remnant polarization and can be used for monitoring degradation processes in the memory cells. However, additional analysis should be performed to reliably establish the relationship

between the operational currents and the level of cell polarization.

3. Multiple write-read cycling (up to  $3 \times 10^7$ ) during fatigue testing of plastic and ceramic parts did not result in any parametric or functional failures. However operational currents linearly decreased with the logarithm of number of cycles, thus indicating fatigue process in the PZT films. Plastic parts manifested significantly smaller changes in operational currents, which could be due to the different die lots used in manufacturing of these parts.
4. Test results confirmed that PZT-based FRAM microcircuits potentially might have perfect retention and virtually fatigue-free characteristics over a wide interval of temperatures and write-read cycles. This, as well as a high radiation tolerance, low power and write time makes these devices very attractive for space applications. However, further improvements in the manufacturing process and/or testing and screening system are necessary to reduce random soft failures in these devices.

## 6. ACKNOWLEDGEMENTS

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## References

- [1] A.Sheikholeslami, P.Gulak, A survey of circuit innovations in ferroelectric memories, Proc. IEEE, v.88, N5, 2000, pp.667-689.
- [2] K.F. Strauss, et al, "Overview of radiation tolerant unlimited write cycle non-volatile memory", Aerospace Conference Proceedings, 2000 IEEE, Volume: 5, 2000, pp. 399-408.
- [3] S.C. Philpy, et al., "Ferroelectric memory technology for aerospace applications", IEEE Aerospace Conference Proceedings, 2000, v. 5, pp. 377-383.
- [4] J.M. Benedetto, et al., "Radiation evaluation of commercial ferroelectric nonvolatile memories", IEEE Transactions on Nuclear Science, v. 38, Issue 6, Part: 1, Dec. 1991, pp. 1410-1414.
- [5] E.M. Philofsky, "FRAM-the ultimate memory", Sixth Biennial IEEE International Nonvolatile Memory Technology Conference, 1996, pp.: 99-104.

- [6] J.J.Lee, et al., "Electrode contacts on ferroelectric PZT and SBT thin films and their influence on fatigue properties", J. Appl. Phys, v.78, #8, 1995, pp.5073-5077.
- [7] J.Chen, et al., "Compositional control of ferroelectric fatigue in perovskite ferroelectric ceramics and thin films", J. Appl. Phys, v.76, #9, 1994, pp.5394-5398.
- [8] J. Chen, et al., "Polarization fatigue in perovskite ferroelectric ceramics and thin-films", Proceedings of the Eighth IEEE International Symposium on Applications of Ferroelectrics, ISAF'92, 1992, pp. 111 – 115.
- [9] D. E. Fisch, et al., "Analysis of thin film ferroelectric aging", IEEE, IRPS, 1990, pp 237-242.
- [10] Gregory, A.; et al., "Thermal stability of ferroelectric memories", 30th Annual Proceedings., International Reliability Physics Symposium 1992., Page(s): 91 –94.
- [11] D Hadnagy, "Making ferroelectric memories". The industrial physicist, Dec. 1999, pp.26-28.
- [12] Woo Sik Kim et al., "Fabrication and characterization of Pt-oxide electrode for FeRAM application". International Conference Microprocesses and Nanotechnology, 2000 Page(s): 186 –187.
- [13] E.M. Philofsky, et al., "The evolution of hydrogen from plastic molding compound and it's effect on yield and reliability of ferroelectric memories", 36th Annual Proceedings, International Reliability Physics Symposium 1998., Page(s): 232 –237.
- [14] W.L.Warren, et al., "Polarization suppression in Pb(Zr,Ti)O<sub>3</sub> thin films", J.Appl. Phys, v.77, (12), 1995, pp. 6695-6701.
- [15] J.M. Benedetto, et al., "Effect of operating conditions on the fast-decay component of the retained polarization in lead zirconate titanate thin films", J. Appl. Phys., v. 75 (1), 1994, pp. 460-466.
- [16] S.D Traynor, "Polarization as driving force in accelerated retention measurements on ferroelectric thin films", 1998, pp. 15-18.
- [17] Ramtron Application Note: FRAM<sup>®</sup> Technology Backgrounder, Technology notes, [www.ramtron.com](http://www.ramtron.com)

analysis and evaluation of hybrids, microcircuits and discrete active and passive components. Currently, he is involved in several projects aimed to evaluate new technologies and components for space applications.

Dr. Teverovsky is an author of more than 50 technical publications and holds several patents on test techniques.

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# Radiation Response of Emerging FeRAM Technology

D. N. Nguyen and L. Z. Scheick

**Abstract**— The test results of measurements performed on two different sizes of ferroelectric RAM (FeRAM) suggest the degradation is due to the low radiation tolerance of sense amplifiers and reference voltage generators which are based on commercial CMOS technology. This paper presents TID testing of 64Kb Ramtron FM1608 and 256Kb Ramtron FM1808.

## I. INTRODUCTION

Ferroelectric memories have received more research attention in recent years. In term of the number of inventions granted by the U.S patent office, there were 120 for the year of 1999 alone. Fast programming time with low power consumption and the rising demands of smart cards and digital cameras have driven the recent activity. In addition, many deep space and near earth missions are looking for alternatives to traditional NVM. Floating-gate memories such as flash memories and EEPROMs with larger storage capability currently dominated the digital camera applications are due in part to its mature process technology. But ferroelectric memories possess superior features over floating-gate devices. These are write-access time and overall power consumption [1]. Table I compares flash memories, EEPROMs and ferroelectric memories. Digital cameras for use in future space rovers and miniature smart instruments will benefit from the fast frequent writes and low power usages of ferroelectric memories.

TABLE I  
Comparison of Nonvolatile Memories

	FeRAM	EEPROM	Flash
Write (ns)	100	$10^6 - 10^7$	$10^4 - 10^5$
Write Voltage	1-3V	12-18V	12-21V
Write cycles	$>10^{12}$	$10^5$	$10^5 - 10^6$
Overwrite	Yes	No	No

The work described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration, Code AE., under the NASA Microelectronics Space Radiation Effects Program (MSREP).  
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In addition to fast write requirements, battery-less smart cards operate from power supplied by an r-f signal from the card reader.

## II. DEVICES DESCRIPTIONS

### A. Ferroelectric Technology

The ferroelectric effect is characterized by the remnant polarization that occurs after an electric field has been applied. The unique chemical atomic ordering of these materials allows a single ion to change its physical location. Figure 1 shows simplified models of a ferroelectric material. The center atom (zirconium or titanium) will move into one of the two stable states upon an external applied electric field. After the external electric field is removed, the atom remains polarized in either state; this effect is the basis of the ferroelectric as a nonvolatile memory. An electric field can reverse the polarization state of the center atom, changing from a logic state "0" to "1" or vice versa.

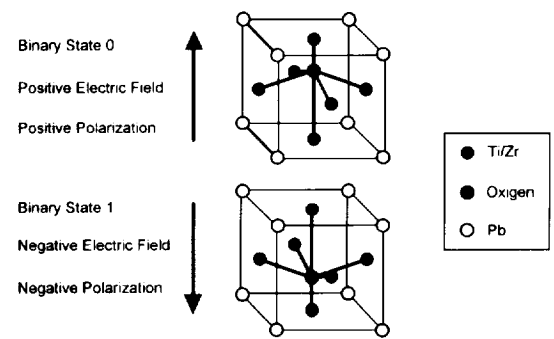


Fig 1. Two stable states in a ferroelectric material

The ferroelectric thin-film material of RAMTRON product is lead-zirconate-titanate (PZT). Figure 2 shows the hysteresis loop exhibited by a PZT ferroelectric capacitor. The total charge for a relaxed "0" state is  $Q_r$  and  $-Q_r$  for a relaxed "1" state. By applying a negative voltage across the capacitor, a "0" state can be changed to "1", and consequently the total charge on the capacitor is reduced by  $2Q_r$ . With a positive voltage across the capacitor, a "1" can be switched back to "0", and the total charge restores to  $+Q_r$ . The nonvolatile polarization,  $P_{nv}$ , is the difference between the relaxed states, the charge density that can be sensed by the sense amplifier circuitry.

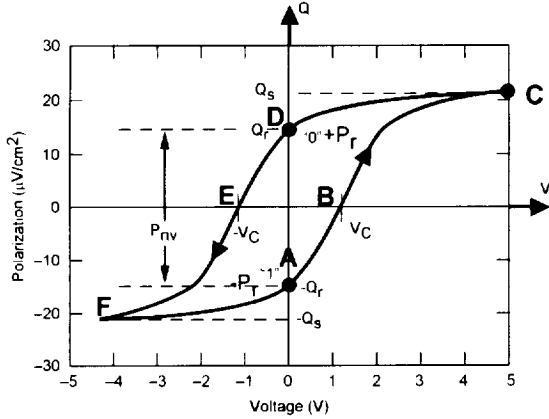


Fig 2. Hysteresis loop characteristic of a ferroelectric capacitor. Applying  $V_{cc} = 0$  to the ferroelectric capacitor results in points D and A. The remnant polarization charge is  $+P_r$  or  $-P_r$  allowing binary data to be stored.

Ramtron FM1608 and FM1808 are built using 2 transistors/2 capacitor bit cells (2T/2C) structures as shown in Figure 3. A sense amplifier connected to the bit lines reads the output by measuring the difference of charge transferred from the two cells. In read operation, BL must be precharged to 0V. WL is selected and PL is pulsed to  $+V_{cc}$  or to the "C" state as marked in Figure 2. If the cell holds "0" state, the polarization is not reversed but the slight movement of the electric charge causes BL to charge up by  $V_1$ . Since no reversal of polarity occurs, the data is not destroyed and a "0" state is retained. If the cell holds "1" state, polarization is reversed, causing a large amount of charge to go to the bit line BL. When reading "1" data, the reversed polarization creates "0" logic state or destroyed the initial data. After the reading of "1" data takes place, the voltage on the bit line is at  $V_{cc}$ . The PL voltage level is at 0V, restores the correct "1" data to the cell. The plate line is usually pulsed to supply both polarities of write signals to the capacitor [2]. The 2T/2C structure is inherently reliable but at the expense of device real estate.

### B. Device Descriptions

The RAMTRON FM1608 is organized as 8,192 x 8 bits and the FM1808 as 32,768 x 8 bits Ferroelectric Nonvolatile RAM. Both parts operate internally at  $V_{cc}$  of 5.0 volts during the erase and write processes. During the write operation, the required electric field needs to polarize the nonvolatile elements takes about 100ns. The entire memory operation occurs in a single bus cycle and therefore there is no data-polling requirement. The memory array of FM1808 is divided into 32 blocks of 1k x 8 each. The

FM1608 has 8 blocks of 1k x 8 each. Each block of 1k x 8 consists of 256 rows and 4 columns.

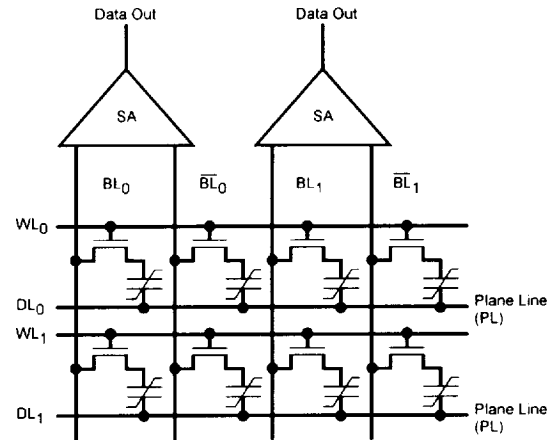


Fig 3. 2-transistor/2-capacitor cells architecture

## III. TEST RESULTS

### A. Test Approach

Three devices of each part type were irradiated with Co-60 at room temperature with a static biased configuration. Electrical measurements were made with the Advantest test system T3342. Data of the following parameters were recorded between radiation levels: standby current  $I_{sb}$ , input currents  $I_{ih}$  and  $I_{il}$ , and functional tests. Devices were programmed with a checkerboard pattern, and then were verified for the integrity of the test pattern. The DUT power supply voltage was removed, and then reconnected for the read operation to test the nonvolatile data. Devices then were placed in the Co-60 chamber and were irradiated at 50 rad(Si)/s at  $V_{cc} = 5.0$  volts.

### B. TID Results

Both RAMTRON device types had very similar test results. They performed normally at 10 krad(Si), but started having read errors at around 12.5 krad(Si). They stopped to function at 25 krad(Si) and did not recover after 24 hours at 100C annealing process. Both device types standby currents went upward rapidly after 10 krad(Si).

#### 1. FM1608 devices:

The 64Kb FeRAM devices were irradiated at the following dose levels: 5 krad(Si), 7.5krad(Si), 10krad(Si), 11.25 krad(Si), 12.5 krad(Si), 25krad(Si) and 50krad(Si). Figure 4 shows the devices function well pass 10 krad(Si). They started having read errors

around 12.5 krad(Si) when the standby current went into mA range. But after rewrite with the same pattern, the parts were functional again. At 25krad(Si), devices failed to read all 8,192 cells. DUTs were programmed with all zeros and then read back. None of the 8,192 locations had registered a "0" state. At 50krad(Si), the input current  $I_{ih}$  is marginally over the specifications limit of 10 $\mu$ A, precisely at 12.3 $\mu$ A.

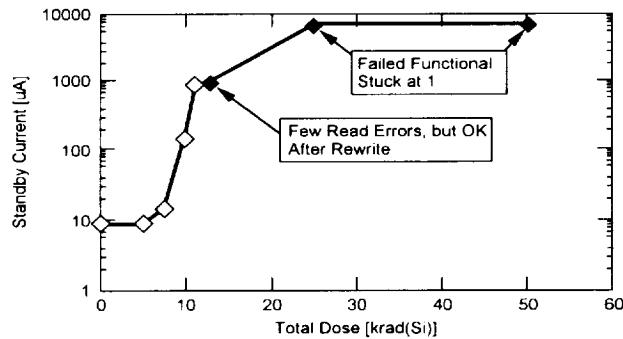


Fig 4. Standby Current vs. Total Dose of 64Kb FeRAM

Figure 5 shows standby currents of two post-irradiated DUTs after more than 100 hours unbiased room temperature anneal versus the number of write/read cycles. Serial number 4278 part had 2 read errors prior to the cycling test. The two read errors stayed until the end of the 9 millionth cycles.

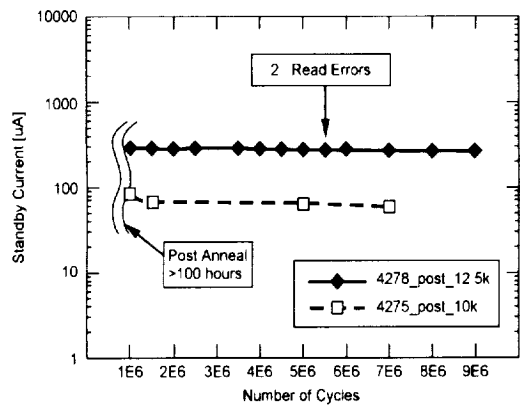


Fig 5. Standby current vs. cycling of FM1608

## 2 FM1808 devices:

The 256Kb FeRAMs were exposed at the following dose levels: 5 krad(Si), 7.5krad(Si), 10krad(Si), 12.5krad(Si), and 25 krad(Si). Figure 6 illustrates its response of standby current versus the total dose. Like the FM1608 parts, DUTs passed at 10 krad(Si) with standby current recorded under 20  $\mu$ A. Three read errors were observed at 12.5 krad(Si) and standby current started going upward to 100  $\mu$ A range.

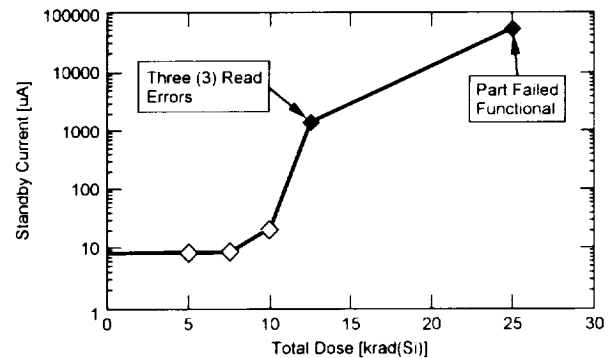


Fig 6. Standby current vs. Total Dose of 256Kb FeRAM

## IV. CONCLUSIONS

The FRAM is affected and seems to have TID problems at around 12.5 krad(Si) and ceases to function at 25 krad(Si). Since writing to FeRAM cells is a direct overwrite process, there is no pre-erase and polling to monitor and keep track of how many write errors accumulated during programming. Ferroelectric thin films have been seen to be inherently resistant to ionizing radiation [3]. In order to operate normally in a radiation environment, ferroelectric technology will need to combine with a radiation hardened CMOS process in order to withstand higher TID levels. Samples of devices of large sizes, 1Mb to 32Mb are being procured. Samples from other manufacturers also are being investigated.

## V. REFERENCES

- [1] A. Sheikholeslami and P.G. Gulak, "A survey of circuit innovations in ferroelectric random-access memories," *2000 Proceedings of the IEEE*, vol. 88, no. 5, pp. 667-689, May 2000.
- [2] E.M. Philofsky, "FRAM-the ultimate memory," *Int'l NonVolatile Memory Technology Conference*, 1996, pp. 99-104.
- [3] S.C. Lee, G. Teowee, R.D. Schrimpf, D.P. Birnie, III, D.R. Uhlmann, and K.F. Galloway, "Total dose radiation effects on Sol-Gel derived PZT thin films," *IEEE Trans. On Nucl. Sci.*, vol. 39, no. 6, pp. 2036-2043, December 1992.

# Characterization of Scaled SONOS NVSM Devices for Space and Military Applications

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**Abstract**—We present results on scaled Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) non-volatile semiconductor memory (NVSM) devices designed specifically for high-density, EEPROMs operating in space and military environments. We describe scaling considerations and process optimization to achieve low-voltage operation (+7V write for 2.5 ms/-7V erase for 7.5 ms) with 10-year retention at 80C. We have conducted studies on ‘oxynitride’ films at temperatures ranging from 22-250C. An extrapolated 10-year memory window of 1.2V is obtained at 22C reducing to an acceptable 0.8V at 80C. SONOS device trap density profiles are compared for both ‘oxynitride’ and ‘silicon-rich’ nitride films.

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## 1. INTRODUCTION

Since the advent of the nonvolatile MNOS semiconductor memory in 1967 [1], there have been a wide variety of roles for nitride-based nonvolatile memory structures. Researchers at Northrop Grumman and Westinghouse Corporations have been involved in this work from almost its inception [2]. Northrop has been working with Sandia National Laboratories and Lehigh University in order to refine this technology for use in applications, such as satellites and nuclear technology. Our work focuses on

the characterization of thermal acceleration effects with a goal of establishing a screening procedure to guarantee 10-year memory retention at +80 C.

In our studies, SONOS nonvolatile memory devices are fabricated with a gate dielectric consisting of an 18 Å tunneling oxide, 80 Å “oxynitride” layer, and a 40 Å so-called ‘blocking’ oxide underneath a phosphorus-doped polysilicon gate [2]. The gate dielectric is programmed by applying either +7 V to the gate terminal for 2.5 msec, or a -7 V pulse for 7.5 msec. The applied voltage attracts electrons or holes to the surface of the silicon depending on the polarity of the gate voltage [3]. Subsequently, these carriers tunnel through an ultra-thin oxide and store in “traps” within a nitride layer. Fig. 1 shows the write/erase operation and Fig. 2 the electric field for tunneling.

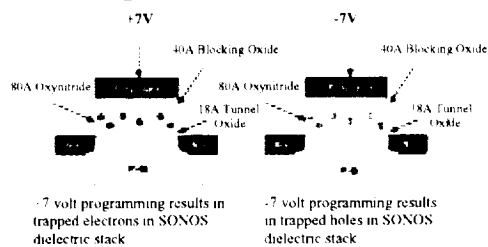


Figure 1—Write/Erase Operation for a SONOS Device

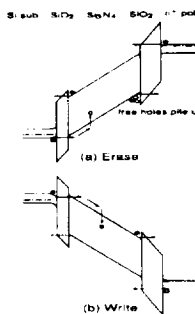


Figure 2 - Tunneling in a SONOS Device



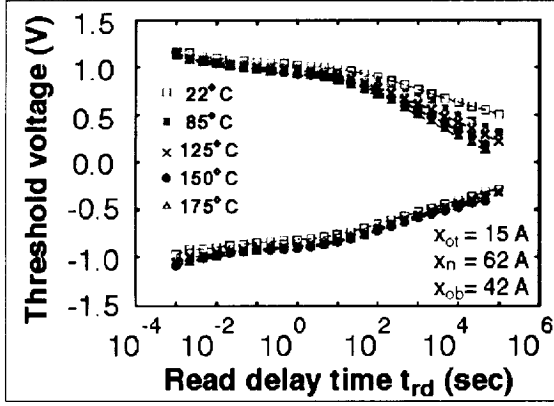


Figure 3 Threshold Voltage decay vs. Temperature for a 'silicon-rich' Scaled SONOS NVSM Device. The device has experienced  $10^3$  erase/write cycles. The initial  $V_{TH}$  is set with a series of erase/write pulses of  $\pm 7V$ , 1msec [13].

## 2. SONOS RETENTION AT ELEVATED TEMPERATURES – MODELING

The decay of the charge stored in the nitride layer at room temperature has been modeled by a number of investigators, such as White and Cricchi [4], Lundkvist, Lundstrom, Svensson [5], Roy and White [6], Kamagaki and Minami [7,8], and Hu and White [9]. These models invoke back tunneling of charge from the nitride to the semiconductor substrate. An internal field due to trapped charge enhances the process of tunneling.

The characterization of charge trapped in a nitride dielectric at elevated temperatures had been investigated for SNOS devices by Sandia researchers [10,11] and researchers from Chalmers University in Sweden [12]. Recently, with the advent of scaled SONOS devices, Lehigh researchers Yang and White [13] have examined the temperature dependence with an amphoteric trap model, which attributes the electron and hole charge storage to a silicon dangling bond. Their results, shown in Fig. 3, indicate the trapped 'electrons' in the nitride layer are thermally excited at elevated temperatures and 'back tunnel' through an ultra-thin tunnel oxide to the silicon. In contrast, the distribution of trapped 'holes' is influenced very little with increasing temperature. This result was explained by suggesting the activation energy for the electron traps lies closer to the conduction band edge in the silicon nitride than the activation energy for hole traps to edge of the valence band in the silicon nitride as shown in Figure 4.

Using this trap model, Yang and White [13] derived an expression for the charge trapped in the nitride,

$$\rho_n(x, E_{TA}, t) = -qg(x, E_{TA})f^- \quad (1)$$

where  $E_{TA}$  is the energy level of the trap,  $f^-$  is the trap occupancy function for electrons, and  $g(x, E_{TA})$  is the density of traps in the nitride (traps/cm<sup>3</sup>eV) at a distance

'x' from the tunnel oxide-nitride interface into the nitride.

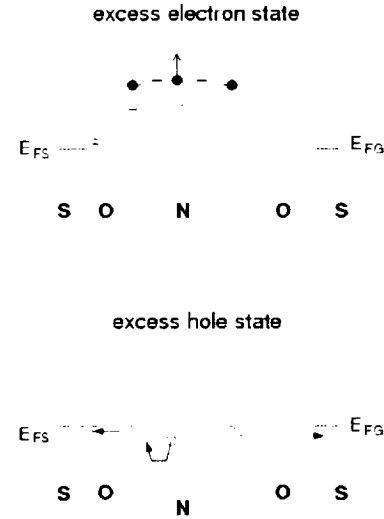


Figure 4 – Storage of Nitride Trapped Charge

The charge stored in the nitride causes a shift in the threshold voltage of the device,  $\Delta V_{TH}$ , which can be written as [13],

$$\frac{\partial \Delta V_{TH}}{\partial \log(t)} = -2.3k_B T X_N \left( \frac{X_N}{2\epsilon_N} + \frac{X_{OB}}{\epsilon_{OX}} \right) g(E_{TA}) \quad (2)$$

where  $X_N$  and  $X_{OB}$  are the thicknesses of the nitride and blocking oxide, respectively, while  $\epsilon_N$  and  $\epsilon_{OX}$  are the dielectric constants of the nitride and blocking oxide, respectively. Equation (2) assumes a uniform distribution of nitride traps and the activation energy responsible for the decay rate is [13]

$$E_{TA} = k_B T \ln(AT^2 t) \quad (3)$$

where A is a constant given as

$$A = 2\sigma_n \sqrt{\frac{3k_B}{m^*}} \left[ \frac{2\pi m^* k_B}{h^2} \right]^{3/2} \quad (4)$$

where  $\sigma_n$  is the trap capture cross-section,  $m^*$  the effective electron mass in the nitride and 'h' is Planck's constant. These relationships were used to interpret measurements of retention at elevated temperatures for retention times out to  $10^5$  seconds for the written state of a scaled SONOS device (See Fig. 3). Since the thermal activation energy of electron traps is near the conduction band edge, the electrons are thermally excited from these traps and back-tunnel through the tunneling oxide. Eqn. (3) shows the trap energy may be probed at a given temperature by measuring the slope of the decay characteristics as a

function of retention time. The capture cross-section,  $\sigma_n$ , may have temperature dependence.

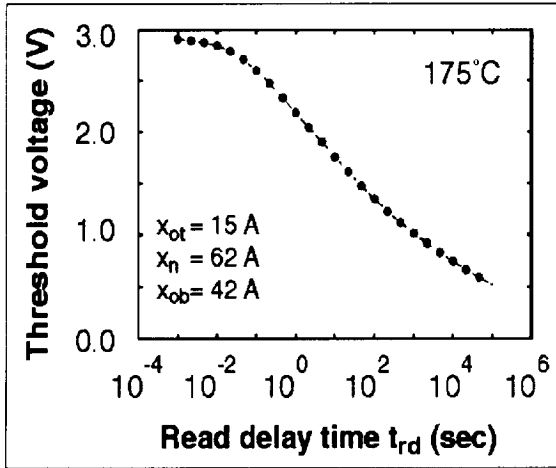


Figure 5 Threshold Voltage decay versus retention time for a Scaled SONOS NVSM device at  $T = 175^\circ\text{C}$ . The device is fabricated with a 'silicon-rich' nitride [13].

Using Eqns. 1-4, the decay rate of the threshold voltage [Fig. 5] was used to extrapolate the trap profile in the nitride of the silicon-rich nitride, as shown in Fig. 6.

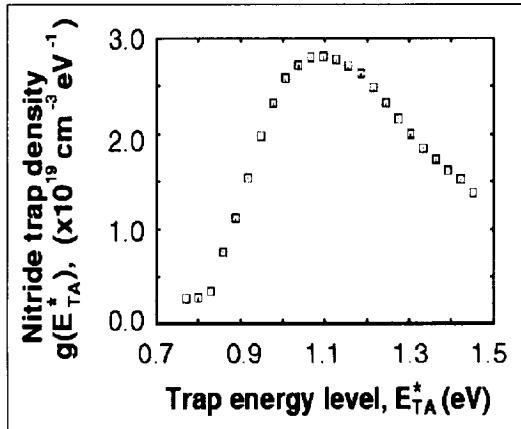


Figure 6 Nitride Trap Density versus Energy for a Scaled SONOS NVSM device with a silicon-rich nitride [13].

### 3. MEASUREMENT TECHNIQUE

Retention measurements at elevated temperatures are performed at the wafer level. As in the experiments of Yang and White, we use a hot chuck, ring probe stand, oscilloscope and an analog circuit [3,14] controlled by a desktop PC. The PC controls the oscilloscope through a GPIB interface with programs written in a LabVIEW™ environment. Fig. 6 illustrates a block diagram of the experimental set-up for dynamic measurements. These measurements include Erase/Write, data retention and endurance measurements as a function of temperature. If we include radiation performance, then these tests are the ultimate tests for NVSM devices from a user's standpoint.

The FPGA-based measurement system in Fig. 7 can execute all of these measurements. The function generator is designed and simulated with XILINX Foundation Software. The bit-streams are generated and downloaded to the FPGAs through a parallel download cable. The analog detection circuit, under the control of the specific erase/write/read pulses sets the operational modes to the SONOS device under test (DUT) and determines the change of the memory-state of the SONOS nonvolatile memory transistor. The TEK460 oscilloscope digitizes the analog threshold voltage output and sends the latter to the computer (PC). The data is filtered and averaged with a LabVIEW™ program on the computer and displayed on the monitor in real time.

The SONOS retention characteristics are monitored by applying programming pulses to the device, waiting a certain time  $t_r$ , and then forcing a constant current through the device and measuring the source voltage of the device as shown in the analog Detection Circuit of Fig. 8.

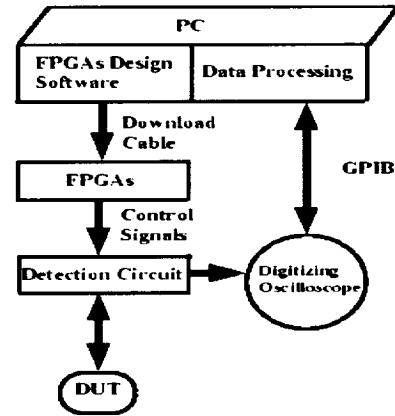


Figure 7 A Block Diagram of the Experimental Setup for Dynamic Erase/Write/Read Measurements [3].

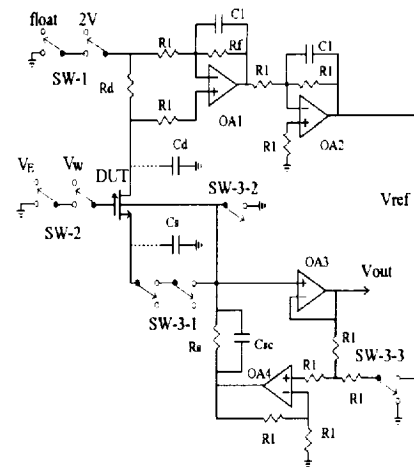


Figure 8 A constant-current, threshold-voltage detection circuit implemented with switches (SW) controlled by FPGAs[3,14]. The threshold voltage is monitored at  $V_{out}$ .

The measurements are performed on a hot chuck, which controls the temperature of the measurement environment and the wafer, as shown in Figs. 9 and 10.

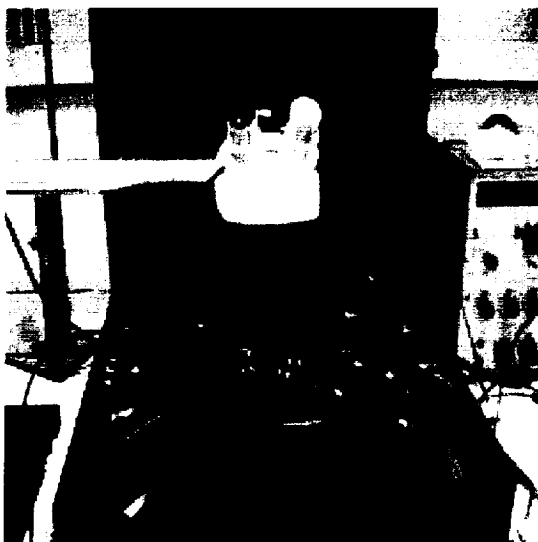


Figure 9 SONOS Wafer & Hot Chuck

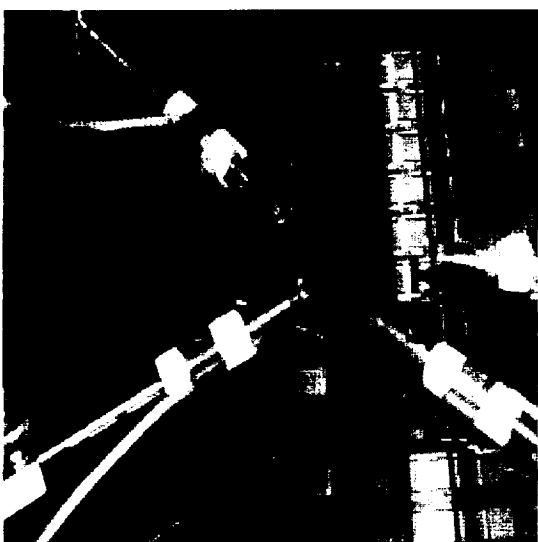


Figure 10 Close-up View of Hot-Chuck Probes on Wafer

The hot chuck is held at temperatures of 22 C, 80 C, 150C, and 250 C. The hot chuck used to collect this data has been operated routinely at temperatures up to 400 C. Due to this wear on the hot chuck, the surface where the wafer is placed is no longer planar. This created some difficulty in making good contacts with the probes onto the terminals of the device. When the device is heated and cooled, there is a degree of vibration associated with the operation of the hot chuck. When the temperature is increased to 125 C, the probes, which make contact on the device expand, and often slide off of the contact windows, scratching the device, and losing contact with the appropriate device terminals – especially for long-term retention measurements to  $10^4$  seconds. We compensate for these effects with special expansion probes and using

smaller sections of the wafers. The smaller pieces are not affected by the hot chuck surface or by vibrations in the laboratory.

#### 4. EXPERIMENTAL RESULTS

In this section, we describe retention measurements at Lehigh University on SONOS devices from the Northrop Grumman Corporation 0.8 um CMOS/SONOS 1M EEPROM project. The ‘oxynitride’ storage dielectric contrasts with devices fabricated with a ‘silicon-rich’ nitride. The thermally activated SONOS retention model is applied using Eqns. 1-4 to the retention data of ‘oxynitride’ SONOS devices taken at elevated temperatures to extract the energy distribution of the electron traps in the nitride. The retention measurements are performed, as described above, at temperatures of 22, 80, 150, and 250 C. A hot-chuck probe stand regulates the temperature. The SONOS devices are programmed with a 7V pulse applied to the gate for 2.5msec and erased with a -7V pulse applied to the gate for 7.5msec. The threshold voltage of the device is read for times ranging from  $10^{-7}$  to  $10^3$  seconds.

The threshold voltage of the device in the Write and Erase states at elevated temperatures is shown in Fig. 11. The results demonstrate the decay rate of the written state is affected by increasing the temperature.

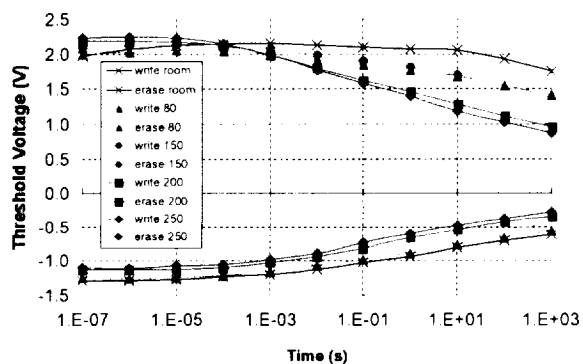


Figure 11 –  $V_{TH}$  vs time at various temperatures for an Oxynitride SONOS NVSM Device. The Write (excess electron) state of the device is affected by temperature. In contrast, the Erase (excess hole) state displays very little temperature sensitivity.

The Write state threshold voltage decay rate increases as the temperature increases. The Erase state decay rate is virtually unchanged. These trends are the same for both the ‘oxynitride’ [Fig. 11] and ‘silicon-rich’ nitride films [Fig. 3]. In both films we observe, for Write and Erase states, a small initial shift of the threshold voltage with increasing temperature.

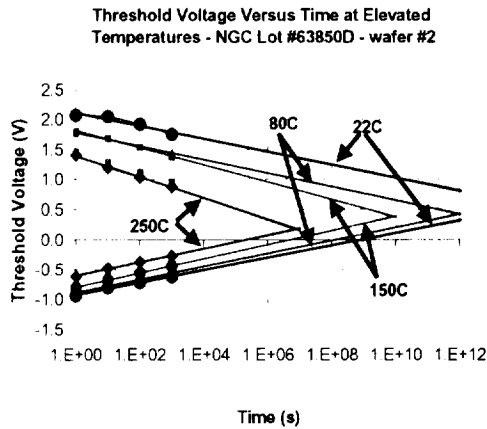


Figure 12 - Extrapolated  $V_{TH}$  vs Temperature

Long-term retention with temperature and radiation is of concern for space and military applications. The retention data has been extrapolated as shown in Fig. 12. At  $3 \times 10^8$  sec (10 years) and room temperature (22C) we have a 1.2V window. At 80C the window has decreased to 0.8V at 10 years and at 150C the window decreases to 0.3V. The data indicates these SONOS devices should be acceptable for 7 V programming and 10 year memory retention applications for operating temperatures below +125 C. Further optimization is continuing for the 1Mb SONOS EEPROM project.

The trap density in the nitride layer of the SONOS device is determined as a function of trap energy using Eqns. 1-4. Eqn. 3 is used to calculate the energies of the traps in the nitride layer. At 250 C the trap energy ranges from 0.6 eV to 1.43 eV. Eqn. 2 is used to calculate the density at points along the threshold voltage curve. The change in threshold voltage divided by the logarithm of the change in time is calculated at each decade of time. The electron trap density,  $g(E_{TA})$ , is plotted versus trap energy,  $E_{TA}$ , as shown in Fig. 13.

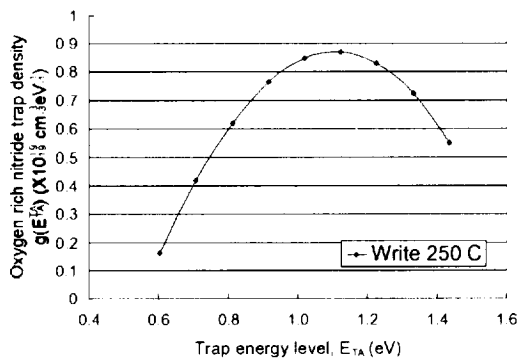


Figure 13 - SONOS Oxynitride Trap Density,  $g(E_{TA})$ , vs trap energy,  $E_{TA}$ , for the Write (excess electron) state.

The electron trap density for the 'oxynitride' film peaks at 1.1 eV below the edge of the nitride conduction band - similar to the 'silicon-rich' nitrides film shown in Fig. 6. The trap density of the 'oxynitride' film is less than the 'silicon-rich' nitride film. This is expected as the presence of oxygen will 'tie-up' silicon dangling bonds, which cause the memory traps in the nitride.

## 5. CONCLUSIONS

The temperature effect on the threshold voltage of scaled (7V programming) SONOS 'oxynitride' NVSM devices has been investigated. At elevated temperatures, the Write state threshold voltage decay rate,  $\partial V_{TH}/\partial \log(t)$ , of 'oxynitride' and 'silicon-rich' nitride SONOS devices increases with increasing temperature, while the Erase state threshold voltage decay rate remains unchanged. We see from Fig. 12 the extrapolated memory retention window at  $3 \times 10^8$  sec (10 years) and 22C is 1.2V, a 0.8V window at 80C, and a 0.3V window at 150C. We will take longer-term retention data in the future to see if there is a change in the decay rates, since the electric fields will be modified in the device with the loss of memory charge.

The nitride trap density is extrapolated from the decay rate of the Write state at 250 C. This allows us to see the trap distribution within the 'oxynitride' band gap. In previous studies of elevated temperature effects, Yang and White [13] have extrapolated the electron trap density for a SONOS device with a 'silicon-rich' nitride layer at 175 C as shown in Fig. 6. The trap density for a silicon-rich nitride layer is roughly three times greater than the density for an 'oxynitride' layer as shown in a comparison chart of Fig. 14. The 'oxynitride' and 'silicon-rich' nitride trap densities peak at the same activation energy, 1.1 eV.

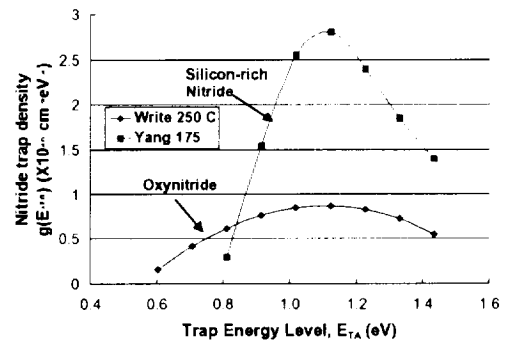


Figure 14 - A Comparison of Trap Densities in 'silicon-rich' and 'oxynitride' SONOS NVSM devices.

These preliminary measurements on scaled SONOS NVSM devices support the validity of high temperature screening measurements in the determination of long-term retention.

## 6. ACKNOWLEDGEMENTS

The authors would like to thank the Department of Energy, the Army Space and Defense and Missile Command in Huntsville, Ala., the National Science Foundation, and Northrop Grumman Corporation for their continual support of SONOS NVSM technology.

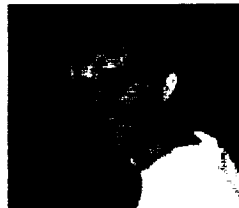
## 7. REFERENCES

- [1] H.A.R. Wegener, A. J. Lincoln, H. C. Pao, M.R. O'Connel, and R. E.Oleksio, "Metal Insulator Semiconductor Transistors as a Nonvolatile Storage", 1967 IEEE International Electron Devices Meeting (IEDM), Abstract 59, Washington, D.C.
- [2] D. Adams, J. Murray, and M.H. White, "SONOS Nonvolatile Semiconductor Memories for Space and Military Applications", NVMTS, San Diego, CA, 2001.
- [3] J. Bu and M. H. White, "Design Considerations in Scaled SONOS Nonvolatile Memory Devices", Solid-State Electronics, 45, 113 (2001).
- [4] M. H. White and J. R. Cricchi, "Characterization of Thin-Oxide MNOS Memory Transistors", IEEE Trans. Electron Devices, ED19, 1280 (1972).
- [5] L. Lundkvist, I. Lundstrom, C. Svensson, "Discharge of MNOS Structures", Solid State Elect, 16, 811(1973).
- [6] A. Roy and M. H. White, "Determination of the Trapped Chare Distribution in Scaled Silicon Nitride MONOS Nonvolatile Memory Devices by Tunneling Spectroscopy, Solid-State Electronics, 34, 1083 (1991).
- [7] Y. Kamagaki, S. Minami, H. Kato, "A New Portrayal of Electron and Hole Traps in Amorphous Silicon Nitride, J. Appl. Phys., 68, 2211, (1990).
- [8] Y. Kamigaki, S. Minami, T. Hagiwara, K. Furusawa, T. Furuno, K. Uchida, M. Terasawa, and K. Yamazaki, "Yield and reliability of MNOS EEPROM products," IEEE J. Solid-State Circuits, 24, 1714 (1989).
- [9] Y. Hu and M. H. White, "Charge Retention in Scaled SONOS Nonvolatile Semiconductor Memory Devices - Modeling and Characterization", Solid-State Elect., 36, 1401 (1993).
- [10] S. L. Miller, "Effect of Temperature on Data Retention of SNOS transistors", 8<sup>th</sup> IEEE NVSM Workshop, Vail, Co. August 1986.
- [11] P.J. McWhorter, S. L. Miller, T. A. Dellin, "Modeling the Memory Retention Characteristics of Silicon-Nitride - Oxide Silicon Nonvolatile Transistors in a Varying Thermal Environment, J. Appl. Phys, 68, 1902 (1990).
- [12] L. Lundkvist, C. Svennsson, B. Hansson, "Discharge of MNOS structures at Elevated Temperatures", Solid-State Elect., 19, 221 (1976).
- [13] Y. Yang and M.H. White, "Charge Retention of Scaled SONOS Nonvolatile Memory Devices at Elevated Temperatures", Solid State Elect., 44, 949 (2000).
- [14] A. Roy, F. R. Libsch and M. H. White, "A Microcomputer-controlled Multichannel Programmable Pattern Generator", IEEE Trans., on Instr. and Meas., IM-36, March 1987.

## 8. BIOGRAPHIES



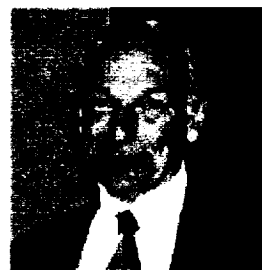
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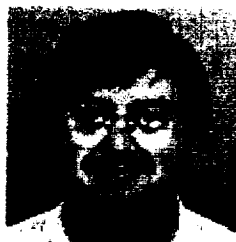
BSEE degree from Northwestern University in Evanston, Illinois. He completed his MSEE at the University of Maryland in College Park, Maryland in 1979.

During his 25year career at Northrop Grumman, Mr. Adams has been involved with all aspects of development of digital, analog and memory silicon integrated circuits for avionics and space applications. His work has included bipolar, CMOS and CCD technologies on both bulk silicon and silicon on insulator (SOI) starting materials. He has successfully served as technical director for numerous products including 16K/64K SRAMs, 64K/256K EEPROMs, 10K/20K/60K CMOS Gate Arrays, 30K Custom ASICs, 45K SOS 1750A CPU, 4K FPGAs and various BiCMOS smart-power devices. He has specialized in radiation-hardened technology and has personally been responsible for several process

integration innovations that have led to the current company portfolio of 100 Krad to 1 Mrad technologies.

Mr. Adams chairs a Yield Enhancement Task Force that is responsible for resolving manufacturing issues and improving product yields for all NGC silicon products. He is also involved in new process technology development. Current activities include 5V/ 15V/40V/ 100V BiCMOS, 0.5  $\mu\text{m}$  BiCMOS (with SiGeC HBT's), submicron (0.12  $\mu\text{m}$  / 0.5  $\mu\text{m}$ ) CMOS/SOI and radiation hard 0.8  $\mu\text{m}$  CMOS/SONOS.

Mr. Adams has authored over 35 technical papers and made 20 conference presentations in the area of digital and memory integrated circuit technology for avionics and space applications. He has received 7 patent disclosure awards.



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**Overview of Non-Volatile Testing and Screening Methods**

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## **Abstract**

Testing methods for memories, and non-volatile memories are have become increasingly sophisticated as they become denser and more complex. High frequency and faster re-write times as well as smaller feature sizes have led to many testing challenges. This paper outlines several testing issues posed by novel memories and approaches to testing for radiation and reliability effects. We discuss methods for measurements of Total Ionizing Dose (TID).



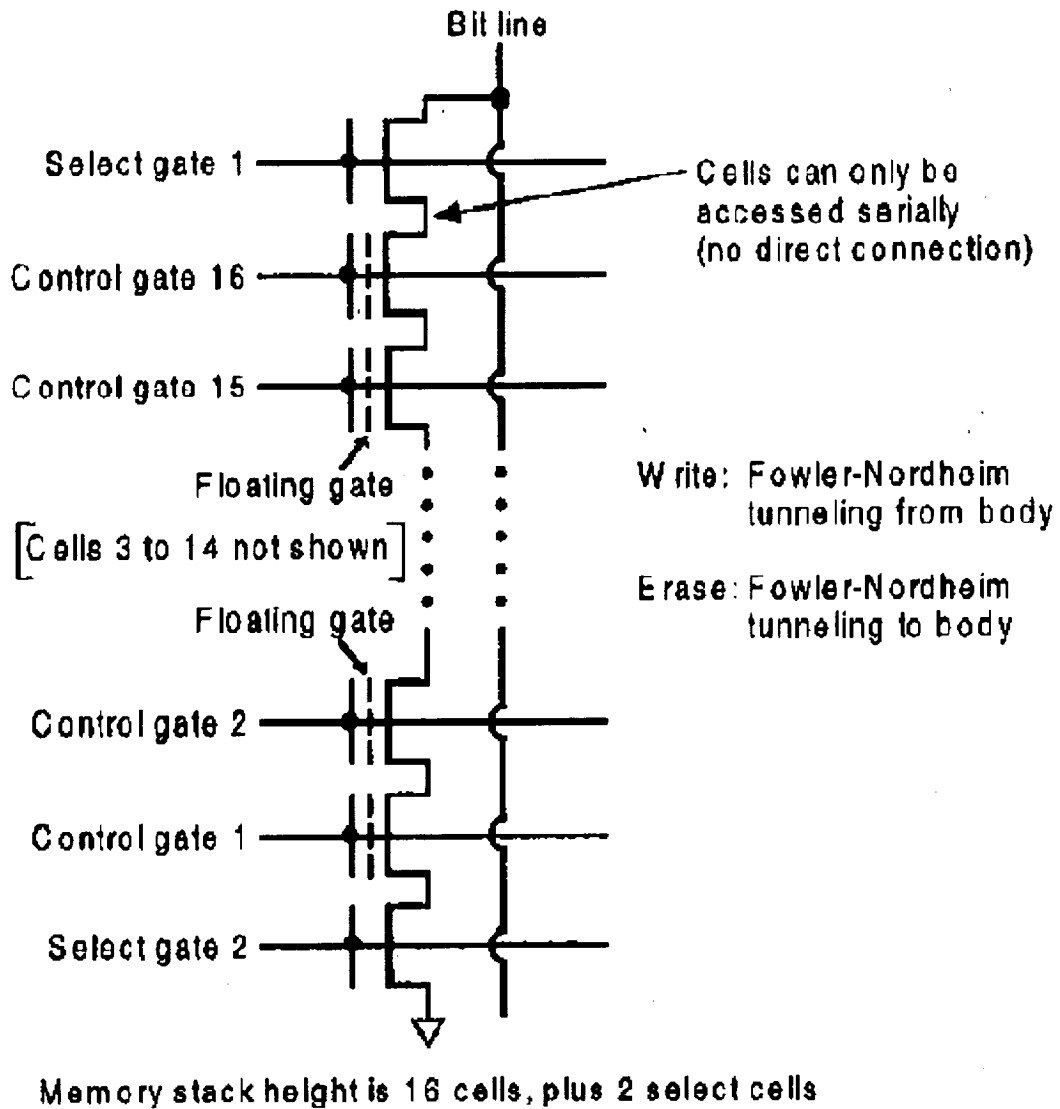
## I. INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) memories can be divided into two main categories: random access memories (RAM's), which are volatile, i.e., they lose stored information once the power supply is switched off, and read-only memories (ROM's), which are non-volatile, i.e., they keep stored information when the power supply is switched off. Flash memories combine those two features. There are different ways to design flash memory cells, and they have different characteristics, depending on the cell design. In flash memories a single cell can be electrically programmed and a large number of cells called block are electrically erasable at the same time. Flash memories provide a high-density storage technology for applications that do not require frequent write/erase operations. The basic structure of a flash-memory cell uses a dual sandwiched gate structure, interposing a floating gate between the body of the device and the control gate. Its structure is similar to EEPROM, but uses a much thinner oxide between the floating gate and channel region. The thin oxide allows charges to be transferred to and from the floating gate by either Fowler-Nordheim (F-N) tunneling from the source or body, or hot-electron injection from the channel region for erasing and writing. Most manufacturers use F-N tunneling for erasure, but different write mechanisms [1].

Two basic approaches have been used to develop high-density flash memories. The NAND structure is shown in Figure 1. The NAND cell is more compact because it does not provide contacts to individual source and drain regions. However, the read and write time is inherently slower in this technology because cells cannot be accessed individually; the read path goes through other cells in the stack. In order to deal with this, the device architecture divides the memory into pages. A page buffer is used to improve read time.

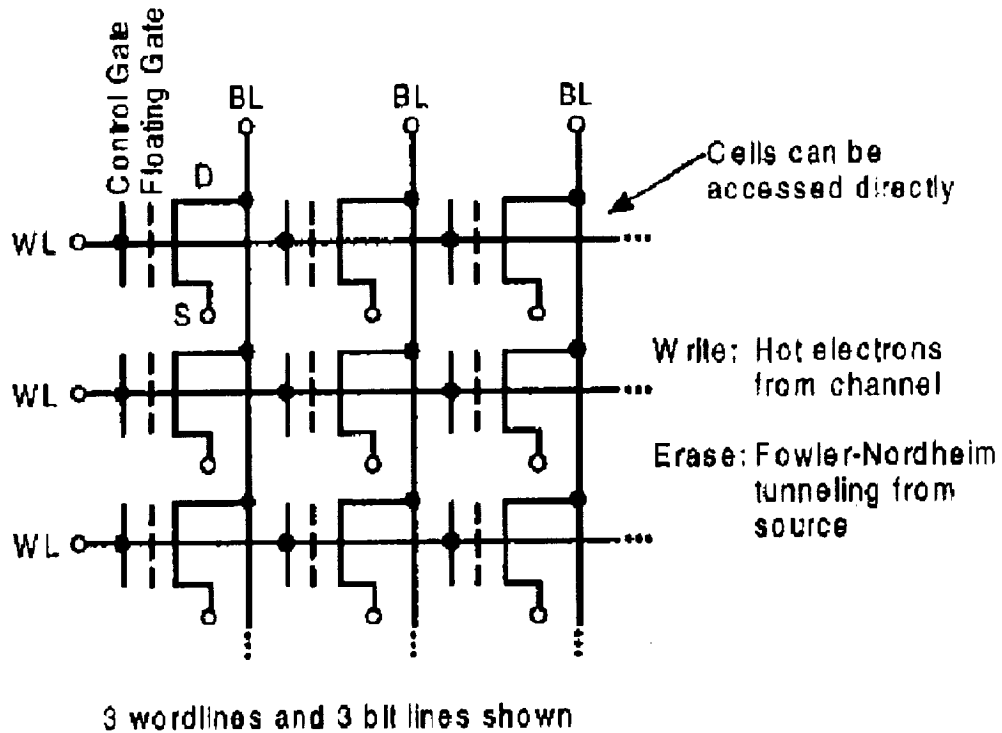
The NAND structure uses Fowler-Nordheim tunneling for erasing and writing. The oxide between the floating gate and body is about 250 Å. This requires higher voltages – typically 20 Volts for erasing and writing.

The NOR structure is shown in Figure 2. In this technology, random access of individual cells is allowed. This approach minimizes access time compared to the NAND structure. The erase function is done at the block level by applying a high voltage ( $V_{pp}$ ) to the source, grounding the control gate and allowing the drain to float. Charge in the floating gate is transferred to the source by Fowler-Nordheim tunneling. Programming is done by grounding the source, and applying ( $V_{pp}$ ) to the control gate [2,3]. The oxide between the floating gate and channel is around 100 Å, to enhance the tunneling effect. Cells in the NOR structure require about 12 Volts for erasing and writing which is lower than the 20 Volts of the NAND structure. Some flash memories produced by Intel can operate at



**Fig. 1. Cell architecture of a NAND flash memory organized in 16-bit stacks**

either 3.3 or 5 Volts. A boosted word-line voltage is required with the lower power supply voltage; internal circuitry detects the voltage and automatically applies the boost voltage [4].



**Fig. 2 Cell architecture of a NOR flash memory**

The overall architecture of either type of flash memory is very complex. Reading can be done relatively rapidly for either cell architecture using conventional circuitry for access and readout. However, erasing and writing are very slow operations (on the order of milliseconds) compared to conventional memories. To overcome this limitation, flash memories are subdivided into blocks, allowing erasing and writing to be done at the block level. Internal registers and buffers provide temporary storage for pages of data, allowing more transparent interface. A write state machine and a command state machine are used to control the complex sequences of operations that are needed. A charge-pump circuit is also required in order to provide the high internal voltages that are needed for erase and write operations. Because of this complexity, flash memories cannot be treated as simple memories. It is quite challenging to determine how they respond in radiation environments.

## II. TOTAL DOSE TESTING

Flash memories can be used in five basic ways [2]: (1) unpowered mode, which only applies power during the relatively short duration that the memory contents are used; (2) a continually powered standby mode, in which the device is ready to begin reading, but the address lines are static; (3) a read-only mode, which applies continuous power to the device, along with address, clock and control sequences for reading, but never applies power to the write circuitry; (4) a read-mostly mode, or powered static mode, which is similar to the previous mode, but applies voltage to the charge pump and may also include brief periods for active writing; and (5) a mixed read and write mode, which involves many write cycles so that write duty cycle is a significant fraction of the total use period. These modes are briefly summarized in Table 1 below.

Description	Bias Condition	Sensitive to charge Pump	Sensitive to Wear Out
Read Only	OFF	NO	NO
Read Only	ON	NO	NO
Read Mostly	OFF	SLIGHT	SLIGHT
Read Mostly	ON	YES	SLIGHT
Intensive Read/Write	ON	YES	HIGH

**Table 1. Possible Operating Modes for Flash Memories**

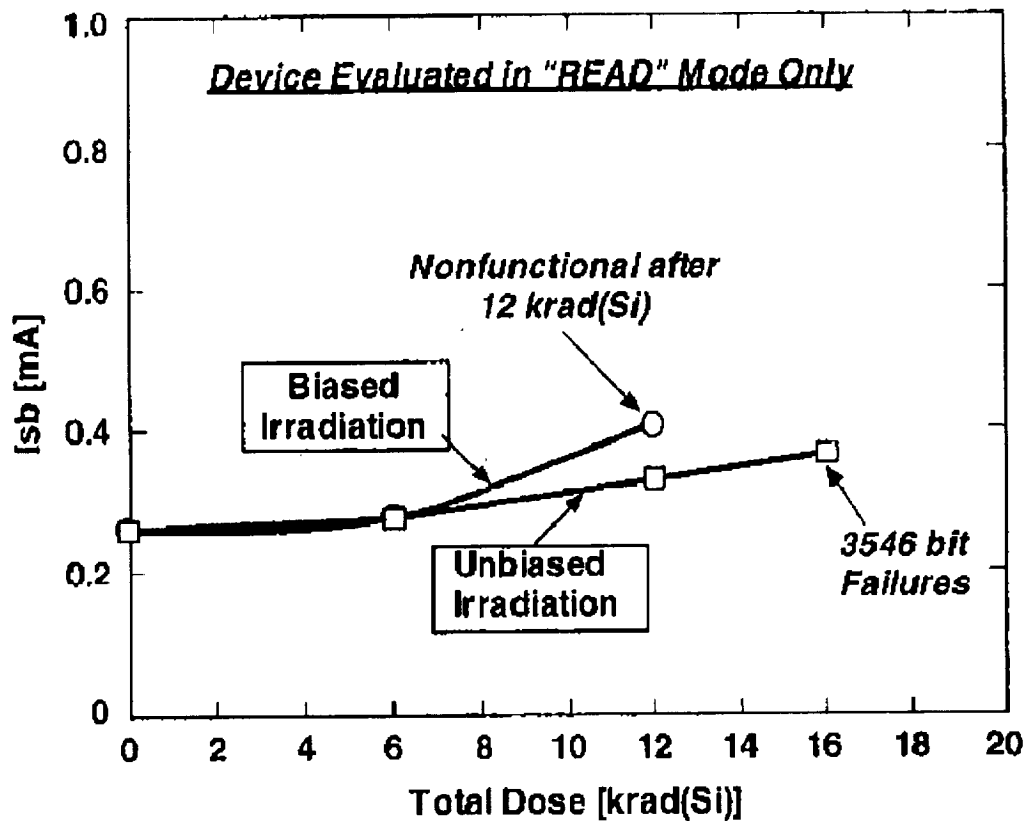
In evaluating flash memories for use in space, it is important to recognize how they will be used. Read mostly applications such as code storage are natural fits because of the very slow write and erase time. In these applications they might not be powered except for brief periods when it is necessary to read their contents. Mode 5 is may be used in some applications (such as data storage during planetary flybys), but usually involve relatively short time durations. We consider two bias conditions that are likely to be encountered during the majority of the time that flash memories are used in space: (1) unbiased (Mode 1); and (2) static biased, where the device is powered, but no address cycling or data access operations are used (Mode 2).

Total dose studies of earlier devices implicated the charge pump circuitry as responsible for device failures in both technologies [5]. This was clearly demonstrated for the 16 Mb Intel NOR device where the erase/programming voltage could be externally supplied; much higher dose levels were achieved when the internal charge pump was not used. Less direct methods were used to show that the charge pump is also the weakest link for the 16Mb Samsung NAND device, based on higher required voltages for erasing and programming after irradiation.

D. Nguyen et al. [3] performed total dose measurements using JPL cobalt-60 test facility at either of two dose rates: 25 rad(Si)/s and 0.012 rad(Si)/s using a series of stepped irradiations. They used a non-repeating pattern generated by a linear congruential pseudo-random generator with a slight modification: discarding every 31<sup>st</sup> number. The algorithm produces a reproducible random sequence of states, starting with a "seed" number. Two seeds were used, 31 and 59, which are both prime numbers. When the second seed is used, the pattern developed by the algorithm produces the opposite state in 1/2 the bits used with the first seed. This tests the ability to program the opposite state in 1/2 of the bit locations after each irradiation. These complex patterns are the basis of a more comprehensive functionality check which is capable of detecting address or detecting errors, unlike simple patterns. Before the first irradiation, the devices were written with a random pattern (seed-31). The pattern was verified by reading the contents of flash devices before and after each irradiation level for all parts that were evaluated in the "read" mode. For full functional mode, the devices were erased and a new random pattern (seed-59) was written to the memory after the first level. After the second level the original pattern (seed 31) was used, interchanging each pattern after each irradiation step in order to verify that a different pattern could be written into each storage location.

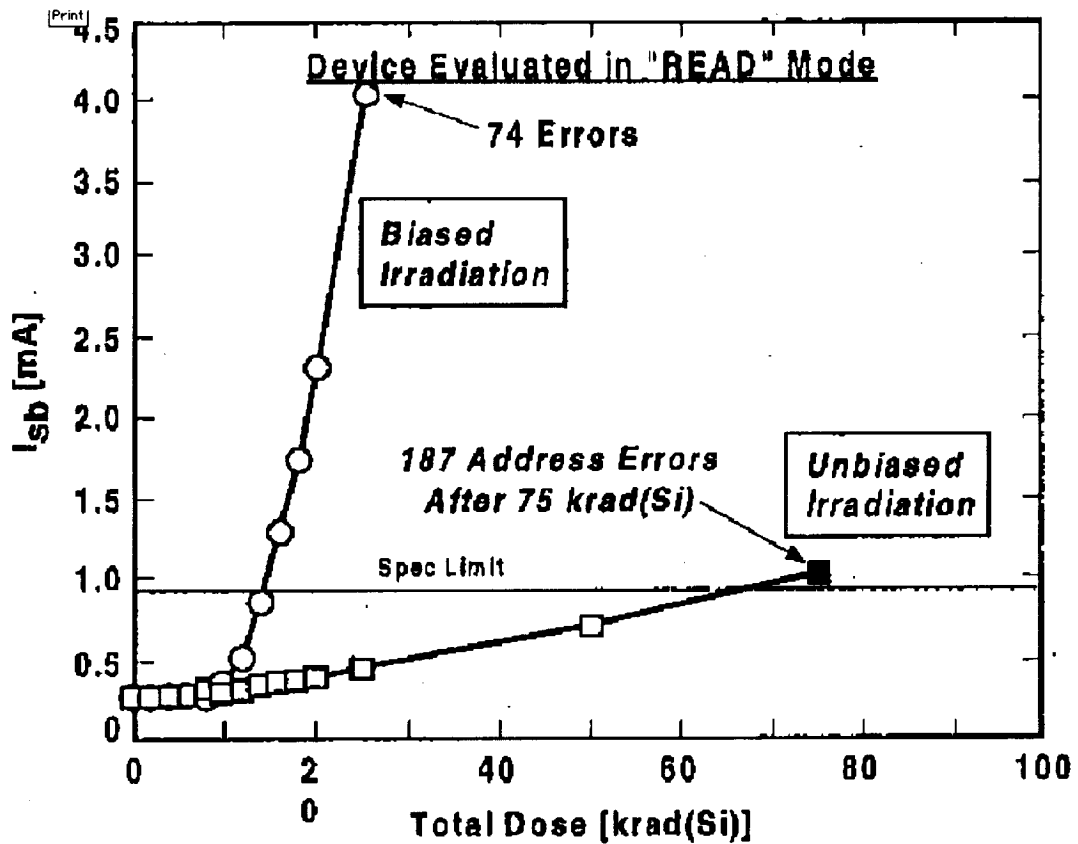
In their studies, some post-irradiation measurements were limited to the "read" mode, making no attempt to verify operation of either erase or write function of the memory. This condition was selected because many applications require very infrequent writing. Other devices were tested more completely after each irradiation level, subjecting each device to a complete erase-write-read cycle (Mode 5). This tests the full functional capability of the memory, and requires that the charge pump and verification circuitry function correctly.

Figure 3 shows test results of their studies for the 32-Mb Intel multi-level flash memory for statically biased and unbiased conditions. With bias applied, the device would no longer function after the second irradiation level [12 krad(Si)]. When tested without bias, the device continued to operate close to 16 krad(Si). Thus, the first versions of the multi-level flash technology failed at lower level than the earlier generation devices (16 Mb at about 25 krad(Si) in erase-write-read mode).



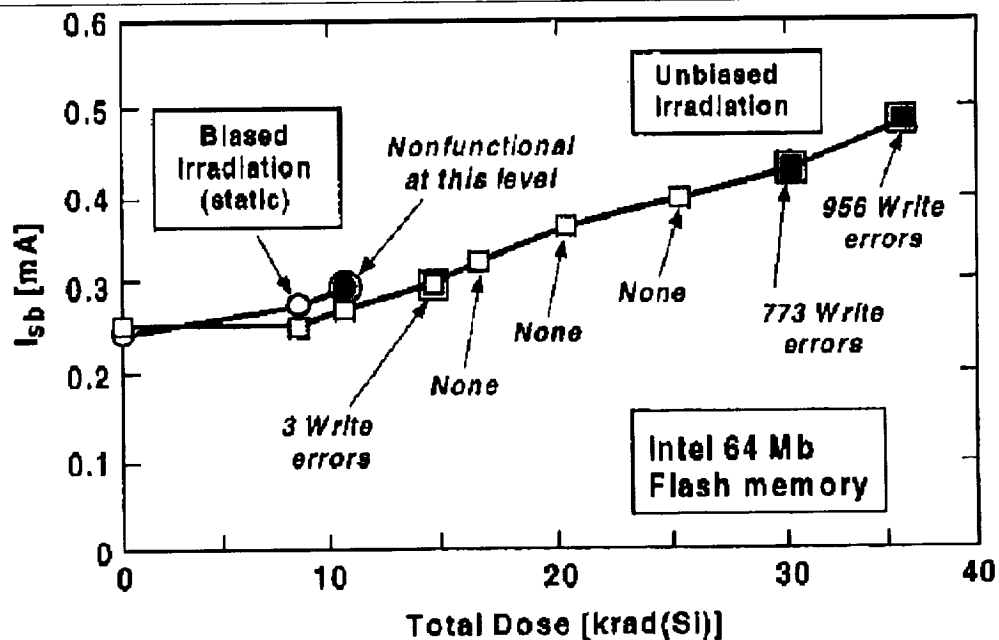
**Figure 3. Total dose results for the Intel 32Mb flash memory evaluated in read mode**

The 64-Mb multi-level flash memory behaves somewhat differently. The standby current increased much more rapidly with increasing radiation levels when bias was applied compared to results for the 32 Mb devices in Figure 4. The 64 Mb devices typically operated to levels well above 20 krad(Si). These results are shown in Figure 5. When tested without bias, the 64Mb devices passed read functionality up to 50 krad(Si) and showed only slight increases in standby current. However, at 75 krad(Si) a large number of addressing errors occurred. These were severe enough to make the device unusable at that level.



**Figure 4. Total dose results for the Intel 64Mb flash devices evaluated in read mode**

Results for the 64Mb Intel device in the fully operational mode (Mode 5) are shown in Figure 5. When irradiations were carried out under bias, the device became fully nonfunctional at 11 krad(Si), in contrast to the tests in "read" Mode3 where the device continued to operate with only a few errors to levels almost twice as great. Without bias, the device also failed at much lower levels when fully operational tests were done between irradiations.



**Figure 5. Total dose test results for the Intel 64Mb flash memory evaluated in full functional mode**

Test results for 128 Mb Samsung devices in the “read” mode are shown in Figure 6. Without biased irradiation, the standby current increased by several order of magnitude at about 20 krad(Si). When tested without bias the device functioned to levels above 100 krad(Si) with only a small number of “read” errors.



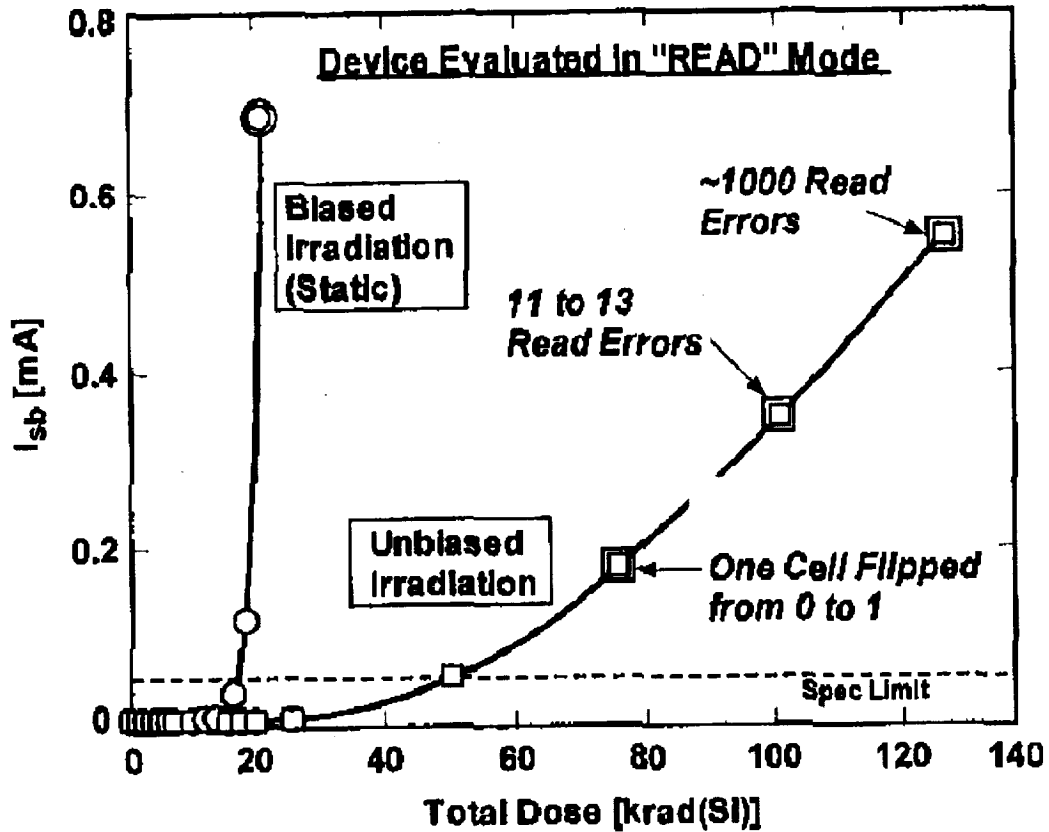


Figure 6. Total dose results for the 128Mb Samsung flash device, tested in read mode

In studies with full functionality tests erase-mode (Mode 5) failures were observed at around 8 krad(Si) under bias irradiation as shown in Figure 7. When fully functional tests were done on devices that were unbiased during irradiation, erase failures occurred at 45 krad(Si).

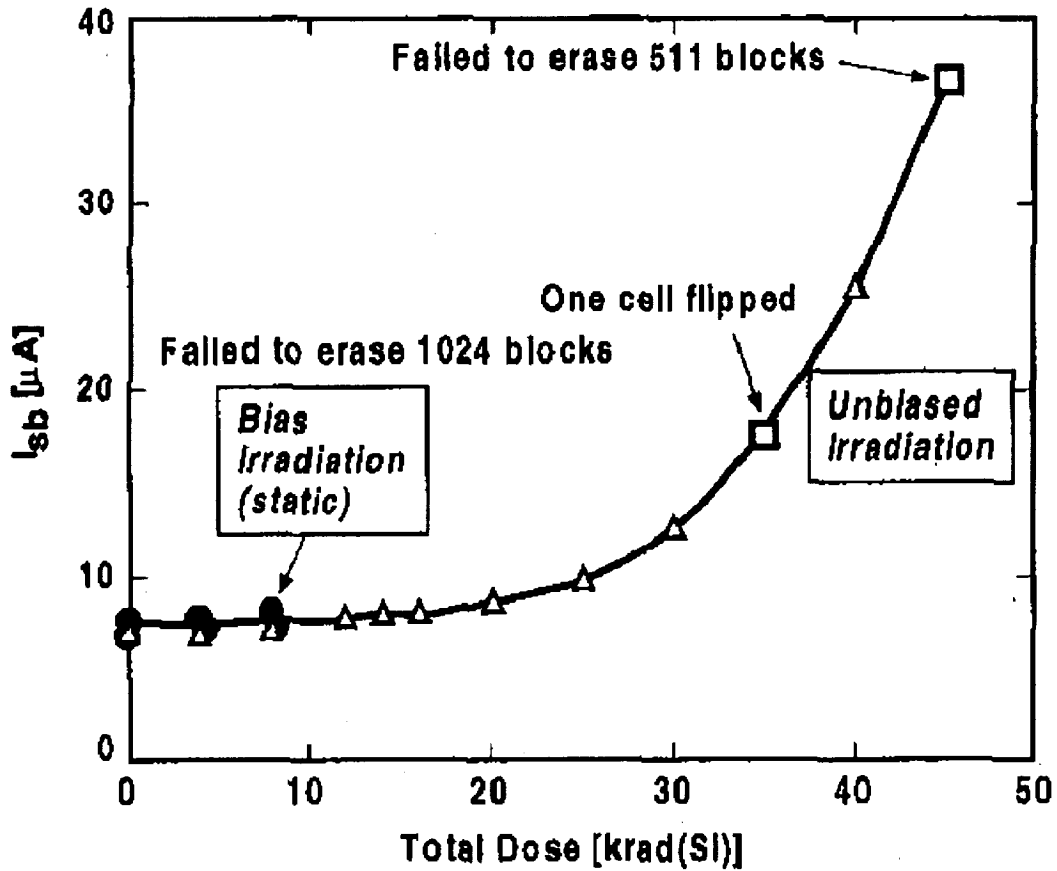


Figure 7. Total dose test results for the 128 Mb Samsung flash memory evaluated in Erase/Write/Read mode (Mode 5).

### III. CONCLUSION

Designing systems to effectively use flash memory while avoiding radiation problems, including destructive effects, is becoming more difficult as the devices are scaled to smaller feature sizes and larger overall arrays size. Charge pump degradation continues to be the most significant degradation mode, even for more advanced flash memories. Microdose effects, although they affecting only a small number of bits, may be on the verge of becoming a serious problem as transistor sizes scale and manufactures push toward the next step in multi-level flash memory designs.

## REFERENCES

- [1] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash Memory Cells- An Overview," Proceeding of the IEEE, vol. 85, p. 1248. (1997)
- [2] H. R. Schwartz, D. K. Nichols and A. H. Johnston, "Single-Event Upset in Flash Memories," IEEE Trans. Nucl. Sci., vol. 44, p. 2315 (1977)
- [3] D. N. Nguyen, S. M. Guertin, G. M. Swift and A. H. Johnston, "Radiation Effects on Advanced Flash Memories," IEEE Trans. Nucl. Sci., vol.46, p. 1744 (1999).
- [4] A. Baker, R. Alexis, S. Bell, V. Dalvi, R. Durante, E. Bauer, M. Fandrich, O. Jungroth, J. Kreifels, M. Lansgraf, K. Lee, H. Pon, M. Rashid, R. Rozman, J. Tsang, K. Underwood and C. Yarigadda, "A 3.3 V 16 Mb Flash Memory with Advanced Write Operation," Digest of Papers from the 1994 International Solid-state Circuits Conference, pp. 146-147
- [5] D. N. Nguyen, C. I. Lee and A. H. Johnston, "Total Ionizing Dose Effects on Flash Memories," 1998 IEEE Radiation Effects Data Workshop Record, P. 100

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# An FPGA-Based Test-bed for Reliability and Endurance Characterization of Non-Volatile Memory

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## Memory Technology Background:

Memory technologies are divided into two categories. The first category nonvolatile memories, are traditionally used in read-only or read-mostly applications because of limited write endurance and slow write speed. These memories are derivatives of ROM technology, which includes EPROM, EEPROM, Flash, and more recent Ferroelectric non-volatile memory technology. Nonvolatile memories are able to retain data in the absence of power. The second category, volatile memories, are RAM-devices including SRAM and DRAM. Writing to these memories is fast and write endurance is unlimited, so they are most often used to store data that change frequently, but they cannot store data in the absence of power. Non-volatile memory technologies with better future potential are FRAM, Chalcogenide, GMRAM, Tunneling MRAM and SONOS EEPROM.

FRAM is a uses a ferroelectric capacitor to store the data. This storage mechanism is quite different from that of other non-volatile memories, that use floating gate technology where the charge is stored. The ferroelectric effect is the ability of a material to store a state of electric polarization in the absence of an applied electric field. An FRAM memory cell is created by depositing a film of ferroelectric material in crystal form between two electrode plates to form a capacitor very similar to a DRAM capacitor. FRAM cell could be one transistor one capacitor (1T1C) or a more robust design using two transistors two capacitors (2T2C) for better fault tolerance (complementary storing). However, rather than storing data as a charge on the capacitor, a ferroelectric memory stores data within a crystalline structure known as Perovskite. The Perovskite crystals maintain two stable polarization states resulting from the alignment of internal dipoles, which are used to represent '1' and '0' states. Since no external electric field is required for the ferroelectric material to remain its polarization, a ferroelectric memory device can retain data in the absence of power.

EEPROM (electrically erasable programmable read-only memory) use memory cells with transistors that are very similar to normal MOS

transistors, but the transistors have a second, floating gate. Applying a programming voltage  $V_{PP}$  (usually greater than 12 V) to the drain of the n-channel EEPROM transistor programs the EEPROM cell. A high electric field causes electrons flowing toward the drain to move so fast they “jump” across the insulating gate oxide where they are trapped on the bottom, floating, gate. The energetic electrons are referred to as hot and the effect is known as hot-electron injection or avalanche injection. EEPROM technology is sometimes called “floating-gate avalanche MOS” ( FAMOS ). Electrons trapped on the floating gate raise the threshold voltage of the n-channel EEPROM. Once programmed, an n-channel EEPROM device remains off even with a logic high applied to the top gate. An unprogrammed n-channel device will turn on as normal with a logic high top-gate voltage. The programming voltage is applied either from a special programming box or by using on-chip charge pumps. In programming an EEPROM, an electric field is used to remove electrons from the floating gate of a programmed transistor. This is in contrast to EPROMs, which must be exposed to a UV-lamp to remove electrons from the floating gate. This usually requires the removal of the EPROM from the system.

### **Reliability Issues of FRAM**

The major non-fabrication-related issues of FRAM reliability include data retention, fatigue, aging, imprint, and radiation. Data retention, one of the most important characteristics of non-volatile memories, is defined as the ability of a memory to maintain stored data between the time it is written and the time it is subsequently read. Although data retention is influenced at a fundamental level by design and manufacturing factors, retention failures are accelerated by high temperatures, which cause thermal depolarization of the poled state in the ferroelectric material. The signal loss due to data retention failures recovers after a rewrite and immediate read.

Fatigue occurs in ferroelectric materials with an increased number of switching cycles (read or write cycles) and is characterized by a decrease in switchable polarization. This process is related to the electrode interfacial areas of the memory cells and electric-field assisted migration of oxygen vacancies within ferroelectric materials.

Aging is similar to retention failure in that it is characterized by signal loss over time, but, unlike retention failures, failures due to aging occur during the retention period and do not recover after a rewrite and immediate read. During the aging process, a gradual stabilization of the domain structure occurs, which causes the ferroelectric material to become less responsive to applied electric fields.

Imprint is a reliability issue specific to ferroelectric material. Accumulation of charge in the ferroelectric cell over time make a capacitor

that has spent a significant amount in one polarity reluctant to switch polarities.

The radiation tolerance of ferroelectric memory is limited by the CMOS circuit elements. Prior studies have shown no significant difference between the radiation tolerance of commercial memory devices with and without ferroelectric material.

### **Reliability Issues of EEPROM**

The reliability issues with EEPROM are very similar with the exception of imprint, which is specific to FRAM. In addition, the process by which fatigue occurs differs, and charge-trapping is an aspect specific to EEPROMs. During programming, the control gate of an EEPROM cell is made positive relative to the source-drain area. The floating gate is capacitatively coupled to the control gate, and when sufficient voltage is generated and the tunneling threshold is exceeded, electrons tunnel through the thin "tunnel" oxide window into the floating gate. The negative charge then remains trapped in the floating gate since inadequate voltage exists, normally to allow the electrons to tunnel back out. To erase the memory cell, the process is simply reversed. To read the cell, the control gate and source are brought to predetermined reference voltages and the current through the cells is measured. The transistor of a programmed cell is "on" and the transistor of an erased cell is "off".

Two basic types of failure occur when EEPROM cell are repeatedly written and erased: dielectric failure and charge trapping. Dielectric failures are the source of very low level random failures. They are caused by leakage through minor unscreenable flaws in the tunnel oxide. On contemporary production EEPROMs, dielectric failures are typically too rare to be noticed by standard lot sampling techniques until several hundred thousand write-erase cycles have passed. After this, they create a very low but visible level of random bit failures.

Charge trapping is the effect that creates intrinsic failure in EEPROMs. During write-erase cycling, small amounts of isolated negative and positive charge become trapped in imperfections in the tunnel oxide. Once trapped, the charge is no longer free to tunnel out of the oxide. In practice, electrons are more commonly trapped, and their presence creates a barrier to the tunneling of other electrons through the tunnel oxide. The apparent voltage needed to tunnel in either direction through the oxide increases. This reduces the amount of charge that can be moved in and out of the floating gate. When the accumulation of trapped charge becomes severe enough, it is no longer possible to move enough charge to clearly distinguish a one from a zero. At this point, the memory cells affected must be abandoned.

It is desirable to be able to program EEPROMs as quickly as possible. However, accelerating the programming of EEPROM cells requires the use of higher programming voltages, which accelerate the charge trapping mechanism and generally degrade the endurance of the EEPROM.

It might seem intuitive that tunnel oxide might degrade with endurance cycling and that data retention would suffer as a result. But the effect of cycling on the retention characteristics of EEPROM memory is very slight. That does occur is not due to increasing leakage through normal tunnel oxide, but the statistical influence of the random failures which are in fact caused by leakage through rarefied defects. The effect of cycling on the retention characteristics of before reaching the intrinsic limit of EEPROM memories is so slight, in fact, that it is usually ignored.

### **Tester Design**

A custom memory tester was designed to create a low-cost, user-customizable testing for non-volatile memory that could perform reliability and endurance tests. The objective was to evaluate the reliability and endurance characteristics of various non-volatile memories for potential use in space applications.

A XILINX XC4010E 10,000 gate, 5V FPGA was chosen for the 5V memories, and a XILINX XC4010XL, a 3.3V version of the XC4010E, was chosen for the 3.3V memories. The tester board contains a parallel port for communication with a PC, an LED for error readout, and an EEPROM socket for PC-independent operation.

The tester can be configured to perform reliability or endurance tests, and each test can log errors in one of two ways. The error data can either be logged on a PC through the parallel port, or the tester can be used by itself, independent of a PC, by using an EEPROM to load the bit stream file and "scrolling" the error information on a 7-segment LED display. The memory tester configuration for a parallel FRAM is shown below.

This test bench offers several advantages over commercial testers when used for reliability and endurance testing. Endurance testing to a chip's specifications could involve more than  $10^{10}$  read/write cycles, which can take up to 28 days for the Ramtron FM24C04 serial FRAM. Commercially available memory testers with high hourly rates may prove extremely expensive for testing NVMs with  $10^{12}$  to  $10^{15}$  read/write cycles. In comparison, the FPGA-based testers are inexpensive and more flexible. If several FPGA boards are used, many chips can be tested simultaneously at a fraction of the cost compared to the commercial testers. The highly portable, PC-independent nature of the test bench would also make it suitable for use in radiation testing, given proper shielding for the tester.

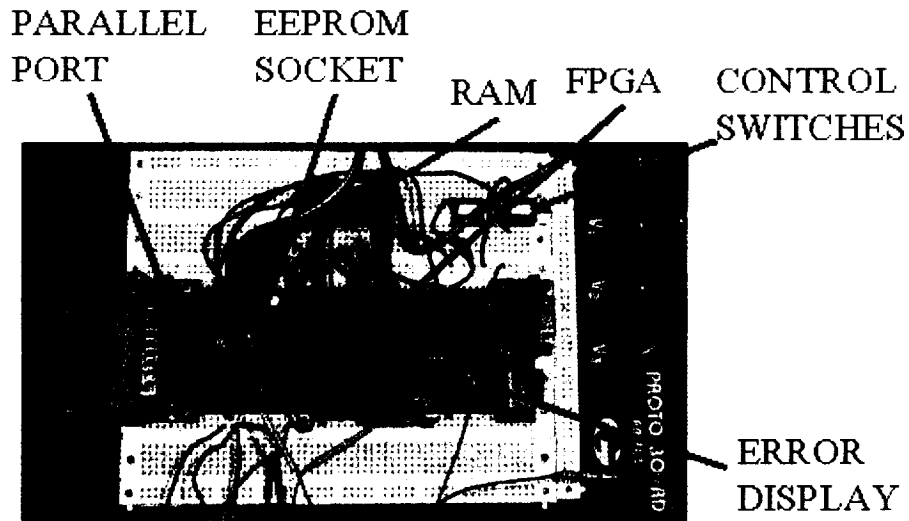


Figure 1: Non-volatile memory tester

### Test Methodology

A MATS+ test was chosen to test the reliability of the non-volatile memories. In order to understand the test procedure, a brief example and explanation of Van de Goor's memory test notation is provided below:

```
UP(W10101010; R; W01010101)
  UP = Perform the entire set of operations in parentheses
  from the first memory address to the last
  W10101010 = Write the data pattern '10101010'
  R = Read back the data
  W01010101 = Write the data pattern 01010101
  (Increment address and loop)
```

The MATS+ reliability test can detect address decoder faults and stuck-at faults, and was programmed to cycle through all the addresses in the memory. This reliability test was chosen because it met the minimum test criteria while fitting into the relatively small FPGA. Again using Van de Goor's notation, the MATS+ test is described as follows:

```
1. UP(W01010101)
2. UP(R; W10101010)
3. DOWN(R; W01010101)
4. LOOP BACK TO 1.
```

In order to test the endurance of the non-volatile memories, the following basic endurance test was used:

```
1. (W01010101; R; W10101010; R)
2. LOOP BACK TO (1)
```



Due to the prohibitive amount of time required to exhaust all addresses in the memories with an endurance test, it was decided that a single address or small range of addresses would be used instead.

Upon an error in during either test, the tester logs the total number of errors that have occurred, the number of read and write cycles at the point the error occurred, the memory address at which error occurred, the incorrect data value read, and (on the reliability test) it indicates the part of the memory test the failure occurred on. If the parallel port version of the tester is used, a simple program logs the data on the screen and gives the user the option of saving the data to a file. The other version of the tester, which is independent of the PC, scrolls the error information corresponding to the most recent error across the LED display, using various symbols to describe the data about to be displayed. An EEPROM is used in this tester so that a PC is not required to download the FPGA bit stream, which makes it completely independent of the PC.

### Test Procedure and Preliminary Results

Memory testing is ongoing, and the results to date are preliminary. Three non-volatile memories are under test: Ramtron FM24C04 serial FRAM, Ramtron FM1808 Parallel FRAM, and the Northrop-Grumman's 256 kb Rad-Hard EEPROM. Reliability tests have produced no errors in any of the memories. Endurance testing on the Ramtron FM24C04 serial FRAM has exceeded the endurance specification of the chip ( $1.0 \times 10^{10}$  read/write cycles) by over four times (it has undergone  $4.2 \times 10^{10}$  read/write cycles) with no errors. Endurance testing on the Ramtron FM1808 parallel FRAM has not yet exceeded the endurance specifications, but no errors have surfaced to date.

	Status	# R/W Cycles (Endurance)	Endurance Spec
<b>Ramtron Serial FRAM</b>	<b>Testbed complete: Both tests running</b>	<b>4.2E10</b>	<b>1E10</b>
<b>Ramtron Parallel FRAM</b>	<b>Testbed partially complete: endurance tests running</b>	<b>.6E10</b>	<b>1E10</b>
<b>NG EEPROM</b>	<b>Testbed work in progress</b>	<b>N/A</b>	<b>10,000</b>

**Table 1: Preliminary Results**

Full test results will be available by December, 2001.

### **Concluding remarks**

A custom memory tester was designed to create a low-cost, user-customizable testing for non-volatile memory that could perform reliability and endurance tests. The tester board contains a parallel port for communication with a PC, an LED for error readout, and an EEPROM socket for PC-independent operation. The main objective is to evaluate the reliability and endurance characteristics of various non-volatile memories for potential use in space applications. Testing is currently in progress for various memory chips. Results are expected from various tests in next two months.

### **Acknowledgments**

Research described in this paper, was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration's Electronics Parts and Packaging Program (NASA/NEPP). The authors acknowledge the help received from Dr. Charles Barnes and Mr. Choon Lee. The authors are grateful to Mr. Michael Fitzpatrick of the Northrop Grumman for the samples of EEPROM parts.

### **References**

- [1]. Ramtron Application Note: FRAM Technology Backgrounder
- [2]. T. Hadnagy, et al., "Retention After Fatigue of Ferroelectric Memories"  
[http://www.ramtron.com/products/techpaperlibrary/Reten&Fatigue\\_Domokos.pdf](http://www.ramtron.com/products/techpaperlibrary/Reten&Fatigue_Domokos.pdf)
- [3]. A. Sharma and Alexander Teverovsky, "Preliminary Evaluation of Data Retention: Characteristics for Ferroelectric Random Access Memories (FRAMs)", NASA Goddard Space Flight Center, pp 1-4.
- [4]. A. J. Van de Goor. "Testing Semiconductor Memories" John Wiley & Sons, Inc.

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## ***SESSION #3: Processing***

Wednesday, November 7, 2001

4:20 PM – 5:30 PM

Chair: *M. White*, Lehigh University

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- 4:20 PM      Copper/low-k interconnect integration into 0.15  $\mu\text{m}$  single poly EEPROM technology; *V. Shekhar, I. Rahim, C. Sardana, and G. Thalapaneni*, Altera Corporation, *C. Lin, M. Ho, Y. Wang, and D. Kuo*, Taiwan Semiconductors Manufacturing Company
- 4:40 PM      Process Optimization for MOCVD of  $\text{SrBi}_2\text{Ta}_2\text{O}_9$  for Non-Volatile Memory Applications; *D. Burgess*, Aixtron Incorporated
- 5:00 PM      Atomic Scale Structure of Giant Magnetoresistive Multilayers: Energetic Adatom and Surfactant Effects; *X. Zhou, W. Zou, R. Johnson, and H. Wadley*, University of Virginia

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# Copper/low-k interconnect integration into 0.15 $\mu\text{m}$ single poly EEPROM technology.

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## Abstract

Successful and reliable integration of Copper and low-k interconnect into single poly non-volatile EEPROM technology is demonstrated for the first time. EEPROM cell reliability and performance of Copper interconnect EEPROM cell is compared with Aluminium interconnect EEPROM cell. Additionally, viability of replacing silicon nitride with oxynitride as a diffusion barrier layer underneath metall to prevent contamination related to charge loss from getting into EEPROM cell is discussed.

## Introduction

Below 150 nm technology use of Cu as interconnect becomes a necessity [1]. Unlike Al, Cu is known to diffuse through oxide. Using a barrier layer such as TaN, Cu diffusion through oxide is prevented. On account of charge loss concerns in programmable logic circuits, the prevention of Cu diffusion is even more critical to EEPROM circuits than to the logic circuits. Successful integration of Cu interconnect technology with non-volatile EEPROM cell (Figure 1: 3 transistors, 1 capacitor and 1 tunneling diode single poly Si EEPROM cell) will allow programmable logic devices with EEPROM memory cell to shrink to and beyond 150 nm gate length.

To prevent interconnect related contamination from entering the EEPROM cell floating gate, furnace grown silicon nitride has been used as a diffusion barrier underneath metall. However, it has a higher dielectric constant associated with it ( $\epsilon = 7.8$ ) which results in higher interconnect capacitance. For shrinking technologies, interconnect capacitance should be as small as possible. By choosing a suitable

composition, plasma enhanced CVD (PECVD) grown oxynitride layer ( $\epsilon$  between 3.8 and 7.8) could be used as a diffusion barrier layer [2, 3] which due to the lower k would provide lower interconnect capacitance. The lower deposition temperature of oxynitride would reduce the thermal budget as well

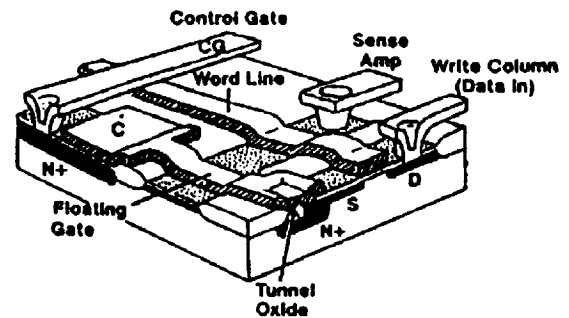


Figure 1. Single-poly Si EEPROM cell view.

## Manufacturing Process

**Front End Process:** The front-end process for both Cu and Al interconnect EEPROM devices includes a p-substrate, STI, twin-well process with single poly-silicon and cobalt silicide. High voltage required for program and erase of the EEPROM cell is supported by N+/p-sub junction in conjunction with a deep phosphorous implant to get a more gradual junction profile. High field threshold voltage ( $V_t$ ) is set by the field implant through the silicon trench isolation (STI).

**Back End Process:** EEPROM cell with Cu back-end comprised W CMP contact plugs along with Cu metall and low-k dielectric material IMD. Cu was deposited on dry-

etched oxide trenches (single damascene) using a combination of sputtering (TaN liner/Cu seed) and electro-chemical plating (ECP). The Cu film was subsequently planarized with CMP followed by nitride passivation. The Al test chip comprised W CMP contacts and via plugs with a TiN/AlCu/TiN liner stack and SiO<sub>2</sub> ILD. Splits for silicon nitride (furnace grown) and oxynitride blanket layer (PECVD-grown using SiH<sub>4</sub> + N<sub>2</sub>O constituent gases) underneath metall was used with Al back-end wafers to compare the effect of these layers as a diffusion barrier layer for unwanted species. A brief process flow is shown in Table 1.

TABLE 1 Process Flow

Logic (Core)	EEPROM Module
OD/STI	(additional steps to the Logic steps) N <sup>+</sup> imp under Tunnel Window
Twin-well Field Implant	
Gate Poly	Tunnel Oxide
LDD Imp for all devices Spacer Formation NMOS S/D PMOS S/D	Deep P Implant at HV S/D
Contact and Metallization	Diffusion Barrier Layer

**Experimental Results and Discussions:**

Characterization of EEPROM cells with Al and Cu interconnects as well as silicon nitride and oxynitride diffusion barrier layers were performed for reliability and performance. The erase and program cycling for the EEPROM cell is done through a Fowler-Nordheim (F-N) tunneling mechanism. Erase and program verification is done through the read path

Reliability and performance comparison of EEPROM cells with Al and Cu interconnects

Performance comparison of EEPROM cells with both types of interconnects was done by taking erase V<sub>t</sub> versus erase time and I<sub>cell</sub> versus program time measurements in figure 2 and figure 3 respectively. I<sub>cell</sub> is the current

through the sense amp when EEPROM cell is programmed (electrons are tunneled back into the substrate) and word line is high (figure 1). According to the graph in figure 2, after 1000 ms of erase time, the difference in V<sub>t</sub> between the Al and Cu interconnects EEPROM cells is less than 1%. According to the graph in figure 3, after 100 ms of program time, difference in I<sub>cell</sub> between the Al and Cu interconnect EEPROM cells is less than 1%. The graphs in figure 2 and 3 reflect, as expected, that performance of EEPROM cells with Al and Cu interconnects is almost the same.

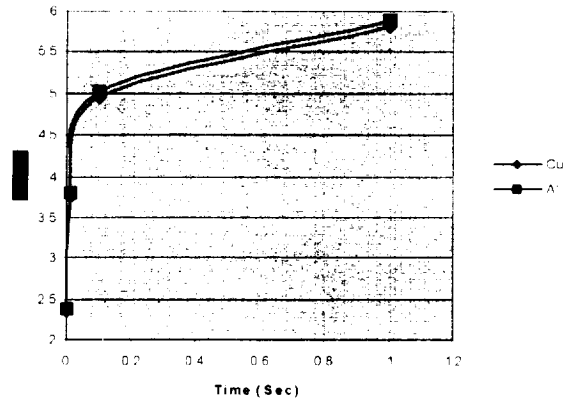


Figure 2: Erased V<sub>t</sub> versus erase time graph for single bit EEPROM cells with Cu and Al interconnects.

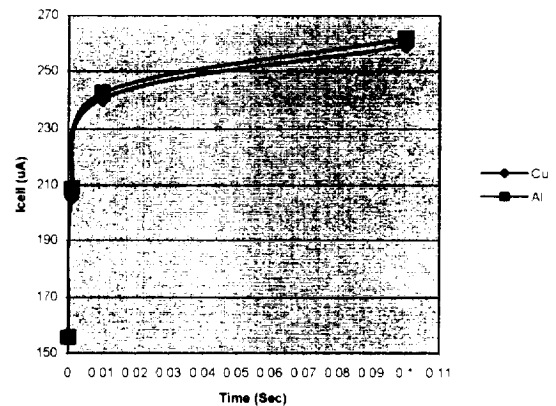


Figure 3: I<sub>cell</sub> versus program time graph for single bit EEPROM cells with Cu and Al interconnects.

Data Retention: Wafer level bake was done on both wafers with Al and Cu backend. The following procedure was adopted for the data retention test (1) program/erase cycling (2) erase margin  $V_t$  (3) bake at 125 °C (4) erase margin  $V_t$ . Step 3 followed by step 4 was repeated for different bake times

Erase margin after 500 hours bake time at 125 °C shifted less than 1.5% for the EEPROM cell with Cu interconnect. This is comparable to the erase margin shift under the same bake conditions for the identical EEPROM cell with Al interconnect. The graph in figure 4 plots erase  $V_t$  versus bake time for both Al and Cu interconnect EEPROM cells. This demonstrates that Cu interconnect technology can be integrated reliably with the non-volatile EEPROM cell

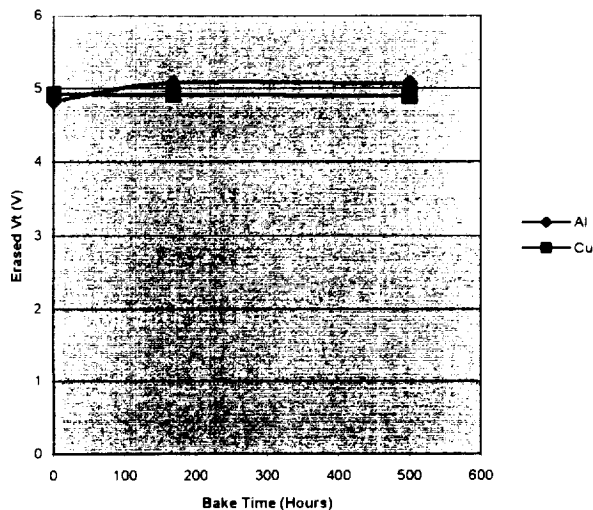


Figure 4: Graph showing erase margin versus bake time for single poly EEPROM cell with Al and Cu interconnect.

#### Reliability comparison of EEPROM cells with silicon nitride and oxynitride barrier layers.

Furnace grown silicon nitride was used as a diffusion barrier layer to prevent contamination from reaching the floating gate of the non-volatile cell. Oxynitrides as barrier layers have

received an increasing amount of interest due to the possibility that, by choosing the proper composition, the excellent electrical characteristics of  $\text{SiO}_2$  and the barrier properties against moisture and other sources of contamination of silicon nitride may be preserved [2]. Additionally, oxynitrides deposited by PECVD at low temperature would be a better choice than furnace-deposited silicon nitride at higher temperature for shrinking technologies due to smaller thermal budget of the former [4-6]

Data Retention. Wafer level bake at 125 °C was done on both wafers with identical EEPROM cells but different diffusion barrier layers of nitride and oxynitride. The same procedure described earlier in this paper was used for the data retention test. The graph in figure 5 shows erase margin versus erase bake time after 500 hours of bake at 125 C for both EEPROM cells. Erase margin shift for EEPROM cell with oxynitride as diffusion barrier blanket layer was more than 12% while that for EEPROM cell with silicon nitride as a diffusion barrier blanket layer was less than 1.5%. However, there was no erase  $V_t$  margin shift from 168 hours to 500 hours. On account of shift in the  $V_t$  margin from zero hour to 168 hours, it is concluded that plasma enhanced oxynitride is an unsuitable choice for diffusion barrier layer.

The possible cause of erase  $V_t$  margin shift from zero hour erase margin to 168 hours might not be due to real charge flow from the floating gate but could be as a result of charges in the oxynitride layer that couple voltage to the floating gate thereby shifting the margin. Charges in the oxynitride layer deposited by PECVD could arise from the creation of dangling bonds (DB) which are enhanced as more O atoms are incorporated in the oxynitride film. However, the formation mechanism of defects in oxynitride films with different compositions is unclear [7]. Also, conventional plasma-assisted CVD with  $\text{SiH}_4$

as silicon source introduces hydrogen in the deposited films that causes thermal instability of physical and electrical properties during subsequent processing [2, 8]. D. R. Cote and co-authors [9] have suggested that PECVD oxynitride film with higher refractive index ~ 1.80 to 1.85 might be more desirable for barrier application. The bonding structural analyses and electrical measurements on PECVD oxynitride films done by these authors have shown that films with refractive indices of 1.75 to 1.80 have low surface states with minimal leakage

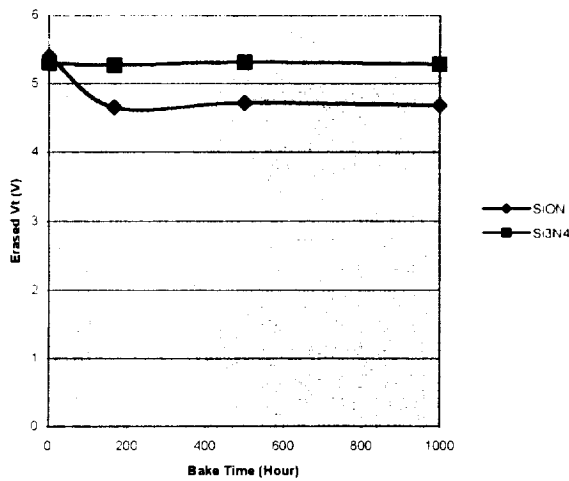


Figure 5: Graph showing erase margin versus bake time comparison for EEPROM cell with silicon nitride and oxynitride as diffusion barrier layers underneath Al metal.

### Conclusions

The experimental results show that Cu/low-k interconnect can be used as an interconnect of choice with non-volatile EEPROM devices without causing significant reliability and performance concerns. Experimental results also indicate that PECVD oxynitride may not be a good substitute for furnace grown silicon nitride presently used as a diffusion barrier layer underneath metal in the EEPROM cell

due to increased charge loss possibly caused by the creation of dangling bonds and charge states in PECVD oxynitride.

### Acknowledgments

The authors would like to thank Myron Wong and Brad Vest from Altera design engineering for their valuable inputs related to the cell design as well as Samit Sengupta from Altera technology engineering for inputs related to Cu structures design. Authors would also like to thank TSMC fab and processing R&D groups for manufacturing and providing the wafers in a timely manner.

### References

- [1] International Technology Roadmap for Semiconductors, 1999, p-167
- [2] O. Sanchez, J. M. Martinez-Duart, R. J. Gomez-Sanroman, R. Perez-Casero, J. of Mat. Sci 34 (1997) 3007-3012
- [3] E.P. Gusev, H.-C. Lu, E.L. Garfunkel, T. Gustafsson, M.L. Green, IBM J. Res. Dev. VOL. 43 No.3 May 1999
- [4] B. Hajji, P. Temple-Boyer, F. Olivie, A. Martinez Thin Solid Films (1999) vol. 354, no. 1-2, p. 9-12
- [5] D. R. Harding, L.U.T. Ogbuji, M. J. Freeman, J. Appl. Phys. 78 (1995) 1673
- [6] O. Sanchez, M. A. Aguilar, C. Falcony, J.M. Martinez-Duart, J. M. Albella, J. Vac. Sci. Technol. A14 (1996) 2088.
- [7] S. Hasegawa, S. Sakamori, M. Futatsudera, T. Inokuma and Y. Kurata J. Appl. Phys vol 89 number 5 P 2598
- [8] R. C. Sun, J. T. Clements, J. J. Nelson, 18<sup>th</sup> Annual Proc. Reliability Phys (IEEE, Las Vegas, 1980) P. 244.
- [9] D. R. Cote, S. V. Ng, A. K. Stamper, D. S. Armbrust, D. Tobben, R. A. Conti, G. Y. Lee, IBM J. Res. Dev. Vol 43 No. 12 Jan/Mar 1999

Process Optimization for MOCVD of SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> for Non-Volatile Memory Applications

Presenter: D Burgess, Aixtron

Material for this presentation was not available at the time of publication



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# Atomic Scale Structure of Giant Magnetoresistive Multilayers: Energetic Adatom and Surfactant Effects

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**Abstract**—The deposition of higher quality giant magnetoresistive (GMR) metal multilayers is essential for improving the performance of magnetic field sensors and nonvolatile random access memories. Improved performance requires reduction of both the atomic scale interfacial roughness and interlayer mixing in the as deposited films. The first step is to develop relationships between controllable process parameters and the atomic scale interfacial composition/structure. We have used atomistic simulation and controlled experiments to begin to address this issue. We show that control of the adatom energy and the use of a silver surfactant can improve the interface structure of multilayers. Increasing the adatom energy causes surface flattening due to enhanced surface reconstruction, but results in interlayer mixing due to impact induced atomic exchanges. A modulated energy deposition scheme was found to reduce both roughness and mixing. The addition of a small quantity of silver was found to reduce the activation barriers for surface atomic assembly and to enable the assembly process kinetics to be shifted to a regime where conventional deposition processes are able to create high quality interfaces.

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3. EFFECTS OF HYPERTHERMAL ENERGY DEPOSITION
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7. SURFACTANT MECHANISM
8. CONCLUSIONS
9. ACKNOWLEDGMENTS

## 1. INTRODUCTION

In 1988, Baibich et al discovered that nanoscale Fe/Cr/Fe multilayers exhibit a very large drop in electrical resistance when a moderate magnetic field was applied <sup>[1]</sup>.

Since then, many other multilayer systems composed of (~50Å thick) ferromagnetic metal layers separated by (~20Å thick) nonferromagnetic conductive metal layers have been found to possess this giant magnetoresistive (GMR) property. The most frequently studied systems have either a Co/Cu/Co <sup>[2,3]</sup> or a NiFe(Co)/Cu/NiFe(Co) <sup>[4,5]</sup> repeated unit. These GMR materials are well suited for sensing small magnetic fields. Intensive research has quickly resulted in the development of sensors for the readheads of hard disk drives. This contributed to the very large recent increases in the hard drive storage capacity <sup>[6]</sup>. Many groups are now also exploring the application of these materials to create nonvolatile magnetic random access memory (MRAM) <sup>[6]</sup>.

Both the readhead sensors and MRAM applications of GMR materials are greatly improved if better GMR properties can be achieved. Relevant GMR properties include a high GMR ratio (defined as the maximum resistance change divided by the resistance at magnetic saturation), a low magnetic saturation field, a high thermal stability, minimal coercivity, and weak temperature dependence. However, efforts to develop a deposition process that can reliably produce a superior combination of these properties have been prolonged because many deposition conditions sensitively affect the atomic scale structure of the multilayers which in turn control GMR properties

When pairs of ferromagnetic layers are separated by an appropriate thickness, the RKKY interaction causes their magnetic moments to align antiferromagnetically in a zero magnetic field <sup>[7]</sup>. Spin dependent electron scattering then results in a relatively high electrical resistance <sup>[8,9]</sup>. If an external magnetic field is applied to align the magnetic moments of the ferromagnetic layers, the spin-dependent electron scattering is reduced, and so is the electrical resistance of the film. Experiments indicated that a significant change of the GMR ratio could occur when the spacing between the ferromagnetic layers is varied by as little as 2 Å <sup>[2]</sup>. In multilayers with rough interfaces, Neel coupling occurs which greatly increases the coercivity of the device. This becomes increasingly significant as the roughness amplitude and wavelength approach the layer spacing. Alloying (mixing) of one layer with the atoms of

another causes an increase in spin independent scattering<sup>[8]</sup> and a loss of local magnetic alignment<sup>[10]</sup>, which also reduce the size of the GMR effect. High quality GMR multilayers must therefore have a precisely controlled layer thickness, very low interfacial roughness and minimal interlayer mixing. The development of processes that result in relatively smooth, unmixed interfaces is critical if the GMR ratios of multilayers are to be increased<sup>[11]</sup>.

Experiments provide clues to identify the key processing parameters sensitive to GMR properties. Similar architecture GMR multilayers have been synthesized by ambient temperature sputtering<sup>[4]</sup>, ion beam deposition<sup>[12]</sup>, and molecular beam epitaxy (MBE)<sup>[11]</sup>. The reported GMR ratio for Co/Cu( $\sim 20\text{\AA}$ )/Co multilayers deposited using these different deposition methods<sup>[13]</sup> are shown in Fig. 1. In the MBE case the GMR ratio data was measured at 4.2 K. Parkin et al have measured the GMR ratio of the  $[\text{Co}(10\text{\AA})/\text{Cu}(9.3\text{\AA})]_{16}$  multilayers as a function of temperature<sup>[7]</sup>. Their experiments indicated that the room temperature GMR ratio is about 63% that at 4.2 K, so in Fig. 1 we have converted the low temperature MBE data to room temperature by multiplying a factor of 63%. Fig. 1 indicates that multilayers deposited using low-pressure magnetron sputtering and ion beam deposition (IBD) are generally superior to those produced using MBE. This is somewhat surprising considering that the GMR multilayers were first discovered using MBE<sup>[11]</sup>, and that MBE has been so successful to deposit high purity, highly crystalline semiconductor films. A notable feature of MBE method is that the energy of its deposition flux is near thermal equilibrium, which is much lower than the other sputter deposition methods. The question is if this low energy contributes to the poor quality of the films, and why.

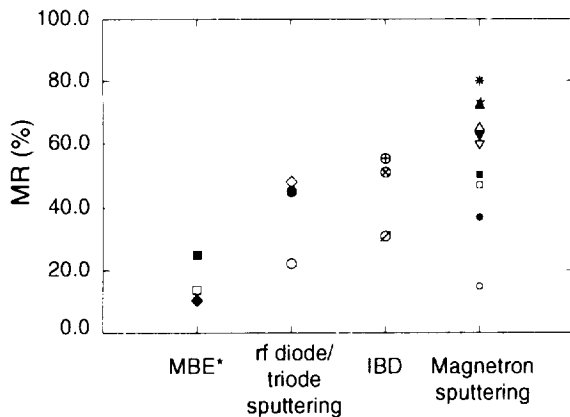


Fig. 1. GMR values reported for different deposition processes. \*MBE data were converted (see text). ■: [14], □: [15], ◆: [16], ◇: [17], ●: [18], ○: [19], ⊕: [20], ⊗: [12], ∅: [21], +: [29], ×: [22], \*: [23], ▲: [24], △: [3], ▼: [25], ▽: [26], ■: [2], ∘: [7], •: [27], ◦: [28].

Kano et al<sup>[29]</sup> studied the effects of deposition temperature on the GMR ratio of the  $[\text{Co}(10\text{\AA})/\text{Cu}(10\text{\AA})]_{100}$  multilayers. Their data are shown in Fig. 2. It indicates that at substrate temperatures above  $100^\circ\text{C}$ , the GMR ratio rapidly decreases as the substrate temperature is increased. On the other hand, the GMR ratio gradually increases as substrate temperature is decreased from  $100^\circ\text{C}$ . The GMR ratio is seen to approach a saturated high value at near room temperature. The results above appear to indicate that process conditions that promote thermally activated atomic assembly during deposition are not favorable for GMR multilayer growth.

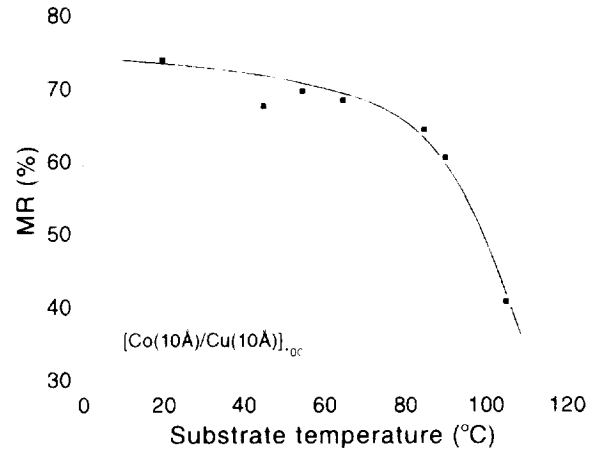


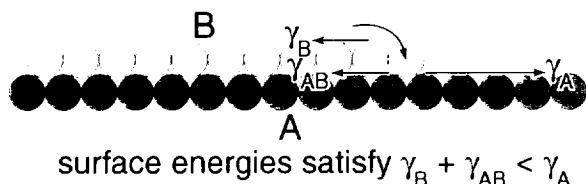
Fig. 2. GMR ratio as a function of substrate temperature.

A simple thermodynamics analysis shown in Fig. 3 can explain some of the observations in Figs 1 and 2. Consider the growth of an A/B/A multilayer stack. Suppose that the bond energy between A atoms is higher than that between B atoms. If atoms A and B are about the same size, then B can wet A because the more strongly bonded A atoms can pull B atoms onto their surface, Fig. 3(a). However, A will then not wet B because the relatively weakly bonded B atoms cannot reconstruct A clusters, Fig. 3(b). This indicates that during the deposition of an A/B/A multilayer system under thermally equilibrated conditions (i.e. kinetic conditions that permit the equilibrium structure to be achieved), the step flow growth mode can only be achieved at either the A on B or B on A interface but not both. It should also be noted that even when the bond strength argument favors the step flow growth mode, surface roughness could still arise when a large strain energy exists due to size differences between the different elements.

In GMR multilayers the surface roughness at completion of each layer growth sets the roughness of the interface created by overgrowth with the next metal. This mechanism is presumed to contribute to the poor GMR multilayers deposited using MBE as seen in Fig. 1. The sharp drop of GMR ratio for films deposited at temperatures above  $100^\circ\text{C}$ , Fig. 2, can also be a result of

significant interlayer mixing due to enhanced interlayer diffusion.

**(a) B atoms wet A surface**



**(b) A atoms do not wet B surface**

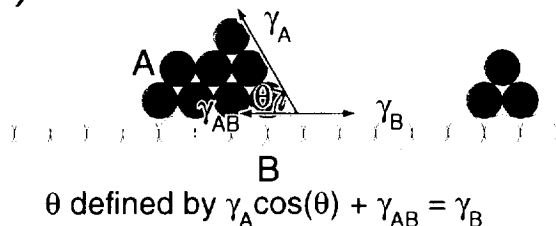


Fig. 3. Surface morphology under thermal equilibrium growth conditions.

The atomic scale structure of multilayers results from atomic assembly processes active during deposition. This assembly can be mediated by controlling the temperature of the surface and the deposition rate which in effect control the time available for a thermal fluctuation to induce an atom to hop from one site to another<sup>[30]</sup>. Hops can also be induced by other (nonthermal) processes such as hyperthermal metal impacts<sup>[31,32]</sup>, inert gas ion assistance<sup>[33]</sup>, and the heat of reaction when atoms are condensed on the film<sup>[31]</sup>. The relative success of the magnetron sputtering and IBD processes reviewed above suggest that the use of growth conditions that constrain thermally assisted processes combined with “hot” metal atoms may be preferred for the growth of GMR multilayers. Atomistic simulations provide a route to explore these ideas in detail.

## 2. ATOMISTIC SIMULATION METHODS

If the atomic scale interfacial structures are sensitively affected by the fluxes incident upon a growth surface, it is important that they be well understood. For the low pressure sputter and IBD processes that can produce good GMR multilayers, the adatoms can have a wide distribution of energies with an average in the 5-10 eV range and a tail extending to above 30 eV<sup>[34]</sup>. The adatom energy can be reduced by increasing the chamber pressure and target to substrate distance<sup>[35]</sup>. Recent experiments have also linked strong variations in the GMR ratio to the existence of secondary inert gas flux incidence upon the growth surface<sup>[36]</sup>.

To realistically predict the effects of energetic impacts, a highly predictive atomistic simulation method must be used. In our work, a molecular dynamics (MD) approach is used to simulate the multilayer growth, including the transition of atoms from vapor to a solid surface and the subsequent surface reconstruction. Because Newton’s equations of motion are used to describe the evolution of atomic positions, the detailed atomic structures of a deposited film and many of the mechanisms active during the deposition can be correctly described provided a high fidelity interatomic potential is used to calculate the interatomic forces. We have adapted the embedded atom method (EAM) potential initially developed by Daw and Baskes<sup>[37]</sup>. EAM assumes that the total crystal energy is the sum of a pairwise potential and an energy required to embed each atom into its local medium with a given electron density. Because this embedding energy depends on the net local environment of each atom, EAM well accounts for the many-body effects. EAM models hence provide a good format for solving problems involving surfaces and other defect states.

EAM potentials developed for atoms of a single element cannot generally be applied to model the behavior of alloys. This arises because the reference states adopted for different elements are often not consistent, and the analytical forms and cut-off parameters of the interatomic potentials of individual elements are incompatible. However, by normalizing the EAM potential<sup>[38]</sup> and using a unified potential cutoff function, we have recently developed a generalized EAM potential database that enables calculation of alloys with any combination of sixteen metals (Cu, Ag, Au, Ni, Pd, Pt, Al, Pb, Fe, Mo, Ta, W, Mg, Co, Ti, and Zr)<sup>[39,40]</sup>. These potentials are well fitted to basic material properties such as lattice constants, elastic constants, bulk moduli, vacancy formation energies, sublimation energies, and heats of solution.

Details of our MD simulation can be found in ref. [41]. Briefly, a computational crystal was created by assigning atom positions according to lattice sites. Periodic boundary conditions were used in the lateral x and z directions to extend the crystal dimensions and a free boundary condition was used for the vertical y direction. Atoms with prescribed kinetic energies were randomly injected (from far above) to the top y surface at a frequency that gave rise to a desired deposition rate. The evolution of atom positions (and hence the atomic structure of the entire system) was then solved from Newton’s equation of motion. To calculate the stress and account for relaxation of the crystal size under the influence of the lattice mismatch between different layers, a Lagrangian form of Newton’s equation of motion was used<sup>[42]</sup>. To prevent the crystal shift due to momentum transfer at the top y surface, the positions of the two bottom monolayers of the substrate atoms were fixed during simulation. Isothermal growth is achieved by applying a temperature control scheme<sup>[41]</sup> to

unconstrained part of the substrate crystal. This region was then advanced upwards as deposition progressed in a way that left several free monolayers at the surface. This enabled the effects of energetic impacts to be realistically simulated.

### 3. EFFECTS OF HYPERTHERMAL ENERGY DEPOSITION

The simulation methodology has been used to analyze the growth of a Cu(20Å)/Ni(20Å) unit as a function of adatom energy at a fixed normal adatom incident angle, a substrate temperature of 300 K and a deposition rate of 1 nm/ns. The detailed atomic structures of the simulated multilayers are shown in Fig. 4, where Ni and Cu atoms are marked with black and white balls respectively. It can be seen that at the low incident energies ( $\sim 0.1$  eV or less) typical of either MBE or high pressure sputtering, the interfaces exhibited both significant roughness and Cu mixing in the subsequently deposited Ni layer. Interestingly, little mixing of Ni is seen in either of the copper layers. This phenomenon has recently been experimentally observed in the atomic scale structures of multilayer stacks<sup>140l</sup>.

Increasing the incident energy from 0.1 to 5.0 eV significantly reduces the roughness of both the Cu-on-Ni and the Ni-on-Cu interfaces. The Ni-on-Cu interface is flatter than the Cu-on-Ni interface at low incident energies, but this difference becomes small when the incident energy increases to 5.0 eV where both interfaces approach a saturation flatness. Increasing the incident energy from 0.1 to 1.0 eV appears to reduce the mixing of Cu in the Ni layer, but the mixing is significantly increased as the incident energy is further increased. Again Cu atoms are dispersed in the subsequently deposited Ni layer much more significantly than Ni atoms are dispersed in the subsequently deposited Cu layer.

Both the amplitude and wavelength of interfacial roughness are expected to influence the GMR ratio. An average amplitude to wavelength ratio  $r_1$  was used to characterize the roughness of the simulated structures<sup>141l</sup>. The value of  $r_1$  as a function of incident energy is plotted in Fig. 5(a) for both the Cu-on-Ni and the Ni-on-Cu interfaces. Fig. 5(a) shows that the interfacial roughness initially decreases with increasing incident energy, reaches a minimum between about 2.0 and 3.0 eV for the Ni-on-Cu interface and at about 4.0 eV for the Cu-on-Ni interface, and then begins to rise as the incident energy is increased beyond 4.0 eV.

When surface roughness is experimentally measured say by atomic force microscopy, the average deviation  $r_2$ , of a surface profile from the mean surface height, is usually obtained<sup>14l</sup>. If the surface roughness is sinusoidal,  $r_2$  can be linked to  $r_1$ . The  $r_2$  surface roughness is also shown (on the right coordinate) in Fig. 5(a).

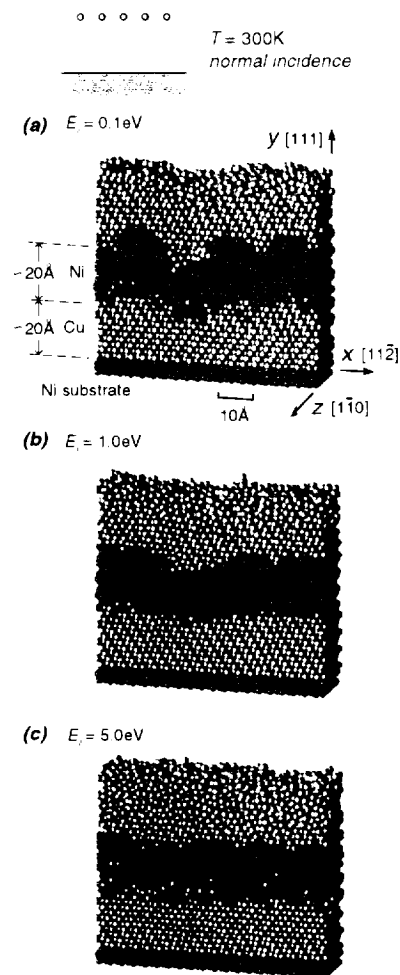


Fig. 4. Simulated multilayer structure as a function of adatom energy.

Kools<sup>14l</sup> has experimentally measured the  $r_2$  surface roughness during the growth of  $\text{Ni}_{80}\text{Fe}_{20}/\text{Cu}/\text{Ni}_{80}\text{Fe}_{20}$  exchange-biased spin-valves. His results are included in Fig. 5(b). The samples used in Kools' experiments were grown using magnetron sputtering at a constant target-substrate distance of 109 mm and various chamber Ar pressures between 1 and 10 mTorr. Using MD predictions of the energy spectrum of sputtered Cu<sup>134l</sup> and a binary collision model for copper transport in an argon atmosphere<sup>135l</sup>, the average incident atom energy was estimated to be about 0.1 eV at 10 mTorr and about 4.0 eV at 1 mTorr. These energies and the equivalent pressures are indicated in Fig. 5. It can be seen that the predicted decrease of roughness with incident energy in the low (thermal) energy range, the existence of a minimum roughness in the intermediate energy range, and the increase of roughness with incident energy in the high (hypertermal) energy regime all agree well with the experiments.

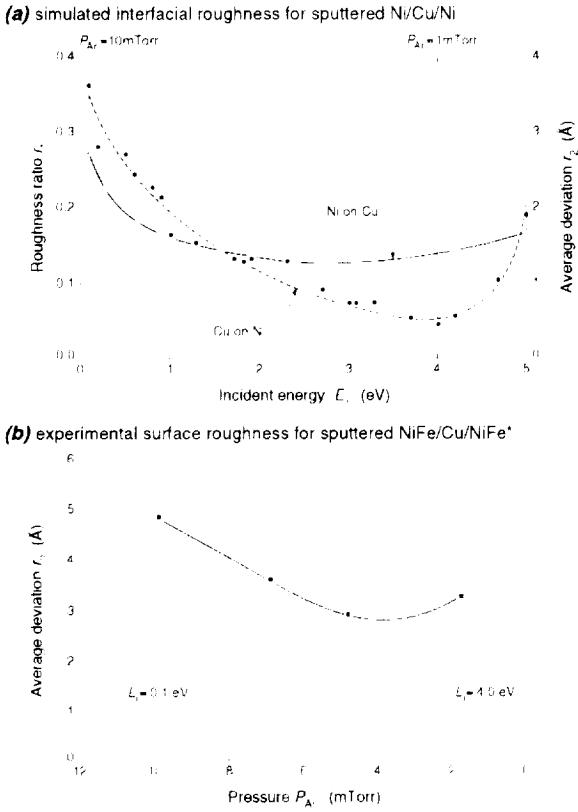


Fig 5. Interfacial roughness as a function of adatom energy.

Fig. 4 qualitatively indicates that the degree of Cu mixing in the Ni layer is affected by the adatom incident energy. The extent of Cu mixing in the Ni layer can be quantified by the probability of finding a Cu atom with many Ni atom neighbors. The probability,  $p$ , of a Cu atom having at least eight Ni nearest neighbors was calculated and is shown in Fig. 6(a) as a function of incident energy. Fig. 6(a) more graphically shows that Cu mixing initially decreases with increasing incident energy, reaches a minimum at an energy of 1.0-2.0 eV, and then increases significantly with increasing incident energy. Serious Cu mixing ( $p \approx 1.7\%$ ) occurs when the incident energy approached 5.0 eV.

A direct experimental measurement of the Cu mixing probability,  $p$ , shown in Fig. 6(a), has not been made. In Kools' experiments with the exchange-biased spin-valve  $\text{Ni}_{80}\text{Fe}_{20}/\text{Cu}/\text{Ni}_{80}\text{Fe}_{20}$  multilayers<sup>[4]</sup>, the extent of Cu mixing into a Ni rich permalloy layer was related to a thickness,  $t_d$ , within which the permalloy lost its magnetism due to Cu contamination. Measured  $2t_d$  values are shown in Fig. 6(b) as a function of Ar background pressure, where the argon pressure range has been converted into estimated incident energy range as described above. The predicted trend of the Cu mixing with adatom energy is clearly seen in the  $t_d$  data of Kools' experiment. In particular, the existence of a minimum

mixing at a pressure of about 8 mTorr (near 1 eV) is in good agreement with the simulations. The experimental data in Fig. 6(b) also indicate that the degree of mixing after high-energy deposition is significantly greater than after a low energy deposition as seen in the MD simulations.

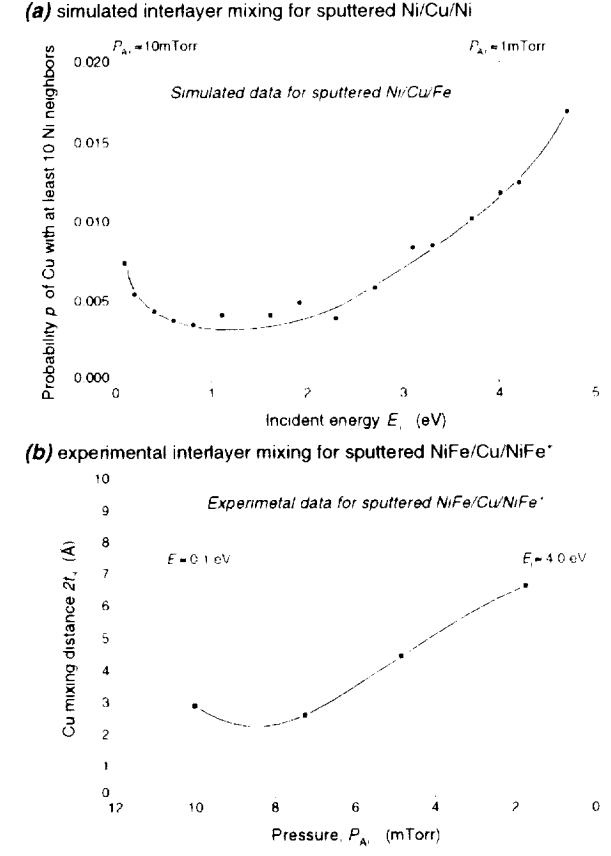


Fig. 6. Interlayer mixing as a function of adatom energy.

#### 4. HYPERTHERMAL ENERGY IMPACT MECHANISMS

To explore the mechanisms of the adatom energy effects observed above, time resolved MD simulations were used to examine individual Cu adatom impacts with a surface asperity on a (111) Cu surface. The change of the asperity during a low (0.1eV) and a high (5.0 eV) energy atom impact is shown in Fig. 7, where the adatom is marked with "A". It can be seen that at the lower energy, the adatom promoted surface roughness by attaching to the sidewall of the asperity. However, the higher energy impact resulted in momentum transfer to the atoms in the asperity and subsequent rapid rearrangement on the surface. This resulted in a local flattening effect. This flattening occurred within a few picoseconds, which is generally much faster than the thermally activated processes. Hypertothermal energy metal atom deposition under thermally constrained conditions therefore may provide potent routes for avoiding interfacial roughness.

Because impacts more easily cause reconstruction on weakly bonded Cu than strongly bonded Ni, the Ni-on-Cu interface is flatter than the Cu-on-Ni interface at low adatom energies.

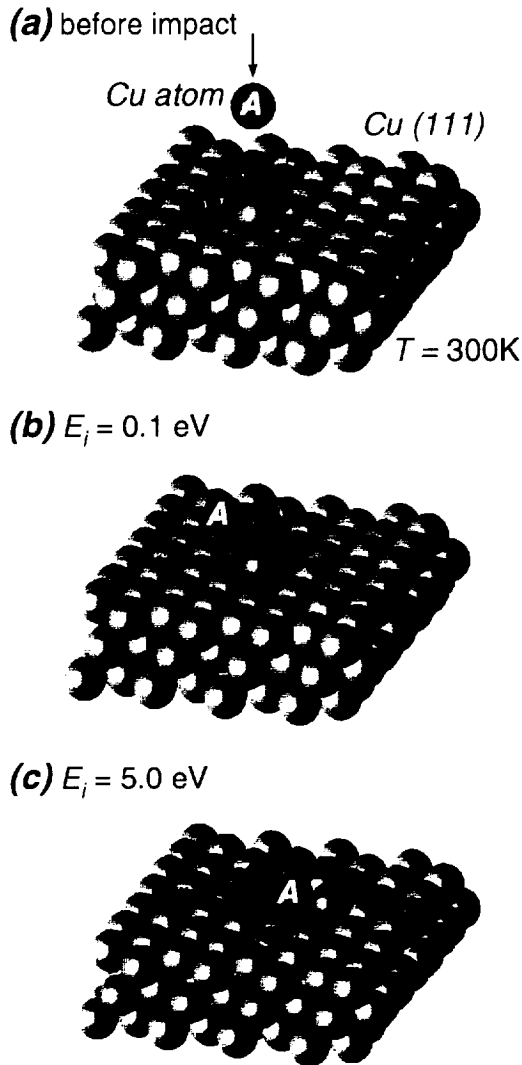


Fig. 7. Impact induced flattening mechanism.

However, energetic atom impacts can cause other phenomena. Fig. 8 shows MD results for a high-energy Ni adatom (marked with "A") impact with a flat (111) Cu surface. It can be seen that during this impact, the Ni atom exchanged with a surface copper atom. This occurred when the Ni adatom penetrated the Cu lattice sufficiently that it was embedded in the Cu lattice and ejected a Cu atom on to the top of the surface. The atom exchange probability has been found to depend on many factors including the adatom, the surface composition, the defect structure of the surface and the energy and angle of the impact<sup>[41,43]</sup>. These results have shown that impact atom induced exchange is the cause of significant mixing during the low temperature deposition condition used for

GMR multilayer growth. The exchange probability is lower on a perfect surface than on a defective (rough) surface, and increases with increasing impact energy. The apparent increase in interfacial roughness at very high adatom energies seen in Fig. 5 is in fact the result of diffused interfacial boundary due to significant interlayer mixing. The exchange probability is also much higher when a Ni atom impacts a Cu surface than when a Cu atom impacts a Ni surface. This arises because surface segregation of Cu in a Ni film is energetically favored, and the lower cohesive energy Cu surface can be more easily penetrated. This finding accounts well for the observations in Fig. 4 that the Cu-on-Ni interface is relatively sharp while the Ni-on-Cu interface is more diffuse, and Cu mixing occurred preferentially in the subsequently deposited Ni layer.

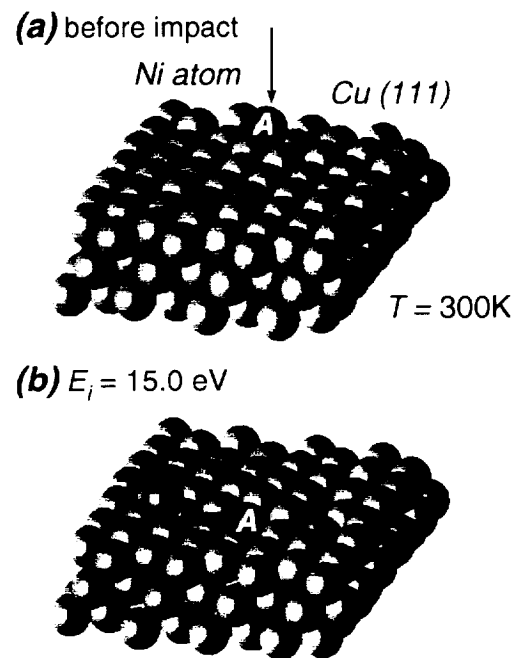


Fig. 8. Impact induced mixing mechanism.

## 5. IMPROVED DEPOSITION PROCESS

The MD simulations have provided compelling evidence that increasing the metal atom kinetic energy helps flatten interfaces. It is presumably this effect that leads to an improved GMR ratio in energetic deposition processes like magnetron sputtering and ion beam deposition. However, the energetic adatoms also induce interlayer mixing at interfaces, especially when the underlying material has a strong tendency to segregate to the surface of the material being deposited. While lowering the adatom energy can sharpen the chemical boundary of the interface, it is accompanied by an increase of the interfacial roughness. As a result, the best GMR properties are obtained from materials grown at an intermediate adatom energy<sup>[4,12]</sup>.

The identification of the asymmetric interfacial structures and their formation mechanisms suggests that the use of different adatom energies to deposit the Cu and the Ni layers may be more beneficial than the use of a single “optimum” energy for the deposition of all layers. In particular, the use of a lower adatom energy for the deposition of the Ni layer on Cu than for the Cu on Ni (interlayer energy modulation) can effectively sharpen the Ni-on-Cu interface. A search of the literature reveals that such a strategy has been experimentally tested and was found to improve the GMR ratio<sup>[41]</sup>. Even better films are anticipated if a process can be developed that allows a modulation of the adatom energy during deposition of each layer (intralayer energy modulation).

To investigate this idea, a simulation was conducted where the first few monolayers of a new layer were deposited using a fixed low energy ( $E_l$ ) of 0.1 eV and the remainder of that layer was deposited at a higher energy ( $E_h$ ). The calculated Cu(20Å)/Ni(20Å) atomic structures at normal adatom incident angles are shown as a function of  $E_h$  in Fig. 9.

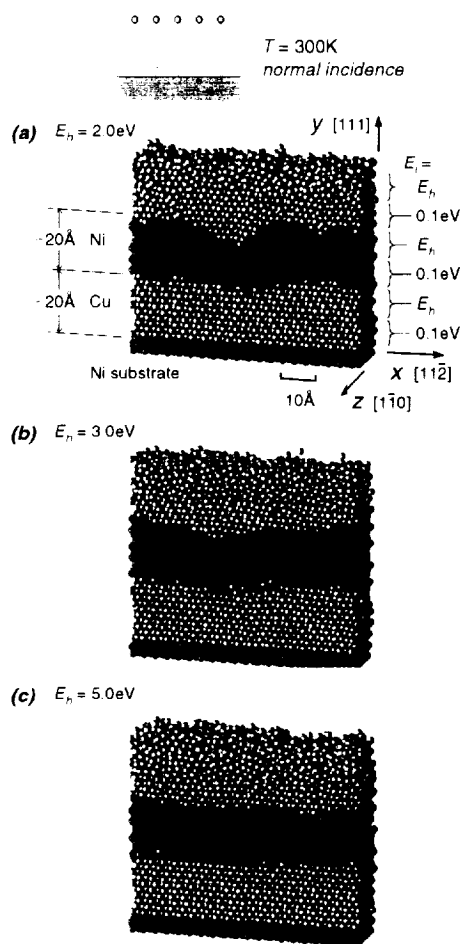


Fig. 9. Simulated multilayer structure as a function of modulated energy.

When compared with the best outcome of the single energy strategy (Fig. 4), Fig. 9 shows that the energy modulation strategy resulted in a significant reduction in both the interfacial roughness and the degree of intermixing. To quantify the improvement, the roughness of both interfaces and the degree of Cu mixing in the Ni layer were calculated as a function of  $E_h$ , Fig. 10. It can be seen that because the atom exchange mechanism was more difficult on flat surfaces, increasing  $E_h$  not only improved the interfacial smoothness, but it also reduced the mixing.

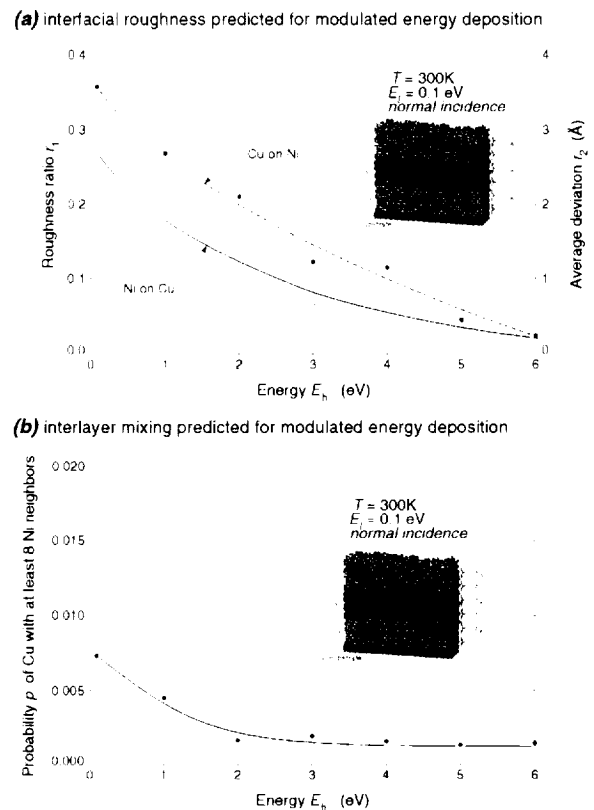


Fig. 10. Multilayer roughness and mixing as a function of modulated energy.

The results and conclusions described above have been found to also apply to Co/Cu/Co and CoFe/Cu/CoFe multilayers<sup>[40]</sup>. Direct experimental validation using three dimensional atom probe methods has been recently achieved for the CoFe/Cu/CoFe system<sup>[40]</sup>.

## 6. SURFACTANT EFFECTS

When strongly bonded materials are deposited on a more weakly bonded surface, the more strongly bound atoms tend to form islands and high surface roughness. The potent effects of hyperthermal adatoms can be used to flatten these islands but the degree to which it can be used is limited by adatom penetration into the more weakly bonded surface. An alternative strategy to promote

flatness is to modify the composition of the surface (by adding additional elements) so that the islands can be flattened using lower energy adatoms. Ideally, the elements to be added should have a high surface mobility and can remain on the growth surface (therefore be only minimally soluble in the film). Possible candidates of such elements include Ag and Au, which can be added during the deposition of the conductive layers.

MD simulations of the deposition of the  $\text{Cu}(20\text{\AA})/\text{Ni}_{75}\text{Co}_{25}(20\text{\AA})$  and the  $\text{Cu}_{80}\text{Ag}_{15}\text{Au}_5(20\text{\AA})/\text{Ni}_{75}\text{Co}_{25}(20\text{\AA})$  multilayers have been performed. An adatom incident energy of 1.0 eV, an adatom incident angle of  $45^\circ$ , a substrate temperature of 300 K, and a deposition rate of 4 nm/ns were employed. The oblique angle of incidence was used because it promoted surface roughening (by flux shadowing) and therefore could more clearly reveal any surface flattening effects due to Ag and Au additions [13]. The results of the simulated atomic scale structures with and without Ag and Au are shown in Figs. 11(a) and 11(b) respectively. To better show the contrast, only three grayscale levels are used in Fig. 11. The dark spheres are used for atoms in the magnetic layers (Ni and Co), white balls are used for Ag atoms, and gray balls are used for other atoms in the conductive layers (Cu and Au). Ag atoms are distinguished because they were found to distribute differently from Cu and Au atoms. Fig. 11(a) indicates that at the oblique incident angle, shadowing can exclude the incoming atoms from parts of the valleys between the randomly formed surface asperities. This results in very high surface roughness during  $\text{Cu}(20\text{\AA})/\text{Ni}_{75}\text{Co}_{25}(20\text{\AA})$  deposition. The roughness not only develops during the deposition of NiCo layer, but also during deposition of the Cu layer. A remarkable finding in Fig. 11(b) is that the surface roughness of the  $\text{Cu}_{80}\text{Ag}_{15}\text{Au}_5(20\text{\AA})/\text{Ni}_{75}\text{Co}_{25}(20\text{\AA})$  unit is greatly reduced. This is accompanied by a significant Ag surface segregation. It can be seen that even though Ag were only added to the conductive layer, many Ag atoms migrated through both the conductive and the magnetic layers to reach the surface. Because this was achieved even at a very high deposition rate used in simulation, a more complete Ag segregation can be expected at experimental deposition rates where atoms have more time to diffuse to the surface. Additional simulations without the addition of Au confirmed that the improved smoothness of the films is the result of the addition of the small amount of Ag during deposition.

To experimentally evaluate the significance of these effects, diode sputter deposited Cu and  $\text{Cu}_{80}\text{Ag}_{15}\text{Au}_5$  single layer films were grown at an Ar pressure of 20.0 mTorr, a plasma power of 175 W, and a target-substrate distance of 38.1 mm. The deposition was stopped at different film thickness, and the surface morphology of the films was characterized using atomic force microscopy. The measured RMS roughness of both the Cu and the  $\text{Cu}_{80}\text{Ag}_{15}\text{Au}_5$  films is shown in Fig. 12 as a function of film thickness. It can be seen that surface

roughness increased as film thickness increased. For the entire film thickness range studied, the roughness of the  $\text{Cu}_{80}\text{Ag}_{15}\text{Au}_5$  films was much lower than that of the Cu films. Scanning Auger microscopy was used to obtain the composition profile through the film thickness. Fig. 13 indicates that the Au and Cu compositions were nearly constant in the bulk of the film, but both dropped near surface. In contrast, strong Ag surface segregation was seen as a sharp rise of the Ag composition near the surface.

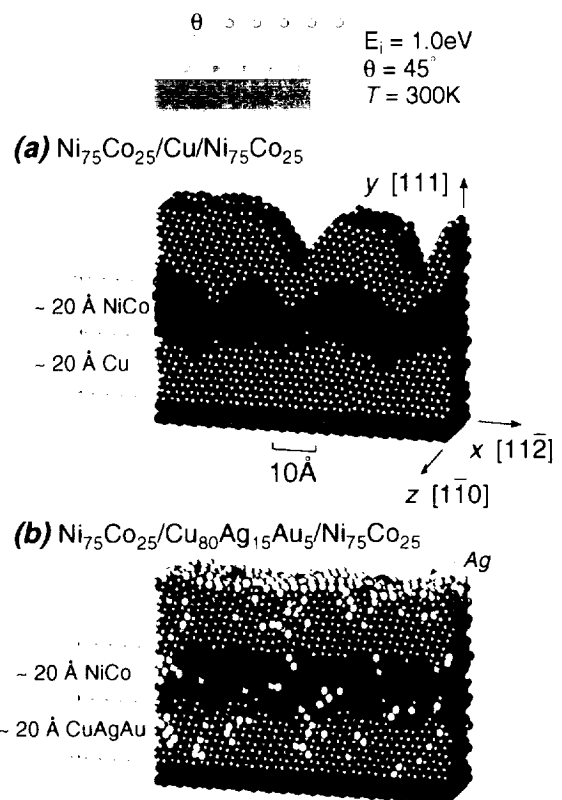


Fig. 11. Simulated effects of Ag surfactant on multilayer structure.

Both simulations and experiments indicated very strong Ag surface segregation and surface flattening effects. It is anticipated that the improved interfaces will enhance the magnetoresistance. Evidence of this is reported in a recent study of diode sputter deposited films [45].

To examine this further, GMR samples containing stacks of both  $[\text{Ni}_{65}\text{Fe}_{15}\text{Co}_{20}(20\text{\AA})/\text{Co}_{95}\text{Fe}_5(15\text{\AA})/\text{Cu}_{80}\text{Ag}_{15}\text{Au}_5(16\text{\AA})/\text{Co}_{95}\text{Fe}_5(15\text{\AA})]_n$  and  $[\text{Ni}_{65}\text{Fe}_{15}\text{Co}_{20}(20\text{\AA})/\text{Co}_{95}\text{Fe}_5(15\text{\AA})/\text{Cu}(16\text{\AA})/\text{Co}_{95}\text{Fe}_5(15\text{\AA})]_n$  multilayers were grown under the same conditions as the single layers above. The GMR ratios were measured and are shown in Fig. 14 as a function of stack repeating number  $n$ . Fig. 14 indicates that the GMR ratio for the multilayer stack with Ag and Au added is about 8% at  $n = 1$  and 18% at  $n = 3$ , while the multilayer stack with no Ag or Au added had no



measurable GMR effect for the entire n range. The addition of Ag hence significantly improves the GMR properties.

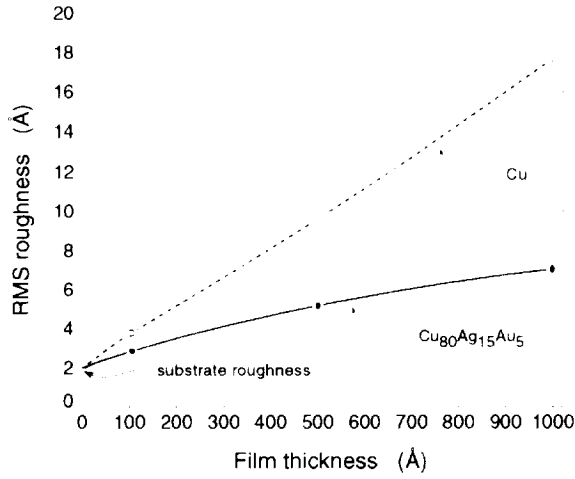


Fig. 12 Experimental RMS roughness of the Cu and the  $\text{Cu}_{80}\text{Ag}_{15}\text{Au}_5$  films as a function of film thickness.

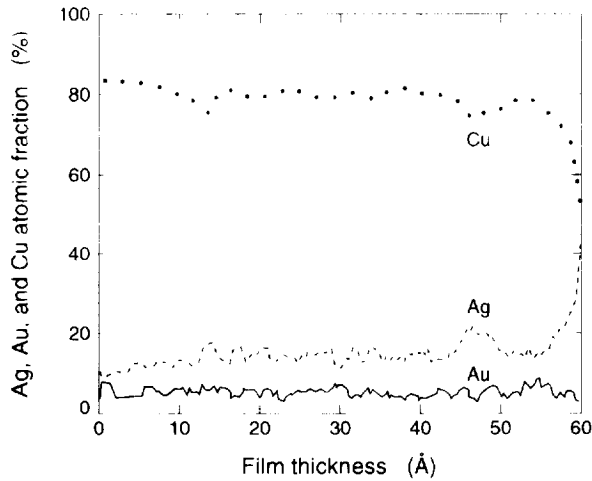


Fig. 13. Ag, Au and Cu composition profiles as a function of film thickness.

## 7. SURFACTANT MECHANISM

To understand the cause of the surfactant effects seen above it is necessary to evaluate the energetics of the different surfaces. To simplify the calculation without losing generality, the EAM potentials were used to calculate the energetics of various surface reactions using two-dimensional crystals composed of Ag, Au and Cu atoms<sup>[45]</sup>. The results indicated that the exchange between a Ag atom on a Cu surface and an underlying Cu atom resulted in an increase of energy. The exchange of a Au atom on a Cu surface and an underlying Cu atom, however, decreased the energy. As a result, Ag atoms tend to stay on the surface while Au atoms are easily

buried in the bulk. While it appears that lower surface energy materials can segregate to the surface, further analysis of the atomic pictures indicated that other factors could also contribute to the surface segregation. For instance, embedding a bigger atom into a lattice composed of smaller atoms was found to be energetically unstable. If the bigger atom was embedded at a near surface site, it could be easily exchanged to the surface. Ag has a size significantly bigger than that of Cu, Ni, and Co. Hence, Ag segregates to the surface. For atoms of the same size, the critical factor for surface segregation was found to be the cohesive energy of the atoms. During energetic impacts, the incoming atom more easily penetrates a lattice of low cohesive energy atoms. This then results in the exchange between the incoming atom and an underlying atom, leaving the low cohesive energy atom at the surface. Thermodynamically the surface segregation of lower cohesive energy atoms to the surface (breaking some bonds) also has less of an energy penalty than for more strongly bonded atoms. This simple rule indicates that for Ag and Au that are of the same size, since Ag has a much lower cohesive energy<sup>[46]</sup>, it should surface segregate. Likewise, Ni and Cu are about the same size, but since Cu has a much lower cohesive energy<sup>[46]</sup> so Cu should segregate to the surface of Ni (Fig. 4). These results suggest that during the deposition of multilayers, Ag atoms continuously segregate to the surface. Other metal atoms deposited on this Ag-rich surface can then quickly exchange with the Ag atoms

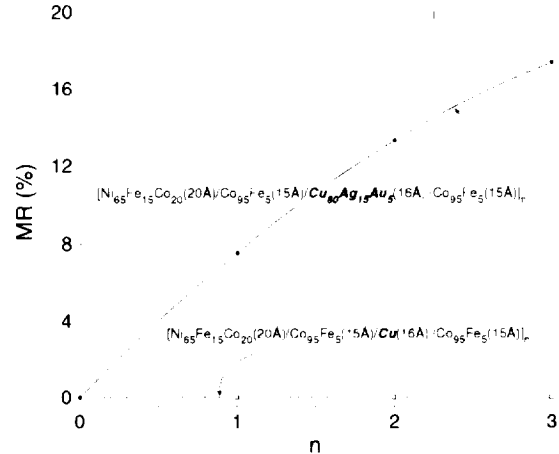


Fig. 14. Experimental GMR ratio for the multilayers with and without Ag surfactant.

Our calculations indicated that Ag also has lower energy barriers for surface diffusion than Cu, Ni or Fe. Consequently, Ag atoms can more rapidly migrate to lower energy ledge, kink and pit sites. The presence of these Ag atoms was found to reduce the Schwoebel barriers for other atoms on top of the terrace and to greatly increase the rate at which they could hop down to the ledge sites. As a result, Ag promoted the step flow growth of much smoother surfaces. Furthermore, because

energetic impact induced flattening more easily occurs on a surface composed of mobile atoms, the hyperthermal processing conditions that can lead to smooth growth are readily accessible if a Ag-rich surface is formed during deposition. The mechanism of rapidly smoothing the local surface asperities also greatly reduces the probability of causing surface shadowing during oblique deposition. As a result, surfactants such as Ag significantly improve the smoothness of the surface and the interfaces of multilayers

## 8. CONCLUSIONS

The search of a method for the synthesis of improved quality GMR multilayers has been a prolonged process. Atomistic simulation and accompanying experiments have led to the discovery that control of adatom energy and manipulation of surfactants can both significantly improve GMR multilayer structure and transport properties. High adatom energy promotes surface flattening due to enhanced surface reconstruction, but is accompanied by interlayer mixing due to impact induced atomic exchanges. While a low combination of roughness and mixing can be obtained at an intermediate adatom energy, a modulated energy deposition scheme was found to further reduce both the roughness and mixing. The addition of surfactants such as Ag was found to lead to significant flattening without intralayer energy modulation.

## 9. ACKNOWLEDGMENTS

We are grateful to the Defense Advanced Research Projects Agency (A. Tsao, D. Healy, and S. Wolf, Program Managers) for their support of this work.

## 10. REFERENCES

- <sup>1</sup> M.N. Baibich, J.M. Broto, A. Fert, F. Nguyen Van Dau, F. Petroff, P. Etienne, G. Creuzet, A. Friederich, and J. Chazelas, *Phys. Rev. Lett.* **61**, 2472(1988).
- <sup>2</sup> S. Honda, S. Ohmoto, R. Imada, and M. Nawate, *J. Magn. Magn. Mater.* **126**, 419(1993).
- <sup>3</sup> S.S.P. Parkin, Z.G. Li, and D.J. Smith, *Appl. Phys. Lett.* **58**, 2710(1991).
- <sup>4</sup> J.C.S. Kools, *J. Appl. Phys.* **77**, 2993(1995).
- <sup>5</sup> K. Meguro, S. Hirano, M. Jimbo, S. Tsunashima, and S. Uchiyama, *J. Magn. Magn. Mater.* **140-144**, 601(1995).
- <sup>6</sup> G.A. Prinz, *Science* **282**, 1660(1998).
- <sup>7</sup> S.S.P. Parkin, R. Bhadra, and K.P. Roche, *Phys. Rev. Lett.* **66**, 2152(1991).
- <sup>8</sup> W.H. Butler, X.G. Zhang, D.M.C. Nicholson, and J.M. MacLaren, *J. Magn. Magn. Mater.* **151**, 354(1995).
- <sup>9</sup> P.M. Levy, *J. Magn. Magn. Mater.* **140-144**, 485(1995).
- <sup>10</sup> D.M.C. Nicholson, W.H. Butler, X.G. Zhang, J.M. MacLaren, B.A. Gurney, and V.S. Speriosu, *J. Appl. Phys.* **76**, 6805(1994).
- <sup>11</sup> J.P. Nozieres, V.S. Speriosu, B.A. Gurney, B. Dieny, H. Lefakis, and T.C. Huang, *J. Magn. Magn. Mater.* **121**, 386(1993).
- <sup>12</sup> S. Schmeusser, G. Rupp, and A. Hubert, *J. Magn. Magn. Mater.* **166**, 267(1997).
- <sup>13</sup> X.W. Zhou, and H.N.G. Wadley, in preparation.
- <sup>14</sup> T. Thomson, P.C. Riedi, and D. Greig, *Phys. Rev.* **B50**, 10319(1994).
- <sup>15</sup> K.P. Wellock, B.J. Hickey, J. Xu, M.J. Walker, and N. Wiser, *J. Magn. Magn. Mater.* **140-144**, 585(1995).
- <sup>16</sup> K.P. Wellock, B.J. Hickey, D. Greig, M.J. Walker and J. Xu, *J. Appl. Phys.* **75**, 7055(1994).
- <sup>17</sup> D.H. Mosca, F. Petroff, A. Fert, P.A. Schroeder, W.P. Pratt Jr., and R. Laloe, *J. Magn. Magn. Mater.* **94**, L1(1991).
- <sup>18</sup> J.B. Youssef, K. Bouziane, O. Koshkina, H.L. Gall, M.E. Harfaoui, M.E. Yamani, J.M. Desvignes, and A. Fert, *J. Magn. Magn. Mater.* **165**, 288(1997).
- <sup>19</sup> H. Zhang, R.W. Cochrane, Y. Huai, M. Mao, X. Bian, and W.B. Muir, *J. Appl. Phys.* **75**, 6534(1994).
- <sup>20</sup> Y. Saito, K. Inomata, and K. Yusu, *Phys. Rev.* **B52**, 6500(1995).
- <sup>21</sup> K. Inomata, Y. Saito, and S. Hashimoto, *J. Magn. Magn. Mater.* **121**, 350(1993).
- <sup>22</sup> K. Kagawa, H. Kano, A. Okabe, A. Suzuki, and K. Hayashi, *J. Appl. Phys.* **75**, 6540(1994).
- <sup>23</sup> G. Rupp, and H.A.M. van den Berg, *IEEE Trans. Magn.* **29**, 3102(1993).
- <sup>24</sup> H.A.M. van den Berg and G. Rupp, *IEEE Trans. Magn.* **30**, 809(1994).
- <sup>25</sup> G. Rupp, and K. Schuster, *J. Magn. Magn. Mater.* **121**, 416(1993).
- <sup>26</sup> H. Ueda, O. Kitakami, Y. Shimada, Y. Goto, and M. Yamamoto, *Jpn. J. Appl. Phys.* **33**, 6173(1994).
- <sup>27</sup> R.J. Highmore, W.C. Shih, R.E. Somekh, and J.E. Evetts, *J. Magn. Magn. Mater.* **116**, 249(1992).
- <sup>28</sup> J.D. Kim, A.K. Petford-Long, J.P. Jakubovics, J.E. Evetts, and R. Somekh, *J. Appl. Phys.* **76**, 6513(1994).
- <sup>29</sup> H. Kano, K. Kagawa, A. Suzuki, A. Okabe, K. Hayashi, and K. Aso, *Appl. Phys. Lett.* **63**, 2839(1993).
- <sup>30</sup> Y.G. Yang, R.A. Johnson, and H.N.G. Wadley, *Acta Mater.* **45**, 1455(1997).
- <sup>31</sup> X.W. Zhou, and H.N.G. Wadley, *Surf. Sci.* **431**, 42(1999).
- <sup>32</sup> X.W. Zhou, and H.N.G. Wadley, *Surf. Sci.* **431**, 58(1999).
- <sup>33</sup> X.W. Zhou, and H.N.G. Wadley, *J. Appl. Phys.* **87**, 8487(2000).
- <sup>34</sup> X.W. Zhou, S. Subha, and H.N.G. Wadley, in preparation.
- <sup>35</sup> H.N.G. Wadley, W. Zou, X.W. Zhou, J.F. Groves, S. Desa, R. Kosut, E. Abrahamson, S. Ghosal, A. Kozak,

- and D.X. Wang, *Mat. Res. Soc. Symp. Proc.* **538**, 323(1999).
- <sup>36</sup> W. Zou, H.N.G. Wadley, X.W. Zhou, D. Brownell, S. Ghosal, and R. Kosut, submitted to JVST.
- <sup>37</sup> M.S. Daw, and M.I. Baskes, *Phys. Rev.* **B29**, 6443(1984).
- <sup>38</sup> R.A. Johnson, *Phys. Rev.* **B39**, 12554(1989)
- <sup>39</sup> H.N.G. Wadley, X.W. Zhou, R.A. Johnson, and M. Neurock, *Prog. Mater. Sci.* **46**, 329(2001).
- <sup>40</sup> X.W. Zhou, H.N.G. Wadley, R.A. Johnson, D.J. Larson, N. Tabat, A. Cerezo, A.K. Petford-Long, G.D.W. Smith, P.H. Clifton, R.I. Martens, and T.I. Kelly, submitted to Acta Mater.
- <sup>41</sup> X.W. Zhou, and H.N.G. Wadley, *J. Appl. Phys.* **84**, 2301(1998)
- <sup>42</sup> M. Parrinello, and A. Rahman, *J. Appl. Phys.* **52**, 7182(1981).
- <sup>43</sup> X.W. Zhou, and H.N.G. Wadley, *J. Appl. Phys.* **87**, 553(2000)
- <sup>44</sup> T.L. Hylton, K.R. Coffey, M.A. Parker, and J.K. Howard, *J. Appl. Phys.* **75**, 7058(1994).
- <sup>45</sup> W. Zou, H.N.G. Wadley, X.W. Zhou, R.A. Johnson, D. Brownell, submitted to Phys. Rev. B
- <sup>46</sup> *Metal Reference Book*, 5th ed. edited by Smith, C. J. (Butterworth, London, 1976)

# Drivers, Accelerators, and Inhibitors for Solid State Drive Markets

San Diego 11/7-8

S 65929

236

## Introduction

Ext. direct storage

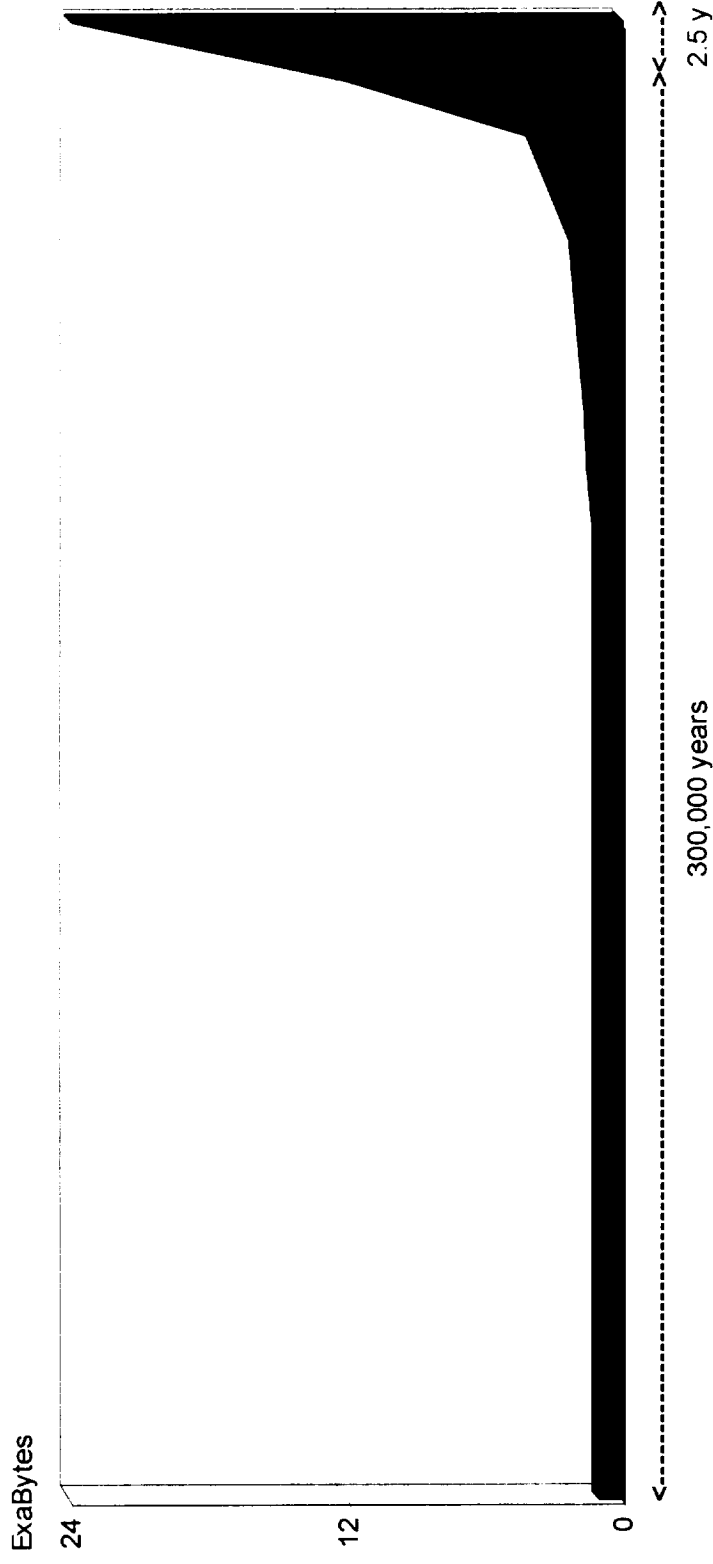
Ext. indirect storage

HDD vs. SSD

Applications

Conclusions

## Storage needs forecast



- Exa =  $10^{12}$
- Storage need driven by continuous industry developments
  - Computers – new computing architectures (distributed computing, pervasive computing)
  - Communications – Internet, exponential growth of data communications
  - Consumer – need for local data storage

## Introduction

Ext. direct storage

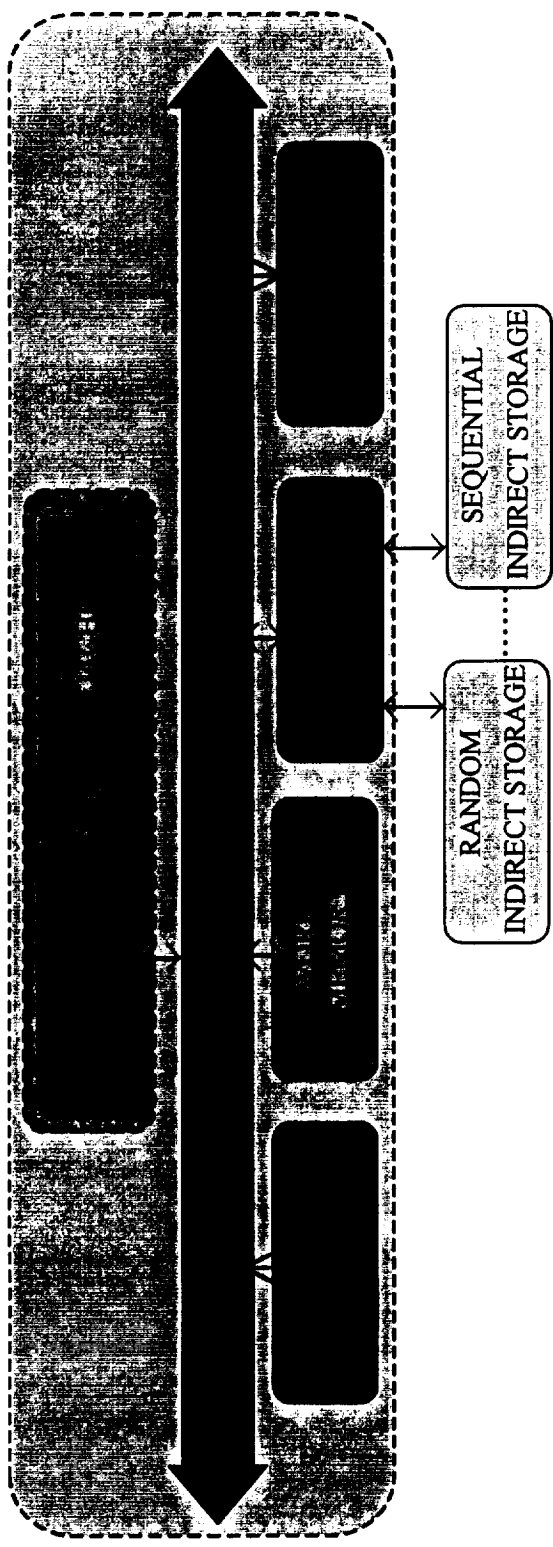
Ext. indirect storage

HDD vs. SSD

Applications

Conclusions

## Direct vs. indirect storage



- Direct memory – fast, high CPU overhead, high cost
  - Cell phones, set-top boxes, cameras, camcorders, ....
- Indirect memory – slow, low CPU overhead, low cost
  - Solid State Drives

Introduction

Ext. direct storage

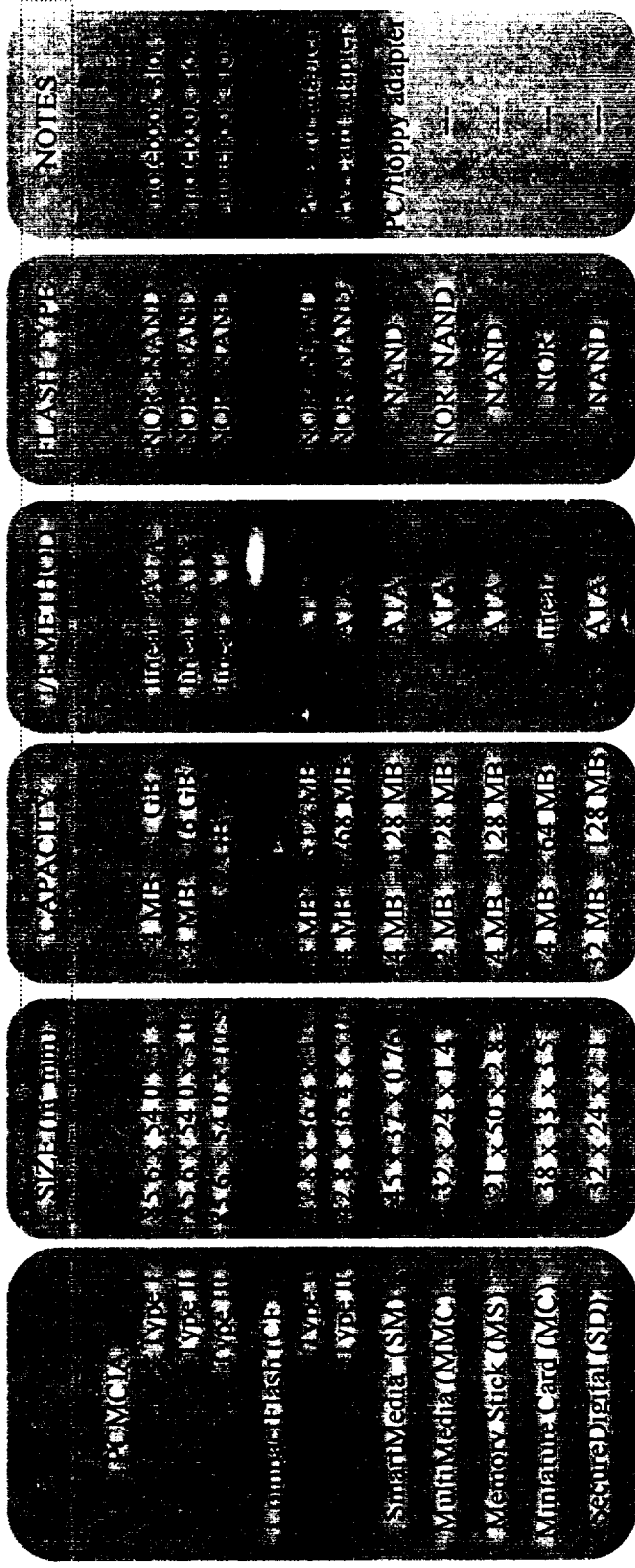
Ext. indirect storage

HDD vs. SSD

Applications

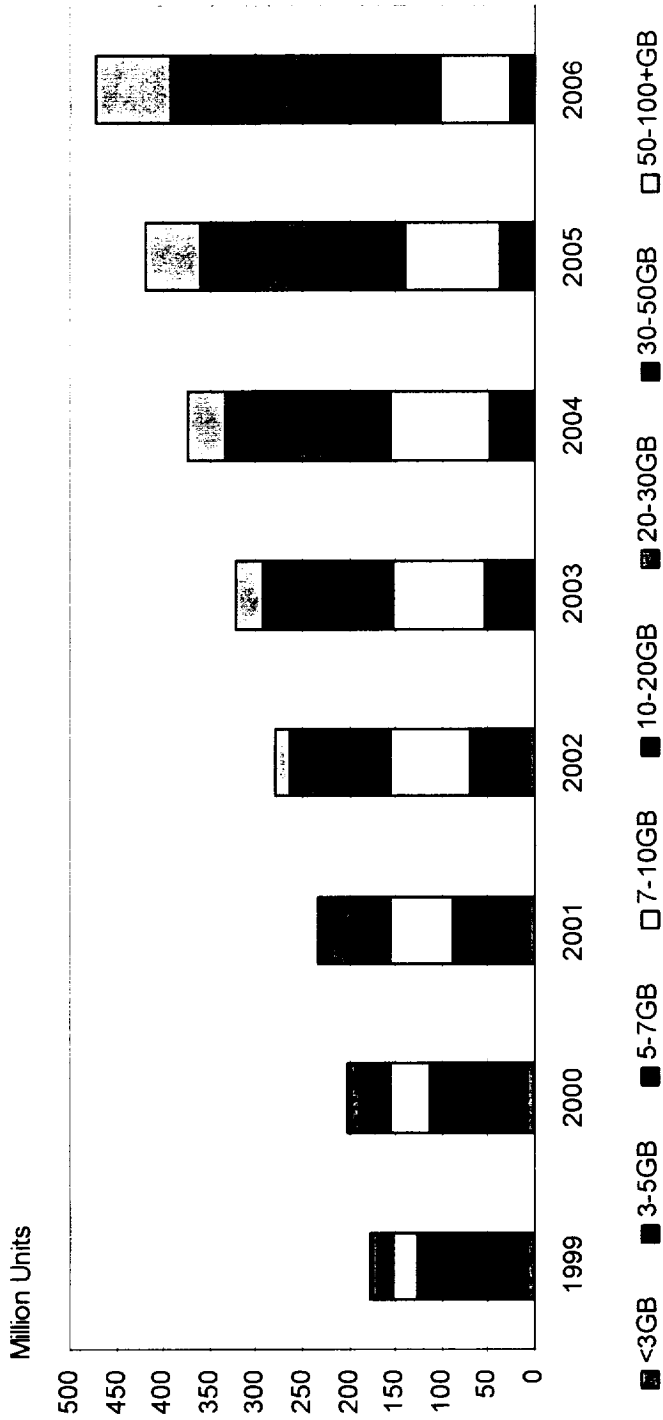
Conclusions

# Memory cards



- First memory cards – battery backed-up DRAM or SRAM
- Current solution of choice– Flash
- Most cards – linear memory extensions
- Memory and functional expansions for consumer products
- Wide variety of products – need for market consolidation

# HDD market structure



- Average storage costs
  - 1991 – 5.23 \$/MB
  - 1997 – 0.10 \$/MB
  - 2001 – 0.022 \$/MB
- Average capacities
  - 1991 – 145 MB
  - 1997 – 2.65 MB
  - 2001 – 9 GB
- Increasing need for medium capacity (10-20 GB) and mobile market (2.5”) drives



Introduction

Ext. direct storage

**Ext. indirect storage**

HDD vs. SSD

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## Solid state storage – performance assessment

$$\text{Figure of Merit} = \frac{\text{Dens} \times \text{Perf} \times \text{Env} \times \text{Rugg} \times \text{MTBF} \times \text{Dens P} \times \text{Perf P}}{\text{Cost}}$$

- Magnetic storage – reference for semiconductor storage
  - Technical parameters
    - Dens = Density
    - Perf = Performance (data transfer rate)
    - Env = Environmental characteristics (e.g. temperature)
    - Rugg = Ruggedness / shock resistance
    - MTBF = Mean time before failure
  - Market parameters
    - Cost = Performance premium
    - Perf P = Performance premium
    - Dens P = Density premium

Introduction

Ext. direct storage

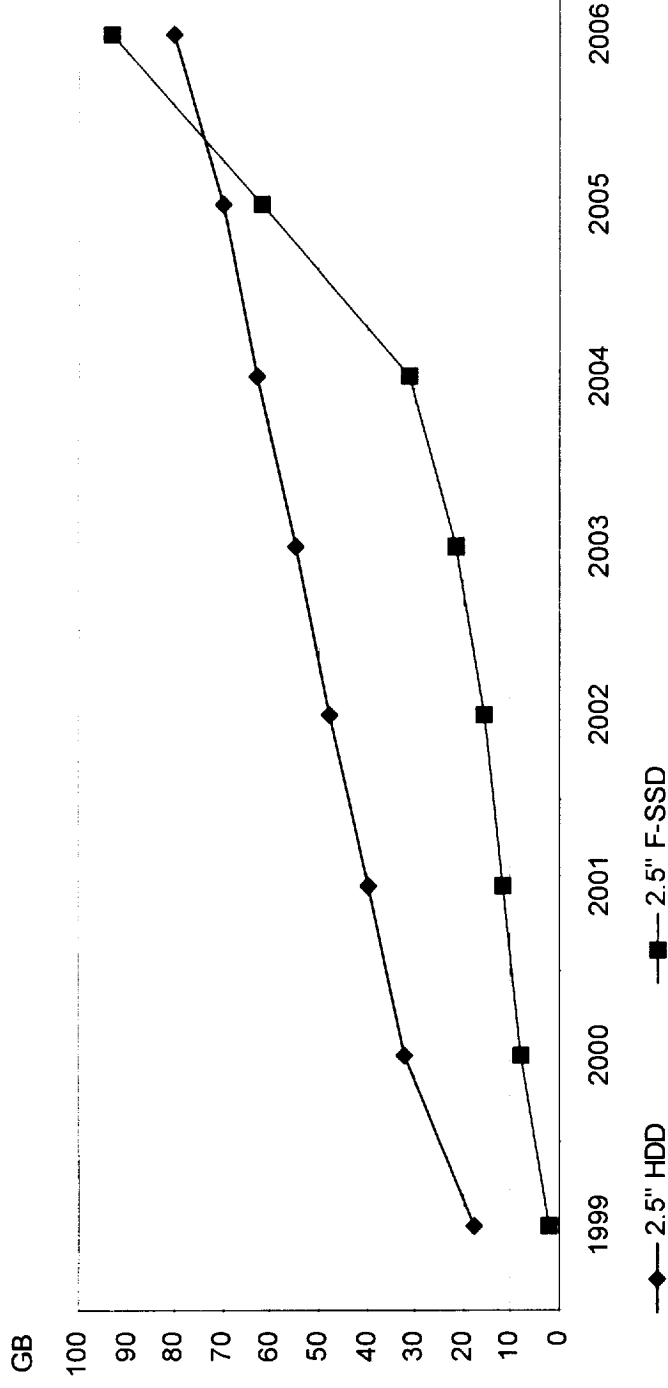
Ext. indirect storage

**HDD vs. SSD**

Applications

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Density



- F-SSD density poised to outperform HDD for standard form factors

- Increasing Flash memory density
- MLC

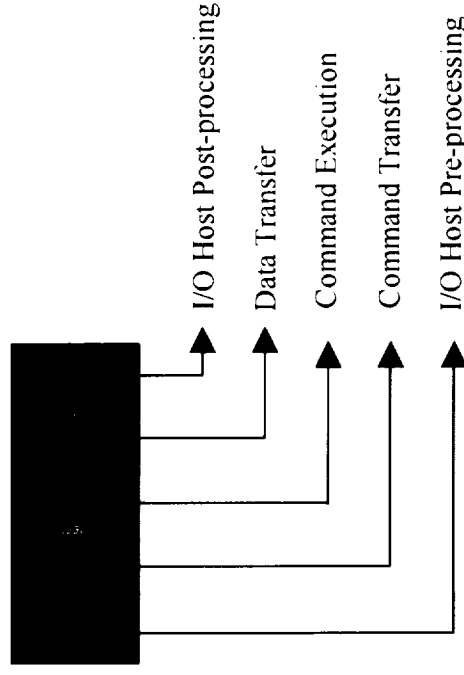
# HDD Performance – Media and interface transfer rate

$$\text{Media Access Time} = 1 / \text{Media Transfer Rate}$$



# SSD Performance – Media and interface transfer rate

$$\text{Media Access Time} = 1 / \text{Media Transfer Rate}$$



Introduction

Ext. direct storage

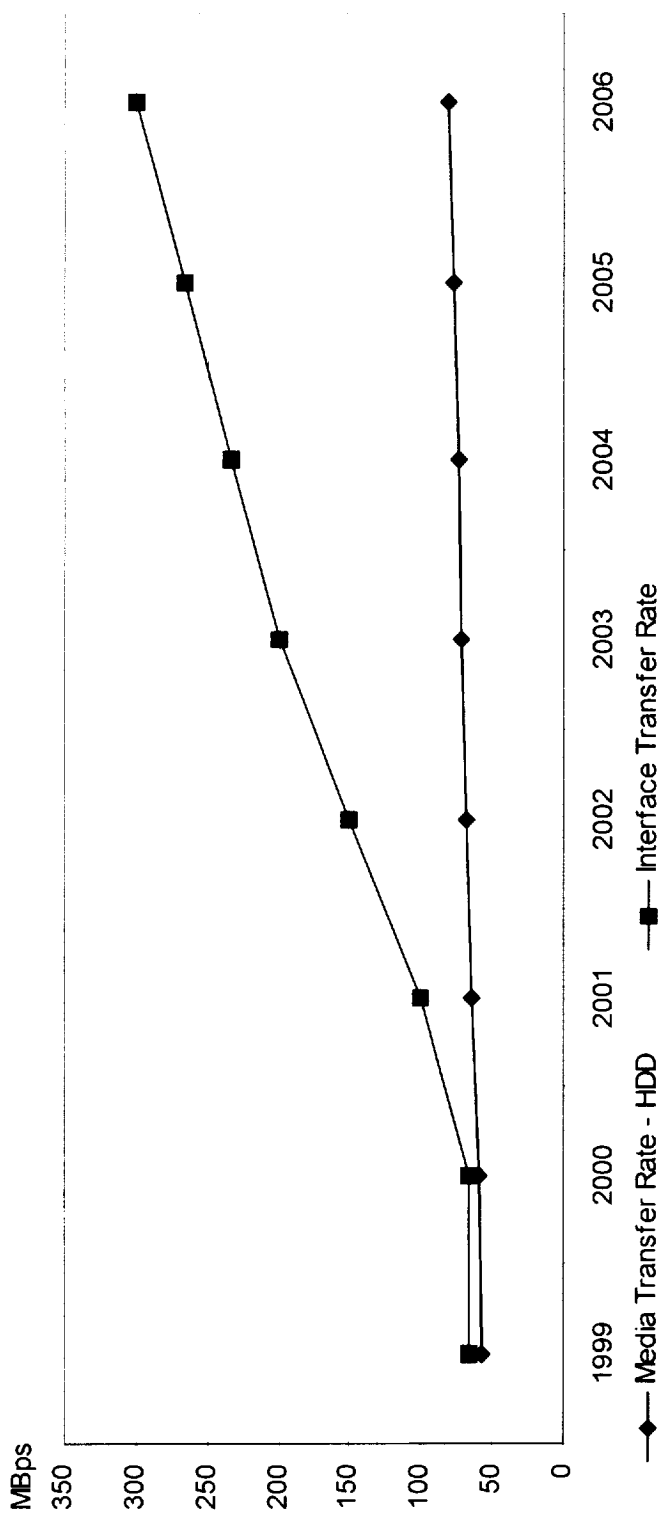
Ext. indirect storage

**HDD vs. SSD**

Applications

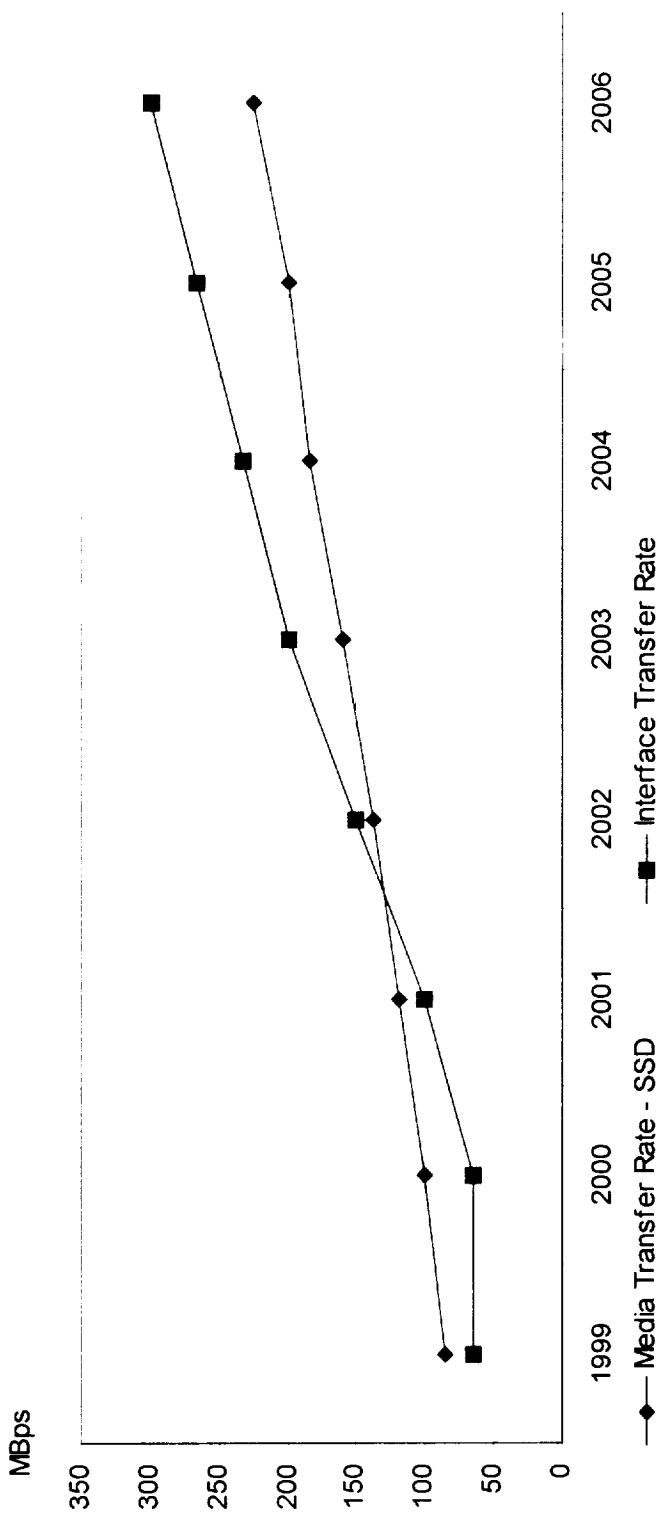
Conclusions

## HDD – Media vs. interface transfer rate



- Small increase of MTR
  - Steady improvements of platter rotation and head moving speeds
  - Mechanical systems offer limited improvement potential
- ITR increase due mainly to proliferation of Fibre Channel
- InfiniBand represents additional ITR improvement potential
- MTR – ITR gap = weakest performance link

# SSD – Media vs. interface transfer rate



- Currently, MTR superior to ITR
- Crossover in 2002
- MTR – ITR gap projected remain small
- Additional gap reduction potential (increased parallelism and internal buffering )

Introduction

Ext. direct storage

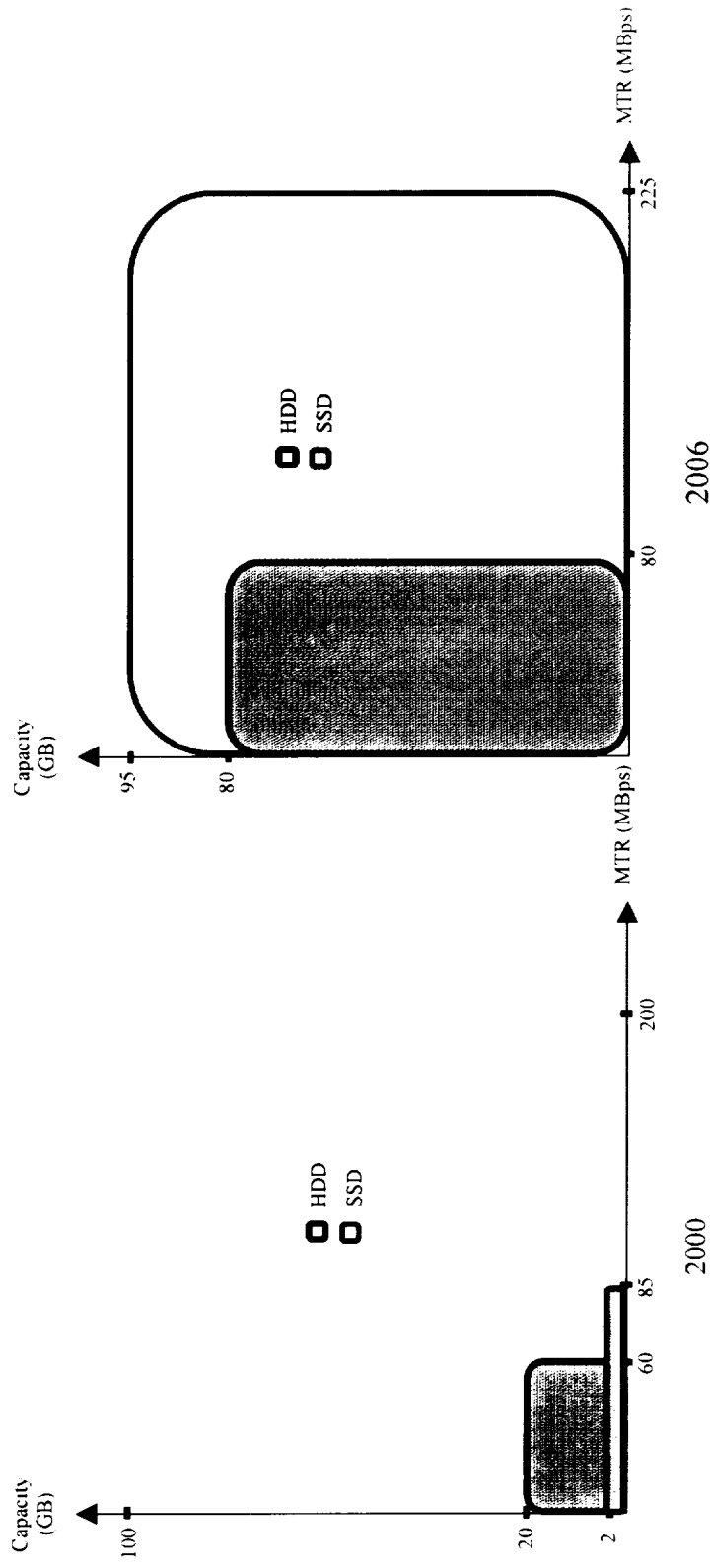
Ext. indirect storage

**HDD vs. SSD**

Applications

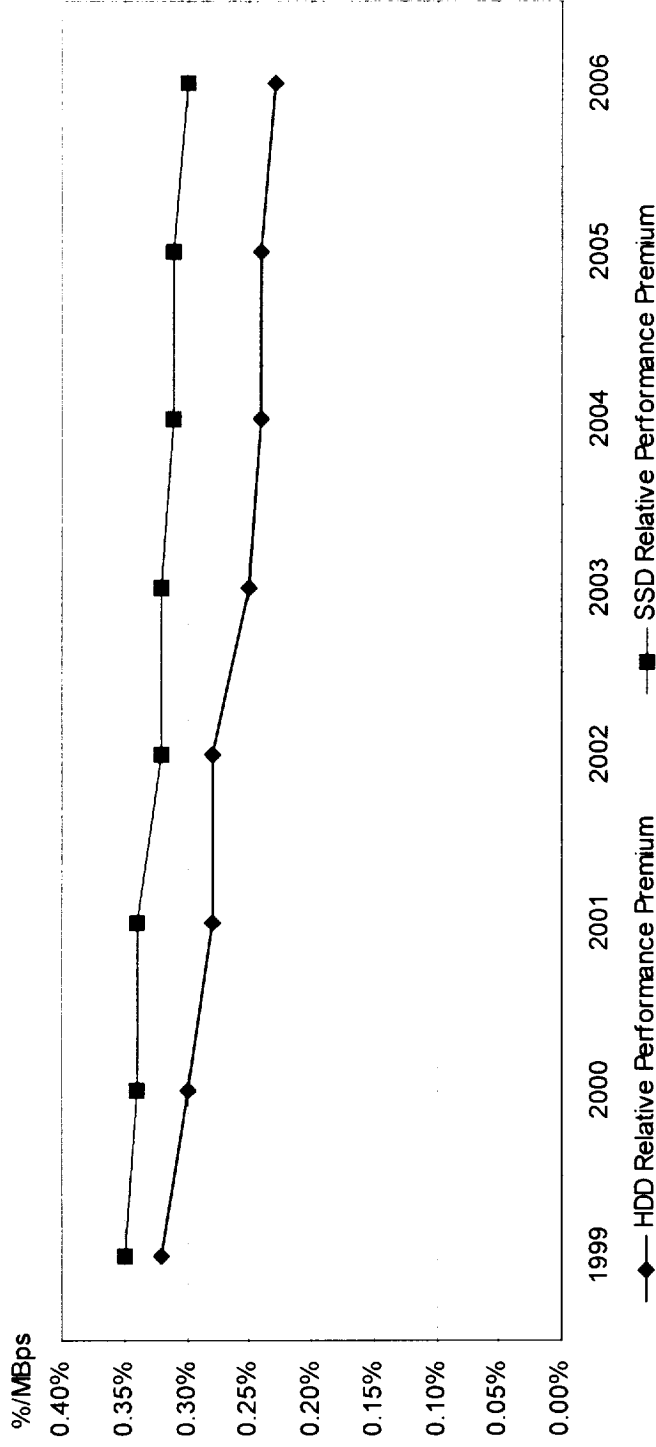
Conclusions

## Product positioning (2.5" drive)



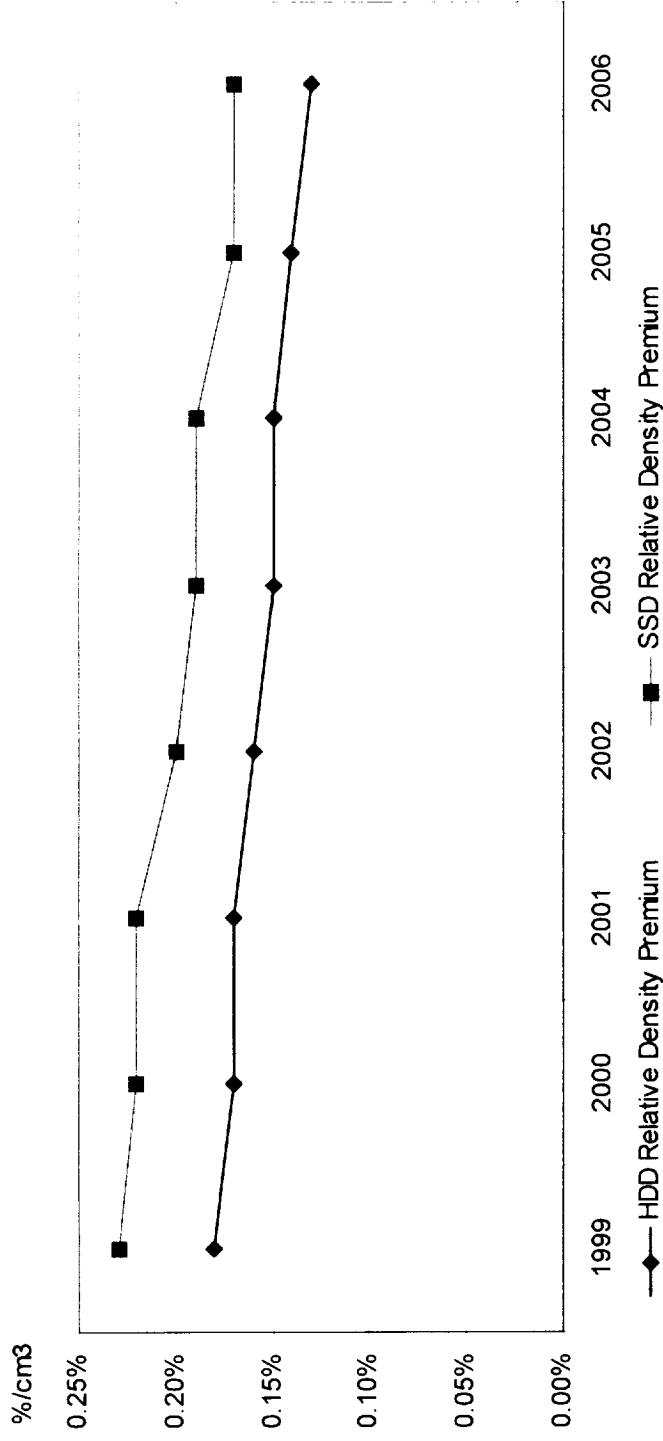
- Capacity improvement potential
  - SSD outperforms HDD approx. 12:1
- Performance improvement potential (in addition to an already 2:1 performance superiority – 120 MBps vs. 64 MBps)
  - SSD outperforms HDD approx. 2:1

# Performance premium



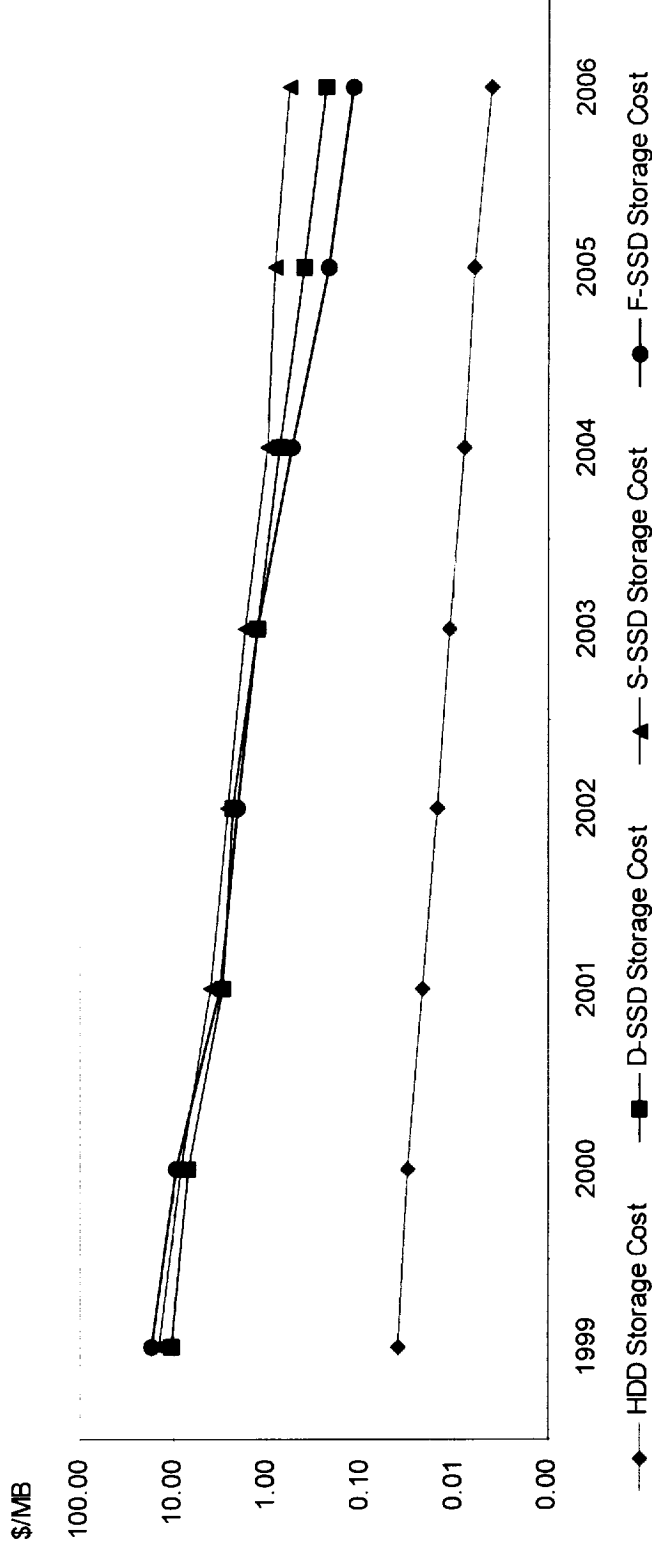
- Represents the premium commanded by every additional MBps above the market average
- SSDs command higher premiums and a slower decline over time

# Density premium



- Represents the premium commanded by every additional MB in a standard form factor above the market average
- SSD premium decreases slightly faster – improvement is expected

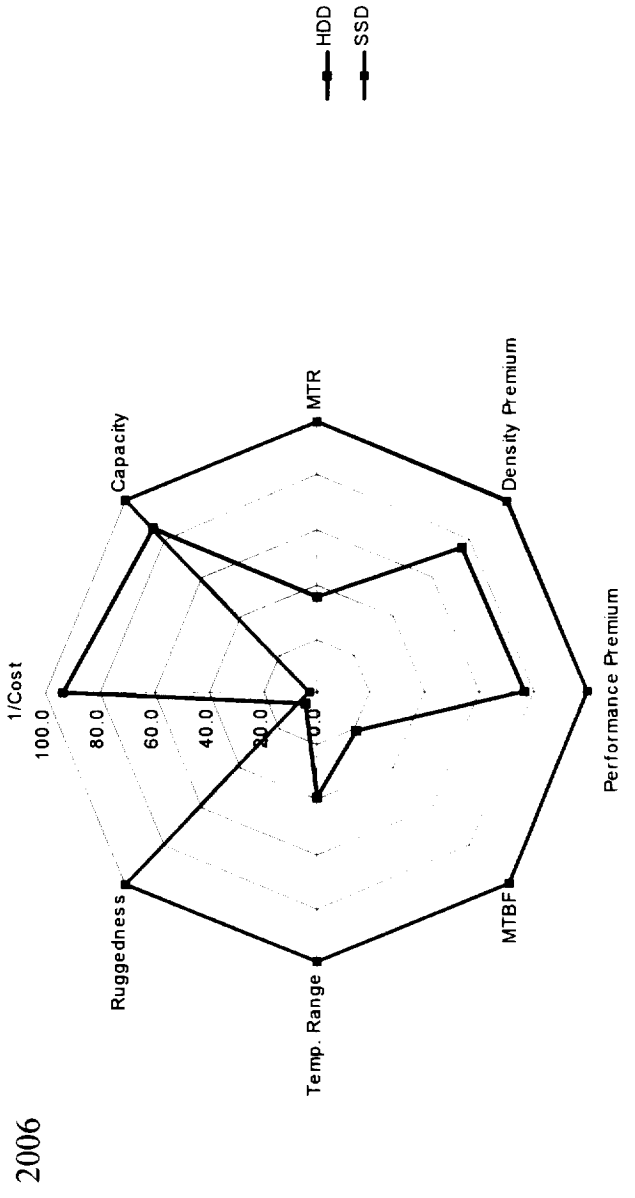
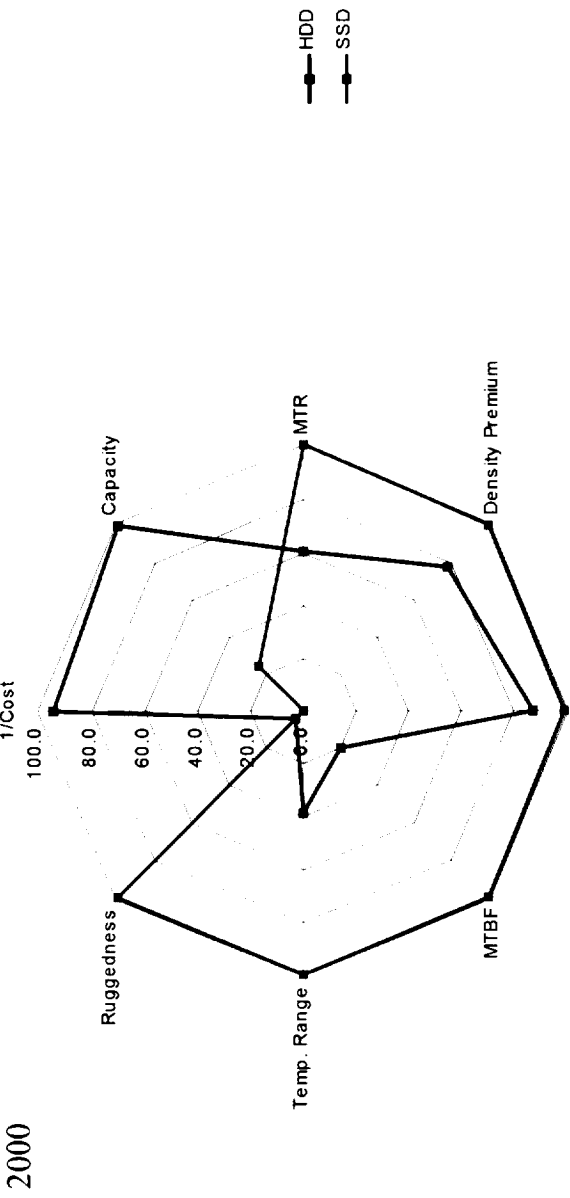




- Logarithmic scale!!
- HDD cost performance forecast to maintain superiority
  - 2001 ratio - 141:1 (3.1\$/MB : 0.022\$/MB)
  - 2006 ratio - 30:1 (0.12\$/MB : 0.004\$/MB)
- Reducing storage cost beyond the forecast reduction remains the single most important challenge for the SSD industry

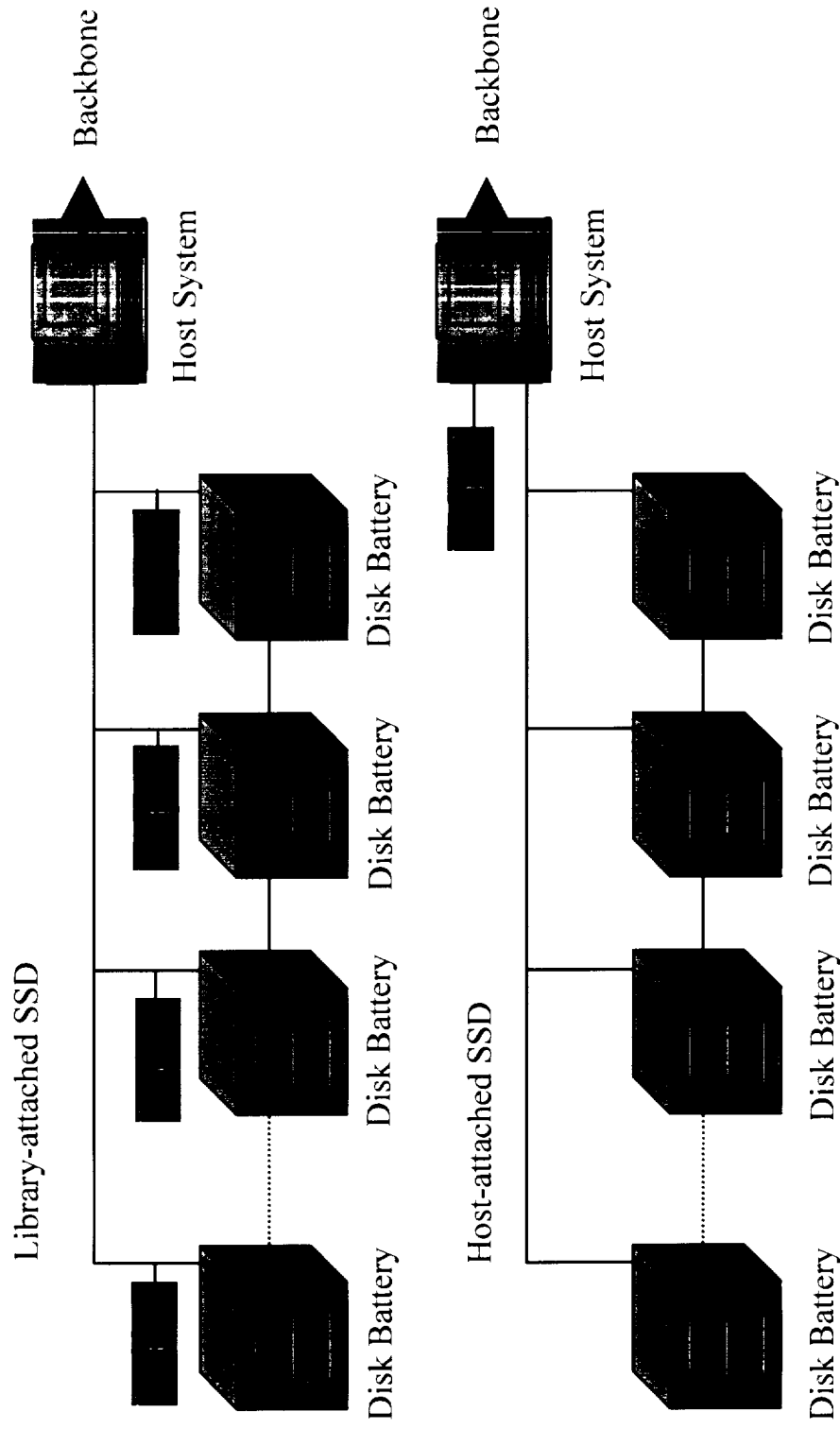
# Competitive assessment summary

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- Ext. direct storage
- Ext. indirect storage
- HDD vs. SSD**
- Applications
- Conclusions



# Data warehousing / mining configurations

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# Streaming AV configurations

Introduction

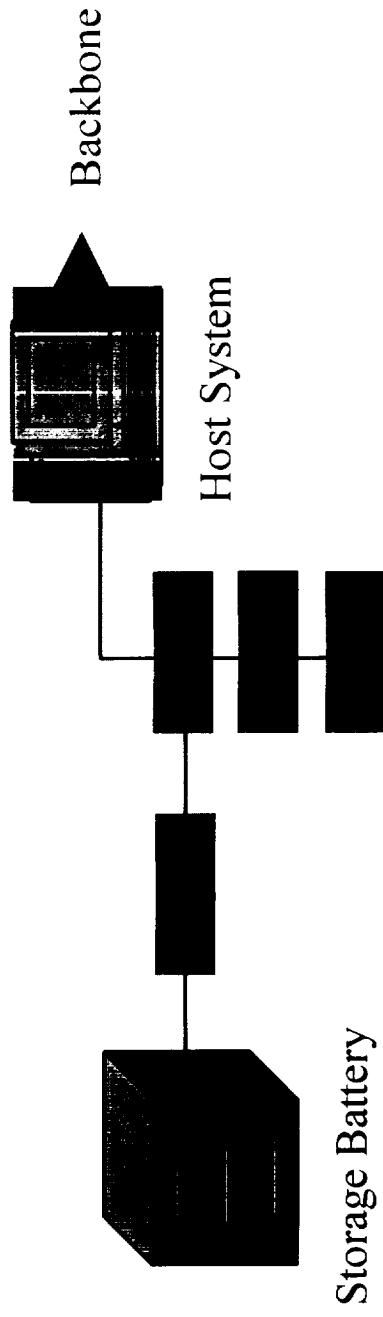
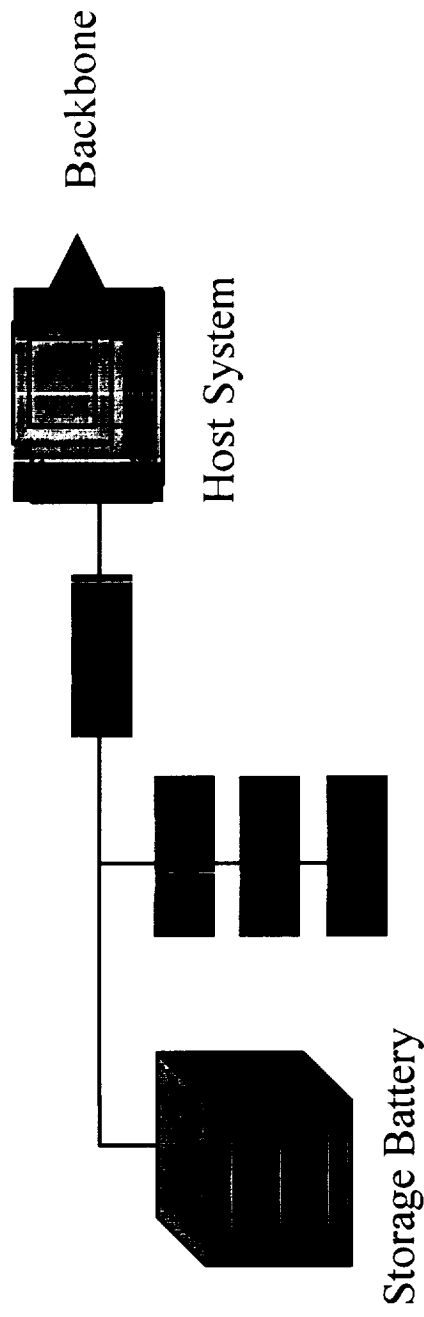
Ext. direct storage

Ext. indirect storage

HDD vs. SSD

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# RAID configurations

Introduction

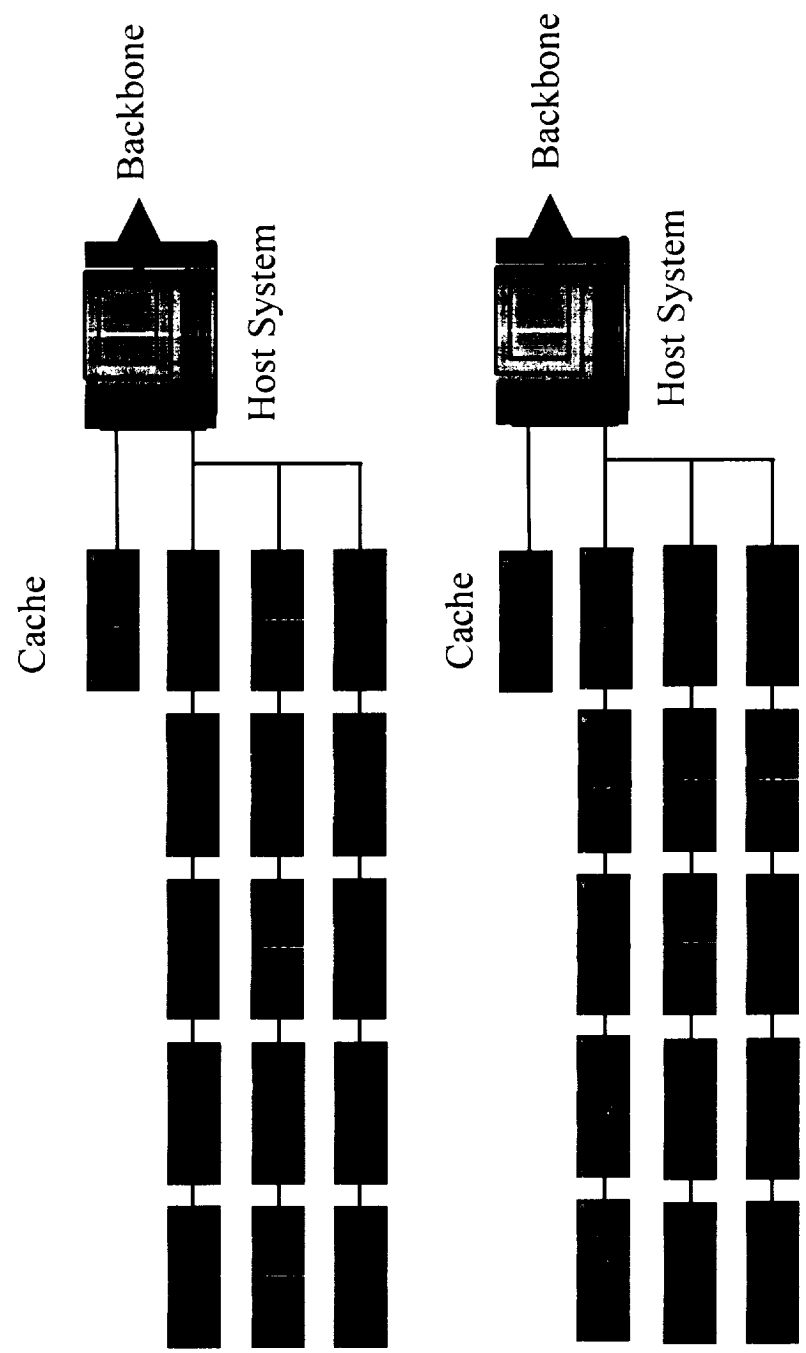
Ext. direct storage

Ext. indirect storage

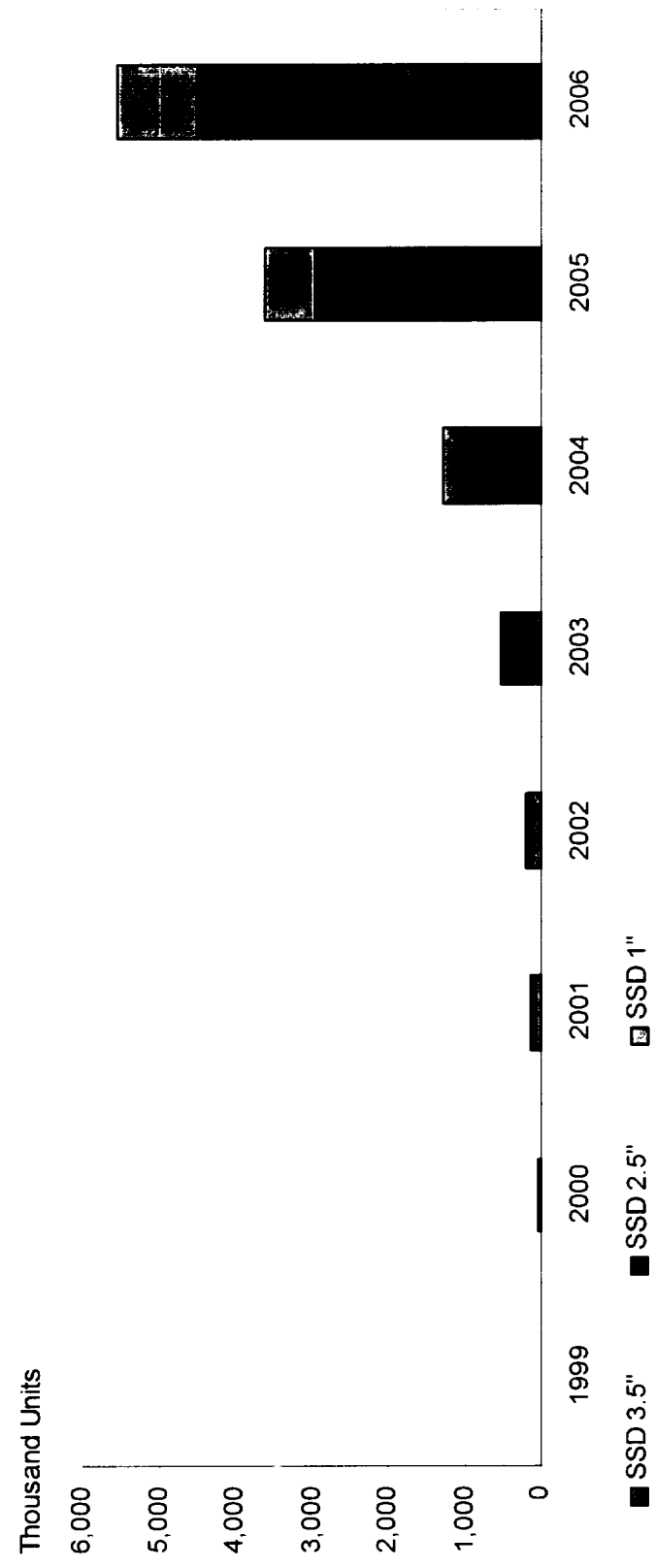
HDD vs. SSD

**Applications**

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# SSD – Total demand forecast (units)

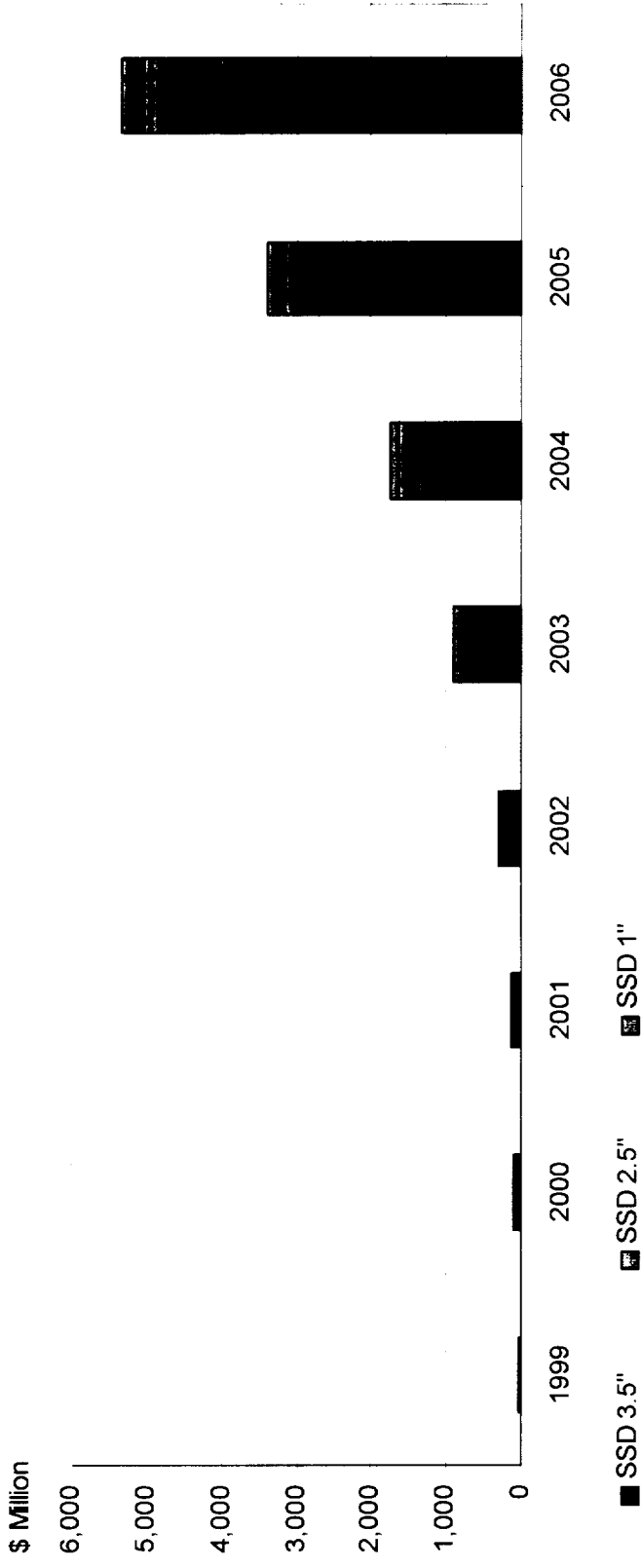


- CAGR (2001-2006)

- 3.5" - 200%
- 2.5" - 242%
- 1" - 234%
- Total - 230%

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# SSD – Total demand forecast (\$)



- **CAGR (2001-2006)**

- 3.5" - 146%
- 2.5" - 206%
- 1" - 209%
- Total - 158%

- **Average capacity ASP / CAGR (2001-2006)**

- -21%

# The ideal NV memory for SSD

- Endurance level:  $10^{12}$
- Energy consumption: 0.01 pJ/bit
- Access time: lowest possible, maximum 50ns
- Cost: HDD level
- Data retention: min. 10 years
- Radiation hard
- Capability to integrate logic



Introduction

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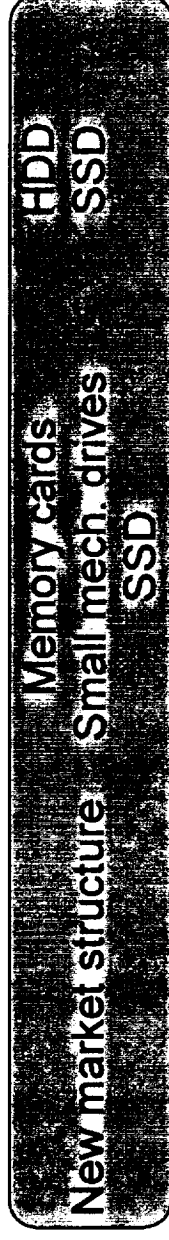
**Conclusions**

# Conclusions

- **Changing market structure**
  - Mechanical storage penetrates small density storage market
  - Semiconductor storage penetrates high density storage market

Direct storage  
(small density)

Indirect storage  
(high density)



- **SDD business model**
  - HDD complement
  - Not HDD replacement
- **SSD market – only marginal replacement of HDD market**

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Conclusions

- SSD market challenges:
  - Mechanical magnetic storage cost
    - 50% decrease every 18 to 24 months
  - Semiconductor storage cost
    - Reduce the cost gap
    - Keep a similar pace
  - Superior performance can offset a 3 to 5 times higher storage cost

# Non Volatile Memory Systems Design: Concept to Reality and Trades along the Way

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**Abstract**—SEAKR Engineering is engaged in designing and building memory systems using non-volatile memory electronics. Primary targeted applications are highly reliable spacecraft data recorders, aircraft reconnaissance recorders, and board level products. This paper identifies the steps that SEAKR takes in determining a preferred system level solution and its implementation. Some key obstacles encountered in past programs are identified along with their solutions.

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- 3. MEMORY TECHNOLOGY SELECTION
- 4. DEVICE QUALIFICATION
- 5. X2000 NVMS CASE EXAMPLE
- 6. ACKNOWLEDGMENTS

## 1. INTRODUCTION

Due to their low cost per bit storage, mechanical based data storage systems such as tape recorders and disk drives have historically been the technology of choice for remote data collection. Recent advancements in non-volatile solid state memory technology have opened opportunities for 100% solid state based solutions. Nowhere is this more accepted than for applications where maintenance is unavailable or mission failure is quite costly. Key examples of such missions are spacecraft and aircraft memory systems.

While solid state electronics are inherently more reliable than mechanical based systems, a number of issues must be addressed before usage of solid state can be assured. One of the most critical items to address for spacecraft applications are radiation effects and their impacts on non-volatile solid state memories. JPL's X2000 is such a program where non-volatile memory is to be used in a Non Volatile Memory Slice (NVMS) under development by SEAKR Engineering.

## 2. MISSION TRADES

Each application has its own unique mission critical items. These critical items can be categorized as either performance based or survival based. Performance based mission critical specifications include items such as data rate, data access time, operational scenario, operational temperature range, power consumption, storage capacity, size and mass. Survival specifications are primarily environmental including radiation, shock, vibration, temperature extremes, salt/fog, and dust. Most of these critical mission items are extracted directly from procurement documents, while some must be experimentally derived.

Once mission critical issues are identified, a design team commences a series of inter-related trades in an attempt to achieve a paper concept that satisfies mission performance and survival requirements at the lowest cost & risk. At SEAKR, our preliminary trade teams are composed of electrical design engineers, mechanical design engineers, component engineers, and the technical program manager.

Trades that are constantly performed for memory technology are performance vs. cost vs. risk. For instance, the newest memory technology consistently provides higher performance over earlier generations. However, it is rare that the newest state-of-the-art memory technology does not need a costly qualification effort. Furthermore, the immaturity of new technology carries a risk that some unknown mechanism leads to premature device failure in the intended environment. As a rule of thumb, the latest state-of-the-art technology fairs poorly in these trades unless performance cannot be achieved with more mature technology.

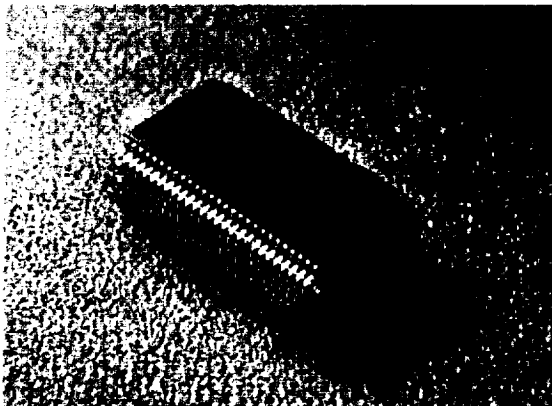
On the other hand, if the intended product that the memory technology is targeted for, has a long production life, then the latest technology becomes preferred. This reversal of trade results is primarily due to cost. For long running production programs, obsolescence of mature technology becomes assured demanding a qualification at some point as newer technology is inserted.

### 3. MEMORY TECHNOLOGY SELECTION

Historically, non-volatile memory technology has been more expensive, with lower performance, than volatile memory technologies. These two critical facts have limited technology trades such that non-volatile memory technology is only considered for those applications that require data retention when powered down, or for extremely large capacity systems that have very low operational power consumption restrictions.

Today some non-volatile memory technologies boast single device capacities equal to volatile memory with costs per bit comparable. Technology selection is now made more on performance and intended application rather than capacity and cost. In general, high data rate systems with extensive read/write cycles are still best satisfied with volatile memory technologies.

Once a memory technology has been identified, how the device is to be packaged is addressed. Standard commercial packaging is universally preferred if possible, however, system mass limitations often dictate denser solutions than standard packaging can achieve. In such cases, stacked memory can be an attractive alternative. SEAKR's preferred approach for stacked memory is to procure stacked solutions from one of the many specialty packaging houses, although in-house stacking is used when extensive customer involvement is anticipated.



### 4. DEVICE QUALIFICATION

If not previously qualified, once a preferred memory technology and packaging approach has been identified, a qualification program is initiated. Device qualification is primarily focused on demonstrating robustness and ability to satisfy survival requirements. In general, a qualification program follows established military

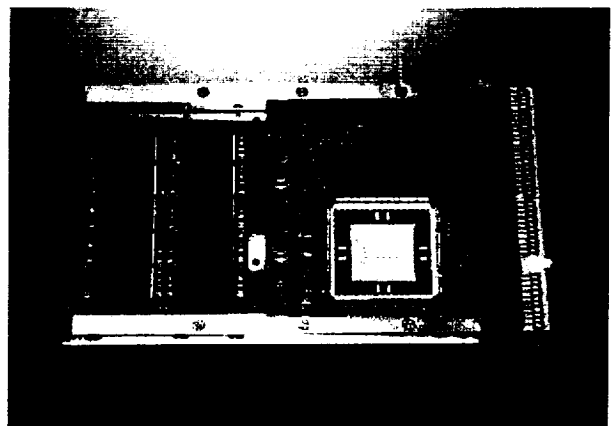
specifications. More recently, automotive industry standards have begun to be used to augment, and in some cases replace historical approaches to device qualification.

Since most of SEAKR Engineering's applications are high-rel, our device qualifications are more extreme than desk top or benign applications require. A typical device qualification program includes 1000 hours of elevated temperature life testing, 100 temp cycles from 55° C to +150° C, solderability, salt spray, shock, outgassing, and resistance to solvents.

In addition to the above qualifications tests for all high rel applications, for spacecraft applications, the most interesting survival requirements arise due to the radiation environment and long mission life.

### 5. X2000 NON-VOLATILE MEMORY SLICE CASE EXAMPLE

In the spring of 1999, SEAKR Engineering was selected to develop and manufacture a number of 256 Mbyte non-volatile memory boards compliant to the Compact PCI bus protocol. Missions targeted by JPL for use of the X2000 NVMS include a science collecting experiment around Jupiter's moon Europa. The radiation environment at Europa is extreme with ionizing radiation exposure for the mission exceeding hundreds of thousands of rads Si. In addition, high energy, heavy ion particle bombardment is also present. Our task was to identify a solution and qualify a non-volatile memory technology that will survive this extreme environment.



Initial technology evaluation efforts targeted technologies with inherent immunity to radiation effects. These technologies included GMRAM, specifically radiation hardened EEPROM, and FRAM. Unfortunately, these technologies were low in density, extremely expensive, or carried a high risk factor due to immaturity. Our technology trade then shifted to more commercial

technologies with Flash EPROM emerging as a likely candidate. We selected several different Flash EPROM devices from several different manufacturers and with assistance from JPL performed radiation testing. These testings included exposing devices to Total Ionizing Dose (TID) radiation and heavy ions. Results were not encouraging as Flash EPROM devices showed TID radiation failures occurring at levels which were orders-of-magnitudes less than the expected environment. Furthermore, some of the Flash devices revealed sensitivity to destructive latchup induced by high-energy particles.

Under normal circumstances, the sensitivity of the Flash device would have disqualified them from further consideration, however, the performance and cost impacts of using other approaches encouraged us to continue our evaluation. Three strategies were undertaken in an attempt to qualify the flash device for X2000:

- 1) Closer examination of the true environment that the devices would be in.
- 2) Further testing to determine if any operational constraint or system design approach might improve tolerance.
- 3) Modification of the environment through the addition of shielding material in an attempt to lessen ionizing radiation exposure.

Once it was determined that the Flash devices could not achieve mission TID requirements, our customer, JPL, performed detailed sector and shadowing analyses on the spacecraft and X2000 processor that our NVMS would be inserted into, and determined a lower TID exposure level than originally expected. In conjunction with this effort, we resumed radiation testing while modifying the operational mode of the devices. We determined that by power cycling the devices, rather than maintaining them at 100% duty cycle, their tolerance to TID could be dramatically improved. Furthermore, we determined that by inserting current limiting resistors, destructive latchup could be prevented on some manufacturer's devices. With this improved information, we were able to identify that by adding additional spot shielding at the Flash device, we could achieve mission survivability.

In addition to radiation induced device failures, the Flash devices have a wear-out mechanism that limits life and they have demonstrated random loss of data known as erratic bit errors. For a mission critical function such as our NVMS, such loss of data is unacceptable. Our solution was to develop a novel error detection and correction (EDAC) circuit design which fully corrected large block failures as well as the erratic bit errors and soft single event upsets. Diagnostic routines can be implemented by the user to determine if the erroneous data is due to a hard permanent device failure or just a random single event effect. For soft single event effects, the data can be corrected and rewritten effectively

removing the error. For hard failures, the corrected data can be written into unused new memory locations and the old failed memory "mapped" out of usable address space.

## 6. ACKNOWLEDGMENTS

SEAKR Engineering would like to express our appreciation to Valerie Thomas, Karl Strauss, Audrey Doran, Gary Swift and the rest of the JPL X2000 NVMS team for their assistance and teamwork in successfully developing the X2000 NVMS.

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## ***SESSION #4: Applications***

Thursday, November 8, 2001

10:50 AM – 12:00 Noon

Chair: *S. Anderson*, SEAKR Engineering

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- 10:50 AM Experiences in Qualifying a Commercial MNOS EEPROM for Space;  
*E. King, R. Laco, G. Eng, and M. Leung*, The Aerospace Corporation
- 11:10 AM Neo-Stacking of Packaged Flash Memory; *K. Gann*, Irvine Sensors  
Corporation
- 11:30 AM High Speed MRAM Buffer for High Capacity Non-Volatile Shock  
Recorders; *R. Sinclair and R. Beech*, NVE Corporation

# Experiences in Qualifying a Commercial MNOS EEPROM for Space

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**Abstract** Qualifying a commercial Non-Volatile Memory (NVM) component for space poses several challenges: detailed information about the process and design is not likely to be available, long-term reliability data are uncertain or insufficient, little, if any, radiation data exist, and the data retention requirement for a space application generally exceeds ten years. In this paper, we describe our experiences in qualifying a commercial 1-Mbit EEPROM (the Hitachi HN58C1001) for space. Since the unique attribute of a NVM is its ability to retain stored data over long periods of time with no power applied to the component, our work focused on determining the data retention lifetime and developing a procedure to screen potential early failures from the part population.

The MNOS transistor is programmed to a  $1$  by applying 15 V across the gate insulator, 5 V to the gate, and about  $10$  V to the body (well). Under this bias condition, electrons are injected into the gate insulator from the channel, where some of them are trapped (stored) in the electron traps that are inherently found in silicon nitride. To erase this  $1$  (program a  $0$ ), the  $10$  V bias is applied to the gate and 5 V is applied to the well. Under this bias condition, holes are injected into the gate insulator from the silicon substrate where they neutralize the trapped electrons. The  $10$  V bias is generated by an on-chip negative high-voltage generator circuit. The erase/write time is about 10 ms, and is controlled by an on-chip timer. A sense amplifier discriminates between the written and erased ( $1$  and  $0$ ) states, respectively.

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## 1 INTRODUCTION

The HN58C1001 is a 128k by 8 bit electrically erasable and programmable read-only memory. The part is fabricated using a CMOS process with the addition of a Metal-Nitride-Oxide-Silicon (MNOS) transistor that is used as the data storage element [1]. The MNOS transistor is schematically illustrated in Figure 1. A data bit is stored in the MNOS transistor in the form of charge that is trapped in the silicon nitride film that is formed above the channel. The presence or absence of charge results in a change in threshold voltage between two states that are defined as a  $1$  and  $0$ . The transistor is interrogated by detecting the channel current that flows when the gate voltage is set at 0 V.

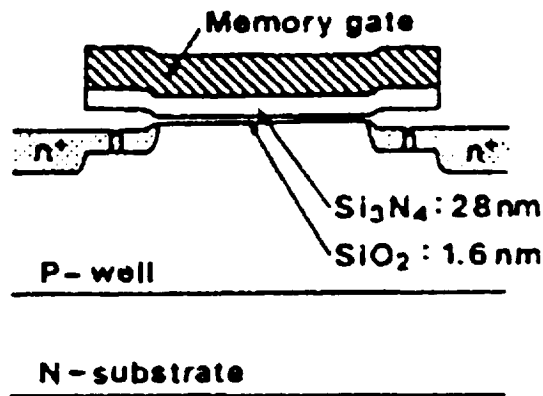


Figure 1 Schematic illustration of the type of MNOS memory transistor used for the HN58C1001

The memory exhibits a high degree of non-volatility due to the retention of the trapped charge in the gate insulator even when the power to the device is turned off. The memory transistor is not totally nonvolatile, however, because the trapped charge (whether holes or electrons) leaks out of the nitride over time, resulting in the decay of the programmed threshold voltage. The dominant charge decay mechanism for the MNOS transistor has been

found to be thermal emission of the charge out of the traps [2]. The retention of the net trapped charge can also be impacted by an exposure to ionizing radiation, because the electron-hole pairs which are created by the radiation can also become trapped, thereby changing the threshold voltage.

## 2. EXPERIMENT

There are three unique characteristics of an MNOS memory device: programming speed, data retention, and endurance. In the primary application under consideration here, data retention was the key characteristic of interest, since the memory was to be written at the beginning of the mission (before any aging or radiation-induced degradation of the part had occurred) and no rewriting of the memory was planned during the mission. The purpose of our experiments was to verify that these memory components were capable of retaining data throughout the mission and to develop a test that could be used to eliminate parts from the part population that were prone to early failure. As a result, we conducted aging tests, total ionizing dose radiation tests, and a variety of electrical tests on the parts.

*Accelerated Aging Tests.* The usual method to determine a device-aging characteristic of a component is to attempt to accelerate the failure mechanism by thermally stressing the part in an oven. Temperature accelerated aging assumes that the intrinsic device life is limited by a thermally accelerated process that can be characterized by an activation energy, and that no intervening processes occur between the accelerated aging temperatures and the lower device use temperatures that would cause the extrapolation of the high temperature data to the low operating temperatures to be incorrect. Based on both the intended application and the objective of isolating the data retention lifetime of the MNOS transistor from any aging of the peripheral circuitry, our aging tests were conducted without power being applied to the part.

The manufacturer claimed that this MNOS memory was capable of retaining data for 20 years. There were two issues with accepting this lifetime value. First, it is based on an activation energy of 1.1 eV for charge leakage from the storage transistor, whereas, it is generally acknowledged that charge leakage is characterized by a range of activation energies rather than a single value [2]. In this case, it is important to know the minimum activation energy to be able to predict that the parts will meet the data retention mission requirement with high confidence. Second, the manufacturer did not disclose the failure criteria that had been used to determine his activation energy. Because of the exponential relationship between activation energy and lifetime, even a small change in the choice of activation energy can result in a change in lifetime prediction of an order of magnitude, or more. In this work, therefore, we conducted thermally accelerated aging tests both to determine a worst-case

activation energy, and to collect degradation data that could be used to predict the data retention lifetime in the application.

Our part population consisted of 21 commercial parts in plastic (epoxy) 32-pin dual in-line packages. The parts all had the same date code. We wanted to expose the parts to a relatively high temperature to accelerate the time-to-failure and shorten the test time, however, there was a concern that the parts would fail because of the plastic package if the oven temperature was set much higher than the specified maximum storage temperature, which was only 125 C. However, tests on the plastic packaging material showed that it could withstand exposure to temperatures up to 275 C before decomposing. As a result, we felt comfortable with using a maximum temperature of 200 C in our accelerated aging tests. Therefore, since data at two temperatures are necessary to determine an activation energy, accelerating temperatures of 175 and 200 C were chosen for these aging tests. Of the 21 parts in our population, 10 were aged at each temperature and one was used as a control.

The parts were preconditioned by writing them with an alternating set of checkerboard (CKBD) and inverse checkerboard (NCKBD) patterns a total of 220 times, checking them for any failures after each write. Half were begun with a CKBD and the other half with an NCKBD. The parts were then soaked in a 150 C oven for 48 hours, and re-tested. The final pattern written into a part prior to the aging test was the inverse of the last written pattern so that there would never be more charge stored on a memory transistor in the part than that associated with a single write.

The parts that were aged at 200 C were pulled out of the oven and tested after every four hours, while the parts aged at 175 C were tested at 22 hour intervals. Toward the end of the aging tests these times were extended since no failures had been observed and it was very much desired to determine a time-to-failure from these experiments before the end of the project.

During these tests, however, no specification failures were observed for final aging times of 755 and 1305 hours at 200 and 175 C, respectively. While finding no errors was positive in some respects, these results did not provide any failure data from which to determine the activation energy or predict the lifetime at normal operating temperatures. On the other hand, we did collect parametric electrical characterization data on the parts during aging from which we could draw conclusions. In particular, the readout access time (time from chip enable assertion to valid data out) turns out to be sensitive to the charge flow through the memory transistor when it is read out. This allowed us to use measurements of the number of errors versus the chip enable access time to estimate a time-to-failure at each of our accelerated aging temperatures. Examples of this error distribution data (for



one quarter of the part's addresses) for two parts, one exposed to 200 C and the other to 175 C, are shown in Figures 2 and 3, respectively

The push out of the access time with thermal exposure can be clearly seen in these figures, although, there is still considerable margin at the times measured to when the access time would have failed the manufacturer's specification limit, which is at 150 ns. It is not obvious how to use these push out data to calculate the data retention lifetime, due to the pronounced ledges that develop over the course of aging in the error distributions. These ledges appear to be primarily due to variations in the stretch-out associated with individual Data I/O lines. For example, Figure 4 shows the error distribution for the 200 C error distribution curve measured at 533 hours that is shown in Figure 3 broken into the error distributions for each of the eight Data I/O lines. We conclude that the large ledge that occurs at 8000 errors in Figure 4 is primarily due to the behavior of the Data I/O3 line in this part. Furthermore, this ledge, in combination with one or more of the even numbered Data I/O lines (which will add to the number of failures observed for DIO3 because an even number output will tend to fail on an address for which DIO3 passes) also produces a ledge at 16,000 errors. Other variations in the access time failures between these ledges are probably due to slight differences in the propagation delays to the various memory transistors. These variations will stretch out the portions of the curves that lie between these ledges

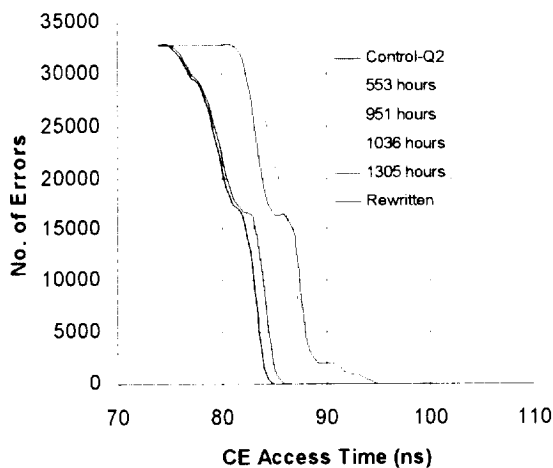


Figure 2 Number of errors in the second quarter of the memory address space for an example part versus the chip enable access time, with aging time at 200 C as a parameter

It is a good assumption that a large percentage of this observed access time stretch out is caused by charge leakage off of the MNOS memory transistors. Unfortunately, other factors are also likely to be involved in the stretch out, not the least of which might be

variations in the sense amps, whose characteristics determine how long it takes for them to determine whether the current out of the MNOS transistor is a 1 or a 0. In general, then, the stretch out in access time will be some combination of how much charge was initially stored in the memory transistor, how much charge has leaked off the memory transistor during aging, the characteristics of the sense amp associated with that memory transistor, and, probably to a lesser extent, variations in propagation delay related to the decoder circuitry and output amplifiers

To determine an activation energy for the charge leakage mechanism, data should be used for which the degradation is due solely to charge leakage. Arguably, the best we can do with the number of errors versus access time data we have is to estimate the number of hours it takes at the two test temperatures to produce the same push out of the access time, and to then use these two temperatures and times to calculate an activation energy. For example, we see in Figures 2 and 3 that the error distribution at 226 hours at 200 C is similar to the error distribution at 1305 hours at 175 C. An analysis of our data using this approach establishes a time-temperature equivalence that results in an activation energy of about 1.2 eV for charge loss/data retention. This value is consistent with, but is a bit higher than the manufacturer's value of 1.1 eV.

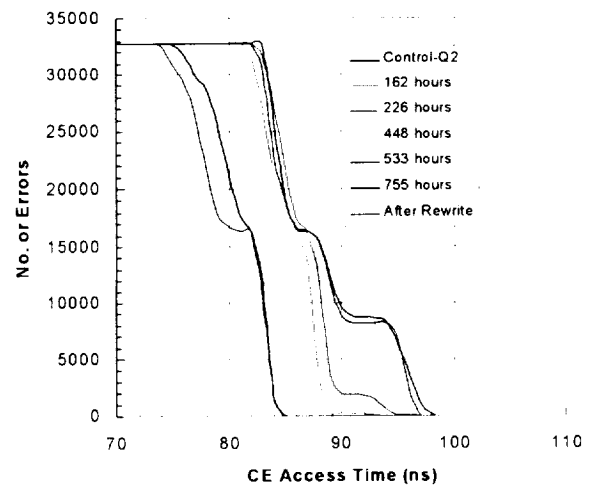


Figure 3 Example of data similar to that shown in Figure 2 except that the aging temperature was 175 C

We can now predict the data retention lifetime at 70 C based on the worst-case data push out rate measured at the two aging temperatures using this 1.2 eV activation energy. The estimated time-to-failure (where failure is defined as the point at which the access time reaches 150 ns) is found to be a few hundred years using this approach, which is well beyond the mission requirement

To lend credibility to the assumption that the access time push out was due only to charge leakage off the memory transistor and was not caused by circuit degradation, the parts were rewritten and tested after these aging tests. All parts continued to meet specification and all access times returned to their initial values to within 1 ns.

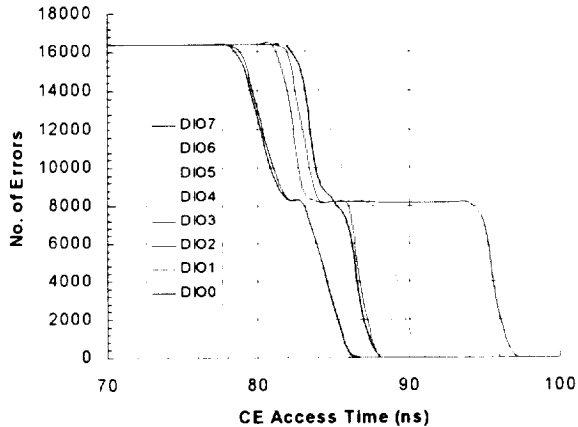


Figure 4. Example of the number of address errors versus the chip enable access time for each Data I/O line. Data correspond to an aging time of 533 hours at 200 C, which is shown in Figure 2 for the combined Data I/O lines

The activation energy for de-trapping charge in silicon nitride given in the literature is 0.35 eV [3]. Even when we use this worst-case activation energy to describe the charge loss in the memory transistor, the predicted time-to-failure at 70 C based on extrapolating our access time push out data to failure (150 ns) is 52 years.

Even though we did not find any failures in our small part population during these aging tests, a review of other data in the community suggested that there was a finite probability of having, perhaps, 1 part in 30 failing earlier than those in the normal population. The one intermittent failure we saw in our aging tests, which is described below, also raises a concern of an early failure issue. Obviously such an early failure would pose a great risk for a space application. Therefore, a considerable effort was invested in developing a stringent test to screen parts subject to such early failure out of the production part population.

#### Total Ionizing Dose Tests

Since power was only rarely to be applied to these memory parts during the mission under consideration, the parts were irradiated unbiased (all leads shorted together). The same parts used in the accelerated aging tests were rewritten with a complementary checkerboard pattern and irradiated in a Co-60 source at a dose rate of 3 krad(Si)/minute to 78 krad(Si) in 26 krad(Si) increments. No significant degradation was observed after 78 krad(Si).

Parts were then divided into two groups and a second aging experiment was begun using temperatures of 175 and 200 C. Although these aging tests were not carried out as long as the original aging tests, the push out of the read out access times for the times we measured were essentially the same. For example, the average change in access time during the post-irradiation aging stress at 157 hours at 200 C was 10.2 ns. This value compares favorably to the average change in access time of 10.0 ns, which was found after 162 hours in the 200 C tests that had been conducted prior to the irradiation.

A word of caution based on experience with other part types, the on-chip bias generator is likely to fail at relatively low total dose levels when the part is irradiated under normal operating voltage conditions. Such bias generator circuits are known to fail at levels in the range of 10 to 20 krad(Si).

#### Intermittent Errors

Some anecdotal data about this part type raised a concern that it was prone to an intermittent failure problem. During our aging test, we saw two instances of an intermittent error problem with one part that may have been the same problem that had been reported by others. In the first instance of this part failing specification, the failure was repeatable over a period of a few hours, but the part passed with no problem the following day. In the second instance the part continued to fail over a two day period, giving us a chance to characterize the failure behavior. It was discovered that the failure was sensitive to power supply voltage, passing at 5.25 V, being marginal at 5.00 V, and consistently failing at less than 5.00 V. Scope traces of the data signals from Data I/O1 and Data I/O2 for normal (passing) operation are shown in Figure 5. At this voltage, the data are correct (Data I/O1 is a  $\epsilon 0_i$  during the first clock cycle and a  $\epsilon 1_i$  during the next, while Data I/O2 is the inverse of Data I/O1). The Data I/O1 and 2 signals are shown in Figure 6 for a power supply voltage of 4.65 V, for two addresses where a failure is observed. In this case, Data I/O1 should be a  $\epsilon 1_i$  followed by a  $\epsilon 0_i$  whereas Data I/O2 should be the inverse of Data I/O1. The problem is a failure of either of these Data I/O signals to go to a  $\epsilon 0_i$  state at these two addresses. Note that in the first pattern shown in Figure 6 the Data I/O2 signal does go to a  $\epsilon 0_i$  but only after a time has elapsed that is well beyond the specified access time of 150 ns. This failure behavior was not observed on the following (third) day.

There are several features of this intermittent failure behavior that seem important. First, this behavior was only seen with aged parts, which implies that it is the result of charge leakage off of the memory transistor. Second, the failure is always due to a Data I/O line not making it to a  $\epsilon 0_i$  level, implying that the problem is related to the electrons, rather than the holes, leaking out

of the transistor's gate insulator. Third, only a small number of addresses fail, implying that the problem is dominated by a few memory cells, rather than to a sense amplifier, or some other part of the circuitry, such as an output buffer. Fourth, the oscillations suggest that there may be an occasional combination of degraded memory transistor and sense amplifier that produces an instability of the overall data readout behavior. On the other hand, it is not at all clear what would cause this failure behavior to disappear after a few hours if it is due only to charge leakage from the memory transistor, since no known mechanism is known that could replace this charge in the gate insulator short of reprogramming.

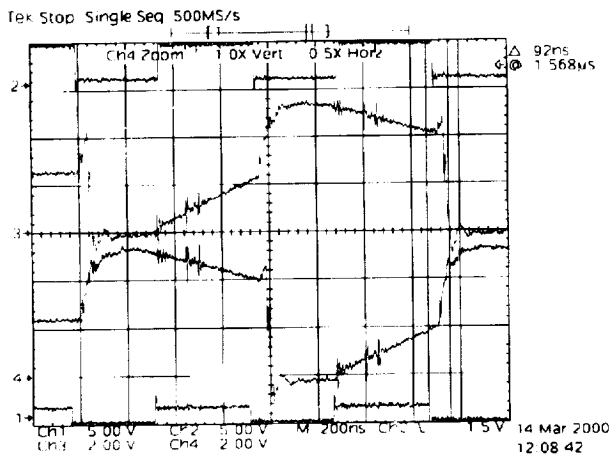


Figure 5. Scope trace of the part experiencing the intermittent failure. The power supply voltage is set at 5.25 V, where the data outputs are stable and correct. The scope traces from top-to-bottom are Output Enable, Data I/O1, Data I/O2, and Chip Enable.

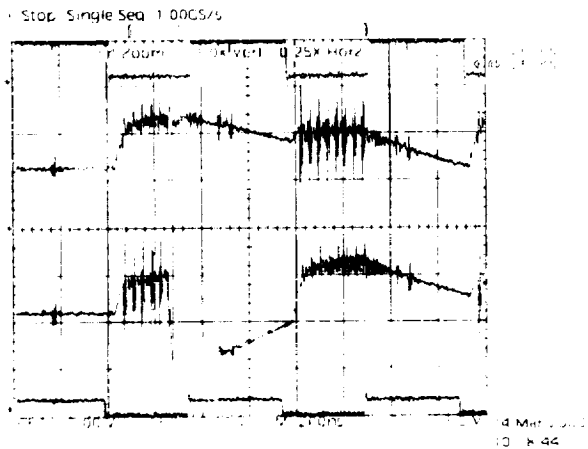


Figure 6. Scope trace showing the intermittent failure. In this case the power supply voltage is set at 4.65 V. The oscillations that occur on both Data I/O1 and 2 can be seen, as well as the delay in Data I/O2 transitioning to the  $\bar{e}0i$  state.

It should be pointed out that there was a concern that this intermittent failure might not be due to the chip inside the package, but to a corroded package pin, or to some other test fixture-related problem. However, neither cleaning the pins, repositioning the part in the socket, nor adjusting the fixture solved this problem. The facts that no other part in our test population exhibited this behavior and that only a very few of the addresses on the part that exhibited the intermittent behavior failed, further support the conclusion that this was not a pin or fixture problem, but a chip-related problem.

### 3. SCREEN DEVELOPMENT

A major program objective was to develop a test that could identify parts that were either weak in terms of their data retention capability, or were prone to the intermittent failure behavior described above. The approach taken was to make sure that this test included all of the worst case operating conditions we could identify. The operating conditions we identified as being most important were the test pattern, the power supply voltage, and the temperature.

#### *Power Supply Voltage and Temperature*

Parts were routinely tested at 4.5, 5.0, and 5.5 V. Although parts did not generally fail specification, one could see from the error distribution versus readout access time data that the push out was worse at 5.5 V than it was at 4.5 V. This is counterintuitive, since CMOS circuits generally operate faster as the power supply is increased. In this part, however, it is suspected that the threshold level of the sense amplifier is higher at the higher power supply voltage, increasing the time it takes to integrate charge from the memory transistor and determine its data state.

On the other hand, we found in tests conducted after those described above that one additionally aged part exhibited a few hundred access time failures when tested at room temperature and with a power supply voltage of 5.5 V. In this case, the part did not exhibit errors at 4.5 or 5.0 V. In addition, the errors decreased in number as the temperature was increased, completely disappearing at a temperature of about 38 C. This behavior was reproducible over a several week period.

#### *Test Pattern*

A test pattern sensitivity was also found in later tests of our aged parts. An analysis showed that an error was strongly correlated to the data that had been previously readout. In particular, reading out a data byte having a high number of  $\bar{e}1i$ s was found to significantly increase the probability that a  $\bar{e}0i$  bit in the next byte would be readout incorrectly. For example, the probability of reading out an error in a data byte was found to increase by over 70% if the data in the prior byte was the worst-

case pattern, e1111 1111 i These pattern sensitivity errors are not solely due to charge leakage off the related memory transistors, however, because the data are generally read out correctly when the pattern is run backward

Based on an analysis of this pattern sensitivity, a special test pattern was devised that was intended to improve the discrimination of weak parts in the population over that of a checkerboard, or other simple pattern. First, we wanted to heavily populate the pattern with e0is, since it is about 26,000 times more likely that a e0i bit will fail than a e1i bit. On the other hand, we wanted to insert a short sequence of patterns periodically in the memory that included data bytes with several e1is to all e1is so that we would increase the likelihood of detecting the pattern sensitive failures that we described above. Finally we included a unique code word located at each Address bit so that the part could not pass the functional test unless every address bit toggled. It was estimated that this new pattern was some 300 times more likely to detect an error than the checkerboard pattern that had been used initially

#### 4. CONCLUSIONS

Tests were conducted to verify that the Hitachi 1-Mbit (128k x 8) MNOS memory component, the HN58C1001, was able to retain stored data for periods as long as the 20 years specified for this part and after exposure to a specified total ionizing radiation dose. In addition, a test was developed to screen parts out of the population that were subject to either premature or intermittent failure

Accelerated aging tests showed that the activation energy for charge leakage from the memory transistor was about 1.2 eV. This result combined with push out of the read out access time at 175 and 200 C suggested that the nominal data retention time for this part is well over the 20 years specified, as long as the temperature remains below 70 C

Total ionizing dose irradiation tests showed that the part was insensitive to a dose of 78 krad(Si) (unbiased irradiation). Subsequent aging tests on the irradiated parts showed that the radiation had little, if any influence on data retention

A test was developed to screen parts that might be prone to early or intermittent failure out of the population. A high percentage of the memory was written with e0is, since a e1i rarely, if ever fails. A sub-pattern was written periodically throughout the memory address space to detect a pattern sensitivity that was found in which failures were observed in a word having a high number of i0is being readout after a word having a high number of e1is. To increase the likelihood of finding a readout failure, this functional test should be performed with power supply voltages of both 4.5 and 5.5 V and at room temperature (or lower), rather than at an elevated temperature. Even though we feel that this test will

increase the probability of finding parts prone to early failure, there is no guarantee that the screen will be successful, since the physical mechanisms responsible for early failures are unknown and we were not able to demonstrate the proposed test on a significantly large part population

#### 5. REFERENCES

- 1 Kamigaki, Yoshiaki, et al., i Yield and Reliability of MNOS EEPROM Products, i *IEEE J. of Sol.-State Circuits*, Vol. 24, No. 6, December 1989, p. 1714
- 2 McWhorter, P. J., S. L. Miller, and T. A. Dellin, i Modeling the memory retention characteristics of silicon-nitride-oxide-silicon nonvolatile transistors in a varying thermal environment, i *JAP*, 68 (4), 15 August 1990, p. 1902
- 3 Wu, Ken, et al., i A Model for EPROM Intrinsic Charge Loss through Oxide-Nitride-Oxide (ONO) Interpoly Dielectric, i *IEEE Proc. of the IRPS*, 1990, p. 145

#### 6. ACKNOWLEDGEMENTS

We wish to acknowledge the support of the Aerospace IR&D program, as well as insightful conversations with Craig Sather and Tom Tsubota

# Neo-Stacking of Packaged Flash Memory

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**Abstract**—A variation on Irvine Sensors' Neo-Stacking process allows extremely dense packaging of Flash or other memory while sidestepping the problems associated with obtaining Known Good Die (KGD). Memory is often difficult or impossible to obtain in die or wafer form, and comprehensive testing and burn-in is prohibitively expensive for many applications. Readily available plastic encapsulated packaged memory chips are pre-tested and can easily be further tested and screened, speed sorted, tested over a different temperature range, etc. However, they cannot be packaged densely enough to meet the requirements for many applications. This paper describes a method for reprocessing and stacking standard packaged memory, along with support circuitry, into a chip-scale footprint with a very low profile.

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1. INTRODUCTION
2. NEO-STACKING
3. STACKABLE LAYERS FROM TSOPS
4. COMBINING TECHNOLOGIES
5. SUMMARY

## 1. INTRODUCTION

Often, flash memory is most readily available in a plastic encapsulated thin small outline package (TSOP). Processes for stacking TSOPs are available from several sources, Irvine Sensors Corporation among them. The process is economical and allows two to eight chips to use the board space of only one. However, the overall volume is not reduced since the stacked TSOPs, plus interposers, form a relatively tall subassembly. For many applications, stacking TSOPs provides the needed density, although for extreme miniaturization, stacking bare silicon chips is required.

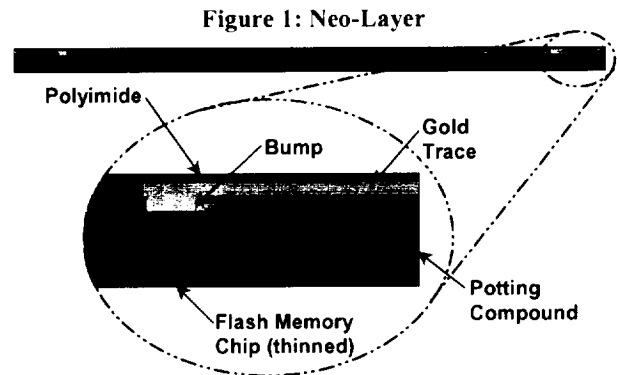
Irvine Sensors Corporation has established processes for bare die stacking that require that the chips be available in either die or wafer form. Obtaining chips in either form is sometimes difficult or impossible. When bare die are

available, an important design issue to be addressed is that of Known Good Die (KGD). Generally, KGD solutions are rather costly. The problems of bare die availability and KGD testing can be addressed simultaneously.

TSOPs are the most readily available part type, and they are already fully tested in that packaged format. The process being developed further processes the TSOPs into smaller, very thin, stackable layers.

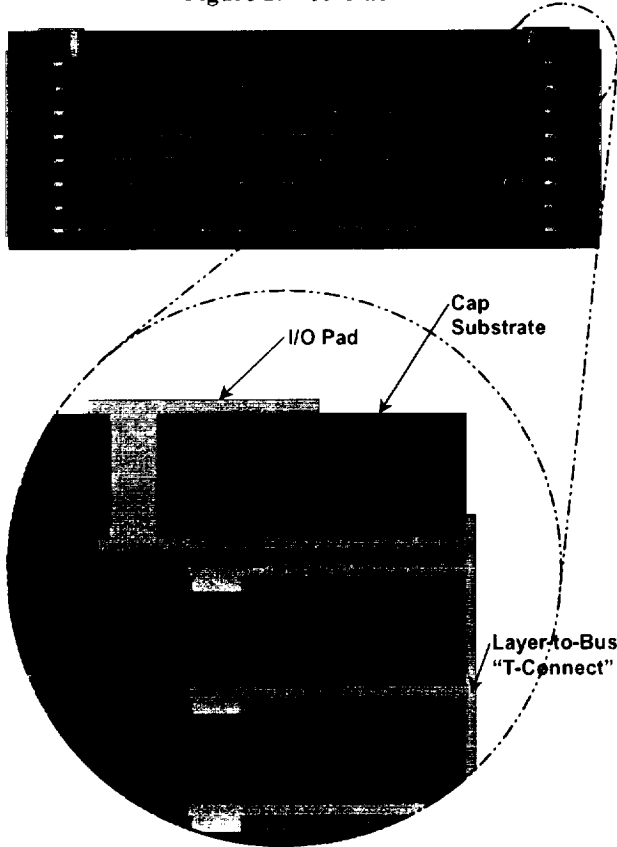
## 2. NEO-STACKING

Irvine Sensors' Neo-Stack™ process starts with a bumped KGD that is encapsulated in a potting compound. Thin film metal traces contact the I/O bumps and route the signals to the edges of the potting material. The layer is ground from the backside resulting in a thin (.25 mm to .10 mm) complete layer, as shown in Figure 1.



A Neo-Stack is created by laminating Neo-Layers with a cap substrate, which uses through-holes to provide I/O paths. Bus metalization is applied on one or more sides to interconnect layers and the cap substrate. The intersection of the layer traces and the bus traces form the "T-Connects", which are key to high reliability. Unlike wrap-around or "L-Connect" approaches where step coverage problems can result in a reduced metal cross section, the trace thickness of T-Connects remain the full thickness as deposited. A complete Neo-Stack is shown in Figure 2.

Figure 2: Neo-Stack



### 3. STACKABLE LAYERS FROM TSOPs

The typical internal construction of a TSOP package lends itself to processing into a stackable layer of almost identical structure to a Neo-layer constructed from a KGD. Within the TSOP, gold wire bonds are used to connect the die I/O pads to the lead frame, as shown in Figure 3.

Standard wafer grinding equipment is used to remove most of the encapsulant material on the top surface, down to the cross section of the gold ball of the interconnecting wire bond. This process leaves a thin layer of encapsulant on the die surface, which serves as the insulating surface for metal trace deposition. Grinding is also used to remove the encapsulant and carrier from the bottom of the die, and to thin the die itself. During this backside-grinding step, the leads are also removed. A final dicing step minimizes the layer footprint, while leaving enough of the original TSOP encapsulant around the die edges to provide an insulating surface for the bus metalization. The process sequence is shown in Figure 4.

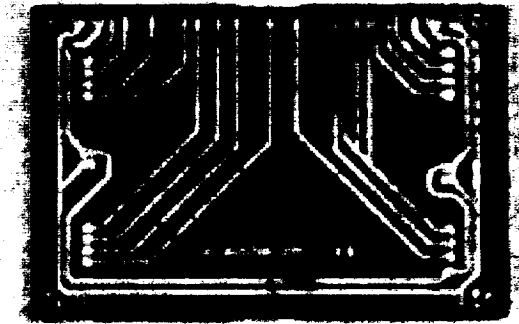
Typical TSOP encapsulant materials are chemically similar to the potting material used in fabricating Neo-Layers, which allows layers made from TSOPs to be stacked with the identical Neo-Stacking process.

### 4. COMBINING TECHNOLOGIES

The material compatibility allows layers made from TSOPs to be stacked along with standard Neo-Layers, which can contain different die types. The only constraint is that the die types in the Neo-Layers must not be so large that the Neo-Layer becomes larger than the memory layers. This is normally not a problem because memory die sizes are usually quite large as compared to other chip types in a typical subsystem.

Irvine Sensors is currently developing two products using modified TSOPs combined with standard Neo-Layers. The first is a stack for the mass memory storage portion of a miniature stacked computer. A single Neo-Layer is stacked together with eight layers of flash memory. The Neo-Layer contains two driver chips, which are procured in bare chip form, and the memory layers are made from standard TSOPs. Fully functional layers of modified TSOPs have been fabricated and tested down to a thickness of four mils (0.01 mm). Figure 5 shows a top view of a flash memory layer with the routing traces applied.

Figure 5: Flash Memory Layer

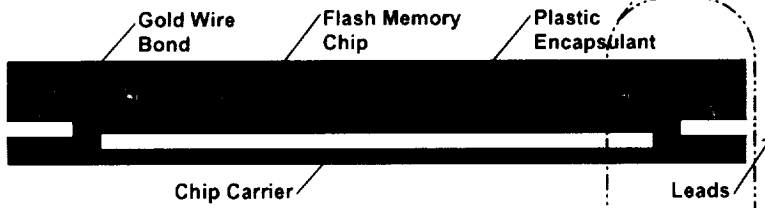


The second product is for use in a space application for NASA. Twelve memory layers are combined with a single Neo-Layer containing a radiation hardened Field Programmable Gate Array (FPGA). The FPGA provides I/O control and an Error Detection and Correction (EDAC) function. The compact assembly is sealed in a hermetic package. This strategy allows the use of Commercial Off-The-Shelf (COTS) components without the reliability compromise usually associated with the use of COTS parts. The original TSOP part has most of the plastic packaging removed, and the finished stacked hermetic component can be screened and qualified in accordance with full military and space requirements. Proof-of-concept stacks containing modified TSOPs have demonstrated the viability of the approach for this program.

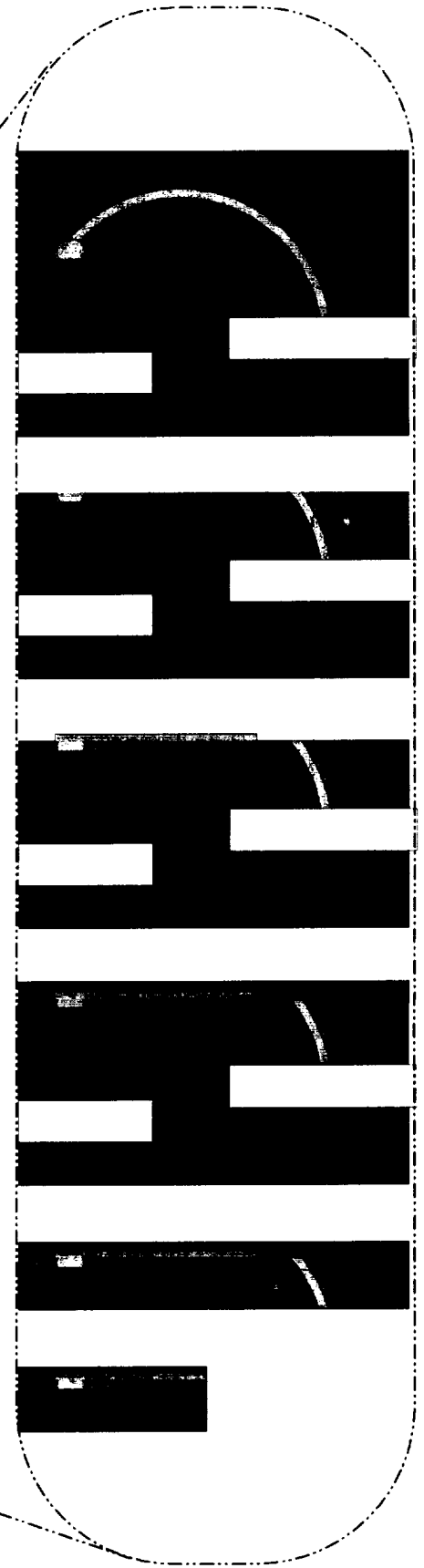
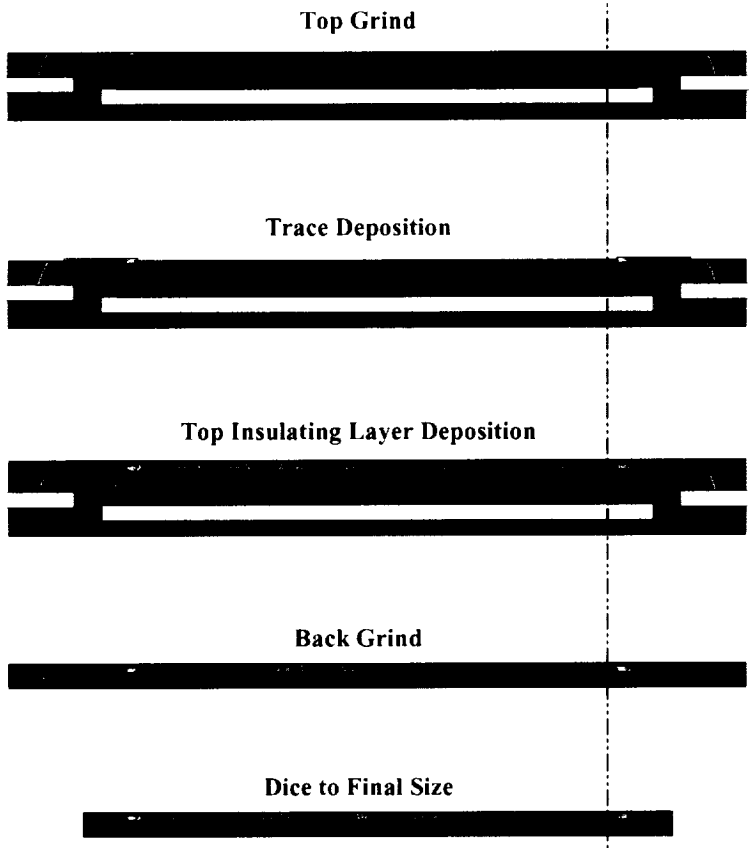
## 5. SUMMARY

Neo-Stacking is a high-density packaging solution intended for use with bare die, and die contained in TSOP or other plastic packages can also be accommodated. The technique described in this paper overcomes the problems of bare die availability and KGD testing by treating the original plastic package as a low-cost temporary test carrier, from which the die is eventually removed. The resulting stackable layer is almost identical to standard Neo-Layers and can be stacked along with Neo-Layers containing other die types.

**Figure 3: TSOP Construction**



**Figure 4: Layer Process Sequence**



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# HIGH SPEED MRAM BUFFER FOR HIGH CAPACITY NONVOLATILE SHOCK RECORDERS

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*Abstract*—High shock data recorders require large amounts of storage in order to capture high resolution data. Also, high speed is needed in order to record pre-trigger data. Nonvolatile storage is important in order to prevent data loss. A system was developed with an 8 megabyte FLASH and a PLD that contained a high speed SRAM buffer memory. A new development in MRAM, using SDT technology along with a unique circuit design, is an ideal nonvolatile replacement for the SRAM. A new film structure and circuit design yields a memory that does not have disturb problems and that has the potential of high production yields. The memory is high speed (less than 10 nanosecond read or write), low power (less than 30 Pico joule writes), has no wear out mechanism, and is inherently RAD Hard, with STD cells tested to 1 Mrad.

processing and can be easily integrated into the Programmable Logic Device (PLD) that is being used in the HSDR design.

## 2. HSDR MEMORY REQUIREMENTS

Previous high shock data recorders have used battery backed SRAM because of the recorders' high-speed requirements. Problems of memory loss during battery failure and high power consumption continue to be an issue with this type of recorder. With the help of SBIR funding from both Eglin AFB and Kirtland AFB, NVE designed an HSDR with the goal of resolving these issues. The first issue has been addressed with the design of an 8-channel recorder that contains 8 megabytes of FLASH memory and a 256 byte SRAM buffer. The recorder is contained on 2 printed circuit boards that assemble to a size of 0.3 x 1.1 x 2.5 inches, or about 1 cubic inch volume. To facilitate manufacture and prototype testing, the 2 circuit boards are built as a single board, that is later cut in half and stacked to form the final recorder assembly. The recorder circuit board is shown, prior to cutting and stacking, in Figures 2-1 and 2-2.

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## 1. INTRODUCTION

Data recorders that measure fast, transient events require large amounts of memory to achieve the resolutions required for wide bandwidths as well as fast buffer memory to capture pre-trigger events and buffer the slower FLASH memory. This has been successfully accomplished in NVE's high shock data recorder (HSDR), for Kirtland AFB. The HSDR contains both an 8 Megabyte FLASH and a 256 byte, high speed buffer SRAM. The SRAM contains a significant portion of the high-speed shock event, and this data can be lost with battery failure during that time. NVE has developed a low power, nonvolatile MRAM, with Spin Dependent Tunneling (SDT) technology, that can replace the current SRAM - eliminating the volatility and power problems of the SRAM. The MRAM is compatible with semiconductor

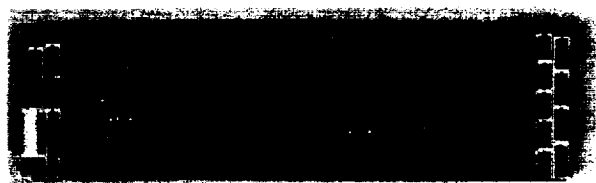


Figure 2-1. HSDR Assembly - Top View



Figure 2-2. HSDR Assembly - Bottom View



Many of the transient events that are to be measured are completed in a matter of a few milliseconds. If a power loss occurs before the pretrigger data in the SRAM buffer, or the data in the internal FLASH integrated circuit buffer, can be written to the FLASH memory, a significant portion of the event data will be lost. This is a concern because the most likely time of failure, for a munitions data recorder, is at impact.

### 3. MRAM BUFFER SOLUTION

To resolve the issues that are discussed above, an MRAM design using Spin Dependent Tunneling (SDT) technology with unique film and circuit design, is being developed by NVE. This design has very low power and has a high speed write which is especially important for buffer applications in battery powered equipment. High speed read and write operation are essential for buffer application, where the buffer memory must first accumulate data while a slow FLASH memory is performing a write cycle, and then quickly flush the data to the FLASH page buffer.

Since the MRAM SDT memory design is compatible with standard semiconductor processing, the memory can be integrated with a PLD or an ASIC which is used to control the operation and provide the data buffering for the high shock data recorder. It also can be used as a stand alone component such as a small serial I<sup>2</sup>C EEROM equivalent component. Since MRAM is inherently radiation resistant, rad hard components using the SDT design can be constructed which would be useful in satellite and missile applications.

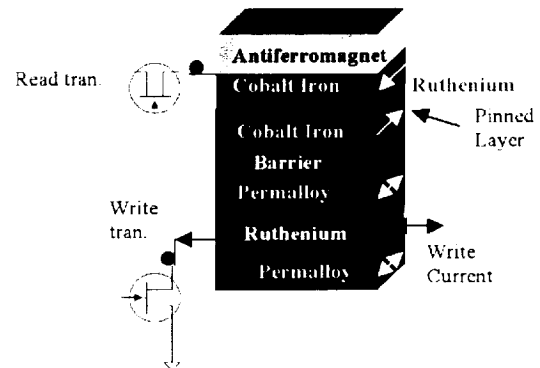
### 4. MRAM BUFFER MEMORY

NVE's MRAM buffer memory uses a write select transistor in each cell, and a sandwich storage structure. The select transistor eliminates the half-select condition that non-addressed cells experience in other MRAM memories - which eliminates write cycle disturbs of neighbor cells. The sandwich storage element provides flux closure during writes - minimizing the required write energy. Also, with an anti-ferromagnetically coupled sandwich, sensitivity to external disturb fields is greatly reduced.

Most MRAM schemes use a 2D current selection scheme to read and/or write the cell. The original MRAM [1] concept and the Pseudo Spin Valve (PSV) [2] concept both use magnetic 2D selection, i.e. two, usually orthogonal, currents, for both the read operation and the write operation. In both cases, all of the cells on both the row and the column that contain the addressed cell will experience a half-select condition. Similarly, Spin Dependent Tunneling (SDT, a.k.a. Magnetic Tunnel Junction, or MTJ) memories [3,4,5] use 2D selection when writing a cell. Again, this creates a half-select condition for all cells on the same row and column as the addressed cell.

In all cases, the half-select condition increases the likelihood of a disturb, and places stringent requirements on the uniformity of the magnetic characteristics of the cells.

The MRAM buffer memory uses an SDT memory cell that has a sandwich film on one side of the tunnel junction, and that contains two select transistors - one that is used during readout and one that is used during writing. Figure 4-1 illustrates this cell structure, showing schematically both the SDT structure and the select transistors. To write the cell, the write select transistor is turned on, and a write current flows through the sandwich portion of the cell. This write current flows in the plane of the SDT film. For a read operation, only the read select transistor is turned on, and a small tunneling current is passed through the cell in order to generate a readout voltage. For a given read current, the readout voltage will depend upon the alignment between the magnetizations of the magnetic films that are adjacent to the top and bottom surfaces of the tunneling barrier.

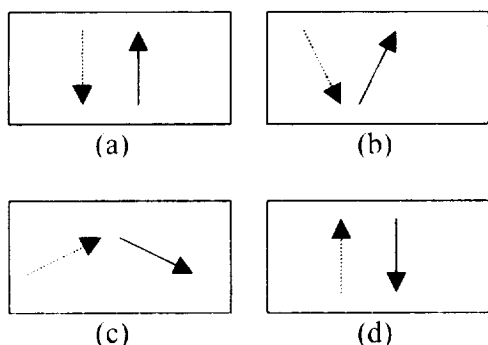


**Figure 4-1. Schematic illustration of the SDT buffer memory cell. The magnetic sandwich that is below the tunnel barrier is the storage element, and is written with in-plane current. Vertical conduction, through the tunnel barrier, is used for readout.**

For the cell shown in Fig. 4-1, the write current only flows through the selected cell. Since no write current flows through adjacent, non-selected cells, the half-select condition that exists in other MRAM is eliminated. Without a half-select condition, the switching uniformity requirement is eased considerably. As long as the write current is set high enough to write the cell that has the highest write threshold, all cells in the memory can be written without disturbing a non-selected cell. Compared to the switching uniformity that is required for a 2D selection scheme, this single current selection scheme greatly improves the manufacturability of the memory. It is the combination of the sandwich storage element and the write select transistor that allows the single current selection scheme to work. In other MRAM cells, the write current flows through a separate current conductor - not through the storage element. The need for the sepa-

rate conductor, combined with the sensitivity of other MRAM designs to disturb fields, makes it impractical to use the single current selection scheme with the other types of MRAM.

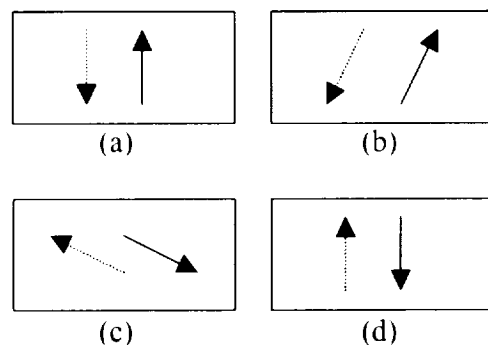
The second key feature of the innovative SDT buffer memory is significantly lower write current than other MRAM cells. This lower write current is due to the closed flux switching behavior of the anti-ferromagnetically coupled Ruthenium sandwich film that forms the storage element in the SDT buffer cell. Consider first the write process in a PSV cell - which is also a sandwich film cell, but is not anti-ferromagnetically coupled and which is written with a tipping field applied. Figure 4-2 illustrates the PSV write process. The tipping field is assumed to be directed left to right in the figure. The combination of the tipping field and the write current that is flowing through the sandwich cause the magnetizations of both layers to rotate in opposite directions - so that they go through a parallel alignment state. This parallel alignment greatly increases the internal demagnetization fields, which leads to a comparatively large write current requirement.



**Figure 4-2. Illustration of the switching process in a PSV cell: a) beginning rest state, b) initial rotation due to tipping field, c) rotation just past parallel, and d) final rest state. The parallel state, as the magnetizations rotate from (b) to (c), is a very high energy state. Solid arrow shows magnetization of top magnetic film, dashed arrow shows magnetization of bottom magnetic film.**

Now consider the switching process in the Ruthenium (Ru) sandwich that is used for storage in the SDT buffer cell. With a thin Ru layer, on the order of 10 Å, the two magnetic films are strongly coupled anti-parallel to each other. As a write current is applied through the sandwich, in a direction that generates fields that are opposing the current direction of both the top and bottom magnetizations, the magnetizations begin to rotate - but stay anti-parallel aligned. Because of the anti-parallel alignment, demagnetization fields, and stray fields, are minimized in this sandwich - and remain at a minimum as the magnetizations rotate. This rotation process is illustrated in Fig. 4-3. In relatively wide sandwich structures, i.e. 2 μm, write currents of 2.5 mA have been demonstrated. This is significantly lower than the write requirements of other

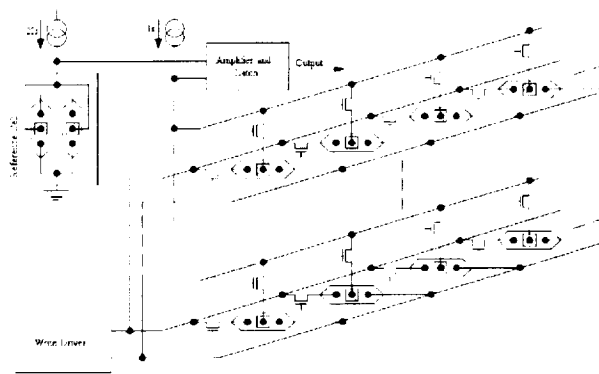
MRAM cells. Cell switching times of under 3 ns have been measured, which should allow nominal 10 ns write times.



**Figure 4-3. Illustration of the switching process in Ru sandwich storage element that is used in the SDT buffer memory cell: a) initial rest state, b) initial rotation after application of write current, c) rotation over half way to new storage state, d) final rest state. Solid arrow shows magnetization of top magnetic film, dashed arrow shows magnetization of bottom magnetic film.**

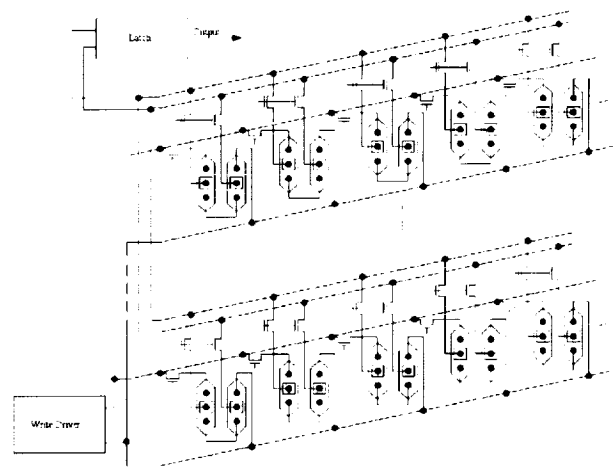
Two different memory array architectures are envisioned for the SDT buffer cell: 1) the 1 Junction per Cell (1JC) architecture, and 2) the 2 Junction per Cell (2JC) architecture. As the name implies, the 1JC memory uses a single SDT element for each cell, or bit, in the memory - each junction is constructed with the Ru sandwich storage element as shown in Fig. 4-1. Similarly, the 2JC memory uses two SDT elements for each cell, with the two elements being written to opposite states during a write operation.

The 1JC memory is denser than the 2JC memory, but has slower readout than the 2JC memory. Fig. 4-4 shows, schematically, the 1JC memory architecture. To write a cell, the write driver is activated and the write select transistor for the addressed cell is turned on. The polarity of the write current determines the written state of the cell. A readout requires a reference, to compare with the read voltage of the selected cell. During readout, the sense current is activated and the read select transistor of the addressed cell is turned on. Also, a 2X sense current is activated, and flows through a reference cell. The reference cell consists of two SDT elements that are in parallel and have been written to opposite states - so that the reference voltage will be halfway between the low and high voltage of a single SDT element. Finally, a sense amplifier is used to compare the memory cell voltage to the reference voltage, and latch the result. Even with 40 mV cell voltage differences - or about 20 mV difference between the cell voltage and the reference voltage, it is expected that the sense amplifier will require an auto-zero step prior to readout. It is this amplifier requirement that leads to somewhat slower readout speed for the 1JC memory relative to the 2JC memory.



**Figure 4-4. Schematic diagram of the 1JC memory architecture. Readout requires that the read voltage of the selected cell be compared with a global reference voltage.**

The 2JC architecture uses a relatively simple latch cell circuit with one SDT junction in each of the two halves of the latch cell. This architecture is shown schematically in Fig. 4-5. The two SDT devices are written to opposite states - one high resistance and one low resistance. To read the memory, the latch is momentarily shorted, so that both outputs are at the same potential, and then released. When the short is removed, the different resistance that is presented to the two halves of the latch, by the oppositely written SDT junctions, causes the latch output to rapidly drive to a known logic level based on which SDT junction is in a higher resistance state. This architecture is very fast and, for small arrays, has higher density than the 1JC architecture because of the lower overhead electronics. The reason that this architecture has higher density for small arrays is that the area that is required for overhead circuitry, such as the sense amplifier, is much larger for the 1JC architecture than for the 2JC architecture. The 2JC architecture also has less stringent requirements on SDT junction uniformity since the two SDT junctions within a given cell act as local "references" for each other - there is no need to match closely to a reference cell that may be located a relatively large distance away. The write operation in the 2JC architecture is the same as that of the 1JC architecture.



**Figure 4-5. Schematic diagram of the 2JC memory architecture. The 2 SDT elements in each cell self-reference one another for readout - requiring only a simple latch.**

## 5. MILITARY APPLICATIONS

Although the basic concept of magnetoresistive random access memory (MRAM) has led to working memory cells on silicon and to limited numbers of working MRAM chips, demonstration of practical manufacturability of MRAM has not been reported. One of the major stumbling blocks to producing MRAM is the stringent magnetic uniformity requirement that the 2D memory organization places on the MRAM cell, an organization which all serious MRAM developments currently employ. Staying with a 2D approach may delay or even preclude the practical manufacturing of MRAM. Because defense applications really need fast and truly nonvolatile random access memories, this could represent a significant difficulty for the Department of Defense. A Phase I program with Kirtland AFB entitled "Radiation-Hardened Non-Volatile RAM" addressed the radiation resistance of MRAM SDT cells and alternative circuit designs to eliminate the problems of disturbs and uniformity found in 2D MRAM memory architectures. Novel memory cells and circuit architectures now make possible the development of a reliable and manufacturable radiation hard MRAM component that will satisfy the on-going need of the military and space community.

Successful demonstration of the resistance of the SDT cell to radiation beyond 1 Mrad was completed during the Phase I effort with Kirtland AFB. This demonstration has established a firm foundation for the development of radiation hard MRAM components. SDT junctions were tested with survival beyond 1 Mrad without catastrophic failures or large parameter shifts.

Applications for this new type of MRAM are not limited to the HSDR buffer applications, but include military satellites and space-based weapon systems. Other applications would include systems that are required to function

in a nuclear battlefield environment, since this technology is completely compatible with space qualified RAD Hard CMOS processes such as those that are available from Peregrine Semiconductor.

## 6. CONCLUSIONS

The development of new MRAM components, that use the SDT cell and memory architecture that is presented in this paper, will eliminate the problems of nonvolatility in shock recorders as well other applications that require small, high speed, low power, random access memory devices. In addition, with its inherent resistance to radiation effects, these devices will be used in space and missile applications. Initial devices with sizes on the order of 1 Kbyte will be developed, with sizes evolving up through 16 megabit as production refinements are completed. Small buffer MRAM devices will be incorporated into PLDs giving them high speed nonvolatile storage which is not available today

## 7. ACKNOWLEDGEMENTS

The authors wish to thank Dr James Daughton and Dr. Author Pohm for their contributions and innovations in the development of these new memory cells

The authors would also like to acknowledge the support of the following sponsors: DARPA (contract # F29601-00-C-0194), Air Force Advanced Research Laboratory at Kirtland AFB (contracts # F29601-99-C-0032 and # F29601-01-C-0121)

## 8. REFERENCES

- 1 J.Daughton, "Magnetoresistive Memory Technology", Thin Solid Films 216, p 162 (1992).
- 2 A. Pohm, J Anderson, R Beech, and J Daughton, "Bias Field and End Effects on the Switching Thresholds of Pseudo Spin Valve Memory Cells", IEE Trans. Magn. 34, No. 4, p 3280 (1997).
- 3 P. Naji, M. Durlam, S. Tehrani, J. Calder, and M DeHerrera, "A 256kb 3.0V 1T1MTJ Nonvolatile Magnetoresistive RAM", ISSCC 2001 Proceedings (2001).
- 4 R.E. Scheuerlein, W.J. Gallagher, S.S.P. Parkin, A. Lee, S. Ray, R. Robertazzi, W. Reohr, "A 10 ns read and write non volatile memory array using a magnetic tunnel junction and FET switch in each cell," 2000 IEEE International Solid State Circuits Conference. Digest of Technical Papers (Cat. No.00CH37056), 128 (2000).
- 5 J. Daughton, "Magnetic Tunneling Applied To Memory", J. Appl. Phys. 81, No. 8, p 3758 (1997).

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Design Hardness Techniques for Radiation Hardened Non-Volatile Memory

Presenter J Benedetto. UTMC Aeroflex

Material for this presentation was not available at the time of publication.

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## ***SESSION #5: Emerging Technologies***

Thursday, November 8, 2001

1:20 PM – 2:00 PM

Chair: *S. Tyson*, Air Force Research Laboratory

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- 1:20 PM      Future Development of Dense Ferroelectric Memories for Space Applications; *S. Philpy and G. Derbenwick*, Celis Semiconductor Corporation
- 1:40 PM      Commercialization of 1T-Cell Ferroelectric Memories for Space Applications; *F. Gnadinger and G. Huebner*, COVA Technologies Inc., *G. Derbenwick and D. Kamp*, Celis Semiconductor Corporation

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# Future Development of Dense Ferroelectric Memories for Space Applications

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**Abstract**—The availability of high density, radiation tolerant nonvolatile memories is critical for space applications. Ferroelectric memories, when fabricated with radiation hardened CMOS, can be manufactured and packaged to provide high density replacements for Flash memory, which is not radiation tolerant. Previous work showed ferroelectric memory cells to be resistant to SEU<sup>[1]</sup> and proton irradiation<sup>[2]</sup>, and ferroelectric storage capacitors to be resistant to neutron exposure.<sup>[3]</sup> In addition to radiation hardness, the fast programming times, virtually unlimited endurance, and low voltage, low power operation make ferroelectric memories ideal for space missions. Previously, a commercial, double level metal 64-kilobit ferroelectric memory was presented.<sup>[4]</sup> Although the capabilities of radiation hardened wafer fabrication facilities lag behind those of the most modern commercial wafer fabrication facilities, several paths to achieving radiation tolerant, dense ferroelectric memories are emerging. Both short and long term solutions are presented in this paper. Although worldwide major semiconductor companies are introducing commercial ferroelectric memories, funding limitations must be overcome to proceed with the development of high density, radiation tolerant ferroelectric memories.

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6. CONCLUSIONS
7. ACKNOWLEDGEMENTS
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## 1. INTRODUCTION

As global space communication systems advance and as the requirements for NASA's deep space missions

become more challenging, the need for radiation tolerant computer systems with increased memory capabilities are essential. The requirements for deep space memory systems are survival in a radiation environment of 1 Mrad total ionizing dose (TID) or more, operation for up to 10 years or more, and the ability to be addressed by the spacecraft computer at least twice every second for the purpose of storing spacecraft state and epoch, or nearly a billion write cycles.<sup>[5]</sup> These advanced computer systems will require large amounts of low power memory packed in the limited area available onboard each spacecraft.

The use of nonvolatile memory in these systems assures a spacecraft's ability to survive fault conditions and autonomously recover.<sup>[5]</sup> Current radiation tolerant nonvolatile memories cannot meet all of the requirements and are not dense enough to achieve the limited area requirements.

In addition to ferroelectric memory, there are several novel nonvolatile technologies in development that potentially could meet the high density, low power, and radiation tolerant requirements. These include magneto-resistive, magnetic tunnel junction, and chalcogenide glass memories. Taking into account the present level of maturity of these technologies, ferroelectric technology may provide the quickest solution for the short term and an excellent solution for the longer term.

Ferroelectric Random Access Memories (FeRAMs) offer high radiation resistance, excellent retention, virtually unlimited endurance, fast programming times, and low voltage and low power operation compared to other types of conventional semiconductor nonvolatile memories. FeRAMs are similar in design and processing to stacked DRAMs, and therefore may be well positioned to provide the high density nonvolatile memories required for radiation tolerant computer systems.

Although, at this time, there is no single manufacturer capable of producing high density radiation tolerant ferroelectric memories that meet all of the

requirements, including low power, there are short term (3 to 5 years) and long term solutions (greater than 5 years). These solutions are discussed in this paper.

## 2. FERROELECTRIC MEMORY COMMERCIALIZATION

Table 1 lists the semiconductor companies that have produced commercial ferroelectric memories, including some of the products manufactured.

Table 1. Ferroelectric Commercialization

<u>Company</u>	<u>Product</u>
Fujitsu	Embedded 64k-bit ferroelectric memory with microprocessor
Matsushita	1k-bit embedded ferroelectric memory in RFID chip
Ramtron	4k-bit FRAM®, 16k-bit FRAM®, 64k-bit FRAM®, 256k-bit FRAM®
Rohm	16k-bit ferroelectric memory

In addition to the companies listed in Table 1, companies pursuing ferroelectric memory development are listed in Table 2. Not included are the numerous university activities worldwide.

Table 2. Major Ferroelectric Activities

<u>Company</u>	<u>Activity</u>
Hitachi	R&D
Hughes/Raytheon	R&D
Hynix	Prototype FeRAM development
Infineon/Toshiba	Stacked 1T/1C 8M-bit and 64M-bit FeRAMs
Mitsubishi	R&D
NEC	Prototype embedded FeRAM
Oki	R&D
Samsung	4M-bit FeRAM R&D
Seiko Epson	R&D
Sharp	High density FeRAM R&D
Sony	1T R&D
STMicroelectronics	R&D consortium with IMEC
Texas Instruments	R&D-high density Embedded FeRAM at 0.18 / 0.13 micron

The commercial market for ferroelectric memories has been slow in developing because of problems in fabricating high density ferroelectric memories on aggressive silicon processing lines. Another reason for the slow commercialization of FeRAMs may be inadequate funding. Dataquest estimated that by early 1999, the FeRAM industry had spent less than \$500 million on research and development, whereas the costs to develop a 1-Gbit DRAM might top \$10 billion.<sup>161</sup>

Further compounding the problem of developing ferroelectric memories for radiation tolerant applications is the small aerospace market compared with the size of the market for commercial memories, and the even smaller market within the aerospace market for radiation hardened nonvolatile memory.

## 3. COMMERCIAL FeRAM RADIATION CHARACTERISTICS

Although the ferroelectric device itself is radiation tolerant, results of radiation testing of ferroelectric memories by NASA and Brookhaven National Labs indicate that most commercial FeRAM devices fail at approximately 10 krad TID. Also, these commercially available ferroelectric memories typically latch up under relatively low heavy ion bombardment<sup>171</sup>. This is primarily due to the radiation softness of commercial CMOS processes used to fabricate these memories. Regarding neutron and proton irradiation, it has been shown that ferroelectric memories should be tolerant to neutron fluences up to  $10^{15}$  neutrons/cm<sup>2</sup> and proton irradiation in excess of  $10^{12}$  protons/cm<sup>2</sup> with no bit failures.<sup>12,31</sup> The authors are not aware of any neutron or proton testing that has been done regarding existing stand-alone ferroelectric memories.

More advanced, commercial ferroelectric processes are now becoming available that provide a higher tolerance to radiation, such as 25 krad for a Hynix 64k-bit FeRAM tested by JPL. However, these levels are still too low to avoid significant spacecraft radiation shielding.

## 4. SHORT TERM SOLUTIONS

To develop a solution for JPL/NASA regarding a low density (1M-bit) radiation tolerant nonvolatile memory, Celis Semiconductor started a program in 1998 to provide a 1M-bit FeRAM using a split wafer fabrication process. This design was to use radiation hardened CMOS underlayer wafers processed at Sandia National Laboratories and ferroelectric



module and finishing layers processed at Matsushita. After wafer processing, advanced packaging of 12 die per package would result in a 1.5M-bit FeRAM. Figure 1 shows the split wafer processing strategy.

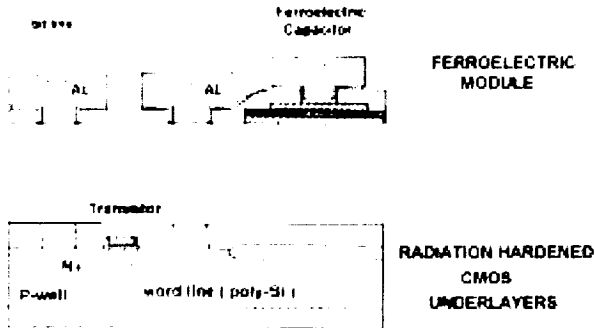


Figure 1. Split Processing Approach

While the circuit design was completed and initial processing results were obtained on test wafers, because of governmental budget cuts, fabrication of the 1.5M-bit memory was not completed. Later in 1999, when government funding was available for the continuation of the program, the required density for a packaged FeRAM increased significantly to the 8M to 16M-bit level. This increased density required more advanced processing not available at Matsushita. Despite these changes in specifications, there are at least three short term solutions for providing radiation hardened ferroelectric memories.

First, a split processing approach can still be used. To successfully use a split processing approach, the wafer diameters of the facility producing the radiation hardened CMOS underlayers and the facility producing the ferroelectric module must be the same. Although an 8-inch wafer can be laser cut to a 6-inch diameter, manufacturers are reluctant to use these cut down wafers. No companies pursuing ferroelectric memories are using 5-inch wafers, thus eliminating all 5-inch radiation hardened facilities from the split processing approach. Plans of radiation hardened facilities to migrate to 8-inch wafers have not materialized. Therefore, the split processing approach must use 6-inch wafers today. Both radiation hardened CMOS and ferroelectric modules are available for 6-inch wafers.

Another short term solution is possible as an alternative to the split processing approach. A new radiation tolerant technology has been developed by Aeroflex/UTMC that uses a modified design, named B<sup>2</sup>JT. This B<sup>2</sup>JT technique, proprietary to UTMC, requires more area and therefore a larger die size.

However, the resulting devices have high radiation tolerance. Figure 2 shows total dose radiation results for a B<sup>2</sup>JT 0.24 x 1 micron n-channel transistor manufactured on an Aeroflex/UTMC WA03 Test Chip.<sup>[8]</sup>

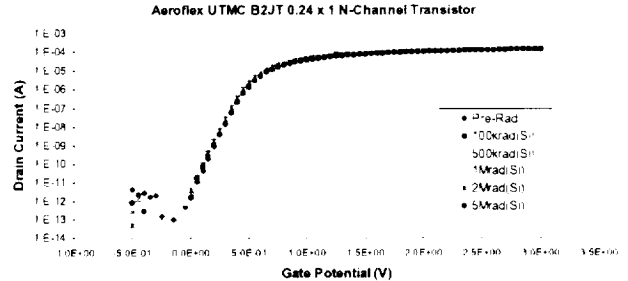


Figure 2. TID Results of B<sup>2</sup>JT Transistor<sup>[8]</sup>

A third short term solution is based on a process innovation of Aeroflex/UTMC. Aeroflex/UTMC has developed a CMOS process that is "Commercial Rad-Hard" (CRH). This process requires the addition of only one or two masks to a commercial CMOS process to achieve a radiation tolerance of up to 300 krad. Memories fabricated using this process would require radiation shielding to achieve the higher doses of radiation encountered in certain deep space missions. The CRH CMOS process technique is also proprietary for use only in facilities licensed by Aeroflex/UTMC. The CRH process has been installed in a licensed commercial wafer fabrication facility, and is presently processed on 5-inch wafers. To use this third solution, a wafer fabrication facility licensed by Aeroflex/UTMC must install and qualify a ferroelectric processing module, or the CRH process must be licensed to a facility using 6-inch wafers. Because of the time and commitment required to install the ferroelectric module or to bring up a 6-inch CRH CMOS facility, this is the least likely of the three short term solutions to occur.

An immediate possibility for providing radiation hardened ferroelectric memories of the required density is to use the split processing approach with 6-inch diameter wafers. More than one U.S. wafer fabrication facility produces radiation hardened CMOS on 6-inch wafers. For the ferroelectric module, Fujitsu is the leader today in commercial FeRAM production on 6-inch wafers producing a commercial 64k-bit FeRAM. This is one solution that the authors are pursuing. Should split processing by one of the U.S. wafer suppliers and Fujitsu be obtained, wafer thinning and die stacking techniques can be used to obtain the required density of the packaged radiation hardened FeRAMs. This type of

advanced packaging not only improves density, but also reduces weight, critical for space missions.

## 5. LONG TERM SOLUTIONS

Greater than 5 years from now, solutions for radiation tolerant nonvolatile memory may come from alternative new semiconductor technologies in development today. These technologies include advanced ferroelectric memories using a single ferroelectric transistor (1T) memory cell, chalcogenide amorphous glass memories, magneto-resistive memories, and magnetic tunnel junction memories, among others. While all these technologies can be made radiation tolerant, each approach has its unique advantages and disadvantages.

A new ferroelectric memory technology is being developed that can provide a long term solution for dense radiation hardened non-volatile memory for space missions. This advanced ferroelectric technology uses a ferroelectric transistor for the storage element instead of a ferroelectric capacitor. The memory cell size would be smaller than a DRAM memory cell and comparable to a Flash memory cell, with all of the favorable electrical and radiation characteristics of ferroelectric memory. Furthermore, the memory architecture provides for non-destructive read out, as compared to the destructive, DRAM-type read out of one-transistor, one-capacitor (1T/1C) ferroelectric memories currently in development.

Celis Semiconductor and COVA Technologies are jointly developing a ferroelectric memory using a 1T memory cell. A cross section of the 1T memory storage element is shown in Figure 3. Comparison of this new memory cell size to other semiconductor memory cell types is shown in Table 3. Memory sizes comparable to those of Flash memory and smaller than those of DRAMs may be obtainable.

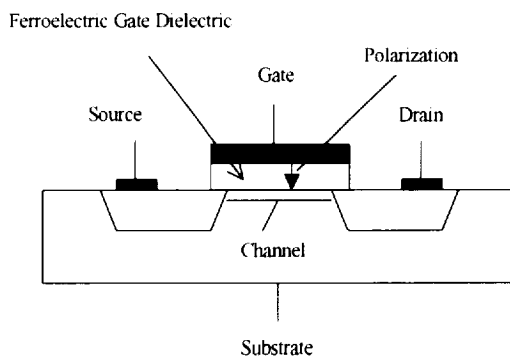


Figure 3. 1T Ferroelectric Memory Cell

Ease of manufacturing is a primary goal of the COVA/Celis advanced ferroelectric technology program. The memory cell is expected to integrate with CMOS more efficiently than a 1T/1C ferroelectric memory cell. Because of the ease of manufacturing, the production of dense radiation hardened ferroelectric memories by United States fabricators may become a reality.

The COVA/Celis ferroelectric memory technology, when mature, may eliminate the use of DRAMs. Because this new technology may replace both DRAM and Flash memories, this new technology may be more readily embraced by semiconductor companies to the point where it will receive the levels of R&D funding and efforts necessary to bring it into the mainstream.

Table 3. Comparison of Memory Cell Sizes.

Memory Cell Type	Cell Size ( $F^2$ )
SRAM	50 - 100
DRAM	7 - 12
Flash	5 - 12
DRO FeRAM (1T/1C)	25 - 75
NDRO FeRAM (1T)	5 - 6

## 6. CONCLUSIONS

The development of a radiation tolerant ferroelectric memories using split wafer processing methods and die stacking can provide a short term solution to meet the needs of today's aerospace marketplace. Longer term, a new ferroelectric technology using single transistor ferroelectric memory cells that is in development may provide very high density nonvolatile memories with non-destructive read out capabilities for the aerospace marketplace.

## 7. ACKNOWLEDGEMENTS

The previous split process FeRAM development program described in this paper was funded under a purchase order from the Jet Propulsion Laboratory, California Institute of Technology. The authors express their appreciation to the Jet Propulsion Laboratory, Sandia National Laboratories and Matsushita for their support of that program. The authors appreciate their numerous discussions and interactions with Jet Propulsion Laboratory, Sandia National Laboratory, Aeroflex/UTMC and Irvine Sensors personnel.

## 8. REFERENCES

- <sup>[1]</sup>J. M. Benedetto, G. F. Derbenwick and J. D. Cuchi-aro, "Single Event Upset Immunity of Strontium Bismuth Tantalate Ferroelectric Memories," *IEEE Transactions on Nuclear Science* (1999).
- <sup>[2]</sup>Measurements performed by Gary Swift of the Jet Propulsion Laboratory in 1999.
- <sup>[3]</sup>R. A. Moore, J. M. Benedetto, J. M. McGarrity and F. B. McLean. "Neutron Irradiation Effects on PZT Thin Films for Nonvolatile Memory Applications," *IEEE Trans Nucl. Sci.* NS-38, 1078-1082 (1991).
- <sup>[4]</sup>S. S. Lee, N. S. Kang, S. C. Philpy and G. F. Derbenwick, "Reliability and Performance of a 64K Ferroelectric Memory," *2000 IEEE Microelectronics Reliability and Qualification Workshop*, Glendale, CA; Oct. 31 - Nov. 1; Session V.3.
- <sup>[5]</sup>K. F. Strauss and T. Daud, "Overview of Radiation Tolerant Unlimited Write Cycle Non-Volatile Memory," *Proc. Of the 2000 IEEE Aerospace Conference*, Big Sky, MT, March 19-25, 2000.
- <sup>[6]</sup>J. Handy, "Where do ferroelectrics fit?," *Dataquest*, Feb 1, 1999 and *EDN*, "Exotic memories, diverse approaches, April 26, 2001.
- <sup>[7]</sup>Programmable Technologies Web Site, "A scientific study of the problems of digital engineering for space flight systems, with a view to their practical solution. Memories - Some Radiation Test Results," <http://klabs.org/memories.htm> (2001).
- <sup>[8]</sup>B<sup>2</sup>JT Test results courtesy of Aeroflex/UTMC, Colorado Springs, CO.

## About the Author



Stephen Philpy is a founder of Celis Semiconductor Corporation. He previously worked for Mostek and UTMC, developers of semiconductor memories and radiation hardened ASICs. He is also a founder of Symetrix Corporation, a developer of ferroelectric materials. He has been involved in the ferroelectrics industry since 1988. He has a BS in Electronics Engineering from Texas A&M University and an MBA from the University of Colorado.

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# Commercialization of 1T-Cell Ferroelectric Memories for Space Applications

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**Abstract** -- A new class of ferroelectric materials is under development with parameters ideally suited for 1T cell technology enabling low voltage operation with improved retention. This paper describes the approach taken to integrate the ferroelectric 1T cell module into a CMOS process with special emphasis on radiation hardness for space applications.

## TABLE OF CONTENTS

- 1 Introduction
- 2 Properties of the New Ferroelectric Material
- 3 Integration of the Ferroelectric Transistor Module
- 4 Summary
- 5 Biography

### 1. Introduction

Standard ferroelectric nonvolatile memories have relatively large memory cell sizes, leading to high manufacturing costs. A 1-transistor (1T) memory cell reduces the area requirements considerably rendering ferroelectric memories cost competitive. The ferroelectric material is deposited directly on silicon with a buffer layer in between silicon and ferroelectric. This interfacial oxide layer is desirable to provide a stable interface. Commonly used ferroelectric materials have relatively high dielectric permittivity so that most of the applied voltage drops over this interfacial layer making low voltage operation difficult. Another challenge in a 1T cell is to achieve adequate data retention, which is negatively impacted by the depolarization field, mobile ionic charges and charge injection.

A new class of ferroelectric materials is under development with parameters ideally suited for 1T cell technology enabling low voltage operation with improved retention. The material is deposited by MOCVD using liquid precursor injection into a flash evaporator.

In order for ferroelectric memories to become mainstream, in addition to a competitive cell size, other manufacturing challenges have to be met. The most important one is the integration of the ferroelectric module into a manufacturing process (e.g. CMOS) in a cost effective and technically reliable manner. This paper describes the potential CMOS integration approaches with special emphasis on preserving the radiation hardness of the process for space applications.

### 2. Properties of the new ferroelectric material

Table I lists the typical parameters we have achieved, measured on a Metal-Ferroelectric-Oxide-Semiconductor (MFOS) capacitor. Figure 1 shows a typical CV plot. The arrows in Figure 1 indicate the direction the hysteresis loop is traversed. For n-type silicon a counter clockwise direction is consistent with ferroelectric switching and distinguishes ferroelectric switching from charge injection at the silicon interface.

The most important characteristics of the new material are the low dielectric permittivity ( $\epsilon_r \sim 10$ ) and the high transition temperature ( $>700^\circ\text{C}$ ). A low  $\epsilon_r$  enables low voltage operation and, indirectly, improves retention, whereas a high transition temperature is important for cost effective and reliable integration of the ferroelectric transistor module into CMOS. The integration challenges will be described in more detail in the next section.

### 3. Integration of the ferroelectric transistor module

Since the new ferroelectric material is a high temperature material with a transition temperature (Curie temperature) of greater than  $700^\circ\text{C}$  (see Table I) the

Parameter	Value	Parameter	Value
Non-switching permittivity	~7	Ferroelectric layer thickness	230 ± 10 nm
Switching permittivity	~ 16	Leakage current (+5V)	5 x 10 <sup>-8</sup> A/cm <sup>2</sup>
Switching speed	<50 ns	Leakage current (-5V)	5 x 10 <sup>-8</sup> A/cm <sup>2</sup>
Switching voltage	~ 1-3 V	Flatband voltage shift (memory window)	~ 2-3 V
Polarization	~0.2 μC/cm <sup>2</sup>	Coercive field	50 kV/cm
Memory cell size potential	<6 f <sup>2</sup>	Curie Temperature	~ 700 °C

Table I Typical parameters for a ferroelectric 1T cell with the new material

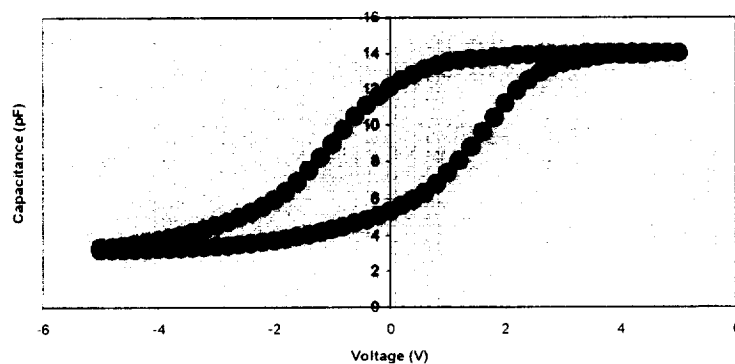


Figure 1 CV curve of MFOS capacitor

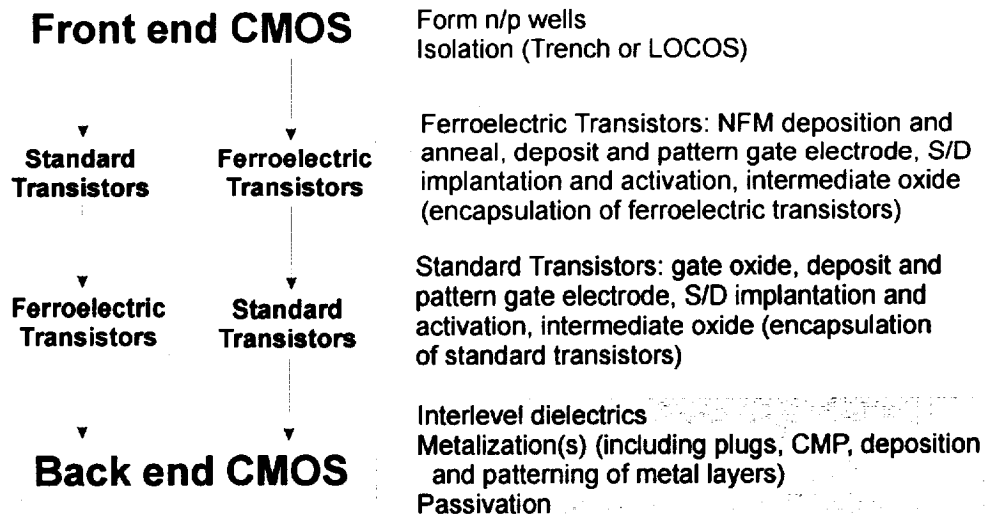


Table II Integration of ferroelectric transistor module into CMOS

ferroelectric transistor module can be integrated into a standard CMOS flow early in the process. The ferroelectric transistors can be formed either before or after the formation of the standard transistors as described in Table II.

The new material has high vapor pressure so that the probability that volatile species could be transported from one part of a wafer to another and introduce contaminants is low.

In order to avoid even this small probability of contamination, the ferroelectric transistors can

be encapsulated with a protective layer if they are formed prior to the standard transistors, or the standard transistors can be encapsulated if they are formed first. For maximum protection both types of transistors can be encapsulated. Figure 3 shows a cross section of a ferroelectric transistor integrated into a one-poly, three-metal layer CMOS process. In this implementation the ferroelectric transistor is formed prior to the standard CMOS transistors and encapsulated with a thin oxide layer deposited with MOCVD.

### Ferro transistors **prior** to standard transistors

1. Form n/p wells
2. Isolation (trench or LOCOS)
3. Form ferroelectric transistors (NFM deposition and anneal, deposit and pattern gate electrode, S/D implantation and activation)
4. Intermediate oxide (encapsulation of ferro transistors)
5. Form standard transistors (gate oxide, deposit and pattern gate electrode, oxide spacers, S/D implantation and activation)
6. Intermediate oxide (encapsulation of standard transistor)
7. Interlevel dielectrics
8. Metalization(s) (including plugs, CMP, deposition and patterning of metal layers)
9. Passivation

### Ferro transistors **after** standard transistors

1. Form n/p wells
2. Isolation (trench or LOCOS)
3. Form standard transistors (gate oxide, deposit and pattern gate electrode, oxide spacers, S/D implantation and activation)
4. Intermediate oxide (encapsulation of standard transistors)
5. Form ferroelectric transistors (NFM deposition and anneal, deposit and pattern gate electrode, S/D implantation and activation)
6. Intermediate oxide (encapsulation of ferro transistor)
7. Interlevel dielectrics
8. Metalization(s) (including plugs, CMP, deposition and patterning of metal layers)
9. Passivation

Table III Process Integration of ferroelectric transistor

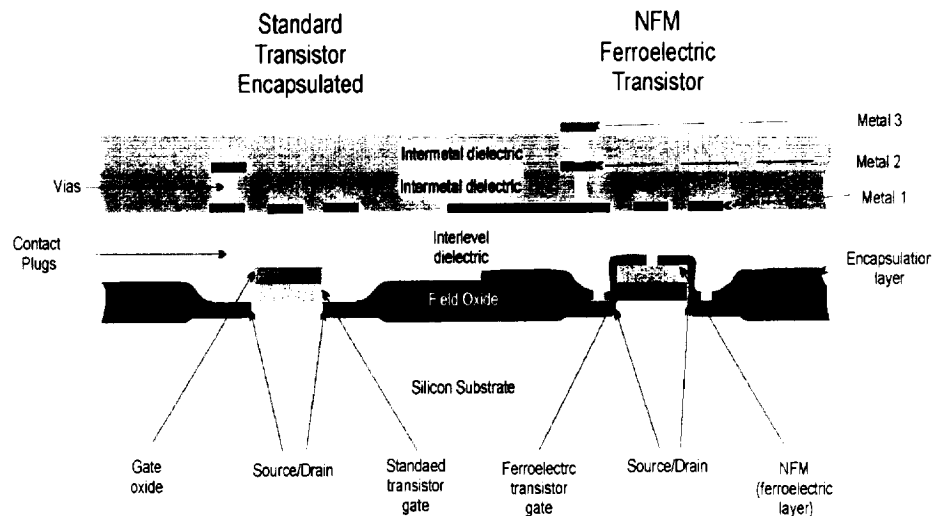


Figure 3 Cross section of standard transistor and ferroelectric transistor integrated into one-poly, three-metal CMOS process

Table III is a brief process flow for these two main variations of integration. The high processing temperature of our new material of approximately 850 °C, which would be unacceptable for a standard 1T1C cell technology, is an advantage for the integration of a ferroelectric transistor. It allows high temperature CMOS processing steps such as junction activation, polysilicon deposition and doping to be performed after the formation of the ferroelectric transistors. Depending on the thermal budget of the CMOS process certain steps could be combined in order to simplify processing. Examples are junction activation of both standard and ferroelectric transistors.

#### 4. Summary

A ferroelectric transistor module based on a new ferroelectric material is under development. In addition to having a low dielectric permittivity enabling low voltage operation and optimum interface properties, the new material has a high transition temperature (Curie temperature) facilitating integration into CMOS. The material can withstand the processing temperatures associated with polysilicon deposition, junction activation and so on. The ferroelectric module can be integrated either before or after the formation of the standard transistors.

The ferroelectric transistors can be encapsulated with an oxide layer preventing any potential contaminants to escape. No major modifications to the CMOS process are required.

The ferroelectric transistor, due to the ionic rather than electronic storage mechanism, is inherently radiation hard. The proposed integration will preserve the radiation hardness of the CMOS process and we expect the ultimate radiation performance to be limited by the radiation hardness of the underlying CMOS process.

#### 5. Biography

Dr. Fred P. Gnadinger is President and CEO of COVA Technologies, Inc., a semiconductor fabrication equipment company in the field of liquid injection - and flash evaporation systems for complex oxide deposition systems based on MOCVD. Prior to COVA he was President and CEO of Microtronix Corporation, a company he founded in 1990 to develop ferroelectric technology and products for nonvolatile memories.

Dr. Gnadinger is the prior Chief Operating Officer and Chief Technical Officer of Ramtron Corporation, a public semiconductor company engaged in the development of semiconductor memories based on ferroelectric technology.

Dr. Gnadinger holds a Ph.D. degree in Electrical Engineering from the University of Kansas, Lawrence, Kansas, and an MSEE degree from the Swiss Federal Institute of Technology (ETH), Zurich, Switzerland. Dr. Gnadinger holds 6 US Patents and several foreign Patents and has numerous publications including a book chapter published by Academic Press, New York. He has also given many talks at Scientific Conferences and has been an invited speaker on several occasions.



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## ***SESSION #6: Magnetic Memories***

Thursday, November 8, 2001

2:20 PM – 3:40 PM

Chair: *J. Zhu*, Carnegie-Mellon University

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- 2:20 PM      Magnetic Random Access Memory (MRAM) and its prospects;  
*K-M Lenssen*, Philips Research Laboratories, *E. Persoon*, Philips  
Semiconductors
- 2:40 PM      Vertical Magnetoresistive Random Access Memory: Promises and  
Challenges; *J. Zhu*, Carnegie Mellon University, *G. Prinz*, Naval  
Research Laboratory
- 3:00 PM      Criteria for Magnetic Tunnel Junctions; *I. Schuller*, University of  
California at San Diego
- 3:20 PM      A Modified MRAM Architecture without a Current Rectifier Per Cell;  
*F. Wang*, University of North London



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# Magnetic Random Access Memory (MRAM) and its prospects

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**Abstract**—Recently the R&D activities concerning Magnetic Random Access Memory (MRAM) have shown an acceleration. Commercial MRAM products are planned to enter the market as early as 2004. In this paper first an overview will be given of the recent developments and the present status of MRAM. Potential issues (like thermal stability, magnetic shielding) will be discussed and some ideas for improvements will be proposed. In order to obtain indications for the most attractive MRAM application areas, the total (multi-billion-dollar) memory market can be divided in three segments: embedded memory, companion memory and removable memory, differing in the percentage of the chip area that is occupied by memory. In each of these segments MRAM will have to compete with different types of conventional memory (that form the present solutions) and therefore will also have to meet different specifications. It is likely that two variants of MRAM will be developed: a high-performance version (with fast read and write) and a low-cost MRAM (with high density) to target the different market needs.

[1,2,3]). This definition implies that its operation relies on a magnetoresistance phenomenon. Early MRAMs based on the anisotropic magnetoresistance (AMR) effect were limited in their use mainly to military and space applications, since the amplitude of the AMR effect in thin films is typically less than 5%.

The discovery in 1988 of the giant magnetoresistance (GMR) effect [4] and a breakthrough in the field of magnetic tunnel junctions around 1995 [5] improved the perspectives of MRAM and enabled, in principle, the realization of MRAMs for general applications. Tunnel magnetoresistance (TMR) effects with amplitudes up to >50% have been shown, but because of the strong bias-voltage dependence, the useable resistance change in practical applications is at present around 30%. While the GMR effect is already applied in commercial products like HDD read heads [6] and magnetic sensors [7], this is not yet the case for magnetic tunnel junctions.

In general, both GMR and TMR result in a low resistance if the magnetization directions in the multilayer are parallel, and in a high resistance when the magnetizations are oriented antiparallel.

The addressing of the MRAM is done by means of an array of crossing lines. Writing a certain cell is equivalent to setting a magnetization in the desired direction (for example, magnetization to the left means '0' and magnetization to the right means '1'). By applying a current pulse to a bit line and a word line a magnetic field pulse is induced. Only the MRAM cell at the crossing point of both lines experiences the maximum magnetic field (i.e. the vectorial addition of the fields induced by both current pulses) and its magnetization is reversed; all other MRAM cells below the bit or word line are exposed to the significant lower field that is caused by a single current pulse and will therefore not change their magnetization directions.

The read-out method depends on the type of MRAM. In the case of exchange-biased magnetic tunnel junctions

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1. INTRODUCTION
2. PRESENT STATUS OF MRAM
3. SOME POTENTIAL TECHNICAL ISSUES
4. COMPARISON WITH OTHER MEMORY TYPES
5. MEMORY MARKET SEGMENTS
6. CONCLUSIONS
7. ACKNOWLEDGMENTS

## 1. INTRODUCTION

An MRAM is a memory (1) in which the stored data are represented by magnetization directions and (2) in which the read-out is done by a resistance measurement (for a recent overview about MRAM see, for example, Refs.

with a fixed magnetization direction the data are stored in the other, free magnetic layer, which of course should not be disturbed by the read-out. In this case the absolute resistance of the cell is measured (if desired, differentially with respect to a reference cell). This cell is selected by means of a switching element (usually a transistor), which implies that in this case one transistor is required per cell.

## 2. PRESENT STATUS OF MRAM

In the last year the R&D activities concerning MRAM have shown an acceleration. In December 2000 IBM and Infineon announced a cooperation on MRAM development [8,9]. It was stated that MRAM products would be commercially available already in 2004; this would relate to 128 Mb or 256 Mb memories in 0.13  $\mu\text{m}$  technology. This timing corresponds to the planning of Motorola who announced samples in 2003 and volume production in 2004. In June 2001 [10] it was even stated that volume production would be only 1.5 year away as Motorola and IBM speed up their development work. Also major progress has been made in the field of MRAM demonstrators: at the ISSCC2001 Motorola presented a complete 256kb MRAM chip in 0.6  $\mu\text{m}$  technology [11]. In the meantime USTC very recently claimed the demonstration of the first commercial MRAM on their website [12], although samples are not yet available. While most others concentrate on TMR, USTC uses the GMR effect in their MRAM.

Other industrial companies active in MRAM research and development include Hewlett-Packard, NVE, Toshiba, NEC, Samsung, Read-Rite and Philips.

In the field of more fundamental research a breakthrough was the observation of 96% spin polarization in a half-metallic ferromagnetic material (a single-crystal film of  $\text{CrO}_2$ ) [13,14]. Although it is still unclear whether it will be easily possible to implement this material in MRAM, this opens up perspectives for significantly larger magnetoresistance ratios in future MRAMs.

## 3. SOME POTENTIAL TECHNICAL ISSUES

In our previous overview [3] we identified already several possible issues or weaknesses of MRAM. In the following some issues will be discussed and some solutions will be proposed without aiming at completeness.

- *Cell size*

As we pointed out already earlier, the cell size is mainly determined by the metal line width that is required because of the current pulses; therefore, the use of copper metallization enables much smaller cells. In the demonstrator of Motorola cell sizes of  $20F^2$  (with  $F$  being the smallest feature size) were already obtained, which is indeed smaller than the size that we had calculated for 0.18  $\mu\text{m}$  technology with TiW/Al metallization [3].

- *Temperature stability*

CMOS processes usually include an anneal step at or above 400°C. Considering our experiences on the thermal stability of GMR sensors [15] this seems to be a serious issue for embedded memories, if one wants to adhere to the standard CMOS process.

- *Resistance and scaling*

The resistance of GMR elements is so small that one can wonder if they can be used to realize MRAM memories that can compete with Flash.

In principle there are two possibilities:

1. if one connects several (let's say:  $N$ ) GMR elements in series in order to increase the total resistance, the magnetoresistance effect is divided by the number  $N$ . That means a net resistance change of  $\sim 1\%$  or less (e.g. 16 elements with 8% GMR effect results in 0.5% resistance change); this means a signal change to be detected of only several mV's (since the resistance per square is around 15  $\Omega$  and an element will comprise a few squares). That is probably too small to realize easily in a reliable low-power and cost-effective way.
2. if one switching element is used per GMR element, one has indeed the whole GMR effect (e.g. 8% resistance change) available to detect, but the difference in resistance between a single GMR element and a transistor is so large, that that it is difficult to measure the resistance change in an efficient way. That would mean that either one has to measure for a long time, or a so complicated read-out method is needed that the total cell area becomes too large.

Therefore we believe that TMR is more promising for MRAM than GMR at this moment.

It should be noted that for TMR the scaling of the resistivity (which depends on the thickness of the tunnel-barrier layer) is crucial in order to be able to follow Moore's law. With the present status this seems however already possible for at least three generations. After that, new tunnel barriers with a lower energy barrier may allow further scaling.

- *Thermal relaxation*

If magnetic elements become very small, their magnetizations can switch spontaneously. In the following we will discuss, using simple estimations, in what range of dimensions limits due to this so-called superparamagnetic effect might be expected.

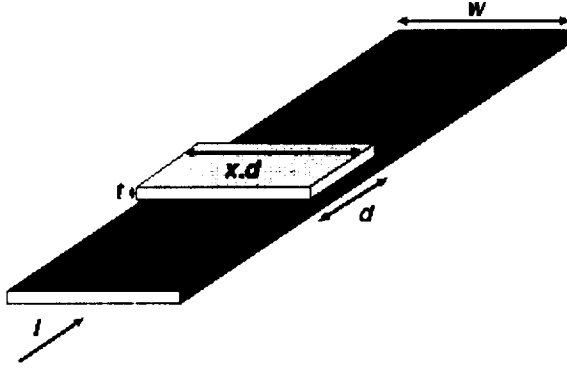


Figure 1 Schematic view of a magnetic element and write conductor

Consider a magnetic element with width  $d$ , length  $xd$  and thickness<sup>1</sup>  $t$  (Figure 1). Then the volume  $V$  is

$$(1) \quad V = txd^2.$$

A current  $I$  in a conductor with width  $w$  that is close to the element induces a write field  $H$ .

For thermal stability at a temperature  $T$  it is required that

$$(2) \quad (K_{\text{eff}}V)/(k_B T) \geq R,$$

with the ratio  $R$  for example  $50^2$ .

The effective anisotropy constant  $K_{\text{eff}}$  is given by

$$(3) \quad K_{\text{eff}} = H \mu_0 M_s / 2$$

(in which  $M_s$  is the saturation magnetization) and so it follows that the general condition for thermal stability is

$$(4) \quad (H \mu_0 M_s V)/(2k_B T) \geq R.$$

This is comparable to the condition mentioned in [2].

A first, very simple estimation is the following. If the write conductor with width  $w$  is close to the element (i.e. on a distance much smaller than  $w$ ) the current  $I$  induces a write field:

$$(5) \quad H = I/(2w).$$

The combination of equations (1), (5) and (4) leads to the condition:

$$(6) \quad (I \mu_0 M_s t x d^2)/(4wk_B T) > R.$$

or, with  $w = xd$ ,

$$(7) \quad d \geq (4k_B TR)/(I \mu_0 M_s t)$$

With  $t = 6$  nm,  $x = 4$ ,  $M_s = 1.4$  MA/m (value for e.g. Co-Fe),  $T = 350$  K,  $I = 1$  mA,  $R = 50$ ,  $\mu_0 = 4\pi \cdot 10^{-7}$  H/m and  $k_B = 1.3807 \cdot 10^{-23}$  J/K this results, for example, in:

$$(8) \quad d > 92 \text{ nm}.$$

It has to be noted that in general  $d$  will be larger than the smallest feature  $F$  of a technology node; so, for example, in a 50 nm technology,  $d$  will probably still be at least 100 nm. It has implicitly been assumed that the distance between the write conductor and the magnetic element is significantly smaller than  $w$ .

This estimation is oversimplified, but it already indicates that the theoretical limits are around the technology nodes of interest for MRAM (50-100 nm)

The exact relation between  $I$  and  $H$  can also be left undefined. In that case the condition (4) can be written as

$$(9) \quad d > \sqrt{(2k_B TR)/(H \mu_0 M_s t x)}.$$

If we fill in again as an example  $t = 6$  nm,  $x = 4$ ,  $M_s = 1.4$  MA/m,  $T = 350$  K,  $R = 50$ ,  $\mu_0 = 4\pi \cdot 10^{-7}$  H/m and  $k_B = 1.3807 \cdot 10^{-23}$  J/K this leads to the condition

$$(10) \quad d \geq \sqrt{(1.1445 \cdot 10^{-11})/H}.$$

Now different values of the write field  $H$  can be filled in. For example, we could argue that the write field should be as small as possible; nevertheless it should be significantly larger than the earth magnetic field (which is around 40 A/m). For example, for  $H = 500$  A/m,

$$(11) \quad d \geq 151 \text{ nm}.$$

is obtained.

If, however, we argue that we want to use at maximum 1 mA through a 50 nm wide conductor (which is significantly closer than 50 nm to the magnetic element), we fill in  $H = 10^4$  A/m and find

$$(12) \quad d > 34 \text{ nm}.$$

Without experimental experience no absolute certainty can be obtained with respect to scaling limits of MRAM due to thermal relaxation of magnetic elements. The estimations are around the smallest feature sizes of the technology nodes of interest (50-100 nm). Depending on the choice of the parameter values smaller answers (e.g. in [16] the authors even claim that their MRAM can be as small as 30 nm), but also larger answers can be obtained (e.g. 100 nm  $\times$  400 nm in [17] but the authors propose their Curie-point written MRAM as a solution which allows further scaling).

On the positive side: magnetic "tricks" may be possible and have not yet been taken into account. For example, NVE proposes thermally assisted writing [2,17]; also it is possible to increase the effective volume of the element by using multiple

<sup>1</sup> The relevant thickness has to be taken, for example the thickness of the magnetic layer in which the data are stored.

<sup>2</sup> The choice of the value may depend on the environment and the required life time.

layers

- **Magnetic shielding**

In order to shield from external magnetic fields a shielding layer may be desirable, since the magnetic bits can be affected by fields as low as 1.5 kA/m. Intuitively, one would take a thick continuous layer, but we found that actually a non-continuous layer will be better in order to avoid the problem of saturation as will be shortly discussed in the following.

First we considered a continuous, softmagnetic layer which is deposited over the whole MRAM as a shield (see Figure 2).

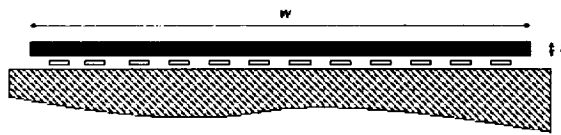


Figure 2. Schematic view of a continuous magnetic layer for shielding

The following calculations show that this method can not always provide the required degree of shielding in practice. We assume that the distance between the MRAM cells and the shield is much smaller than the width of the shield.

The first problem is saturation (particularly in the middle part of the shield).

$$(13) M = \chi(H_{\text{appl}} - NM)$$

with the demagnetization factor  $N = t/w$  in good approximation, the susceptibility  $\chi$ , the externally applied field  $H_{\text{appl}}$  and the magnetization  $M$ . Saturation occurs if  $M \geq M_s$ . It can be derived that the following inequality has to be obeyed in order to avoid saturation:

$$(14) N > (H_{\text{appl}}/M_s) - 1/\chi$$

For example, for values of  $H_{\text{appl}} = 80$  kA/m,  $M_s = 800$  kA/m and  $1/\chi$  negligible this means  $(t/w) > 80/800 - 0 = 0.1$ . Since the width  $w$  of the MRAM chip is in the order of 1 mm this would result in an unrealistically large value of the layer thickness  $t$ .

Second, the shielding factor should be sufficient. Below saturation the magnetic field is given by:

$$(15) H = H_{\text{appl}} / (1 + N\chi)$$

So, for example, in order to attenuate a field of 80 kA/m to 0.8 kA/m:

$$(16) (t/w) > 99/\chi$$

This means again that the ratio  $(t/w)$  should be as large as possible. For widths in the order of a chip

diameter this is very impractical or even impossible. As a (at first sight contra-intuitive) solution we propose to use a discontinuous shield.

In this case  $w$  can be, for example, in the order of 1  $\mu\text{m}$ , which makes the required values for  $t$  in order to fulfil the relations (14) and (16) practically feasible. Of course, care has to be taken that the distance between shield and memory cell is small enough in order to avoid 'distance losses'.

If the shielding that is obtained by this idea would still be insufficient, the sensitivity of the MRAM itself to external fields could be reduced, for example by implementing the idea of an earlier patent application [18]. The combination of these ideas can provide an MRAM that is much more robust against external disturbing fields than presently existing or proposed MRAMs.

#### 4. COMPARISON WITH OTHER MEMORY TYPES

In [3] we already compared MRAM with other types of embedded non-volatile memory. Although strong progress has been achieved in the field of MRAM (as discussed above), the main strengths and weaknesses have roughly remained the same.

MRAM is, however, not only a potentially interesting alternative for non-volatile memories like Flash and EEPROM, but also for volatile memories like SRAM and DRAM. For all of these conventional memories foreseen problems in scaling have been reported. Further, the use of MRAM is not on beforehand limited to only embedded memory.

It is commonly known that Flash technology faces problems, like the rapid increase in the number of masks, the limited endurance and the power consumption. MRAM is an interesting alternative since it is much faster and does not show the endurance limitations. For DRAM problems are expected for further scaling, since the aspect ratio cannot continue to increase [20]. MRAM might be able to replace DRAM and has the additional advantage of non-volatility.

And even the radiation hardness of MRAM may become important for commercial applications, since radiation in the operation environment is reported to cause significant problems for small SRAM devices [21].

Of course, one of the most intriguing promises of MRAM is that it may replace more than one type of conventional memory.

#### 5. MEMORY MARKET SEGMENTS

The total (multi-billion-dollar) memory market can be divided in the following three segments (see also Figure 3):

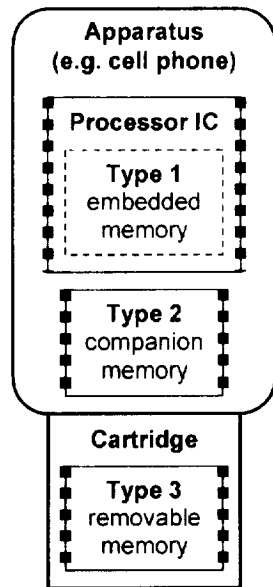


Figure 3: Schematic view of the three types of memory

- Type 1: Embedded MRAM*  
 Embedded MRAM focuses on IC solutions in which the embedded memory typically fills 50% of the chip area. In this market segment MRAM mainly has to compete with current embedded Flash and SRAM applications. In order to replace embedded Flash the cell size of MRAM ( $\sim 20F^2$ ) is probably already competitive. Since the cell size of SRAM is relatively large ( $\sim 150F^2$ ), replacement by MRAM would even result in a significant area reduction in this case. Combined with the general trend to move off-chip memory to on-chip memory (particularly for low-power and high-speed applications), MRAM has clear advantages if it can provide the desired speed (which is probably the case for replacement of all but the fastest SRAM).
- Type 2: MRAM as companion IC*  
 This type of ICs typically contains  $\sim 90\%$  of memory; mainly DRAM, SRAM or Flash. As discussed in the previous section, MRAM can offer advantages over all these three memory types, but in order to be really competitive the requirements for the cell size are more stringent, probably around  $12F^2$ .
- Type 3: MRAM for removable (mass) storage*  
 This last type of ICs consists for more than 90% of memory. Probably this will be the largest market in volume, but low cost will be of utmost importance. The present 2-bits-per-cell NAND-flash has an equivalent cell size in the order of  $4F^2$ . This means that MRAM would need a similar cell size for this market segment, unless the present memory solutions would run into serious problems.

As can be concluded from the above, speed is expected to be the dominant factor for competitiveness for type 1, while for type 3 this will be cell size.

For the 1T1MTJ MRAM on which most current R&D efforts are focused the lower limit for the cell size is probably not much below  $10F^2$ . That means that the required cell sizes for type 1 and type 2 applications may be feasible, but that the cell size will be too large for type 3 applications. Of course, multibit MRAM cells could be considered [22]. A more principal solution is, however, to leave out the transistor from some or all of the MRAM cells in a memory array and work with real cross-point geometry cells. This would enable to reduce the cell size significantly, but at the cost of a larger read time. If the transistors would be removed from all the cells in the array, this even allows, in principle, to stack memory arrays on top of each other and/or on top of logic. Although still speculative, this is a very intriguing perspective for reduction of memory area and cost. Speed will probably be the limiting factor for type 1 applications, so in order to achieve the required performance, a transistor per cell will probably remain desirable.

## 6. CONCLUSIONS

We have given a short overview of the recent developments and the present status of MRAM. Some potential issues, in particular thermal relaxation and magnetic shielding, have been discussed and some possible solutions proposed. We believe that TMR is more promising for commercial MRAM than GMR at this moment because of the low resistance and magnetoresistance ratio of the latter. We have made a division of the total potential MRAM market into three segments (embedded, companion and removable memory). Since for embedded memory speed is probably the limiting factor, while for removable memory this is density, we consider it likely that two variants of MRAM will be developed: a high-performance version (based on a 1T1MTJ cell) and a low-cost version (based on a 0T1MTJ cell).

## 7. ACKNOWLEDGMENTS

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## REFERENCES

- [1] M. Johnson, "Magnetoelectronic memories last and last...", IEEE Spectrum, February 2000, 33 (2000)

[2] J. Daughton, "Magnetoresistive Random Access Memory (MRAM)", <http://www.nve.com>, (2000)

[3] K.-M.H. Lenssen, G.J.M. Dormans and R. Cuppens, "Expectations of MRAM in comparison with other non-volatile memory technologies", Proceedings Non-Volatile Memory Technology Symposium 2000 (November 15-16, 2000, Arlington VA, U.S.A.), pp.26-31 (2000)

[4] G. Binasch, P. Grünberg, F. Saurenbach and W. Zinn, "Enhanced magnetoresistance in layered magnetic structures with antiferromagnetic interlayer exchange", *Phys. Rev.* **B39**, 4828 (1989); M.N. Baibich, J.M. Broto, A. Fert, F. Nguyen Van Dau, F. Petroff, P. Etienne, G. Creuzet, A. Friederich and J. Chazelas, "Giant magnetoresistance of (001)Fe/(001)Cr magnetic superlattices", *Phys. Rev. Lett.* **61**, 2472 (1988)

[5] J.S. Moodera, I.R. Kinder, T.M. Wong and R. Meservey, "Large magnetoresistance at room temperature in ferromagnetic thin film tunnel junctions", *Phys. Rev. Lett.* **74**, 3273 (1995)

[6] See, for example, C.H. Tsang, R.E. Fontana Jr., T. Lin, D.E. Heim, B.A. Gurney and M.L. Williams, "Design, fabrication, and performance of spin-valve read heads for magnetic recording applications", *IBM J. Res. Dev.* **42**, 103 (1998)

[7] For a recent overview about GMR sensors see, for example, K.-M.H. Lenssen, D.J. Adelerhof, H.J. Gassen, A.E.T. Kuiper, G.H.J. Somers and J.B.A.D. van Zon, "Robust giant magnetoresistance sensors", *Sensors&Actuators A85*, 1 (2000)

[8] Press releases from IBM and Infineon (see, e.g. [http://www.chips.ibm.com/news/2000/1206\\_infineon.htm](http://www.chips.ibm.com/news/2000/1206_infineon.htm) or [http://www.infineon.com/news/press/012\\_020e.htm](http://www.infineon.com/news/press/012_020e.htm))

[9] "IBM and Infineon unveil magnetic memory chips", <http://www.cnn.com/2000/TECH/computing/12/07/ibm.reut/index.html> (2000)

[10] J. Aslett, "Magnetic RAM to hit market a year early", *Electronics Times*, June 18, 2001, <http://www.electronicstimes.com/story/OEG20010615S0027>

[11] P.K. Naji, M. Durlam, S. Tehrani, J. Calder and M.F. DeHerrera, "A 256kb 3.0V 1T1MTJ Nonvolatile Magnetoresistive RAM", Digests of the ISSCC 2001, paper 7.6 (2001)

[12] <http://www.unionsemiconductor.com/VideoClips.htm>

[13] Y. Ji, G.J. Strijkers, F.Y. Yang, C.L. Chien, J.M. Byers, A. Anguelouch, Gang Xiao and A. Gupta, "Determination of the Spin Polarization of Half-Metallic CrO<sub>2</sub> by Point Contact Andreev Reflection", *Phys. Rev. Lett.* **86**, 5585 (2001)

[14] R. Colin Johnson, "Magnetic spin locks data into MRAMs", *EE Times*, July 17, 2001, <http://www.eetimes.com/story/OEG20010717S0064>

[15] K.-M.H. Lenssen, A.E.T. Kuiper, J.J. van den Broek, R.A.F. van der Rijt and A. van Loon, "Sensor properties of a robust giant magnetoresistance material system at elevated temperatures", *J. Appl. Phys.* **87**, 6665 (2000)

[16] J.-G. Zhu, Y. Zheng and G.A. Prinz, "Ultrahigh density vertical magnetoresistive random access memory", *J. Appl. Phys.* **87**, 6668 (2000)

[17] R.S. Beech, J.A. Anderson, A.V. Pohm and J.M. Daughton, "Curie point written magnetoresistive memory", *J. Appl. Phys.* **87**, 6403 (2000)

[18] K.-M.H. Lenssen and H.W. van Kesteren, "Device comprising a first and a second ferromagnetic layer separated by a nonmagnetic spacer layer", US Patent 6,252,796

[20] M. Oishi and T. Matsumoto, "US makers ready MRAM for post-DRAM era", *Nikkei Electronics Asia*, 26-40, May 2001

[21] A. Cataldo, "SRAM soft errors cause hard network problems", *EE Times*, August 17, 2001, <http://www.eet.com/story/OEG20010817S0073>

[22] R. Zhang, M.M. Hassoun, W.C. Black Jr., B. Das and K.A. Wong, "Demonstration of a four state sensing scheme for a single pseudo-spin valve GMR bit", *IEEE Trans. Magn.* **35**, 2829 (1999); W.-C. Jeong, B.-I. Lee and S.-K. Joo, "Three level, six state multilevel magnetoresistive RAM (MRAM)", *J. Appl. Phys.* **85**, 4782 (1999)

## BIOGRAPHIES



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## Vertical Magnetoresistive Random Access Memory: Promises and Challenges

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### Introduction

Today, the most common archival memory in a computer system is the disk drive, in which data is stored in magnetic disks. When a computer is turned on, data is first loaded from the disk drive into the memory system, i.e. SRAMs and DRAMs, all of which require standby power to maintain their memory states. Since retrieving data from a disk drive is a relatively slow process (the data access time of a disk drive is at least 100,000 times slower than that of computer memory), the "booting" period of a computer or the opening of an application can be long and frustrating.

A new kind of random access memory is on the horizon of commercialization and is being referred to as magnetic (or magnetoresistive) random access memory, or MRAM[1]. In this new kind of memory, a bit, "0" or "1", is stored as the orientation of the magnetic moment in a small size thin film element and, since no electric power is needed to maintain the memory state, it is non-volatile. At present, they are focused toward replacing the slow and expensive FLASH memory. Some of the designs even have the potential to replace SRAM, DRAM and perhaps disk drives in some applications. The ability to use MRAM for replacing disk drives will enable the entire computer system to be made on a single silicon chip, opening a new era for portable and miniaturized computers.

Here, we would like to introduce an MRAM design that is targeted for ultra-high area storage density, fast access time, low cost, robust performance, and good extendibility. It is referred to as the vertical magnetoresistive random access memory, or VMRAM [2]. Besides this design, there are three other major existing designs that have been reported in various literature [3][4][5][6]. They will be briefly mentioned for performance comparison reasons.

### The Design and Operation Mechanisms of the VMRAM

The memory element in the VMRAM device is a circular shaped giant magnetoresistive (GMR) multilayer thin film stack with a circular hole in the middle. The simplest structure of a memory element, or a memory stack, consists of two ferromagnetic layers, one thin and one thick, sandwiching a non-magnetic conductive layer. Electrodes are connected on the top and bottom of the magnetic stack, as shown in Fig. 1. A large number of memory elements, e.g. 256 of them, are connected in series to form what we call the "bit line". (A memory array would consist of a large number of bit lines in parallel.) For each

memory element, there are two pairs of parallel conducting wires running over and under the memory element for read/write addressing in an array, which are referred to as word lines. An example of word line arrangement is shown in Fig. 2.

One of the keys to this design is that each magnetic memory element is shaped like a washer, resulting in a circular orientation of the magnetic moment, either clockwise or counterclockwise. The magnetic moment orientation of a memory element can be switched, either from clockwise to counterclockwise or vice versa, in the following way: current pulses in the word lines, flowing in the directions shown in Fig. 3, generate a radial magnetic field, rotating the magnetic moment into the radial direction. A subsequent current pulse sent through the bit line will generate a circular magnetic field, switching the magnetic moment into the new circular orientation. The combination of the word line and bit line current fields not only produces a very efficient and reliable switching mode, but also provides the necessary addressing scheme for selecting a single memory cell along a bit line. The threshold of the current magnitudes for switching the magnetic moment direction, referred to as switching currents, is proportional to the thickness of the memory element (as well as the saturation magnetization).

The read operation relies on the vertical giant magnetoresistive effect in the memory stack: when the magnetization orientation in the two magnetic layers in the memory stack have the same orientation, the resistance of the stack is low; when they have opposite orientation, the resistance is high. In a VMRAM memory cell, a "1" or "0" is stored as the magnetic moment orientation, clockwise or counter-clockwise, in the thicker layer of the magnetic sandwich. To read the memory state, two current pulses with opposite directionality are sent sequentially through the bit line with word lines turned on to address a selected element along a bit line. The magnitudes of the bit line and word line current are set large enough to switch the magnetic moment of the thin magnetic layer in the memory stack, but not large enough to switch that of the thick layer. During this operation, the magnetic moment of the thin layer is switched back and forth for interrogating the moment orientation of the thick layer. The difference in the voltage values of the bit line between the first and second current pulses, positive or negative, determines the moment orientation in the thick layer, hence the memory state. This dynamic readout scheme requires no transistor in each individual bit cell for addressing.

In a write operation, relatively larger magnitudes of both the word line current and bit line current are used to rotate the thick layer moment of a selected memory element. Computer simulation shows that either a read cycle or a write cycle of an individual memory element finishes within 1 nanosecond.



### **Comparisons with Other Existing MRAM Designs**

In all the existing MRAM designs other than the VMRAM, the magnetic moment in the memory elements is linearly oriented. The main problem of the linear magnetization mode is the stray field (outside of the element) and the demagnetization field (within the element) generated from the magnetic poles formed at the ends of the elements. If the ends are flat as shown in Fig. 4, the strong demagnetization field can yield formation of complicated edge domains and cause the switching field threshold of the magnetic moment to fluctuate uncontrollably. Therefore, in practice, the ends of the memory elements are tapered into sharp tips to eliminate edge domains. The requirement for sharp ends may force the size of the memory element to be much larger than the critical dimension of fabrication technology. Possible shape variation of the tapered ends from element to element due to a fabrication process could yield severe variation of the switching field, degrading the write addressing capability in a memory array. In addition, the stray field from the element ends, even tapered ends, generates interference with adjacent memory elements in an array, limiting the packing density of the memory cells.

The circular magnetization mode in the VMRAM design is the most stable magnetic configuration and the magnetic flux closure produces no stray field and no demagnetization field. The elements can be packed as close as the fabrication technique allows. A single bit memory cell can be as small as  $4\lambda^2$  where  $\lambda$  is the critical dimension (It is possible to fabricate the outer diameter of the washer shaped element same as  $\lambda$ ). It is estimated that the ultimate storage density for the VMRAM design is around 400 Gbits/in<sup>2</sup>, provided the required fabrication technology is available. This density is over an order of magnitude higher than that of present hard disk drive technology. With the present 0.18 micron (critical dimension) technology, a memory array can reach an area density over 5 Gbits/in<sup>2</sup>, assuming that all the CMOS electronics are buried underneath the memory array. The zero-transistor per bit feature in the VMRAM design also enables multilayer stacking of the memory arrays in order to increase single chip memory capacity. In contrast, the present magnetic tunneling junction MRAM design requires one transistor per bit for read addressing, adding cost and limiting storage density.

### **Challenges and Promises**

In any MRAM device, writing a bit requires reversing (switching) the magnetic moment of a memory element. This is done by applying current-generated magnetic fields using word lines. For existing suitable magnetic materials, word line current magnitude is on the order of several milliamperes. These current levels require much larger size transistors for the electronic circuit than SRAM and DRAM in which the current levels are significantly lower. The write current in a MRAM device can be reduced by fabricating very thin magnetic films while maintaining good film quality or by finding low moment magnetic materials with high spin polarization for a sufficiently large giant magnetoresistance effect. However, at very high area densities, i.e. very small memory element sizes, the switching current (minimum write current magnitude for switching the

magnetic moment direction) of a memory element must not be made too small to avoid thermally induced spontaneous switching. For all existing MRAM designs other than the VMRAM, the demagnetization field generated from the ends of the elements effectively enhances thermal instability. For the washer shaped memory elements in the VMRAM design, the magnetization flux closure mode generates no demagnetization field, therefore they can be made smaller than the memory elements of any other existing MRAM designs while retaining the same thermal stability.

The signal level in MRAM varies from design to design. For the magnetic tunneling junction MRAM design, the voltage level between a "1" and "0" is on the order of 10 millivolts, while for the VMRAM design, the signal voltage level is on the order of several millivolts. However, signal level is not the only issue. More important is the signal-to-noise ratio (SNR), which strongly depends on the ratio of the resistance difference between the "1" and "0" states to the nominal resistance of the memory element, often referred to as the magnetoresistance ratio. The larger the magnetoresistance ratio, the higher the SNR and the faster each read cycle could be made in a memory chip.

For a memory element in the VMRAM design, the resistance difference between a "1" and "0" can be as large as the nominal resistance itself, i.e. 100% magnetoresistance ratio, if the memory stack consists multiple repeats of the GMR sandwich with the presently available magnetic materials, such as CoFe(thick)/Cu/CoFe(thin)/Cu multilayer. For the present magnetic tunneling junction, e.g. CoFe/Al<sub>2</sub>O<sub>3</sub>/CoFe, the magnetoresistance ratio is around 20% to 40%. One of the key factors that determines the magnetoresistance ratio is the spin polarization factor of the magnetic material, e.g. Co has a spin polarization factor of 35% and Fe has a spin polarization factor of 45%. There are many materials that have a polarization factor approaching 100%. If these highly spin polarized materials can be used to fabricate the VMRAM memory stack, one magnetic sandwich would be enough to produce a much larger magnetoresistance ratio, hence, a much higher signal amplitude. Materials with close to 100% spin polarization could yield magnetoresistance ratio to be orders of magnitudes higher than presently used GMR materials. Utilizing those materials, each VMRAM element would, then, behave like an ideal electronic "switch", similar to a transistor only with added nonvolatility. The memory elements could then be easily made into field-programmable logic gates [7]. A chip made of such magnetoelectronic "switches" that not only can remember, but also compute at same time, is a natural platform for the idea of software and hardware co-synthesis [8].

From the magnetic core memory, which was the first commercialized computer memory, to the first MRAM chip (used in military applications) that Honeywell made utilizing the anisotropic magnetoresistive (AMR) effect [9], to today's MRAM designs, magnetic nonvolatile memory has come a long way. Its immediate potential to replace FLASH memory is becoming so realistic that it is almost certain that MRAM chips will be used in cell phones and palm computers in the very near future. Today, the demand for

nonvolatile memory is greater than ever. Last year's revenue of FLASH memory is over \$10 billion and the market is rapidly growing. With its significantly superior performance, MRAM technology is positioned to be a great financial success. Like most high-tech products, a robust design suitable for large scale manufacturing with high yields will be the key to that success.

**References:**

- [1] G. A. Prinz and K. Hathalway, "Magnetoelectronics," *Phys. Today*, vol. 48, pp.24, (1995).
- [2] J. Zhu, Y. Zheng, and G. A. Prinz, "Ultrahigh density vertical magnetoresistive random access memory," *J. App. Phys.*, vol. 87, pp.6668 (2000)
- [3] W. J. Gallagher *et al.*, "Microstructured magnetic tunnel junctions," *J. Appl. Phys.* 81, 3741 (1997)
- [4] S. Tehrani, *et al.*, "High density submicron magnetoresistive random access memory," *J. Appl. Phys.*, Vol.85, pp.5822 (1999).
- [5] M. Johnson, "Magnetoelectronic memories last and last....," *IEEE Spectrum*, pp. 33, Feb , 2000.
- [6] B.A. Everitt and A.V. Pohm, "Pseudo spin valve magnetoresistive random access memory," *J Vac. Sci Tech. A*, vol. 16, no. 3, pp.1794 (1998)
- [7] W. C. Black Jr. and B. Das, "Programmable logic using giant-magnetoresistance and spin-dependent tunneling devices," *J. Appl. Phys.*, vol.87, pp.6674 (2000).
- [8] R.K. Gupta and G. DeMicheli, "Hardware and Software Cosynthesis for Digital Systems," *IEEE Design & Test*, vol.10, No.3, pp.29, (1993)
- [9] J. M. Daughton, "Magnetoresistive memory technology," *Thin Solid Films*, 216, 162 (1992)

Figure 1. Schematic drawing of a VMRAM memory element and the paired word lines that runs over and under the memory element for read/write addressing. In practice, the giant magnetoresistive (GMR) stack is repeated for sufficient signal amplitude with presently available GMR materials.

Figure 2. The VMRAM memory element is a washer-shaped giant magnetoresistive memory stack. The memory stack consists of two ferromagnetic layers, one thick and one thin, sandwiching a conductive metal layer, e.g. CoFe/Cu/CoFe. In each magnetic layer, the magnetic moment is circularly oriented with a stable flux closure configuration, clockwise or counterclockwise that corresponds to the two stable states. The memory elements are connected in series to form a bit line. The bit line current generates a circular magnetic field in each memory element. The orientation of the moment in a magnetic layer is stable until a reversing circular magnetic field generated by the bit line current reaches beyond a threshold, yielding the moment to reverse. The thick and thin layers have distinctively different switching threshold. Depending on whether the magnetic moments of the two magnetic layers are parallel or antiparallel to each other, the resistance of the memory stack is low or high respectively

Figure 3. Word lines arrangement for addressing. The current in the word lines over and under the addressed memory cell (red-dashed-box) generates a radial field in the washer-shaped magnetic stack, significantly reducing the threshold of the bit line current for switching the magnetic moment directions. The radial field along with the circular field generated by the bit line current creates a robust switching mode and a robust addressing scheme.

Figure 4. The dynamic read scheme that relies on the giant-magnetoresistive (GMR) effect. By sending bit line current pulses with opposite directionality, the magnetic moment direction of the thin magnetic layer in the memory stack are switched back and forth for interrogating the moment direction of the thick magnetic layer.

Figure 5(a) Magnetic poles, generated at the ends of a linearly magnetized rectangular magnetic element, produce a demagnetization field in the interior and stray fields in the surrounding exterior. The demagnetization field often results in complex magnetic domains and causing the field threshold for switching the magnetic moment direction to fluctuate uncontrollably. The stray fields create interference for adjacent memory elements.

Figure 5(b) By tapering the ends of a linear mode memory element, the magnetic poles at the ends are spread and become significantly weaker.

Fig. 1

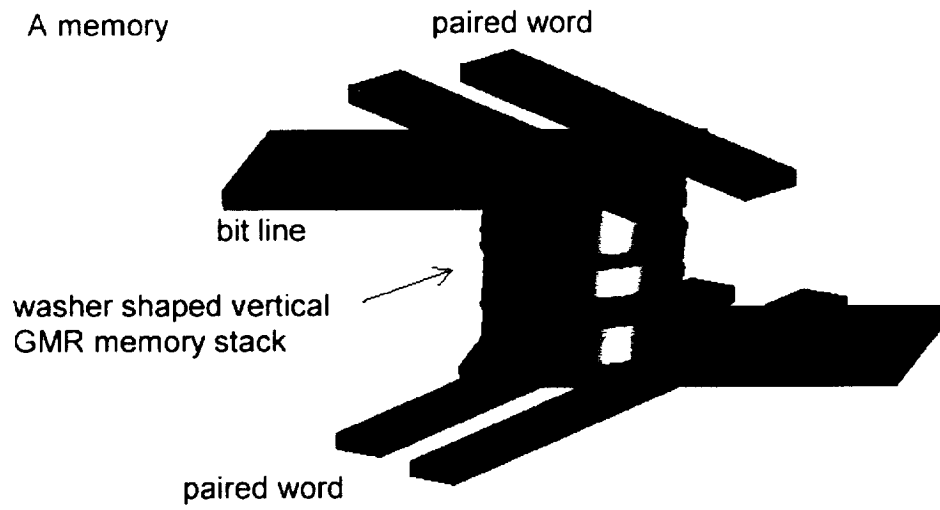


Fig. 2

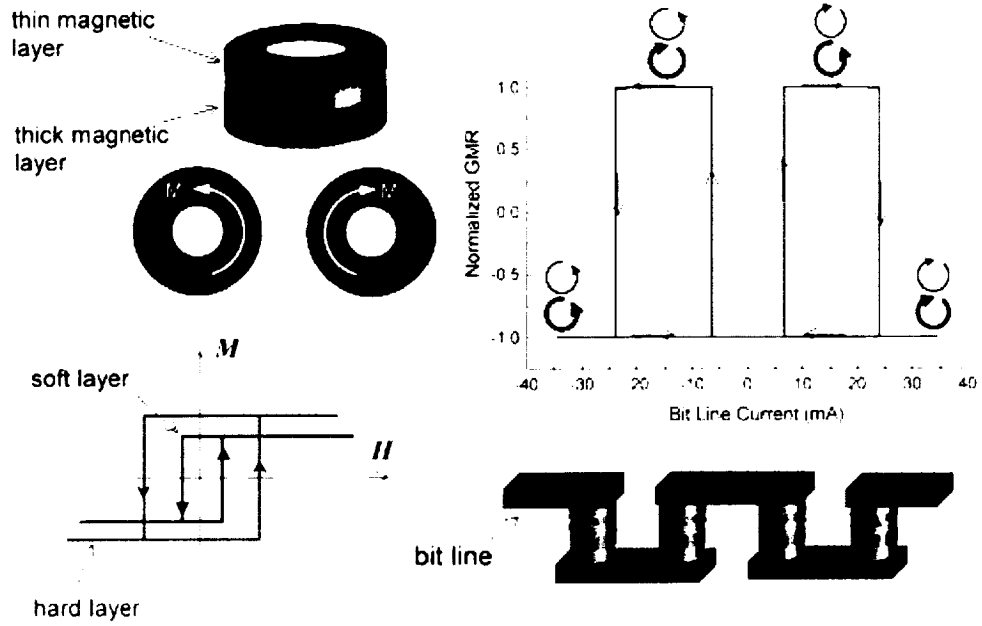


Fig. 3

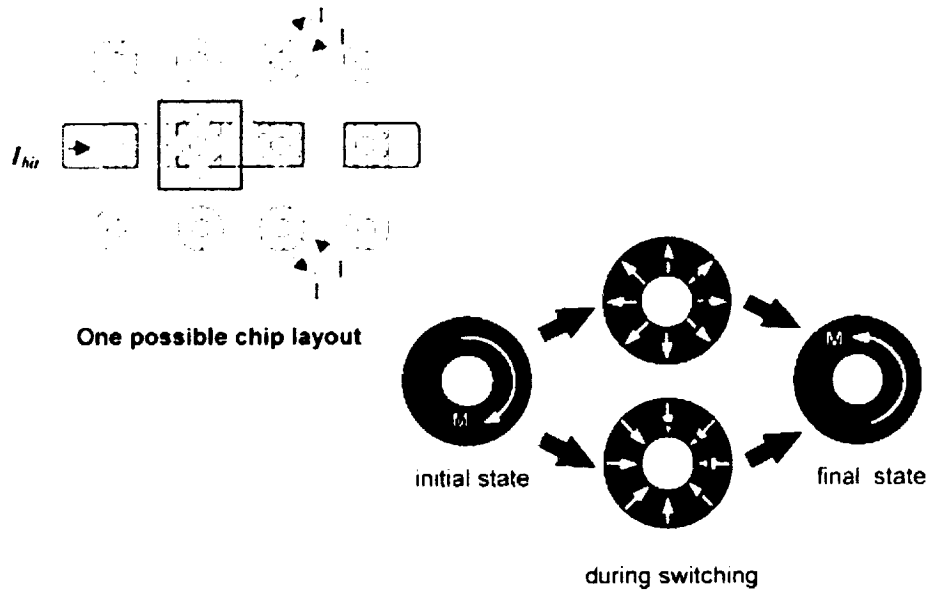


Fig. 4

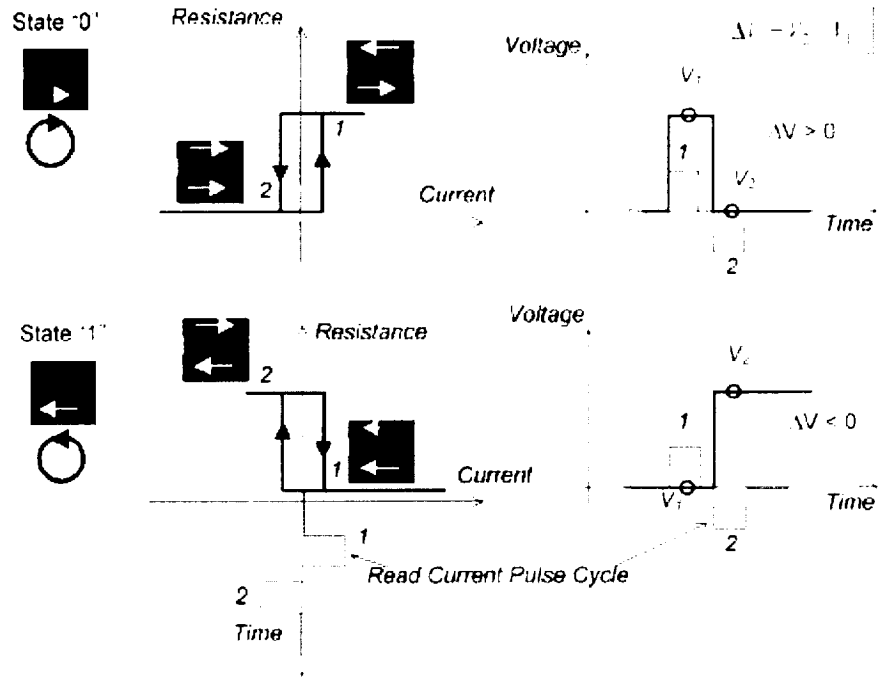
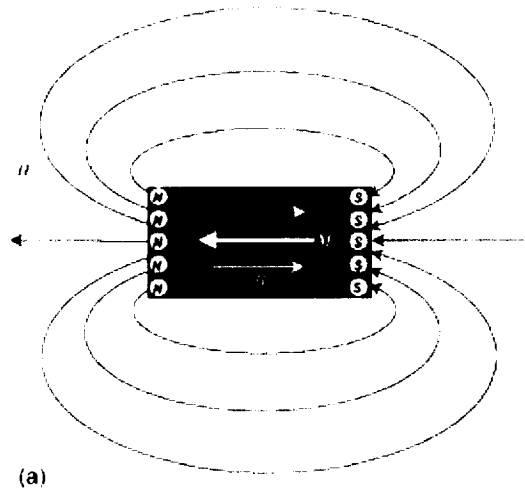
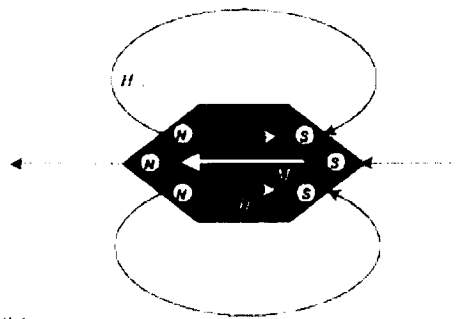




Fig. 5



(a)



(b)

Criteria for Magnetic Tunnel Junctions

Presenter: I Schuller, University of California – San Diego

Material for this presentation was not available at the time of publication.

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# A Modified MRAM Architecture without a Current Rectifier Per Cell

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**Abstract**— This paper modifies the magnetic RAM (MRAM) architecture by removing a current rectifier per cell without sacrificing performance. A read operation of stored data is maintained by introducing a simple concept of "virtual ground" of operational amplifier. The modified MRAM design offers a reduced element area with a little penalty of an addition of one switch per column, which occupies a very small silicon area. As a result, a tenfold improvement in storage density has been achieved by an experimental device

to other solid state memories such as battery-backed CMOS RAM and flash memory. The information stored in CMOS RAM must not be critical to the product, as battery failure is most certain to happen during the lifetime of the product. From the throughput point of view, the slow erase and write times of flash memory result directly from the fundamentals of the flash memory technology itself and any effort to accelerate the process by using higher voltages will shorten the life of the memory.

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## 1. INTRODUCTION

Unlike the semiconductor RAMs, magnetic random access memory (MRAM) that stores information as the orientation of magnetization of a thin ferromagnetic film can hold stored information for long periods of time, and is thus inherently nonvolatile. Nonvolatile memory can be used as reliable caching to improve I/O performance by reducing the I/O bottleneck between processor and mechanical disk in a general computing system[1]. Nonvolatile memory also plays a significant role in today's handheld device and mobile computing environment, such as personal digital assistants (PDAs), calculators, notebooks, and palmtops, etc[2]. MRAM with the capability of being rewritten allows the end-user to store their application and file data. Storage of system configuration and control code in the form of an MRAM allows the OEM to provide field updates to their software. MRAM is a solid state memory which is light and does not have the mechanical limitations of a disk drive. MRAM also exhibits some excellent properties superior

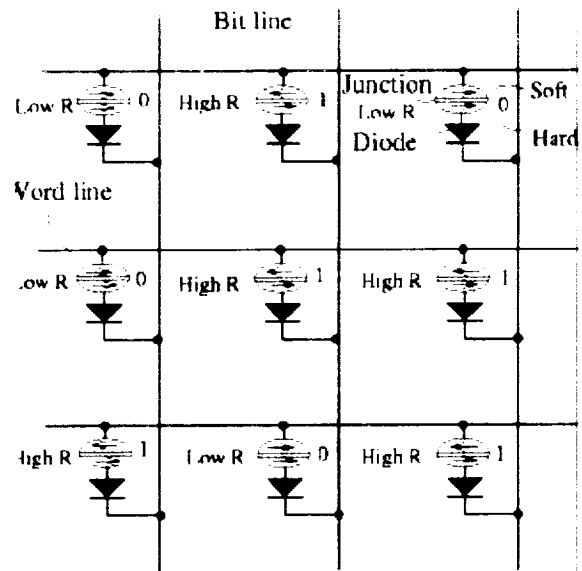


Figure 1 The traditional MRAM architecture with a diode per bit.

In a conventional MRAM, current rectification is desirable to reach readout operation. As shown in Fig.1, each array cell is located at each intersection of every bit and word line in a cross-point array. The basic array cell is a current rectifier (diode) connected in series with a storage element (magnetic tunnel junction). Magnetic tunnel junction is sandwich structured: a magnetically-soft layer, a very thin tunnel barrier, and a magnetically-hard layer. The junction element has two stable magnetic states which correspond to the parallel/antiparallel magnetization orientation. Then two stable magnetic states cause two different values of resistance. With such a one-diode-per-cell architecture it is possible to flow a sense current through a single chosen cell by forward-biasing the diode connected in series with that cell, blocking all alternative current paths by reverse-biasing the rest of the diodes. In the absence of such diodes all the junctions would otherwise be electrically connected to one another, the sneak current paths through other junction elements making the resistance measurement of an individual cell, to determine "0" or "1", impossible. However, such a junction-diode series puts a severe constraint on the storage density since a current rectifier (diode or transistor) per cell is likely to be very large, occupying the space of tens of memory cells.

This paper modifies the MRAM architecture by removing all the current rectifiers. The simplified architecture offers all the advantages of MRAM. In addition, it gives a reduced element area which produces a higher storage density.

## 2. ARCHITECTURAL MODIFICATION

The modified MRAM architecture without any current rectifier is shown in Fig.2. In a read operation, it is necessary to measure the value of any individual junction resistance in order to determine "0" or "1". Due to mutual electrical connection between all the junctions as mentioned in Introduction, any direct measurement would result in inevitably introducing the contribution from the rest of the resistors. This difficulty has been overcome by making use of a concept of "virtual ground" of operational amplifier[3]. Since the input impedance of an operational amplifier is considered very high or even infinite, referring to Fig.2, no current can flow into or out of the inverting input terminals, thus this point is at 0V, commonly referred to as virtual ground. Referring again to Fig.2, a voltage across the selected Bit 32 under a read condition is established by setting the selected Word line 3 to an input voltage excitation  $V_{in3}$ , and clamping the bit line 2 to virtual ground 0V (setting the electronic switch  $K_2$  to read mode, which occupies a very small silicon area). The bit line 1,3 are clamped to actual ground 0V by setting the switches  $K_1$  and  $K_3$  to standby mode. Referring now to Fig.3, the un-selected Word lines 1,2 remain at the standby voltage level, 0V. Although there are a large number of possible current paths in the cross-

point organization, no ambient current path, except the dotted path  $I_s$  through the chosen Bit 32, exists because all the bit lines are set to virtual or actual ground. Thus the un-selected Bits 11,12,13,21,22,23 have zero voltage drop and do not conduct. The un-selected Bits 31,33 conduct but do not contribute to the read output.

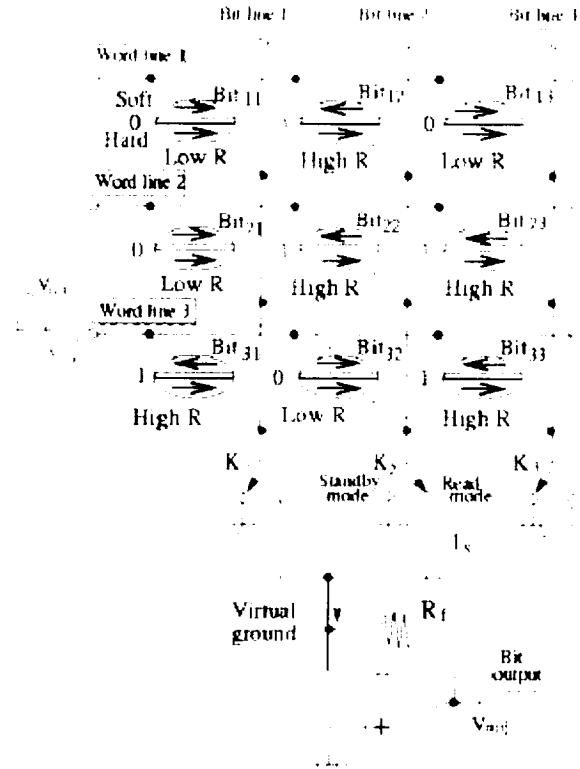


Figure 2 Read operation in a 3x3 bit diode-free MRAM.

The magnetic state of the memory cell is detected or read by applying a voltage across the selected junction and measuring the current through the junction. In the example of Fig.2, the resistance  $R_{32}$  of the selected Bit 32 determines the sense current  $I_s$ . In the bit line control circuitry this current is converted to a voltage  $V_{out}$  to read the datum stored in selected Bit 32. The operational amplifier has its noninverting input terminal brought to ground. As mentioned above, no current can flow into or out of the inverting input terminals. This forces  $I_s$  to flow through the feedback resistor  $R_f$  to produce a sense voltage  $V_{out}$  at the output terminal. The read signal gain is equal to the ratio between  $R_f$  and  $R_{ij}$ . The low resistance state and high resistance state of  $R_{ij}$ , at the intersection of the  $i$ 'th word line and the  $j$ 'th bit line, produce different values of sense current  $I_s$  in inverse proportion and therefore different values of output voltage  $V_{out}$ . Referring again to Fig.3, the output voltage  $V_{out}$  has two discrete values corresponding to the two magnetic states. While not shown in Fig.3, the output voltage  $V_{out}$  will be compared to a reference voltage level set to a value

halfway between the expected values for the two possible states of the memory cell and the difference will be amplified further to provide full logic levels. After the data is read, referring again to Fig.3, the voltage on Word line 3 is returned to the standby value. The magnetic state remains unchanged after the read operation.

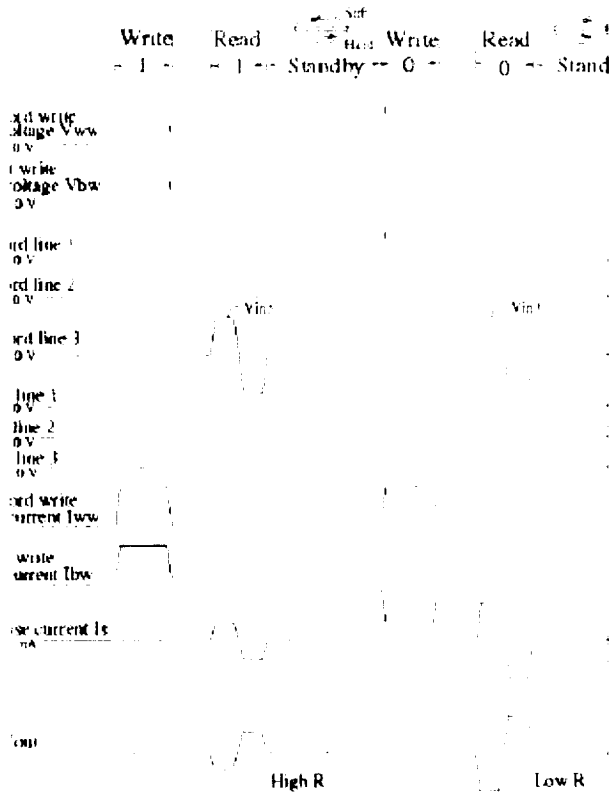


Figure 3 Voltage and current levels during MRAM read and write operations.

In a write operation, sufficiently large currents, supplied by a voltage source through load resistors, are passed through both a word line and a bit line, and the self-field of the combined currents at the intersection of the energized word and bit lines will rotate the magnetization of magnetically-soft layer of the single particular junction located at the intersection. As illustrated in Fig.3, the (actual) ground of the energized lines ensures that all the bits in contact with the energized word and bit lines have zero voltage drop and do not conduct, otherwise the leakage currents may damage the junctions.

### 3. ENGINEERING REALIZATION

To realize this first architectural demonstration of diode-free MRAM, reported to date, a multibit memory chiplet was fabricated, as shown in Fig.4. The junction dimension is 2 μm and the corresponding storage density is 5 MegaBits/cm<sup>2</sup>. Contact windows were opened in the insulator layer in order for the top leads and bottom leads

to directly access the junctions without any diode or transistor current rectifier. The output voltage gives two discrete values (the voltage difference is 96 mV) corresponding to the two magnetic states. The proposed architecture is workable.



Figure 4 Micrographs of an MRAM without any current rectifier.

### 4. CONCLUSION

Storage density and access time are the twin keys to computer data storage devices. Although new electronic devices, processor organizations and software have contributed to enormous advances in computer technology, they would have been worthless without the denser and faster memories that were developed with them. Magnetic RAM (MRAM) is a very important technology for applications where the nonvolatility, fast access, higher density, in-system reprogrammability, radiation hardness and low power consumption are required[4]. This paper modifies the traditional MRAM architecture by removing all the current rectifiers, which are used to block the ambient current paths in a read operation. The new architecture makes use of a simple concept of "virtual ground" of operational amplifier[5]. The modified MRAM design offers a reduced element area with a little penalty of an addition of one switch per column, which occupies a very small silicon area. The

overall improvement in storage density is over tenfold. An engineering device with this new architecture has been tested. No performance has been sacrificed and, in addition, the fabrication process has been greatly simplified.

## REFERENCES

- [1] M. Baker, S. Asami, E. Deprit, J. Ousterhout, and M. Seltzer, "Non-volatile memory for fast, reliable file systems", Proceedings of the 5th International Conference on Architectural Support for Programming Languages and Operating System(ASPI.OS), Boston, pp.10-22, ACM Press, 1992
- [2] B. Bickford, "Nonvolatile memory requirements in a mobile computing environment", International NonVolatile Memory Technology Conference, 1996
- [3] F. Hughes, Op Amp Handbook, Prentice Hall, London, 1993
- [4] S.Tehrani, B. Engel, J.M.Slaughter, E.Chen, M.DeHerrera, M.Durham, P.Naji, R. Whig, J. Janesky and J. Calder, "Recent development in magnetic tunnel junction MRAM", IEEE Transaction, MAG-36, No.5, pp.2752, September, 2000
- [5]F. Wang, Diode-Free Cross-Point Array Architecture for Magnetic Random Access Memories, GB and US patent pending, 15 September, 1999

and Technology for the 21th Century Edited by Springer. To date, he has been invited to give 6 public lectures on this invention by universities or institute in Japan, UK, Portugal, Netherlands and Belgium. So far, he has published 50 Journal papers and 40 Conference Proceeding papers. His research interest covers Web Database, Hierarchical Storage Management (HSM), Nonvolatile RAM-based Mobile Database, RAID Mass Storage, Network-Attached Storage, E-Commerce and Multimedia, etc. He is now supervising 2 PhD students and 8 MSc students and 8 undergraduate students.

## Biography



Dr. Frank Wang is now a Senior Lecturer at School of Informatics and Multimedia Technology, University of North London, United Kingdom. He obtained B.Sc. in Computer Science, M.Sc. in Computer Science, Ph.D. in Information Technology at University of Plymouth, UK. In 1995, he invented a new concept Magnetic Random Access Memory (MRAM) using spin-tunneling effects as a new computer data storage device. This high-speed and high-capacity digital memory is a combination of traditional semiconductive memory and magnetic hard disk but shares the advantages of the above two. This is his most favourite contribution during his career, which brought him to the attention of the international community. Recently, he contributed two book chapters concerning this invention in Encyclopedia of Science and Technology edited by Elsevier and Frontiers of Science

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