Flight Computer Design for the Space Technology 5 (ST-5) Mission[1]

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Abstract—As part of NASA's New Millennium Program, the Space Technology 5 mission will validate a variety of technologies for nano-satellite and constellation mission applications. Included are: a miniaturized and low power X-band transponder, a constellation communication and navigation transceiver, a cold gas micro-thruster, two different variable emittance (thermal) controllers, flex cables for solar array power collection, autonomous ground-based constellation management tools, and a new CMOS ultra low-power, radiation-tolerant, +0.5 volt logic technology. The ST-5 focus is on small and low-power.

A single-processor, multi-function flight computer will implement direct digital and analog interfaces to all of the other spacecraft subsystems and components. There will not be a distributed data system that uses a standardized serial bus such as MIL-STD-1553 or MIL-STD-1773. The flight software running on the single processor will be responsible for all real-time processing associated with: guidance, navigation and control, command and data handling (C&DH) including uplink/downlink, power switching and battery charge management, science data analysis and storage, intra-constellation communications, and housekeeping data collection and logging. As a nano-satellite trail-blazer for future constellations of up to 100 separate space vehicles, ST-5 will demonstrate a compact (single board), low power (5.5 watts) solution to the data acquisition, control, communications, processing and storage requirements that have traditionally required an entire network of separate circuit boards and/or avionics boxes. In addition to the New Millennium technologies, other major spacecraft subsystems include the power system electronics, a lithium-ion battery, triple-junction solar cell arrays, a science-grade magnetometer, a miniature spinning sun sensor, and a propulsion system.

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1. INTRODUCTION

This paper describes all of the hardware and software interactions and operations for the Space Technology 5 (ST-5) single-board flight computer. This computer, together with the software that runs on it, does much more than just command and data handling (C&DH), but it is called the C&DH subsystem. In order to put the C&DH design in perspective, the paper starts with an overview of the ST-5 mission and a review of the spacecraft technologies that will be flight validated by ST-5. Following that, there is an introduction to the spacecraft itself, with a discussion of the spacecraft's mechanical design and two-slot "card cage" that houses the C&DH electronics circuit card (or board) and the power system electronics circuit card (or board). A summary of the key C&DH requirements leads into a more in-depth presentation of all the C&DH interfaces and functions, including how the electronics hardware and flight software operations are partitioned in order to meet the overall requirements for ST-5. The details of the C&DH board design are given in terms of the processor, memory, gate arrays, power conditioning, physical dimensions and layout. A description of the development, integration and test flow precedes the paper's conclusion, and a list of acronyms appears at the end for easy cross-reference.

2. ST-5 MISSION OVERVIEW

The Space Technology 5 mission is a part of NASA's New Millennium Program (NMP). The ST-5 project is an in-house development managed at the Goddard Space Flight Center in Greenbelt, Maryland. A primary goal of ST-5 is to provide a proof-of-concept demonstration for future nano-satellite constellation missions. The project will accomplish this by developing and flying a satellite constellation comprised of three small, low-power, full-service spacecraft, each with a total mass of about 25 kilograms (kg). During the three-month mission, each of the spacecraft will demonstrate several NMP nano-sat and constellation-enabling technologies. Major goals include showing that multiple spacecraft can operate together as a single constellation (and not just a group of individual units) and showing that a very small spacecraft is capable of research-quality science measurements.

Each 25-kilogram spin-stabilized spacecraft has a total power budget of approximately 22 watts, which is provided by high-efficiency, triple-junction solar cell arrays and a lithium-ion battery. The three ST-5 spacecraft will be launched as "secondary" payloads into a highly elliptical geo-synchronous transfer orbit, with a period of about 10.5 hours, a perigee distance of about 220 kilometers and an apogee distance of about 38000 kilometers. All three will share the same orbit plane, and the separation distance between spacecraft near apogee is expected to be between 100 and 1000 kilometers. The spacecraft spin rate will be about 20 revolutions per minute (RPM).

3. NEW MILLENNIUM PROGRAM TECHNOLOGIES

The purpose of NASA's New Millennium Program is to develop and flight validate the critical "breakthrough" technologies that are needed to enable the space science and Earth science missions of the future. For ST-5, the Constellation Communication and Navigation Transceiver (CCNT) will enable intra-constellation, S-band cross-link communication of data and "science events" between the three spacecraft. The CCNT will also have a Global Positioning System receiver to allow orbit determination and inter-spacecraft ranging measurements. The CCNT will fulfill a part of the constellation objective of the mission. Another constellation enabling NMP technology is a set of autonomous ground-based constellation management software tools.

The other key technologies to be demonstrated by ST-5 are focused on the small, low-mass and low-power theme. These technologies include a miniature and low-power X-band transponder for uplink and downlink, a cold gas micro-thruster (CGMT) propulsion system, two variable emittance controllers (VEC) for the thermal subsystem, "flex" harness interconnects for the solar panels, and a new type of 1/2 volt CMOS ultra low-power, radiation-tolerant (CULPRiT) logic. The 1/2 volt CULPRiT technology, which is latchup immune and hardened for up to 100 kilorads of total ionization dose, will be verified as an integral part of the C&DH subsystem.

4. ST-5 SPACECRAFT OVERVIEW

Each of the three spacecraft for the ST-5 mission will be identical. Each spacecraft (S/C) is roughly a flat cylinder shape, approximately 20 inches (51 centimeters) in diameter and 11 inches (28 centimeters) tall. The S/C mass budget is around 25 kg and the power budget is about 22 watts. The ST-5 spacecraft design is composed of many subsystems, including a science instrument and the small, low-power, low-mass and constellation-enabling NMP technologies.

Core spacecraft subsystems include a high efficiency power system, a magnetically clean structural and electrical system, a miniature digital sun sensor (DSS), a compact low-power flight computer with embedded flight software, a lightweight small volume mechanical structure and an all-passive thermal control system

The science instrument is a small, low-power, high-resolution magnetometer (MAG) that will make in-situ measurements of the Earth's magnetic field throughout the orbit. A deployable MAG boom will position the magnetometer's sensor head about 1 meter away from the center of the S/C. ST-5 will perform science measurements from all three spacecraft in a way that validates the concept of operating a constellation of spacecraft as a single instrument platform. The spacecraft is capable of storing

one orbit's worth of magnetometer data. Each spacecraft processes its magnetometer data in real-time, and is capable of both alerting other spacecraft to the presence of science events, and receiving alerts to collect magnetometer science data at a high rate. The MAG data will also be used as part of a ground-based attitude determination algorithm. The high sensitivity of the MAG has been a significant design driver, because magnetic materials and electrical current flow topologies can easily generate magnetic fields at the nano-Tesla level. This is especially true for a very small S/C where the magnetometer's sensor head cannot be placed at the end of a boom that is many meters long.

4.1 Mechanical Design

The basic shape of the ST-5 spacecraft is a right octagonal prism, or 8-sided flat "cylinder." The spacecraft spin axis is the axis of symmetry or axis of rotation of that "cylinder." The top and bottom "decks" are octagons, and eight small solar panels cover the outsides of the eight side walls of the "cylinder." A rectangular "brick shaped" card cage enclosure mounts in between the two decks and joins the two decks together. The longest dimension of the card cage is slightly less than the diameter of the S/C.

Figures 1 and 2 show the physical layout for an ST-5 vehicle. The battery, magnetometer electronics, transponder electronics and radio frequency (RF) components, and one of the VEC boxes are mounted to the top deck as shown in Figure 1. This view is looking "up" toward components on the inside of the top deck, and "up" toward the empty rectangular area where the 2-slot card cage enclosure would attach to the top deck. The spacecraft X and Y coordinate axes are also shown in Figure 1. The transponder's X-band antenna (not visible in Figure 1) is mounted to the outside of the top deck.

The CCNT, propulsion system gas tank, thruster control electronics (TCE), two externally accessible direct access test connectors, and another one of the VEC boxes are mounted to the bottom deck as shown in Figure 2. This view is looking "down" toward components on the inside of the bottom deck, and "down" into the empty rectangular opening of the card cage enclosure box that is attached to the bottom deck. In Figure 2, the view (with respect to Figure 1) has been flipped about a horizontal line, so the X axis still points to the right, but now the Y axis points up. In Figure 2 the two card cage slots are parallel to the X axis, with the planes of both circuit cards being normal to the spacecraft Y axis.

In Figure 2, the Power System Electronics (PSE) board will slide into the card cage slot nearest to the upper part of the figure, and the C&DH board will go into the slot nearest to the lower part of Figure 2. Since the card cage enclosure almost bisects the usable inside volume of the spacecraft, the CCNT, TCE and tank are referred to as being on the "PSE side" of the spacecraft. In a similar fashion, the MAG electronics and both of the VEC boxes are referred to as being on the "C&DH side" of the spacecraft. Side views of five of the eight solar panels can be seen around the uppermost five sides of the octagons in Figures 1 and 2.

The CCNT's deployable S-band antenna boom (not visible in Figure 2) is mounted to the outside of the bottom deck. Not shown in either figure is the deployable boom for the magnetometer's sensor head. Both booms are stowed or "folded" during launch and ascent, and then deployed after the S/C is spun up to about 20 RPM as it separates from the launch vehicle.

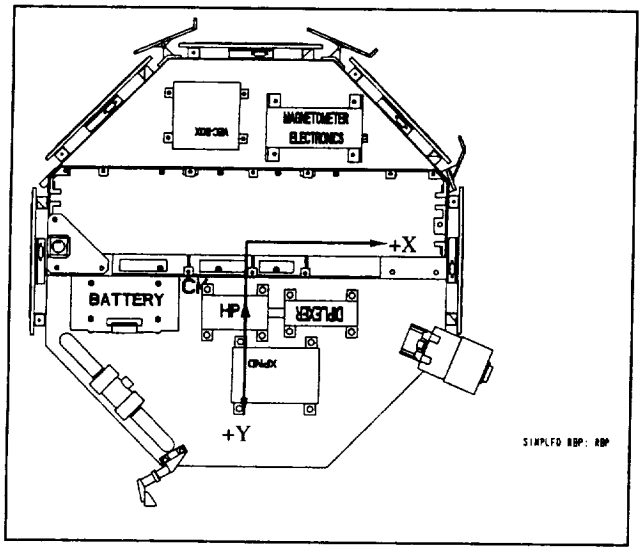


Figure 1: Bottom-Up View of Top Deck

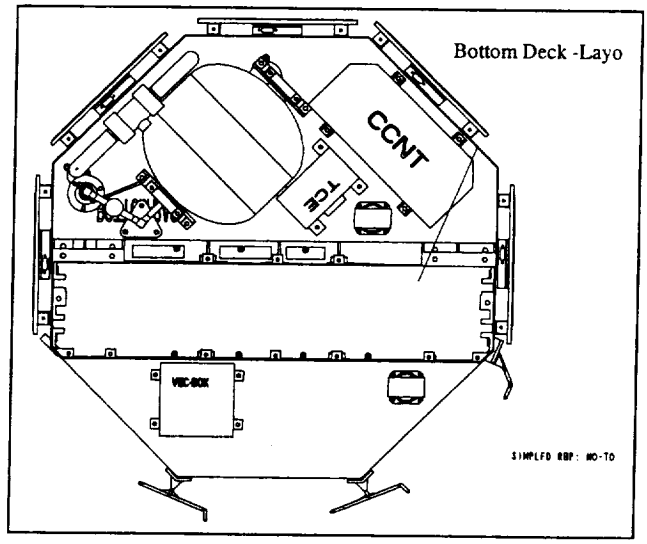


Figure 2: Top-Down View of Bottom Deck

4.2 Card Cage with Backplane

The central card cage enclosure (roughly 46 x 24 x 11 cm) will house two surface-mount circuit board assemblies in two slots, one slot for the multi-function flight computer (called the C&DH board), and the other slot for the power system electronics (PSE) board. This enclosure serves as the major spacecraft structural element connecting the top and bottom decks, and also has a backplane for inter-board communications and external I/O expansion. The card cage also serves as the main heat conduction path from the C&DH and PSE boards out to the S/C structure.

All electrical interfaces between the PSE and C&DH, including those for: +5V power distribution from PSE to C&DH, digital signals to and from the PSE, and analog signals from the PSE, will go through matching pairs of connectors on the backplane. For both the C&DH board and the PSE board, some of the power and signal input/output (I/O) goes directly from connectors on those boards. For S/C components and subsystems on the C&DH side of the S/C, the power distribution is from the PSE board, across the backplane, and "through" the C&DH board to the destination subsystem. For S/C components and subsystems on the PSE side of the S/C, much (but not all) of the signal distribution is from the C&DH board, across the backplane, and out to the destination subsystem through a backplane I/O connector. The reason for these routing topologies was to minimize the magnetic fields generated by flowing currents; and a system-level requirement was developed to have all power and signal wires to any given subsystem leave the card cage enclosure through a single connector.

There are two jumper-selectable signals (bits) on the backplane that will be used to determine the CCSDS spacecraft identification for each of the three members of the ST-5 constellation. These two signals (bits) will be directly readable by the X-band transponder and by the C&DH flight software.

4.3 Power System Electronics (PSE)

The main functions of the power subsystem are to collect energy from the eight solar array panels, store any excess solar energy in the 9 ampere-hour lithium-ion battery, draw stored energy from that battery during periods of peak power demand (or during up to one hour of eclipse), and provide switched power outputs (with on/off control) to a number of different S/C subsystems. The PSE maintains an un-regulated +7.2 ± 1.2V power bus and a regulated +5V power bus. The PSE has switchable +5V regulated outputs for the sun sensor, VEC #1, VEC #2 and the thruster control electronics. It also has switchable +7.2V un-regulated outputs for the magnetometer and MAG boom deployment actuator, the propulsion system's tank pressure sensor, the CCNT and its S-band antenna deployment actuator, and the transponder's X-band downlink high power amplifier. All of the switched power outputs have over-current protection, where the trip level can be adjusted for each load. The +7.2V power to the transponder's X-band uplink receiver is not switchable (always left on). The +5V power to the C&DH card is always left on, but can be cycled on-off-on by a ground-to-transponder "special command" if necessary. The PSE has it own one-milliampere current source for power system thermistors, and has a set of analog multiplexers for collecting power system signals that will be digitized on the C&DH board. The PSE card switched power services and the collection of power system telemetry are controlled by C&DH processor read/write transactions over the backplane's local 16-bit parallel data bus.

Energy balance will be maintained on a per orbit basis, and the battery will be fully charged prior to eclipse entries. The power system's energy balance and battery charge state algorithms will run on the C&DH processor. Periods of peak power demand are expected to be during X-band downlink passes and when the CCNT is being validated. Note that the ST-5 spacecraft is NOT powered on during launch and ascent, and that a key function of the PSE is to sense physical separation from the launch vehicle and autonomously turn on the S/C. The PSE provides an externally accessible test connector for supplying ground power, charging the battery, and directly measuring the power system's health and status signals.

5. C&DH Board Requirements Summary

Figure 3 is a block diagram showing the C&DH at the center of the ST-5 architecture, with interfaces to all other subsystems. The C&DH provides the micro-processor and memory required to do the command and control, telemetry, data collection, data storage, and on-board processing for almost the entire spacecraft. The C&DH interfaces to the power system electronics, magnetometer, digital sun sensor, variable emittance controllers, CCNT, cold gas micro-thruster, tank pressure transducer, X-band transponder and various thermistors as described in Section 6.

The C&DH command uplink and telemetry downlink paths are CCSDS compliant. They support a 1 kilobit per second (kbps) uplink command rate and a downlink telemetry rate that is selectable to be either 1 kbps or 100 kbps. Uplink codeblock error detection and de-randomization are performed on ground-to-spacecraft command frames. On the downlink path, cyclic redundancy check (CRC), Reed-Solomon encoding, pseudo-randomization and ½ rate convolutional encoding is performed on all telemetry frames as they are sent to the transponder for communication to the ground.

The C&DH's on-board solid state recorder (SSR) memory has error detection and correction (EDAC) and has a usable capacity of 15 megabytes. The plan is to downlink the contents of the SSR during a 20-30 minute ground station pass at 100 kbps. Major portions of the SSR memory are

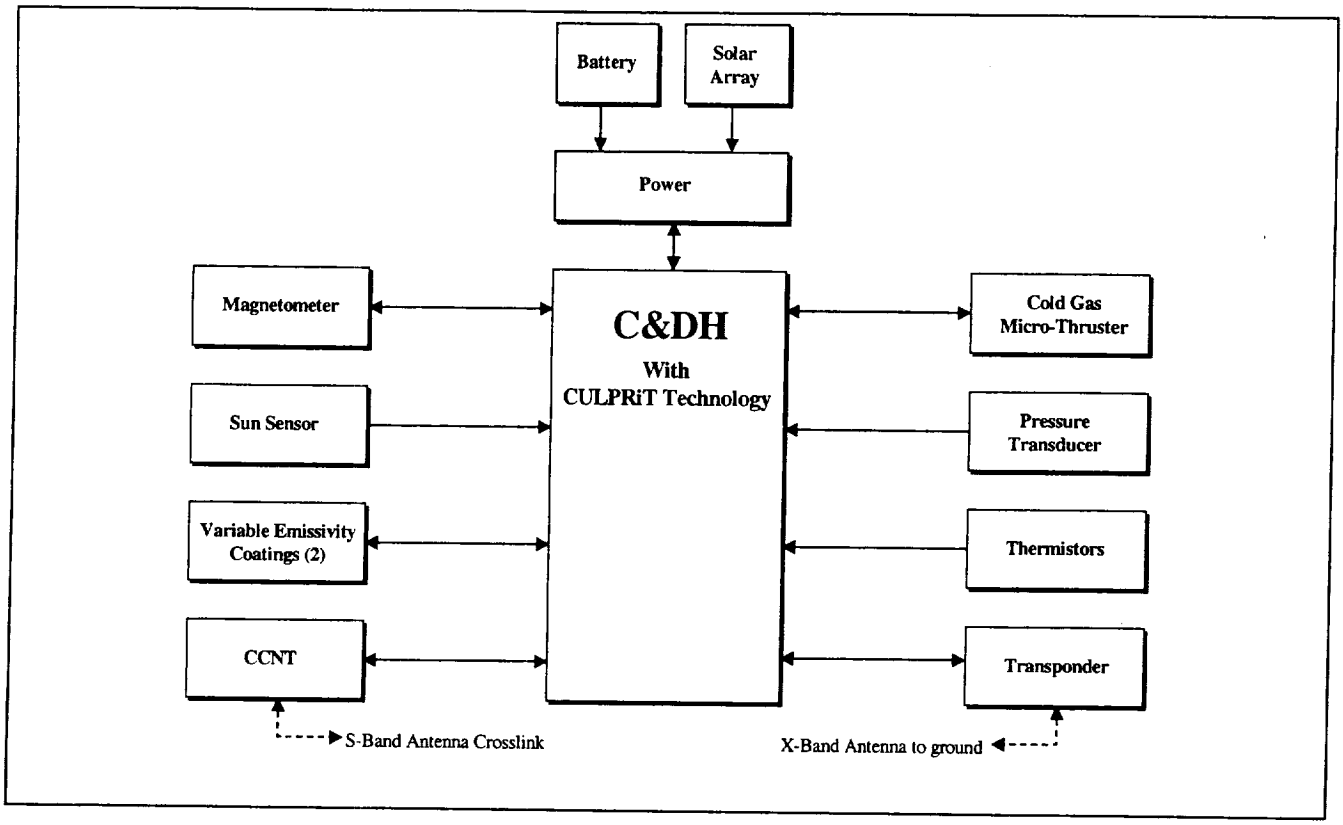


Figure 3: Block Diagram of Spacecraft Components, Subsystems, Architecture and Interfaces

for magnetometer science data and CCNT cross-link/ranging/orbit telemetry, but the C&DH must also be able to store two whole orbit's worth of health, safety and other NMP technology validation telemetry. Examples of this telemetry include: analog communications parameters from the transponder; voltages and currents from the battery, solar array and power system; sun crossing times and elevation angles; propulsion system tank pressure and thruster firing history; science event warning records; analog validation data from the variable emittance controllers, and temperatures from all over the spacecraft. A single analog-to-digital converter (ADC) on the C&DH board will do all digitization of analog telemetry.

The C&DH maintains a seconds counter/timer and a sub-seconds counter/timer with a resolution of one microsecond. The design supports the correlation of spacecraft clock and coordinated universal time (UTC) to within 5 milliseconds. The spacecraft clock maintains less than 1 second of drift over a 10.5 hour orbit. The two counter/timer circuits support time tagging of data and scheduling of flight software tasks. The time of the Sun's crossing through the field-of-view of the sun sensor is latched and used to calculate the spin rate for attitude control algorithms and to phase thruster firing relative to the sun vector. Science event detection and magnetometer vectors are also time-tagged in order to correlate science data events between spacecraft. The time of every 16th telemetry frame over the downlink is latched and used to correlate time to UTC.

The C&DH controls power distribution and autonomous power safing by performing command arming, verification and firing of power switch services. Control of deployment actuation is performed for the magnetometer boom and S-band cross-link antenna. The C&DH also controls magnetometer sensitivity, emittance setting for the variable emittance controllers, X-band transponder operational mode, and thruster firing. Software will also do low-pass filtering and science event detection on the MAG data.

The C&DH is designed to be single event latch-up immune, with radiation hardening for up to 40 kilorads of total ionization dose, and a single event upset LET threshold of 35 MeV-cm^2/mg. The electronics operating temperature range is –20°C to +50°C, and the survival range is –40°C to +60°C. The C&DH volume is approximately 17.75 x 8.75 x 1.25 inches (45 x 22 x 3 centimeters). C&DH mass is approximately 1.5 kg, and average power consumption is less than 5.5 watts. There will be an externally accessible C&DH direct access test connector for memory loading, hard-line (baseband) serial uplink and downlink, etc.

6. C&DH Interfaces and Functions

6.1 Power System Electronics (PSE) Interface

The PSE provides regulated +5V power to the C&DH through a backplane connector. This power is normally on whenever the spacecraft is powered, except that the C&DH power can be momentarily cycled on-off-on by a hardware special command signal that goes directly from the transponder to the PSE.

All flight software (FSW) control and monitoring of switched power services are done by digital data transfers between the PSE and the C&DH over a 16-bit parallel bus on the backplane. The FSW will write to and read from a switched service register on the PSE card in order to turn power services on and off, where there is one bit in that register for control of each switched service. Due to magnetics requirements, the PSE switched power services that go to subsystems on the "C&DH side" of the spacecraft actually flow over the backplane and "through" the C&DH board. This applies to the +5V power to VEC1 and VEC2, and the +7.2V power to the MAG boom actuator and the MAG electronics.

The PSE provides dedicated analog signals to C&DH that are used to measure bus voltage, bus/load current, battery voltage and battery current. The PSE also has a multiplexed analog output signal to C&DH that is used to monitor solar array voltage, solar array current, battery half-voltages, PSE +5V supply voltage, battery cell temperatures, solar array temperatures, and PSE board temperature. For this multiplexed analog signal, the C&DH drives the multiplexer channel select signals to the PSE over the backplane. For more details on analog telemetry collection, see Section 6.9.

6.2 Magnetometer (MAG) Interface

The magnetometer senses magnetic field strength and polarity along three nominally orthogonal axes. The sign and magnitude of the field for each of the three axes is digitized to 17 bits. The range of field values that can be sensed, along with the resolution of the field strength values, is controlled by a MAG range select signal (bit) that goes from C&DH to MAG. When the range is set for low resolution, the MAG can sense fields from approximately one nano-Tesla (1 nT) up to about ± 64000 nT. When set for high resolution, the MAG can sense fields from approximately 0.1 nT up to about ± 1000 nT. FSW can change the MAG range select bit in response to a field strength change or a science event warning as required.

The MAG transmits its data on a synchronous serial interface to the C&DH, with a total of 52 bits for each sample of the magnetic vector field. There are 17 bits for each of the three axes, and 1 bit for the MAG range/sensitivity setting. The 52-bit MAG "vectors" are generated at a regular 16 Hz rate (every 62.5 milliseconds) based on an oscillator inside the MAG electronics. C&DH hardware will do the serial-to-parallel conversion and time-tagging required for FSW to read and process the data from MAG. The "time-tag" for each 52-bit MAG vector will consist of a seconds count and a sub-seconds count, accurate to 0.25 milliseconds. Each time-tagged MAG vector will require 16 bytes of memory.

The C&DH's SRAM buffering concept will accumulate sixteen time-tagged MAG vectors at a time, and then interrupt FSW at a 1 Hz rate. Two MAG data receive buffers in SRAM will be written into and read out by flight software (FSW) in a "ping-pong" arrangement. When FSW reads out the 256 bytes of time-tagged MAG vector data every second, it will then process that data for a science event (SE) and store it on the solid state recorder. Flow control is implemented at the receiving end, where FSW can enable or disable the flow of MAG vector data into the SRAM buffers.

The C&DH can collect and digitize analog telemetry for MAG total current, MAG electronics temperature and MAG sensor head temperature as described in Section 6.9.

6.3 Digital Sun Sensor (DSS) Interface

As the ST-5 spacecraft rotates at approximately 20 RPM, the Sun will pass through the field-of-view of the digital sun sensor (DSS) every 3 seconds. When this occurs, the DSS will generate a pulse that will cause the C&DH hardware to sample the sub-seconds count, and latch the eleven (11) bits of sun elevation angle data from the DSS. The C&DH hardware will then interrupt the flight software to signal that a new time-tagged measurement of elevation angle is available. All of the time-tag and elevation data will be held in registers until the next DSS pulse, so FSW will be required to service the DSS elevation data interrupt (by reading that data) within about 3 seconds. The C&DH can collect and digitize analog telemetry for DSS electronics temperature as described in Section 6.9.

6.4 Variable Emittance Controller (VEC1 and VEC2) Interfaces

For each of the two VECs, FSW will be able to set or clear two control bits to the VEC and read a status bit from the VEC. One control bit will set VEC mode to automatic or manual. In automatic mode, the VEC will adjust its emittance as necessary to regulate temperature around a fixed set-point. In manual mode, the second control bit will set the VEC to a low emittance state or a high emittance state. The status bit will confirm that VEC power is on, that the VEC's self-test passed, and that the VEC's multiplexed analog telemetry output signal is valid.

Regardless of whether either VEC is on or off, the C&DH will be able to collect and digitize analog telemetry from two thermistors for each VEC as described in Section 6.9. In addition to these four thermistors, each VEC has an active analog output that is internally time-multiplexed to make sixteen different analog measurements from inside that VEC. There is an analog channel select clock signal from C&DH (one for VEC1 and another for VEC2) that will select which of the sixteen internal analog signals will appear at the VEC's multiplexed analog output. The C&DH hardware will support an "automatic" process to sequentially select each of the sixteen analog channels and digitize that channel's signal. FSW will only have to initiate this automatic process, and when hardware has done all sixteen analog-to-digital conversions, and stored all sixteen bytes of digitized data in the SRAM, it will interrupt FSW to signal that the VEC analog data is ready to read from SRAM.

6.5 Constellation Communication & Navigation Transceiver (CCNT) Interface

The main flow of information between the C&DH and CCNT will be in the form of N-byte message packets over a full-duplex, 38.4 kbaud asynchronous serial data link. All message bytes will be sent in a 10-bit "frame," with one start bit and one stop bit. The bytes in each message will be formatted according to the JPL-developed BlackJack Data Link Protocol.

The transmission of BlackJack (BJ) message packets from C&DH to CCNT will be controlled by FSW pre-loading any one of eight CCNT transmit buffers (in the SRAM) that defines the size of the transmit message and the bytes to be sent. After pre-loading a transmit buffer, FSW will only have to write to a transmit start address to command the hardware to initiate and complete the message transmission. The FSW will then be able to do other tasks like GN&C computations, MAG data processing, etc., while the outgoing BJ bytes are serialized and transmitted automatically under FPGA control. When each BJ message transmission process completes, the C&DH hardware will set a CCNT transmit done interrupt bit.

The types, sizes and rates for BlackJack message packets from CCNT to C&DH will vary as required for different modes of CCNT operation. A series of CCNT receive buffers (in the SRAM) will be used to regulate the flow of BJ message data from the CCNT, and thereby greatly reduce the frequency of interrupts required for FSW to receive and store the CCNT messages. The CCNT receive buffers will each hold 256 bytes. Each time that one of these buffers fills, the C&DH hardware will notify FSW and the next receive buffer will start filling. There will be thirty-two (32) receive buffers in the SRAM, and these buffers will be arranged in a "circular queue" structure where the buffers always fill in the order 0, 1, 2...29, 30, 31, 0, 1, etc. In a sense, this 32 x 256 allocation of SRAM will be set up like an 8-kilobyte FIFO. The C&DH hardware will maintain readable counters to keep track of which receive buffer is actively being filled, how many unread receive buffers still need to be read out, and which receive buffer holds the oldest unread data. Having multiple CCNT receive buffers (which can be read out individually or in groups and at any time) will provide a very flexible design with low FSW overhead. The only constraint is that the flight software must keep up with the average rate of data flow from the CCNT. Very large BJ messages to or from CCNT will be able to "span" multiple transmit or receive buffers (if necessary). Flow control will be implemented at the receiving end for packet transfers in both directions.

When the local C&DH processor "detects" a science event through real-time analysis of MAG vector data, it will send a science event warning (SEW) to the local CCNT as a BJ serial message packet (see above). The local CCNT will then pass this science event warning on to the other members of the constellation over the S-band cross-link. When the local CCNT receives a science event warning message over the S-band cross-link from a remote CCNT in one of the other spacecraft in the constellation, the local CCNT will generate a pulse on a discrete signal line to the local C&DH. When the C&DH hardware detects this pulse, it will latch the seconds count, latch the sub-seconds count, and interrupt FSW to signal that a SEW has been received. The incoming science event warning was implemented as a discrete signal because the FSW does NOT interpret (but only stores) BlackJack messages from the CCNT.

The C&DH can sense the CCNT total current and S-band power amplifier temperature as described in Section 6.9.

6.6 Propulsion System (Tank, Pressure Sensor, Thruster) Interfaces

The ST-5 spacecraft will have a single-thruster "cold gas" propulsion system in order to initially orient and then maintain the S/C spin axis with respect to the sun line and the ecliptic plane. The interfaces to the propulsion system will provide for on-off control and validation of the New Millennium technology cold gas micro-thruster (CGMT), and for collection of analog telemetry from the gas tank, thruster and thruster control electronics.

The times of thruster on-off control pulses can be phased with respect to the rotation of the spacecraft (via the 0.33 Hz sun sensor output pulses) or with respect to a 2 Hz clock that is derived from the spacecraft's mission elapsed timer. For either of these two thruster pulse "phasing modes," the FSW will write to a thruster pulse delay register and a thruster pulse width/duration register. Both programmable registers are set up as down-counters. The 2 Hz phasing mode will be used for spacecraft Δ-V maneuvers, and the DSS phasing mode will be used for initial sun acquisition and sun-precession maneuvers.

The pulse delay register resolution is 1 millisecond, and it sets the amount of time between the DSS pulse edge (or 2 Hz clock pulse edge) and the thruster valve open pulse. The maximum pulse delay is 8192 milliseconds for the DSS pulse phasing mode, and 499 milliseconds for the 2 Hz pulse phasing mode.

The pulse duration register resolution is 50 milliseconds, and it sets the amount of time that the thruster is actually on and firing. This is the same as the time between the thruster valve open pulse and the thruster valve close pulse. The pulse duration can be integer multiples of 50 milliseconds over the range from 50 to 450 milliseconds, with a special feature for leaving the thruster "on continuously" for the larger integer multiples such as 500, 550, 600, etc.

The C&DH can measure tank temperature, tank pressure and tank pressure-temperature calibration, CGMT temperature and TCE temperature. Please see Section 6.9.

6.7 X-band Transponder Interface

The C&DH supports electrical interfaces to the X-band transponder for uplink and downlink with the ground station, for control and monitoring of the internal operation of the transponder, and for sensing temperatures and other analog parameters that are inside the transponder.

The 64-bit CCSDS uplink command codeblocks are verified and stored by C&DH hardware as they arrive from the ground and through the transponder over a synchronous serial interface at 1 kbps. Flight software will be interrupted for the arrival of each uplink codeblock. ST-5 mission operations planning calls for one X-band downlink pass (20 to 30 minutes at either 1 kbps or 100 kbps) for each 10.5 hour orbit. The C&DH solid-state recorder (SSR) will store all of the spacecraft science data and health/status telemetry collected during that orbit, as a series of CCSDS-formatted Virtual Channel Data Units (VCDU). The C&DH design will provide a 1024 x 32 bit FIFO for rate buffering the downlink data as it flows from the SSR to the FIFO (where whole VCDUs are transferred under FSW control). The C&DH hardware then pulls 32-bit words from the FIFO and prepares them for synchronous serial baseband transmission to the transponder. The hardware will add a CRC checksum and the Reed-Solomon check symbols to the FIFO data, and do rate ½ convolutional encoding on the data as it is serialized. As the serial stream is sent through the transponder, it is up-converted to X-band for transmission from the transponder to the ground.

The C&DH and transponder will have separate 1 kbps synchronous serial data links to allow 16-bit command and control words to be sent from the C&DH to the transponder and allow 16-bit status words to be sent from the transponder to the C&DH. The command interface will be used to control the internal configuration of the transponder and set the downlink bit rate to 100 kbps or 1 kbps. A transponder hardware-decoded "special command" signal will go from the transponder to the PSE in order to cycle the C&DH power on-off-on and reset the Mongoose 5 processor. The transponder supports analog signals to and from the C&DH that are used to measure HPA temperature and crystal oscillator temperature, and sense the automatic gain control setting, carrier loop stress, and RF power level. Please see Section 6.9.

6.8 CULPRiT Logic Technology Interface

The CMOS ultra low-power radiation-tolerant (CULPRiT) logic technology will be validated in a Reed-Solomon encoder that is part of the telemetry downlink path. The CULPRiT encoder can be selected by a multiplexer to replace a standard Reed-Solomon encoder that is implemented in a conventional +5V CMOS logic process. The CULPRiT logic process lowers transistor turn-on thresholds to on the order of a tenth of a volt, so that the CULPRiT supply voltage can be as low as +0.5V. This alone could lower dynamic power dissipation for CULPRiT parts by a factor of 100. Control of positive and negative analog bias voltages is then applied to adjust the switching thresholds for process variations. This bias control will be done with a 10 kHz pulse-width modulated digital signal in conjunction with an analog low-pass filter. Power consumption measurements will be made by sensing current from the +0.5V supply.

6.9 Analog Telemetry Collection Interface

Analog telemetry includes all of the analog voltage, current, and temperature (thermistor) signals that are collected and digitized from many different subsystems and from all over the spacecraft. A number of analog telemetry measurements have already been mentioned for the PSE, MAG, DSS, VEC1 and VEC2, CCNT, propulsion system, transponder and CULPRiT logic technology. In addition to these, the C&DH board monitors voltage and/or current for its on-board supply regulators (+3.3V, +2.5V and +0.5V), and for the CULPRiT bias voltages. Also monitored are the temperatures for the C&DH crystal oscillator, the spacecraft top and bottom decks, the card cage side walls and the nutation damper. Two 1-milliampere current sources (one on the PSE board and one on the C&DH board) will be used to generate voltages across thermistors. The other analog telemetry signals will be actively driven at the source.

To sample and digitize the telemetry signal from any one of the analog sources (thermistors or active signals), there will be analog multiplexers on the C&DH card, and analog multiplexers on the PSE card. All of these multiplexers will funnel down to the input of a single 8-bit analog-to-digital converter (ADC) on the C&DH card, and this ADC will be used to digitize all of the analog signals on the spacecraft. Each analog telemetry signal, regardless of whether that channel is a thermistor or voltage or current, will have a unique 8-bit analog channel number (ACN) that defines the setting of analog multiplexer switches required to route that analog signal to the input of the ADC.

An automatic analog telemetry collection mode will significantly offload the processor FSW from having to do all the low-level micro-operations like: writing each set of analog multiplexer channel select bits (same as the ACN), waiting for the analog signal chain to settle, starting the analog-to-digital conversion, waiting for the analog-to-digital conversion to complete, and then reading the 8 bits of digitized data. For this automatic mode, FSW will pre-load any one of sixteen analog collection control tables (in the SRAM) that defines: the number of analog channels to digitize, which channels to digitize, and what order to digitize them in.

After pre-loading a control table with a table length and a sequence of analog channel numbers, FSW will then write a 4-bit number to an analog collection start address. This 4-bit number will select which of the sixteen analog collection control tables will be used to automatically sample and digitize the next group of analog telemetry measurements. After FSW has written to the collection start address, the analog data collection will proceed automatically under FPGA control. C&DH hardware will handle all the micro-operations for analog multiplexer bits and the analog-to-digital conversion, and then store the 8-bit data into an SRAM analog telemetry data table that is like a "mirror image" of the corresponding control table. When the entire analog data collection process completes, the C&DH hardware will interrupt FSW to signal that ALL the analog data is ready for readout from SRAM. Multiple control tables (which can be pre-loaded and then started in any order and at any time) will provide a flexible design with very low FSW overhead. The only constraint is that there cannot be more than one control table running at any given time because there is only one analog-to-digital converter.

7. C&DH Board Design Details

A block diagram of the C&DH electronics design is shown in Figure 4 below. This single processor system will interface to all other spacecraft subsystems and will support: data acquisition and control for the entire spacecraft, attitude control and maneuvering, command uplink and telemetry downlink, intra-constellation cross-link communications and science event detection. The C&DH design utilizes a variety of different memory types, and has a full set of registers for control, status and I/O functions. Many of these registers are internal to the Mongoose 5 processor itself, and many more are incorporated into the three Field-Programmable Gate Arrays: the M5 FPGA, the Uplink/Downlink FPGA and the Instrument FPGA.

7.1 Processor and Memory

The flight computer (C&DH board) is designed around a single Mongoose 5 (M5) 32-bit radiation-hardened reduced instruction set computer. The M5 processor is based on the LSI Logic LR33300 (with instruction cache, data cache and floating point unit) and will be clocked at 12 MHz. The M5 design also has a DRAM refresh controller, two general purpose 32-bit counters, a number of external interrupt pins, two full-duplex universal asynchronous receiver transmitter (UART) ports, and built-in Hamming code EDAC for 32-bit transactions on the memory bus. Memory types include electrically erasable programmable read-only memory (EEPROM), dynamic random access memory (DRAM) and static random access memory (SRAM).

The M5 processor was selected because of its reliability and recent familiarity from the Earth Observer-1 (EO-1) mission launched in November 2000 and the Microwave Anisotropy Probe (MAP) mission launched in June 2001. A significant fraction of the ST-5 flight software can be reused from MAP with little or no modification.

EEPROM—The C&DH hardware design provides 2 megabytes of EEPROM for non-volatile program storage, organized as 512k by 32 bits. The EEPROM is divided into two distinct regions: bootstrap EEPROM and re-writable EEPROM. The flight software residing in the 256-kilobyte bootstrap region of EEPROM is the loader code, which is necessary for loading new software into the re-writable region of EEPROM or into the processor's local portion of DRAM. The bootstrap region of EEPROM is permanently write-protected so that it cannot be overwritten. Any changes to the bootstrap region of EEPROM must be made before the EEPROM device is mounted to the C&DH board.

The code and data residing within the re-writable region of the EEPROM is a complete copy of the final flight software available at ST-5 launch. For faster real-time program execution, this software is available for copying into DRAM at processor boot-up. When the M5 processor is powered up to begin its initialization sequence, it will start fetching and executing instructions from EEPROM and then copy a portion of EEPROM into DRAM. Once the flight software has been copied over to DRAM, the M5 will begin executing instructions from DRAM. Note that the contents of the re-writable region of EEPROM can be only be changed on the ground through the use of an external write-enable jumper at the C&DH direct access test connector. Since ST-5 is only a 3-month mission, the content of the ground re-writable region of EEPROM is NOT re-programmable in flight. However, post-launch changes to the flight software are possible by uploading new instructions and data to DRAM.

DRAM—The dynamic RAM has a built-in error detection and correction (EDAC) capability that can correct and count single bit errors, and detect multi-bit errors caused by single event upsets. The C&DH electronics design has a total of 40 megabytes of DRAM, and that DRAM is organized into 40-bit "groupings." Since each 40-bit "grouping" includes eight bits used for Hamming code EDAC, there are actually 32 megabytes of usable DRAM, organized into roughly eight million 32-bit words. The 32 megabytes of DRAM are for processor code and data storage, and for solid-state

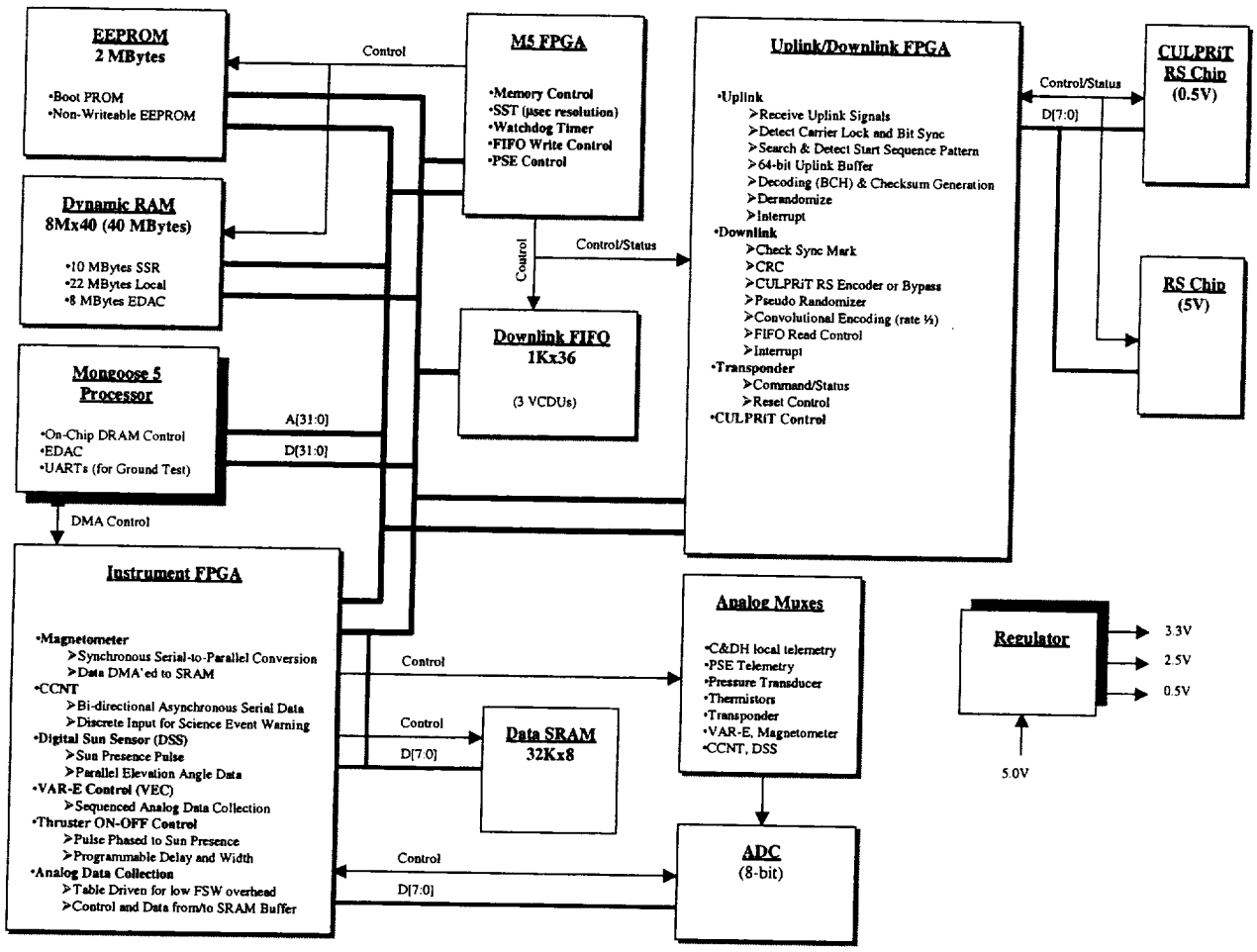


Figure 4: Block-Level Schematic of C&DH Board Design

data recording of all the spacecraft's telemetry over a 10.5-hour orbit. The current DRAM allocation for the processor's "local" memory for code, data, stack, etc., is 7 megabytes. After copying the required instructions and data from EEPROM to DRAM, the normal (and much faster) execution of the FSW will be out of DRAM. The current DRAM allocation for solid-state recorder (SSR) telemetry storage is 15 megabytes. The remaining 10 megabytes of DRAM are reserved.

SRAM—The C&DH hardware design will use a byte-wide SRAM for general-purpose buffering, collection and temporary storage of incoming MAG vector data, incoming and outgoing CCNT data, VEC1 multiplexed analog telemetry, VEC2 multiplexed analog telemetry, and spacecraft-wide analog/thermistor telemetry. The design will allow FSW to have continuous read-write access to a 16k block of SRAM, with interleaved hardware access to this same SRAM space through a direct memory access (DMA) controller.

The hardware will do DMA write cycles to SRAM to accumulate: incoming time-tagged MAG vector data, incoming CCNT messages, multiplexed analog telemetry from VEC1 (and VEC2), and analog/thermistor telemetry from all over the S/C. For BlackJack messages transmissions from C&DH to CCNT, the FSW will first write to SRAM to pre-load the entire outgoing message to CCNT. The hardware will do DMA read cycles from SRAM to fetch BJ message bytes and send them to the CCNT. For automated analog telemetry data collection (thermistors and active analog signals), the FSW will first pre-load an SRAM table that defines and controls the collection of analog telemetry data. Hardware will then do a DMA read from SRAM to select each analog channel, and then do a DMA write cycle to SRAM after each analog signal is digitized. When the entire table of analog measurements has been digitized, the FSW will do a series of reads from SRAM to collect the analog telemetry for storage on the SSR.

The SRAM part used for bi-directional data buffering is 32k bytes (32768 x 8). Since only 16k bytes are required for the C&DH hardware and software design, the part is divided into two redundant banks. From a software standpoint, the SRAM addressing is completely independent of whether Bank 0 or Bank 1 is selected.

7.2 Field Programmable Gate Arrays (FPGA)

The flight computer design currently has three Actel RT54SX32S field programmable gate arrays (FPGA): one for uplink-downlink data flow to the X-band transponder interface, and a second for spacecraft timer and thruster control functions. A combined analog telemetry signal collection and direct memory access (DMA) controller will be implemented in the third FPGA to off-load much of the processing required to handle multiple, asynchronous data streams and greatly reduce the average processor interrupt frequency. The RT54SX32S FPGA core uses a +2.5V supply while the FPGA I/O pins require a +5.0V supply. These FPGAs also have built-in triple mode redundancy to reduce the probability of single event upsets.

M5 FPGA—The M5 processor FPGA will mostly control onboard memory decoding for DRAM and EEPROM. A seconds timer, sub-seconds timer (SST) and watchdog timer will also be included in this device. The SST consists of a 22-bit up-counter clocked by a 1 MHz clock, so the C&DH board can keep track of sub-seconds time at a resolution as fine as 1 microsecond. The sub-seconds count can be "latched" and stored at the occurrence of certain events, the value then being used by the spacecraft to "time-tag" specific data and events. The purpose of the watchdog timer is to provide a method by which the C&DH board can autonomously reset itself in the event that the processor flight software departs from normal operation.

Uplink-Downlink FPGA—The uplink-downlink FPGA will decode uplink command data and encode downlink telemetry data. The uplink portion will receive an uplink serial data stream, detect carrier lock and bit synchronization conditions, search for the start sequence pattern, decode the BCH checksum, and de-randomize the serial data stream.

The downlink portion will: check for the 32-bit downlink synchronization mark, do the cyclic redundancy check calculation, do the Reed-Solomon (RS) encoding algorithm, randomize the data, and do rate ½ convolutional encoding. The flight software will read CCSDS VCDUs from the SSR portion of DRAM and write them into the FIFO. The FPGA will then read 32-bit words from the FIFO, and perform the operations just described. One RS encoder will be implemented in a standard +5V CMOS logic process. The CULPRiT +0.5 volt logic technology will be validated in a second RS encoder. The downlink portion of the FPGA will be able to select between either of the two RS encoders.

Instrument FPGA—The Instrument FPGA will control: the collection of serial digital data from the MAG and CCNT, the transmission of serial data to the CCNT, and the collection of analog telemetry data from all over the spacecraft. This FPGA will also contain the DMA controller that will be used to access the SRAM buffers, and the I/O interfaces for the two VECs. The collection and time-tagging and buffering of MAG science data will be per section 6.2. The transmit and receive interfaces for BlackJack messages to and from the CCNT were covered in section 6.5. The automatic analog data collection will be table-driven as described in section 6.9.

7.3 Flight Software Interrupts

There are a number of different events that can potentially interrupt the M5 processor's execution of the flight software. For each event that can interrupt the processor, there is a readable bit in an interrupt status register. Many (but not all) of the interrupts are "maskable," and for each bit in the interrupt status register there is a corresponding bit in an interrupt mask register. As each event occurs, if the mask bit for that interrupt is 1, then FSW will be interrupted immediately. Otherwise FSW can poll the interrupt status register to see if that event occurred. Some of the interrupt events include: uplink codeblock ready, downlink FIFO needs data, EDAC error status, sun sensor elevation data available, thruster pulse complete, MAG data buffer full, CCNT receive buffer full, CCNT message transmit done, science event warning received from CCNT, S/C analog telemetry collection done, and analog telemetry data ready for either VEC1 or VEC2.

7.4 Power Distribution and Mechanical

The PSE will provide +5.0V power to the C&DH, and regulators on the C&DH board will then derive the +3.3V, +2.5V and +0.5 volt supplies required by the various C&DH components. The M5 processor, EEPROM, FIFO, FPGAs and standard Reed-Solomon encoder use the +5V supply. The DRAM uses the +3.3V supply, and only the FPGAs need the +2.5V supply. The CULPRiT device uses the +0.5V supply. The first voltage regulator will convert +5.0V down to +3.3V. A second regulator will down-convert from +5.0V to +2.5V, and a third regulator will take the +5.0V down to +0.5V. Telemetry for voltage level and current draw will be provided for each regulator output.

The complete C&DH board assembly will be composed of two surface-mount printed circuit boards that are populated with electronic components on one side only. The two circuit boards (referred to as side A and side B for the complete assembly) are then laminated to a central aluminum heatsink. Cross-connections between the A side and B side are implemented through the use of "z-wires." Figures 5 and 6 show a preliminary layout concept for the A and B sides of the C&DH board assembly, with dimensions in inches. The 0.5 inch wide strip along the top edges of both sides is reserved for external I/O connectors. The two backplane connectors (a 110-pin and a 164-pin) will be mounted along the bottom edges of the two circuit boards. The two round holes along the long dimension centerline of the circuit boards are for "stiffener rods" that will fix the heatsink with respect to the card cage side walls. In Figures 5 and 6, it is worth noting that the z-wires, decoupling capacitors, and transient voltage suppressors are not shown. In other words, this will be a very dense board.

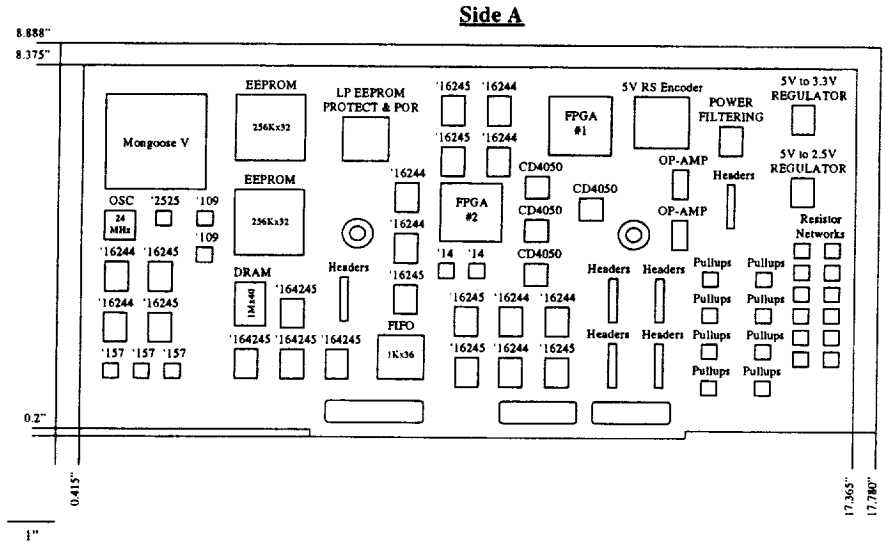


Figure 5: C&DH Board Assembly, Side A

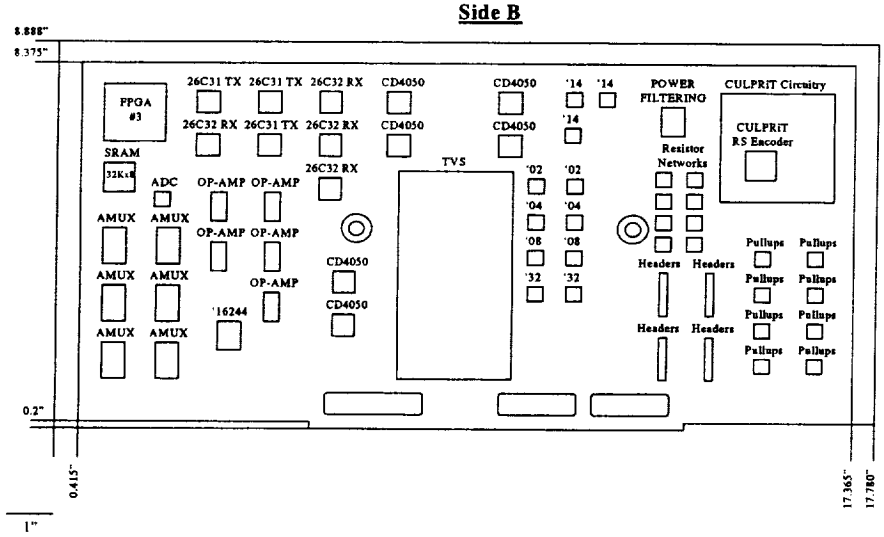


Figure 6: C&DH Board Assembly, Side B

8. C&DH Development Flow

Figure 7 shows the key C&DH development milestones and flow plan, starting from breadboard testing and ending at delivery of the third fully tested flight card cage to spacecraft #3 integration. There will be two C&DH breadboards; one dedicated to flight software development and the other for a "flat-sat" testbed where all subsystem prototypes and interfaces will be verified. The breadboards will be functionally equivalent to the flight units and will have the same electrical I/O connectors, but they will not be in the same physical format. Upon completion of breadboard testing, any C&DH flight design refinements will be based on breadboard hardware and software test results. Four flight units will be built in a time-staggered sequence, one for each of the three ST-5 spacecraft and one for a flight spare. There will not be engineering test units. Breadboard testing will start in March of 2002. Design, layout, fabrication and testing of the flight units will continue through the second half of calendar 2002. After stand-alone acceptance testing of C&DH flight unit #1 is complete, card cage #1 integration and testing with PSE flight unit #1 will begin. The first phase of environmental testing will be done at the card cage level. To meet the aggressive schedule with a relatively small development team, the stand-alone testing of later C&DH flight units will be done at the same time as (in parallel with) card cage testing of earlier C&DH flight units. Card cage testing is expected to begin in late 2002 and continue through the summer of 2003. The ST-5 mission is scheduled to launch in 2004.

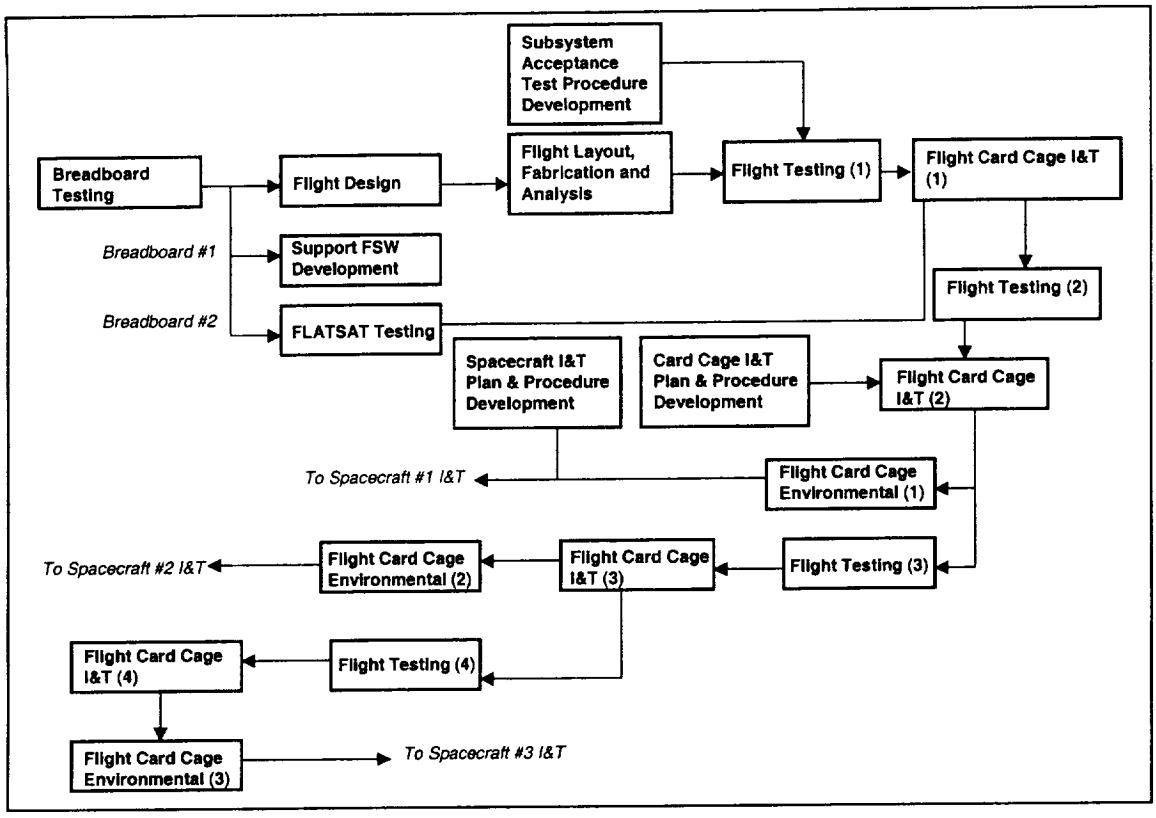


Figure 7: Development Flow for C&DH Design, Fabrication, Integration and Test Activities

9. CHALLENGES

Two of the many C&DH development challenges thus far have been power consumption and available board area. Design techniques to lower switching frequencies are being implemented to reduce power. To off-load a very busy processor that has to handle many asynchronous processes and data streams, a number of low level I/O and buffering functions will be implemented in hardware. To reduce board area, the C&DH design will use dense FPGAs, stacked memory, lead-less chip carrier components, and the widest available bus components. The flight software team is working hard to minimize their requirements for EEPROM, and the hardware designers have shrunk the number of FPGAs from four down to three.

One of the trade-offs introduced by trying to achieve a very low power design is the added complexity of having +5.0V, +3.3V, +2.5V and +0.5V power supplies, where each one has a regulator, voltage telemetry, etc. To minimize the impact we are partitioning the design to put all of the +3.3V components on the A side (of the two-sided board assembly) and all of the +0.5V components on the B side.

Another major challenge anticipated by the C&DH team is the timely delivery and integration of the CULPRiT technology. On the breadboards we are designing to accommodate two different CULPRiT fabrication runs; one that has built-in +5V to +0.5V logic level translators, and one that does not. And to reduce the possibility of noise problems for the +0.5V logic signals, the CULPRiT encoder (on B side of board) will be kept away from the high-speed +5V logic (on A side of board).

The very aggressive development, integration and test plan will be another formidable challenge. This plan may require simultaneous support from a small team of C&DH personnel at the breadboard, flight unit, card cage and spacecraft level, while three parallel S/C development flows proceed in a staggered but overlapping sequence. To save time and allow for parallel efforts, a significant amount of design and interface documentation will be prepared up front. This should help to enable the simultaneous development of flight software, ground support equipment and flight hardware. In addition, all of the external electrical interfaces are identical for the breadboards and flight units, so that integration and test procedures that are debugged during breadboard integration with support equipment simulators can be reused again and again during flight unit integrations on spacecraft #1, #2 and #3.

10. Conclusion

A compact, low-power, multi-function flight computer is being designed at NASA's Goddard Space Flight Center to meet the stringent requirements of a technology validation and nano-sat constellation trailblazer mission. Three identical spacecraft will be developed, integrated and tested during calendar years 2002 and 2003, with a launch to geosynchronous transfer orbit in 2004.

The ST-5 spacecraft is much smaller and less complex than some of its predecessors, such as the NMP Earth Observing 1 (EO-1) spacecraft and the Microwave Anisotropy Probe (MAP) spacecraft. These two predecessors were both much larger (by about 25x in mass and 50x in volume), with spatially distributed subsystems requiring a fiber-optic data bus, and roughly 600 watts of power available at +28VDC. ST-5 will have have about 22 watts of power available at +7VDC. MAP and ST-5 are spin-stabilized, where EO-1 is a three-axis stabilized design. And relative to EO-1 and MAP, the cost per spacecraft will be reduced by about 15x. For EO-1, the C&DH, uplink/downlink and housekeeping functions required three processors on four circuit boards, and the EO-1 attitude control/propulsion functions required one additional processor and four additional circuit boards. On ST-5 the same basic spectrum of C&DH, uplink, downlink, housekeeping, attitude control and propulsion tasks will be performed by a single, highly-integrated processor and a single circuit board.

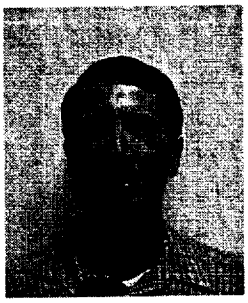
Validation of the CMOS ultra low-power radiation-tolerant (CULPRiT) logic technology will be a hugely successful breakthrough for the New Millennium Program. The ST-5 mission will demonstrate a CULPRiT Reed-Solomon encoder in the telemetry downlink path. A CULPRiT data compression chip is currently under development at the Institute of Advanced Microelectronics at the University of New Mexico, and CULPRiT technology processors could be the next logical step. A 50 to 100-fold decrease in electronics power consumption would enable a whole next generation of small space science missions.

Overall, the ST-5 mission has the potential to significantly explore the challenges of the low-power and miniaturized spacecraft subsystems that will be critical to the realization of large but low cost constellation mission architectures.

11. Acronym List

ACN	=	Analog Channel Number
ADC	=	Analog-to-Digital Converter
BJ	=	BlackJack (Data Link Protocol)
CCNT	=	Constellation Communication & Navigation Transceiver
CCSDS	=	Consultative Committee on Space Data Systems
C&DH	=	Command & Data Handling
CGMT	=	Cold Gas Micro-Thruster
CMOS	=	Complimentary Metal Oxide Semiconductor
CRC	=	Cyclic Redundancy Check
CULPRiT	=	CMOS Ultra Low-Power Radiation-Tolerant
DA	=	Direct Access (test connector)
DMA	=	Direct Memory Access
DRAM	=	Dynamic Random Access Memory
DSS	=	Digital Sun Sensor
EDAC	=	Error Detection and Correction
EEPROM	=	Electrically-Erasable Read-Only Memory
FIFO	=	First In First Out (buffer memory)
FPGA	=	Field Programmable Gate Array
FSW	=	Flight Software
GN&C	=	Guidance, Navigation & Control
GSFC	=	Goddard Space Flight Center
HPA	=	High Power Amplifier
Hz	=	Hertz
I/O	=	Input/Output
JPL	=	Jet Propulsion Laboratory
kbps	=	kilobits per second
kg	=	kilogram
MAG	=	Magnetometer
MET	=	Mission Elapsed Time (or Timer)
MHz	=	MegaHertz
M5	=	Mongoose 5 processor
NASA	=	National Aeronautics and Space Administration
NMP	=	New Millennium Program
nT	=	nano-Tesla
PROM	=	Programmable Read-Only Memory
PSE	=	Power System Electronics
RF	=	Radio Frequency
RPM	=	Revolutions Per Minute
RS	=	Reed-Solomon
S/C	=	Spacecraft
SEW	=	Science Event Warning
SRAM	=	Static Random Access Memory
SSR	=	Solid State (data) Recorder
SST	=	Sub-Second Timer
ST-5	=	Space Technology 5
TCE	=	Thruster Control Electronics
UART	=	Universal Asynchronous Receiver Transmitter
VCDU	=	Virtual Channel Data Unit
VEC	=	Variable Emittance Controller
XPDR	=	X-band Transponder

12. BIOGRAPHIES



Dave Speer is an embedded systems engineer with Northrop Grumman Electronic Systems, Space Technology and Services group in College Park, MD. He is currently involved in the design of the Command and Data Handling electronics for the ST-5 spacecraft. Prior to ST-5, he was responsible for design, integration, testing and documentation of the Attitude Control Electronics for the New Millennium EO-1 spacecraft. Before joining Northrop Grumman, Mr. Speer was employed at NASA's Jet Propulsion Laboratory (JPL) and at United Technologies Optical Systems (UTOS). While at JPL and UTOS, he designed and implemented real-time software and electronics hardware for embedded processor solutions to a wide variety of spacecraft and aircraft subsystem needs. Applications have included flight computers, data acquisition and control systems, imaging systems and electro-optic sensors, laser radars and ground support equipment. Mr. Speer has earned bachelor's and master's degrees in Physics from Dartmouth College, and a master's degree in Electrical Engineering from Georgia Tech.

George Jackson is an electrical engineer at NASA Goddard Space Flight Center's Flight Electronics Branch. He is currently the lead engineer for the ST-5 C&DH development. He began his career at NASA's Wallops Flight Facility as a co-op student in 1991. From 1994 – 1995 he designed, built and tested aircraft data systems for airborne science projects at Wallops. In 1995 he transferred to the Radiation Effects and Analysis Group at Goddard where he conducted radiation testing on fiber optic and opto-electronics components and was lead engineer for a fiber optic experiment on the Naval Research Lab's Microelectronic and Photonic Test Bed. From 1997 – 2000 he worked on the Earth Orbiter –1 program, designing the science input board for the Wideband Advanced Recorder Processor (WARP) and supporting WARP development through board, box and spacecraft level I&T and early orbit operations. He earned a Bachelor of Science degree in Physics from Salisbury State University in 1994 and a Master of Science degree in Electrical Engineering from George Washington University in 1999.

David Raphael is an electrical engineer at NASA/Goddard Space Flight Center's Flight Electronics Branch. He is currently the lead designer for the ST-5 C&DH development. He began his career at NASA as an intern for two summers in the SICA (Summer Institute in Computer Applications) program in 1991 and 1992. From 1994-1996, he served as a technical lead at NASA's Wallops Flight Facility for all sounding rockets missions involving the MMP-900 encoder systems, for which he wrote a NASA Reference Publication. In 1996, he transferred to the Flight Development Group at Goddard where he worked on the Earth Orbiter -1 program, designing the processor board for the Wideband Advanced Recorder Processor (WARP) and supporting WARP development through board, box and spacecraft level I&T and early orbit operations. He earned a Bachelor of Science in Electrical Engineering from Hofstra University in 1992, and a Master of Science in Electrical Engineering from the Johns Hopkins University in 1999.