MOSAD AND STREAM VISION FOR A TELEROBOTIC, FLYING CAMERA SYSTEM

FINAL REPORT SUMMARY

MOSAD©, Multiplexed OverSample Analog to Digital conversion, is a low power on focal plane analog to digital, A/D, process that places an oversample A/D at each pixel site. Two full custom designs for a visible light staring array were developed with this approach. One design approach uses a silicon photo diode in combination with photo gates at the pixel and the other approach uses an all photo gate sensor for detection. Both arrays were designed with a 320X240 format with the pixels placed on 16 micron centers. There are a total of 76,800 MOSAD A/D's on the chip, one per pixel. The devise is a monolithic integrated circuit that includes the sensors, A/D's and readout circuitry. A production 1.2 micron CCD/CMOS process provided by Supertex was used in the fabrication of the sensor. The A/D uses charge well switching at the pixel to convert the accumulated analog signal to digital data. There was negligible impact on the pixel area due to the A/D such that a fill factor of 73% was achieved with front side illumination for both approaches.

A complete camera system was built to demonstrate the technology. The system includes the camera assembly, driver interface assembly, a frame grabber board with integrated decimator and Windows 2000 compatible software for real time image display. The camera includes the sensor, either photo gate or photo diode, mounted on a PC card with support electronics. A custom lens mount attaches the camera to C or CS mount lens. Testing was done with a Tamron 13VM2812 CCTV CS mount lens. Both an RS644 and an RS422 parallel interface card assembly was developed to attach to the frame grabber board.

The final iteration cameras were tested at the Amain facility and pictures were taken. At 400 samples per second, measured on chip power consumption is under 10 milliwatts. Noise measurements at sample rates from 400 samples per second to 1,600 samples per second were taken for both parts. It was found that the photo gate noise performance was four times better than the photo diode. At 28 times oversample, the photo diode achieved 7 to 9 bits performance and the photo gate achieved 9 to 11 bits. Nonuniformity variation was below the noise floor. Nominally, the 28 oversample quantization error for delta sigma A/D is calculated at 7.6 bits.

An issue with the column compare sense amplifiers was discovered after the final iteration sensor was fabricated. This is a high current switching transient that, in mass, causes large spikes on the references. Incorrect sampling of the pixels results from these spikes. The photo diode was more susceptible to this transient than the photo gate. It was determined that the photo gate internal capacitance was sufficiently higher than that of the photo diode to provide filtering of much of the noise cause by the transient. This explains why the photo gate noise performance was superior. A new column compare design was developed that corrects the current switching spike, but this was not built due to funding and time limitations. There were issues with the Supertex process as well. Only three wafers out of ten survived in the run. These wafers were out of specification, having slightly high IDS, source drain leakage current. Yield at wafer sort was low, under 40%. In spite of these issues, the camera proved the fundamental MOSAD concept for visible light imaging. Performance is superior to CMOS designs and competitive with CCD as measured with the defective column compare sense amplifier. The simple N channel sensor provides a path to space based radiation hardening that can exceed either CMOS or CCD sensors. With the knowledge developed in this program, larger MOSAD array sizes and better performance can be achieved with future designs.

MOSAD and Stream Vision for a Telerobotic, Flying camera system
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APPROACH

MOSAD, Multiplexed Oversample A/D, per pixel

Multiplexed Oversample Analog to Digital Conversion, MOSAD, is a per pixel A/D approach that puts a Delta Sigma A/D modulator at the pixel. With MOSAD, the modulator integrators at each pixel are multiplexed into a common quantizer, with the quantizer being either 1 bit or n bits. This is shown in Figure 1. The division of the electronics is such that the integrator and subtractor of the Delta Sigma are at the pixel, the quantizer is shared at the edge of the array on a column. A decimation filter, if required, is time shared off the focal plane for processing all pixel. This minimizes the amount of electronics and power dissipation on focal plane for the A/D process yet provides a noise immune digital output from the focal plane.

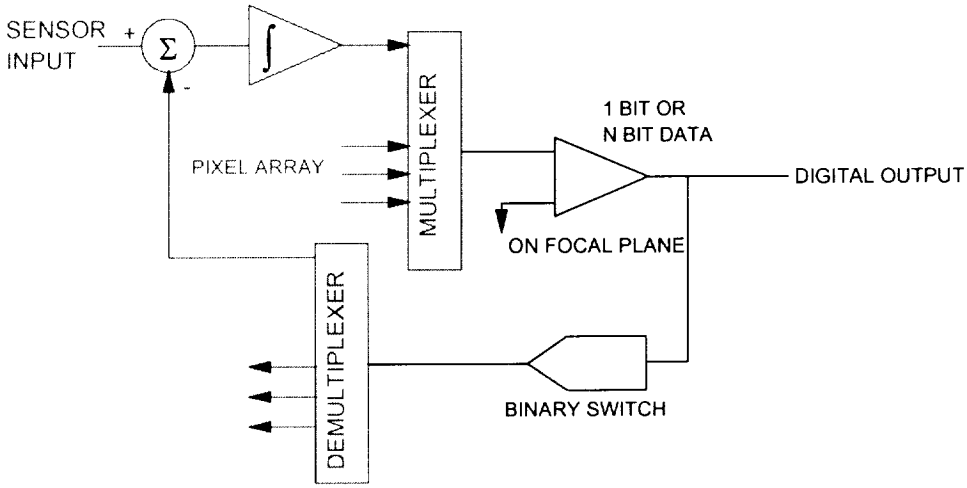


Figure 1 MOSAD per pixel oversample converter diagram

The ability to multiplex integrators onto a common quantizer is achieved through the self calibrating nature of the feedback process. Noise, offsets and nonlinearities added by the multiplexing process follow the well understood Delta Sigma noise equation for the forward loop and are attenuated by oversampling. Pixels are all referenced to true zero with detector dark current the only source of offset. Gain calibration per pixel may be required for the converter since it is set by the feedback subtraction. Typical semiconductor process variations can provide better than 1% gain accuracy across the array without calibration.

The one loop Delta Sigma modulator was selected as the method for A/D conversion. A generic schematic of the one loop circuit is shown in Figure 2 using CMOS switching electronics. This is a single ended switch design in which charge is only removed from the integration capacitor. Bipolar switched Delta Sigmas, which are more common for audio designs, alternately remove or add charge to the integration capacitor. Signal integration occurs with the accumulation of charge on the photo detector capacitance. The charge is sensed at the end of the column when the pixel is selected. As shown, generically this can be multi-bit sensing. The multiplexer is depicted with an isolation amplifier and switch, S_1, this is not a requirement to

implement the MOSAD Delta Sigma multiplexer but is shown for clarity. Offset error due to threshold variation of the amplifier is removed by the Delta Sigma continuous differentiation, sample to sample subtraction, of the output. Feedback demultiplexing is shown with the switch, R_1. Subtraction is charge removal which occurs by opening the connection path from the integration capacitor to the subtraction capacitor C_2. A fixed amount of charge is removed by charging the capacitor to a fixed voltage. Gain error occurs with threshold variation of the subtraction transistor relative the subtraction charge voltage. A bipolar switched design can avoid the threshold variation effect on gain with the addition of a high gain transimpedance amplifier to the integration capacitor. This would be inappropriate for a monolithic sensor as it would use excess pixel fill area.

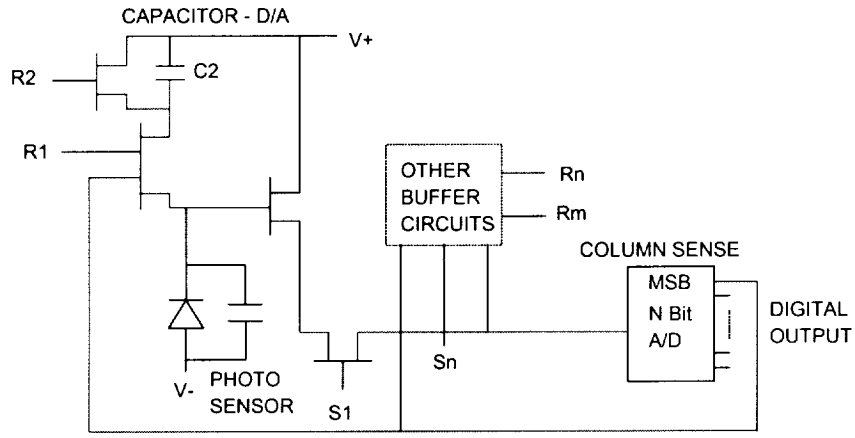


Figure 2 MOSAD monolithic photo sensor pixel architecture

For the single integrator circuit approach, the equation defining quantization error is as follows;

$$R(dB) = 6.02(N + 1.5D) - 3.41 \quad [1]$$

where R is quantization error in dB, N is the bit resolution of the sampler and D is the oversample above Nyquist in octaves (2^D is the sample frequency above Nyquist). This equation is an approximation for a one loop Delta Sigma. Generally, the one loop Delta Sigma A/D can achieve 2 bits better performance than the equation predicts for most of the dynamic range. In actuality, the one loop sigma delta has a variable quantization error that is dependent on signal amplitude. Figure 3 is a simulation plot of a one loop sigma delta with a 28 oversample value and a one bit output quantizer. An optimized low pass FIR filter was used to decimate from the oversample rate to Nyquist. The plot steps in 1% increments over a normalized dynamic range of 0 to 1. Vertical axis is noise amplitude, horizontal axis is dynamic range position. The scale is 1/500, 9 bits, on the vertical major tick marks and 1/1000 on the minor vertical tick marks. In this analysis, from the above equation, N = 1 and D = $\log_2(28)$ or 4.807. Solving equation 1 predicts a nominal quantization error of 7.67 bits. From the plot it is seen that the quantization error is different depending on signal amplitude. Except for the bottom and top 3% of the dynamic range, quantization error is better than 8 bits. For about 90% of the dynamic range, quantization error remains better than 10 bits. At the outer 3% of dynamic range bands, quantization noise peaks reducing accuracy to approximately 6 bits.

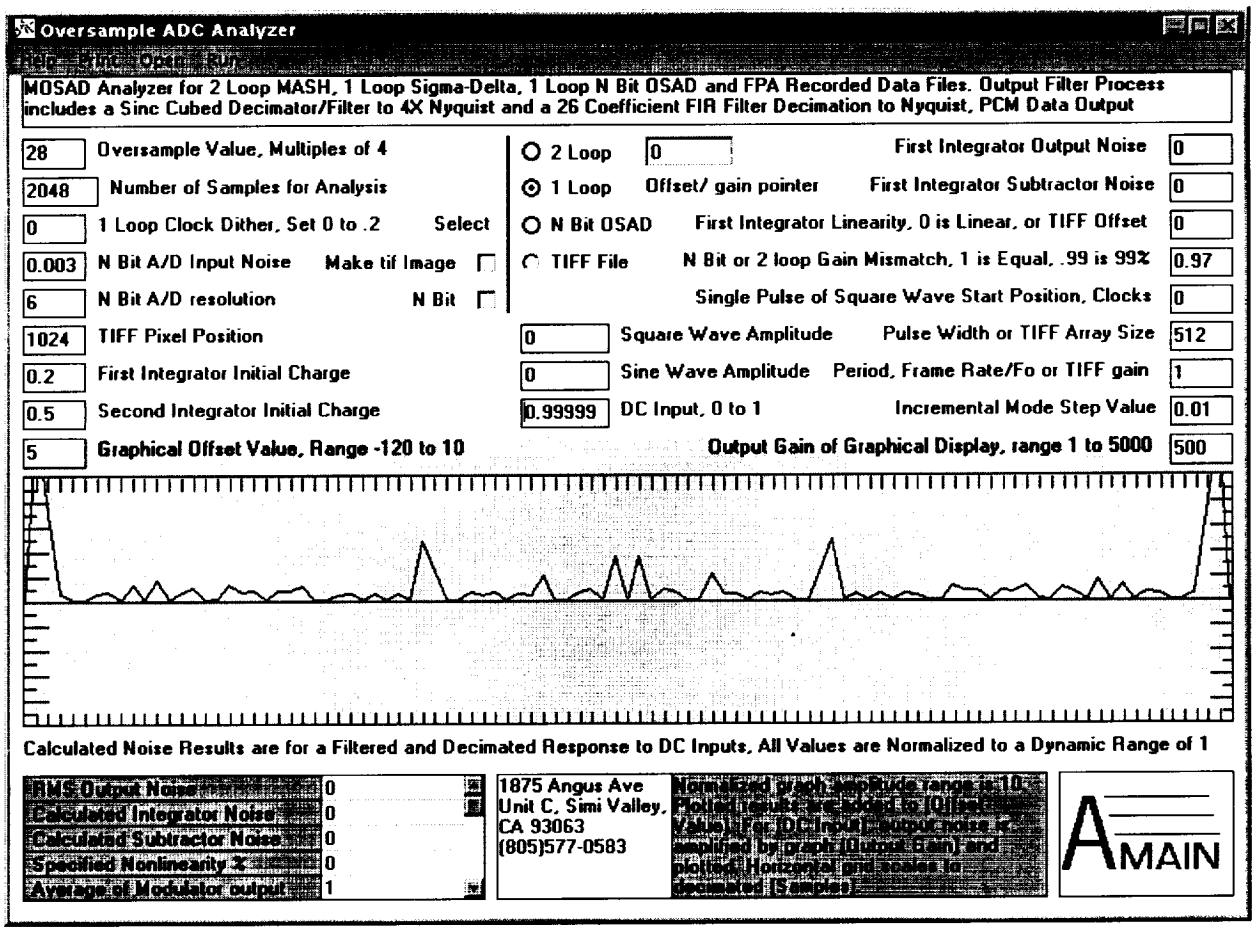


Figure 3 Simulation of a one loop Delta Sigma quantization error output with a one bit quantizer

Alternate Detector Sensor Approaches

There are two circuit approaches that were developed as the pixel A/D modulator. These are shown schematically in Figures 4 and 5. Figure 4 is the photo diode design and Figure 5 is the photo gate design. Both designs use a pixel read sampling approach similar to a non-destructive CID output with a read well attached to the column for direct readout (DRO). This eliminates the need for an isolation buffer amplifier on the multiplexer as shown in Figure 2, thus improving fill factor. The read well is shared by two adjacent pixels. This reduces by one half the attenuation of the output signal due to the capacitance load of the non selected floating gate outputs on the column. To further keep column capacitance low, the column is split in two with the upper half reading out the top and the bottom half reading out the bottom. For a 240 pixel column, the output signal will be attenuated by a factor of 60 to 1 with the multiplexing approach described. This attenuation has been important for analog CID readouts since it represents a factor by which the output voltage is reduced, or noise increased. With the MOSAD DRO digital sense, signal attenuation does not present a significant issue, as noise is also attenuated as defined in equation 1. A column sensor is used to measure the pixel response. With these non-buffered output designs the column sensor is 1 bit, N = 1, to provide maximum noise immunity. The issue for MOSAD then is to maintain sufficient amplitude for detection by column sense amplifiers, much like semiconductor dynamic random access memories, DRAMs.

In the photo diode DRO design shown in Figure 4, photon induced charge is collected in the wells under gates labeled Photo Diode and PG2/Select. A potential barrier separates the photo diode capacitor from the readout well. As with conventional non-destructively read CID designs, the readout well is connected to a floating gate common to all readout wells on the column. Charging, clearing and sensing of the floating gate is controlled at the end of the column with a sense amplifier and feedback control. The method of sensing, however, is much different from conventional CID analog readout. To sense charge, the readout well is biased as normal for conventional CID. PG2/Select potential is dropped for the selected pixel forcing its collected charge to be pushed into the photo diode. The photo diode capacitance being limited size, will spill excess charge over the potential barrier into the readout well. This caused a capacitive voltage shift on the floating column line. The small voltage variation can be sensed on the column as a minor blip. Sensing is 1 bit digital, the charge blip is either sufficient amplitude to trigger a binary 1 or no charge is sensed and a binary 0 is generated. A fixed amount of charge must be removed from the pixel when a 1 is sensed. This keeps the wells from overflowing and provides the processes for Delta Sigma A/D conversion.

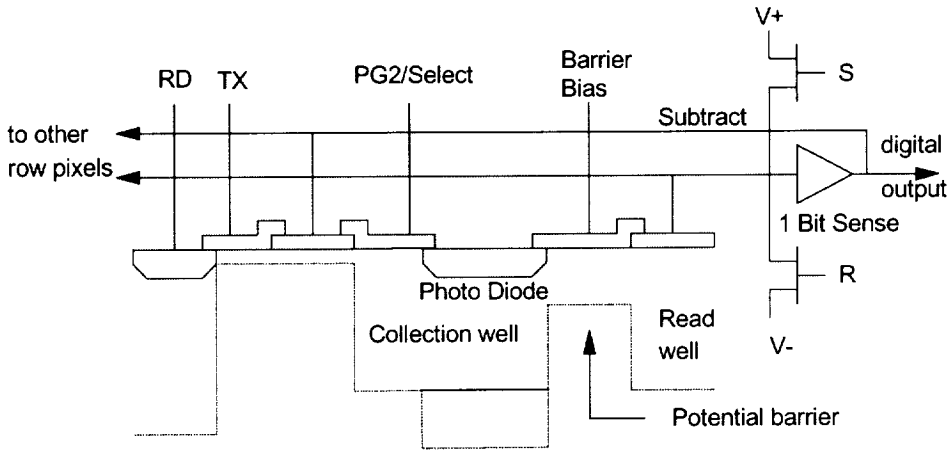


Figure 4 Photo diode DRO 1 loop MOSAD pixel cell

Charge removal consists of clearing the charge from the photo diode capacitor. The amount of charge removed is calculated from the photo diode capacitance and the potential barrier voltage. On the opposite side of the pixel from the read well, a charge sink drain removes charge from the circuit on subtraction and also acts as an anti-blooming stop. This drain runs along the row and is shared by adjacent pixels providing an blooming block. During the sense operation, the variable portion of accumulated charge is spilled into and held by the sense well. A fixed amount of charge is held in the photo diode capacitor. Equivalently, the photo diode capacitor performs the same function as C_2 of Figure 2. On sensing a 1, this charge is dumped into the drain RD by appropriately biasing the feedback and TX gates. The drain. RD, also acts as an anti-blooming stop. If a 0 is sensed, the feedback is held off preventing charge removal. On completion of the sensing operation, the variable portion of the charge under the sense gate is returned to the collection wells and the next dwell period is started. At this point the collection wells will contain the variable charge and the fixed charge if no subtraction took place. The approach used for charge subtraction is different than described in Figure 2, but functionally equivalent.

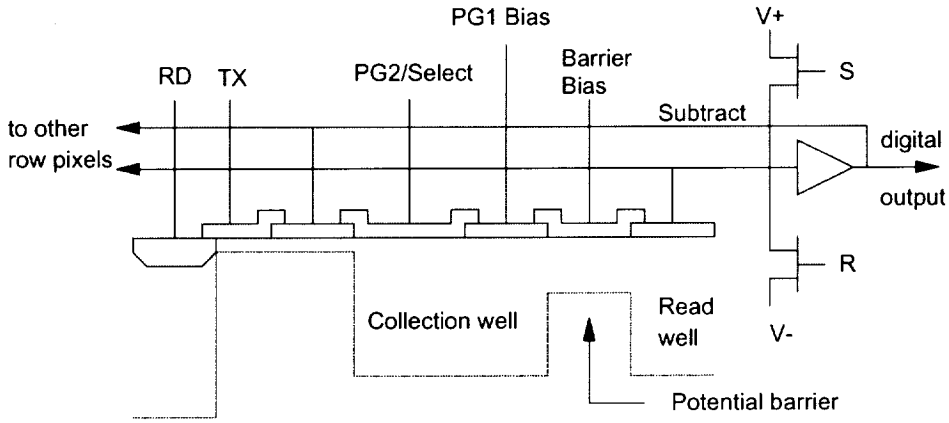


Figure 5 Photo gate MOSAD DRO schematic

The difference between the photo diode and the photo gate designs are in the collection well. In the case of the photo gate, the entire collection area is induced by a gate voltage over the well, PG1 and PG2/Select. The photo diode uses a conventional doped diode as part of the collection well. In this particular design, the photo diode was built with a lightly doped N region over the P well. Both approaches were developed for front side illumination application.

These two design approaches were selected for their potential of high radiation tolerance in a space borne background. There are no complimentary transistors in the array which can cause latch up. Complimentary logic is in the periphery control logic where there is sufficient space to design guard bar and other anti latch up approaches into the circuitry. The collection area uses charge wells like CCDs but does not sequentially transfer charge to the edge. Loss of charge transfer efficiency is not an issue. There is no analog sensing of the pixel output. This protects against errors or nonuniformity induced due to transistor threshold shifts. A potential for gain shift under radiation exists with threshold shift of the Barrier gate. Changes here will cause the subtraction charge to change. In the case of the photo gate design, the Barrier and PG1 gate thresholds will shift in the same direction thus reducing the effects. This is not the case for the photo diode which will see more of a gain change under radiation as the Barrier threshold shifts and the diode capacitance does not.

System Focal Plane Architecture

The array size chosen for implementation under this study is 320X240 pixel. This provides a sufficiently detail image for evaluation of the imaging capability and performance measurement. A block diagram of the physical pixel readout scan approach is shown in Figure 6. This diagram shows half of the readout with the half column of 120 pixels being sensed by individual sense amplifiers. The other half of the readout is read in the same manner. An interlaced progressive scan approach was used in the row select logic. Oversampling eliminates progressive scan temporal skew. The frame scan starts with the first row (top of array top half) and one hundred twenty first row (top of array bottom half). Odd rows are read first followed by even rows. There is a two row dead time between each half array scan resulting in 62 row scan periods for the odd rows and 62 row scan periods for the even rows. For accessing the full frame of pixels, CMOS shift register are used to position the row select pointer. The pointer is initiated with the start of frame. It shifts down the right side of the array pointing to the odd rows. The pointer is then passed to the left side shift register that points to the even rows.

The MOSAD comparators are arranged at the end of each half column and are time shared with the pixels on the column at readout. Further multiplexing of the column outputs, to reduce pinout count, is in the digital domain since all data is digital. This secondary column multiplexer is also a CMOS shift register requiring internal clock lines. To allow attachment to different logic devices, independently selectable voltages are used to power the output drivers. Both the positive and negative values can be set. A 40 to 1 digital multiplexer is used to group the column outputs. This produces 8 digital outputs per array half or 16 outputs for the device. The output format is a 1 bit Delta Sigma one loop response per pixel.

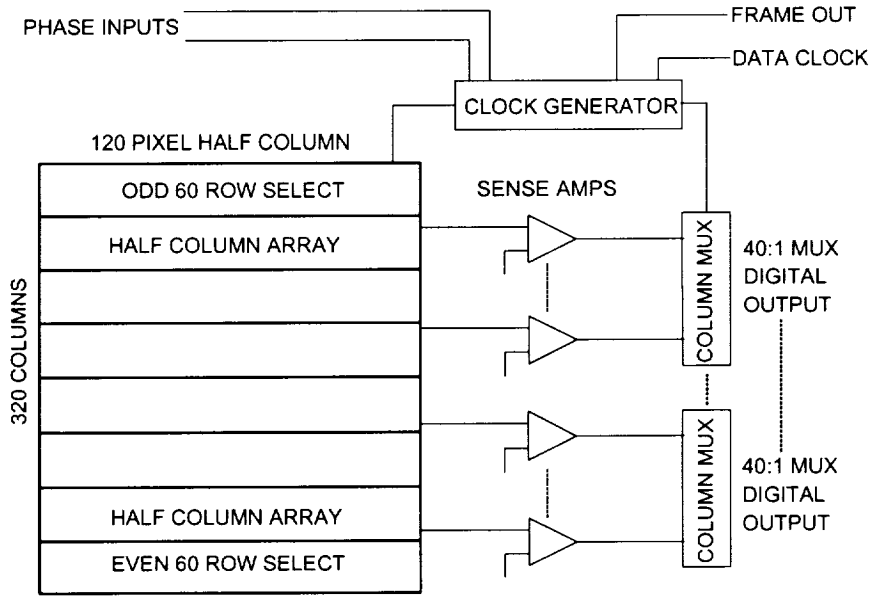


Figure 6 Block diagram of half array pixel scan approach

A two phase input clock operating at the output sample rate is used as the base timing reference. The two clock phases are square waves, 90^0 out of phase, generated by an off focal plane clock source. Output data, start of frame and data clock out are all derived from this clock input. An internal clock generator converts the two phase input into the clocking for the column multiplexer and for data clock generation. A second clocking unit down converts to the row scan rate and counts off the number of row scans to generate the start of frame pulse.

DESIGN

The Supertex 1.2 μ CMOS/CCD process was used for developing the prototype cameras. This process provides for a P CCD well for N channel CCD device construction. An N well CMOS switching logic process is also built in common on the same die. The CCD well supports a double poly overlapping gate design, two metal layers and both a lightly doped and a normal doped N active region. Gates are depletion mode N channel with the option for buried channel or surface channel. For this design, a surface channel approach was chosen. This is allowed because of the noise rejection characteristics of the MOSAD sensor which will reject the higher noise of the surface channel device. The CMOS portion supports P and N active regions, a single poly gate and two metal layers. Transistors, both N channel and P channel, are enhancement mode with a nominal 0.7 volt threshold. There are other devices also available with the process, none of which were required for the design. All of the devices are built to operate with a single power

supply nominally set at 5 volts. The readout design is partitioned such that the sensor array is built with the CCD structure and the control logic is built with the CMOS structure.

There are five major sub modules that make up the imaging array. They include the pixel array, sense amplifier, column multiplexer, row select logic, and timing and control logic. The pixels are laid out on 16 micron square centers in two 320X120 half array. Referring to figures 4 and 5, subtract and output wells are connected by metal in the column direction. The controls RD, TX, P2/Select, PG1 Bias and Barrier bias are connected in the row direction. RD is the anti-blooming and subtraction drain which is biased at +5 volts. Row select for subtraction is controlled by the TX line. This is normally set at 0 volts and switches to +5 volts when the pixel is selected for charge subtraction. The PG2/Select normally is set to +5 volts. It pulses to 0 volts to push charge into the output read well then returns to +5 volts. To induce the collection well in the photo gate pixel, PG1 is biased at +5 volts. The photo diode does not require the PG1 gate but relies on the diode capacitance for well capacity. A variable voltage potential is used as the Barrier bias. It can be set to any value that keeps a channel open to the read well. Since the threshold was not specified for the Supertex depletion mode devices, the operating value for the barrier bias is set at +1.2 volts. This creates a 3.8 volts potential difference for the subtraction well.

Figure 7 is the schematic of the column comparator. This design was developed after the final iteration. Testing showed the original design had high current transient spikes that cause a severe noise problem. The comparator logic performs several functions in setting up and reading the pixel as well as generating the subtraction feedback command. The pixel read approach is a capacitively coupled technique. Charge from the pixel is injected into a read well capacitor attached to the column. This is sensed at the comparator as a change in voltage on the column. The column is floating. To set up the column for a read, the commands CLR and CHG are used to clear the column of previous charge and then precharge the column to a sense potential. A three stage amplifier with a gain of approximately 20,000, amplifies any change in the floating column caused by the pixel charge injection. An offset is introduced into the amplifier input by the control HLD such that the signal must exceed the offset before it is amplified.. This provides as much as 5 millivolts of noise rejection. A two phase clocked quantizer samples the amplifier output and latches the result into a storage flip-flop. This creates the signal DIGOUT which is read as the output for the pixel and is fed back as the subtraction command.

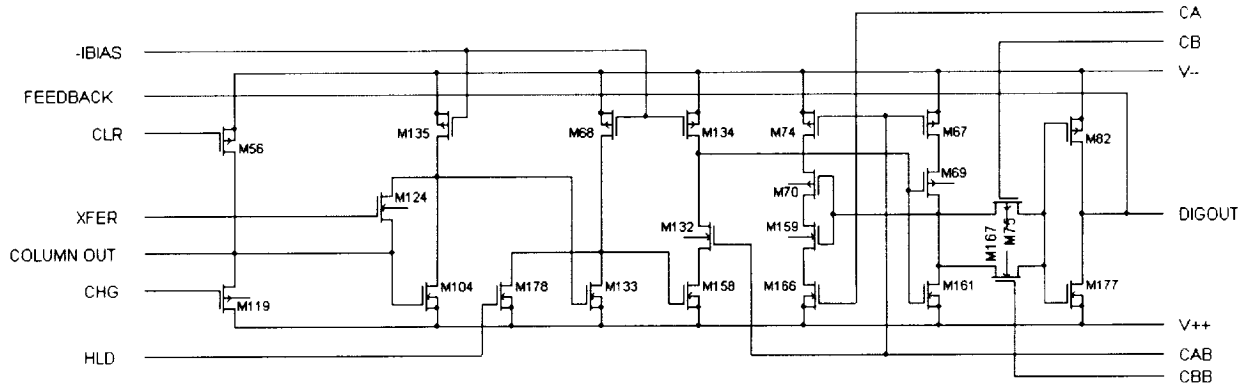


Figure 7 Revised column comparator developed after the final fab iteration

Figure 8 is the schematic of the column multiplexer and output driver. Each column output connects to a column multiplexer circuit. The circuit selects (SEL and SELB) either the column (DIGIN) or the shifted input from the adjacent column (SHIFTIN). Both the shifted output (SHIFTOUT) and focal plane output (DRIVEOUT) are shown. The multiplexer circuits are arranged in groups of forty. A DRIVEOUT circuit is attached to the fortieth multiplexer and the SHIFTOUT circuits are attached to the other thirty nine multiplexers. To provide the forty to one multiplexed output, the select command occurs at the row scan rate and there are forty C8 clocks per select command. The output driver is a CMOS digital switch with isolated rails (+VDRIVE and -VDRIVE). This allows the output voltage swing to be set at any range within the operating +5 volt power supply (V++).

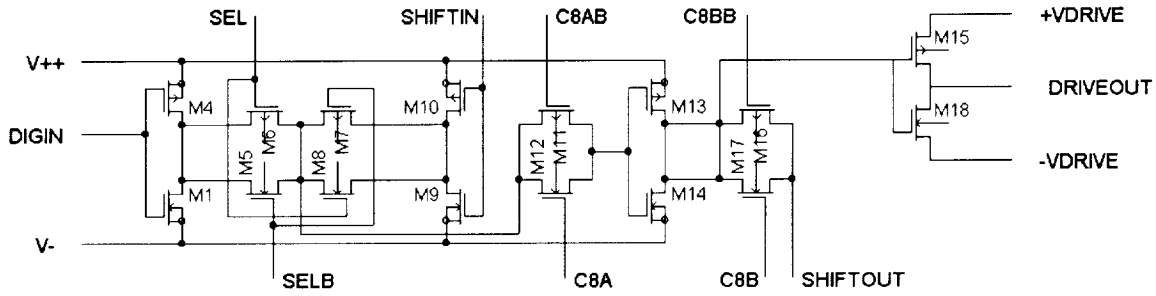


Figure 8 Column multiplexer and output driver.

The above circuits are discussed in more detail as they represent the critical areas for noise performance and switching speed limits. Two other remaining significant circuit blocks are the row scan logic and the timing and control. The row scan logic uses a four stage, two phase shift register per row. A bit is sequentially shifted four positions per row, starting with the top row. Two pulses are generated as the bit passes through a row. These are the PG2/Select command and the TX command. The PG2/Select command is generated first causing the selected row of pixels to be read. This is followed, the next clock period, with the TX command which enables the subtraction operation for the row of pixels. The remaining two clock periods allow time for the reset and precharge of the read column.

There are four separate circuit components that compose the timing and control. These include the two phase clock generator, frame timing generator, column comparator timing generator and the column multiplexer timing generator. There are also delay registered used to align and distribute the timing signals. Two clock structures are used in the system. Column multiplexing is controlled by the high speed clock which runs at the input oscillator rate. Row scanning is controlled by the row clock. This clock runs at a tenth the speed of the column multiplexer clock and four times the row scan rate. This sets the 40:1 row scan to column multiplexer ratio.

There is a low speed clock running at twice the frame rate to control the pixel Barrier bias. Odd even pairs of pixels share a common read well. To facilitate the interlace scanning, the Barrier bias is switched off, 0 volts, to the pixels that are not in the scan sequence. Thus the odd pixels are disconnected during the even pixel scan and vise versa. This insures that the residual charge in the read well will be returned to the correct pixel after a read operation. The Barrier bias switching is very low speed using under two row scan periods to settle. This accounts for the

two row dead periods between half array scans. This provides stability to the reference which is critical in establishing the gain and a measure of noise performance for the A/D conversion process.

Sensor Layout

Figures 9 and 10 are the physical layouts for the pixels of the two approaches. In Figure 9, the photo diode and Figure 10 is the photo gate. The nomenclature depicted for the component elements is different in the layout from that of the schematics, figures 4 and 5, but functionally the same. Both layouts achieve a fill factor of 73% in a 16 micron pixel using the Supertex 1.2 μ CCD design rules. For the photo diode design, the diode portion of the area is 30% of the pixel. The maximum gate fill factor possible with this process for this pixel size is 87%. This fill factor limitation is due to the process requiring a separation of at least 2 μ between pixels. In our design this separation runs in the column direction. The subtract and output metal lines stack over the separation, thus not using gate fill factor. Loss of fill factor from the allowable maximum is due to the poly contacts and gate separation rules needed to construct the read well and subtraction well. Also, the drain which run perpendicular to the column in the row direction uses surface are. Both the drain and read well are shared with adjacent pixels on the column. This cuts in half their effect on fill factor loss.

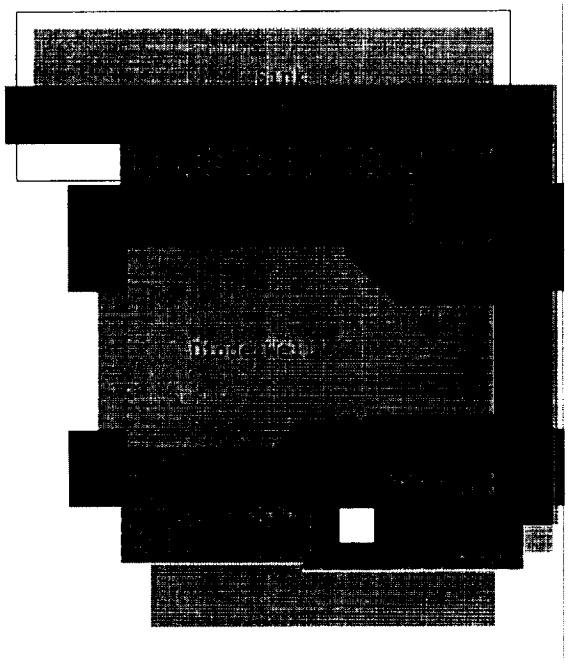


Figure 9 Photo diode layout

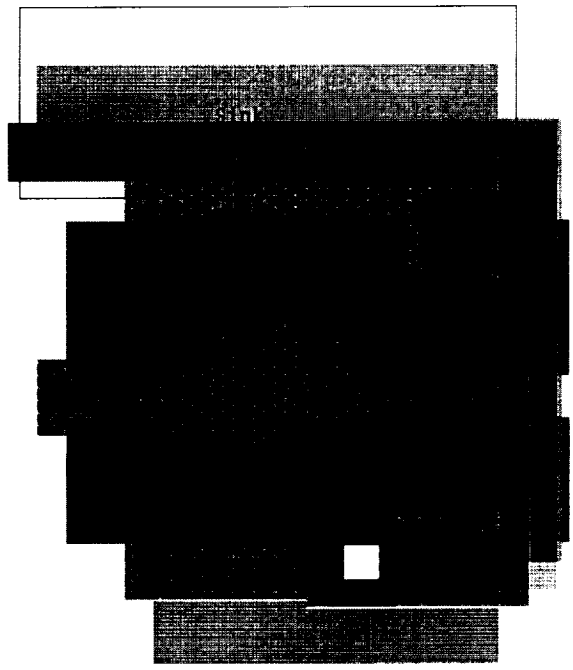


Figure 10 Photo gate layout

Well capacity is determined by the Bias well capacitance, Barrier potential and the oversample rate above Nyquist. Bias well capacitance is determined by the layout and the capacitance of either the gate or the photo diode. In both layouts the well capacity was maximized. The photo diode capacitance, CCD well drain, is not specified by Supertex. An accurate calculation can not be completed. Photo gate capacitance is specified at a nominal 0.45 ff/μ^2. In this layout, the Bias well capacitance is 18 ff based on the 40 μ^2 area and the total gate area is 59 μ^2 with a 26 ff capacitance to V++. With a 1.2 volt Barrier bias, 3.8 volt well potential,

capacity is $4.3X10^5$ electrons per sample. An oversample value of 28 produces $1.2X10^7$ electrons capacity.

The layout of the column comparator is shown in figure 11. Transistor sizing was such that a stepping distance of 32 microns, two pixels, was set as the size for the column increment. This required that two comparators be laid out in tandem to match the pixel step size. The critical sensing portion of the two comparators are laid out together on the column lines. Capacitances are matched to insure sense gain is the same for both columns. Power busses are separated such that the sensing portion shares power with the pixel array and the digital portion shares power with the digital logic. Circuit and layout are correct, however, the separation of the power busses was incomplete. All of the N wells are connected. This allows a current path through the well for logic switching transients to influence the sense logic. This is also true for the P substrate. Since sensing is referenced to V++, N well potential variations can affect the sensor.

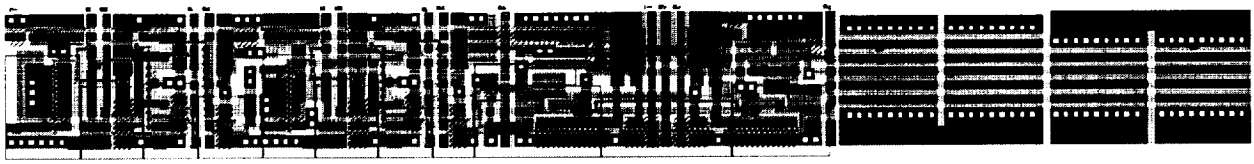


Figure 11 layout of dual column comparators

A layout of the clock generator is shown in figure 12. This clock generator creates the two phase clocks used for row scan and for column multiplexing. The input requirement is two square waves 90 degrees out of phase operating at the data clock rate. This supplants an original approach for external eight clock pulses, four for the row scan and four for the column multiplexing. One of the clocks for the column multiplexor connects to an output pad to provide a reference clock for the data output. The start of frame marker is derived using a counter driven by the clock generator. This circuit layout is shown in figure 13. Start of frame occurs every 4,960 data clocks. Data is read out in burst of two blocks, each block consisting of 2,400 sixteen bit words. There is a 80 clock blank time between each data block. The start of frame pulse is 10 data clocks in duration. An output data clock is also generated on focal plane.

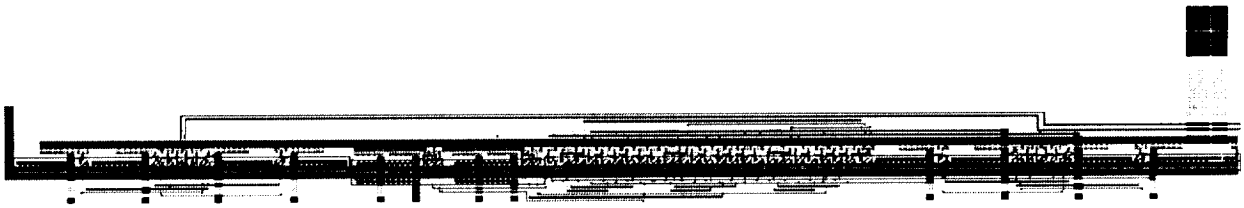


Figure 12 Clock generator circuit

Figure 13 Frame mark generation counter

Figure 14 is a diagram of the physical layout of the entire device. Both the photo diode

array and photo gate array are identical at the top cell level. The active area die size is 6.49 by 5.81 mils and the photo sensitive area is 5.12 by 3.84 mils. This calculates to a 48% overhead for support electronics and I/O pads. Bonding pads are arranged on top and bottom edges as dual pads to allow separate support for wafer probing and die attach. There are 29 pads total. Data output requires 18 pads of which 16 are for digital data and two, +Vdrive and -Vdrive are for the output binary voltage references. Four pads are used for device power, two for V++ and two for ground. They place diagonally opposite one another near the array corners to reduce effective internal buss resistance. Four pads are required for timing including the two phase input clock, output data clock and start of frame. The three remaining pads are input biases including a current bias for the amplifier constant current loads, the Bias voltage for the Barrier potential that set A/D gain and the operational amplifier bias that sets noise tolerance.

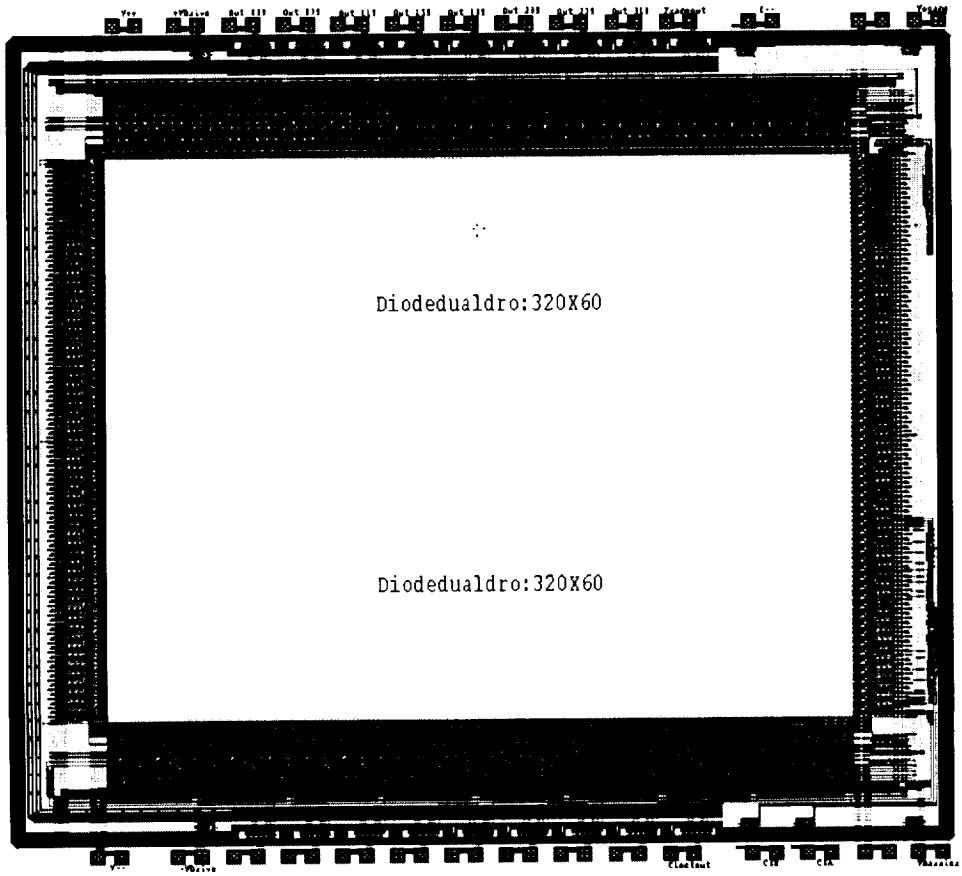


Figure 14 Top composite diagram of the focal plane array

The top cell hierarchical reference, Diodedualdro: 320X60, refers to the half array of dual pixels, in this instance it is the diode array. Each half array is 320X120 pixels. To insure identical pixel responsivity at the juncture of the two half arrays, they adjoin together on the horizontal drain. This allows the column metal busses to be split apart over this biased active region where there is no photo sensitivity. Layout, photo sensitive area and stray capacitance remains identical for all of the pixels over the array.

The designation for array type is marked on the upper right corner on the metal 2 layer. Figure 15 is a close up view showing how the die is marked. The nomenclature 320X240 D under the AMAIN-MOSAD reference indicates that this array is a diode array. The gate array is

marked with the nomenclature 320X240 G.

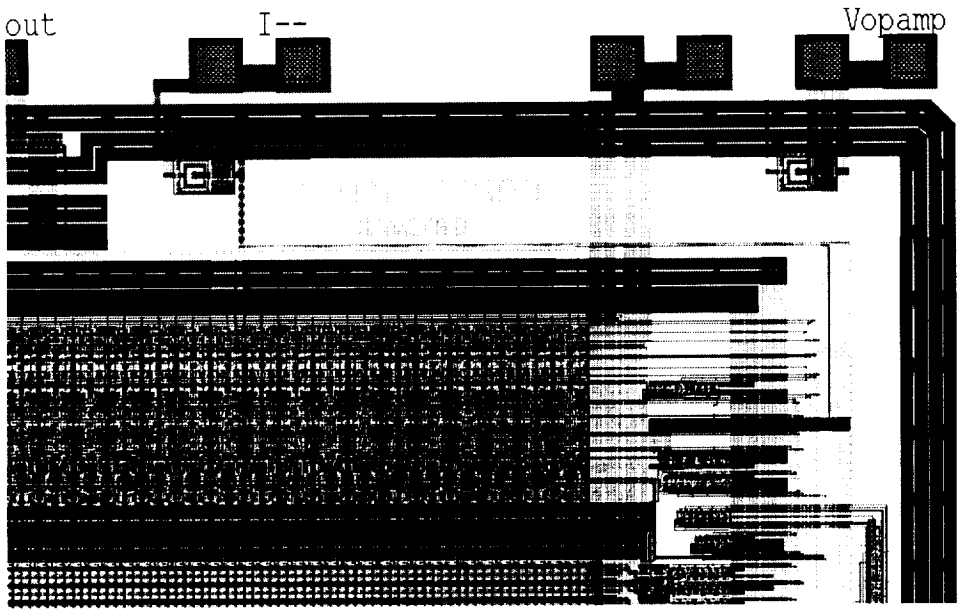


Figure 15 upper right corner designating array type

Camera design

A complete stand alone camera system was built and demonstrated as the end product of this development program. The camera consists of two electronic assemblies. A PC board to house the camera chip, support electronics and lens mount is the main assembly. A second daughter board to support computer interfacing was also developed. The design for the camera board is shown in the schematic of figure 16. This design is a modification of the original breadboard used for demonstrating the previous iteration camera chips. The electronics include the clock generator, a stable 5 volt power supply and other passive components including resistors and capacitors for biases and transient suppression. There are three 8 pin header ribbon cable style connector also on the board. These allow attaching the interface daughter card or ribbon cables for connection to other electronics. Two of the headers carry the 16 data outputs. The third header interconnects power and timing signals. A CMOS inverter biased in the astable state forms the on board oscillator. The frequency is crystal controlled and is set at the required data rate. Two serially linked inverters with an RC delay between them create the shifted two phase clock from the oscillator output. The biases Vbarrier, Vopamp and I– are derived on the board from filtered resistor networks attached to the five volt supply and ground. Raw power for the 5 volt regulator and the +Vdrive and -Vdrive are supplied to the camera board externally.

Figure 17 is the top side layout of the two sided camera PC board. Only the active components are surface mount including the sensor, oscillator IC and power supply. All other components are through hole mount. Dimensions are 2.1" X 2.1"on a side. All of the components are mounted on the top side including the lens mount. The board attaches flat against the lens holder with two screws. This provides a light sealed optical cavity for the imager with provisions for either a CS or C style lense attachment. There are two parts to the lens mount assembly. The primary mount that holds the lens is tubular shaped with C internal threading. It has two 4-40

tapped mounting holes for screw attachment to the PC board. To allow for height adjustment, a second threaded insert is used with the primary mount. It threads in on the PC board side of the mount. This allows adjusting the flange height correctly for the back focal length distance of the lense to suite either C or CS lenses. Figure 18 is a photograph of the camera board with a Tamron 13VM2812 CCTV CS mount lens mounted to the camera. This photograph was taken close up, approximately one inch distance, with the MOSAD photo gate camera.

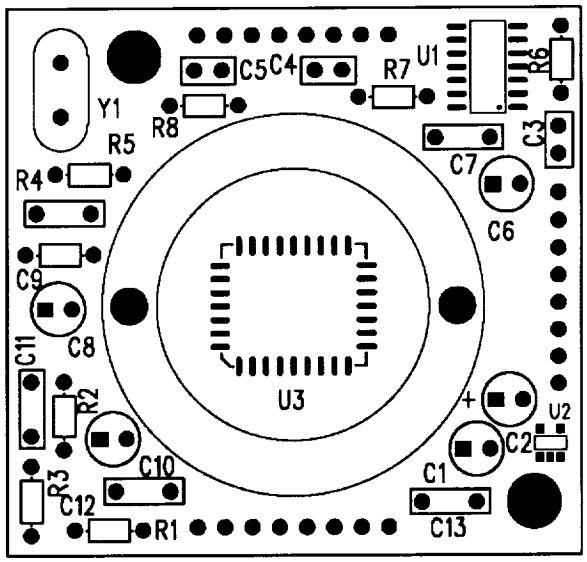


Figure 17 Top side assembly of camera board

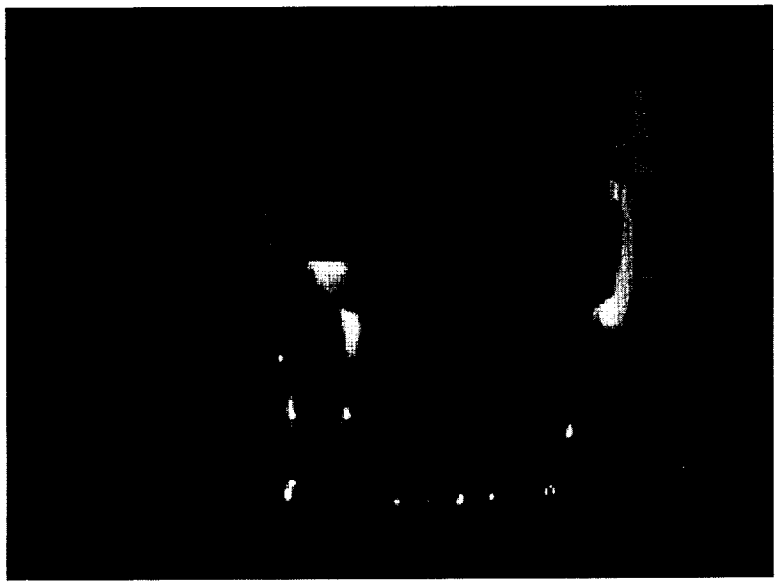
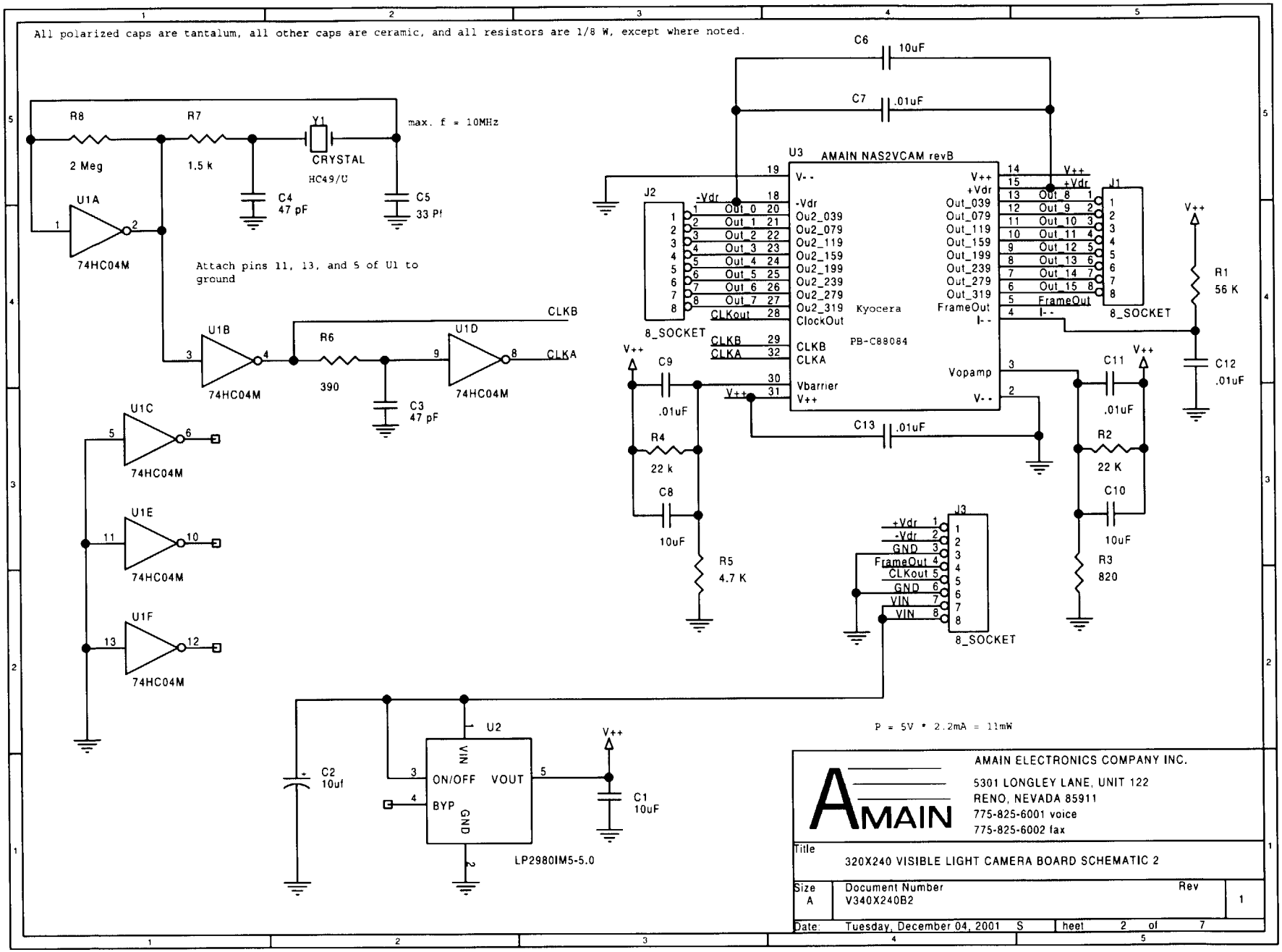


Figure 18 Photograph of camera taken with a MOSAD

Two interface daughter boards were developed for the camera, one supports RS 644 protocol and the other supports RS422. The schematics of the two boards are shown in figures 19 and 20. Functionally, both boards are the same. The difference is in power levels. On board


All polarized caps are tantalum, all other caps are ceramic, and all resistors are 1/8 W, except where noted.
R8
2 Meg
R7
1.5 k
Y1
CRYSTAL
HC49/U
max. f = 10MHz
C4
47 pF
C5
33 Pf
U1A
74HC04M
Attach pins 11, 13, and 5 of U1 to ground
U1B
74HC04M
R6
390
C3
47 pF
U1D
74HC04M
CLKB
CLKA
U1C
74HC04M
U1E
74HC04M
U1F
74HC04M
C6
10uF
C7
.01uF
U3
AMAIN NAS2VCAM revB
Kyocera
PB-C88084
V- -
-Vdr
Ou2_039
Ou2_079
Ou2_119
Ou2_159
Ou2_199
Ou2_239
Ou2_279
Ou2_319
ClockOut
CLKB
CLKA
Vbarrier
V++
+Vdr
Out_039
Out_079
Out_119
Out_159
Out_199
Out_239
Out_279
Out_319
FrameOut
I- -
Vopamp
J2
8_SOCKET
Out_0 Out_1 Out_2 Out_3 Out_4 Out_5 Out_6 Out_7
CLKout
J1
8_SOCKET
Out_8 Out_9 Out_10 Out_11 Out_12 Out_13 Out_14 Out_15
FrameOut
R1
56 K
C12
.01uF
C9
.01uF
R4
22 k
C8
10uF
R5
4.7 K
C13
.01uF
C11
.01uF
R2
22 K
C10
10uF
R3
820
J3
8_SOCKET
+Vdr
-Vdr
GND
FrameOut
CLKout
GND
VIN
VIN
P = 5V * 2.2mA = 11mW
U2
LP2980IM5-5.0
VIN
ON/OFF
BYP
VOUT
GND
C2
10uf
C1
10uF
AMAIN ELECTRONICS COMPANY INC.
5301 LONGLEY LANE, UNIT 122
RENO, NEVADA 85911
775-825-6001 voice
775-825-6002 fax
Title
320X240 VISIBLE LIGHT CAMERA BOARD SCHEMATIC 2
Size
A
Document Number
V340X240B2
Rev
1
Date: Tuesday, December 04, 2001
Sheet 2 of 7

power is 3.3 volts for the RS644 board and 5 volts for the RS422. The camera drive references are generated on the interface cards using a 2.5 volt regulated source for +Vdrive and ground for -Vdrive. Either board attaches to the camera with three 8 pin socket connectors aligned to the camera headers. Connector pin friction is sufficient to hold the boards together and mounting holes for screws and standoffs are provides for permanent mount. Figures 21 and 22 are the top side layouts of the boards. Components mount on the top side as well as the 4 pin power header and the 40 pin data output header. The three 8 pin sockets mount on the backside for camera attachment.

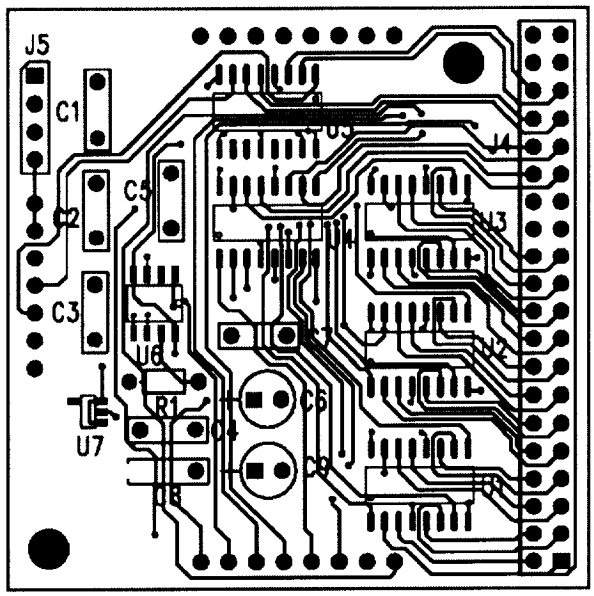


Figure 21 RS644 board layout

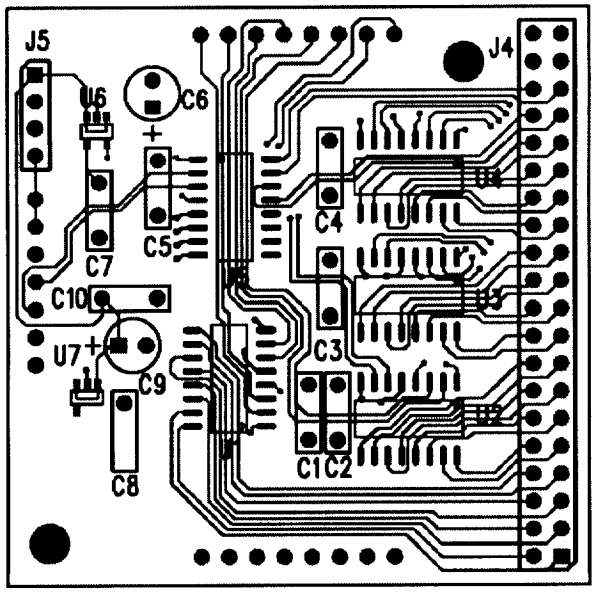
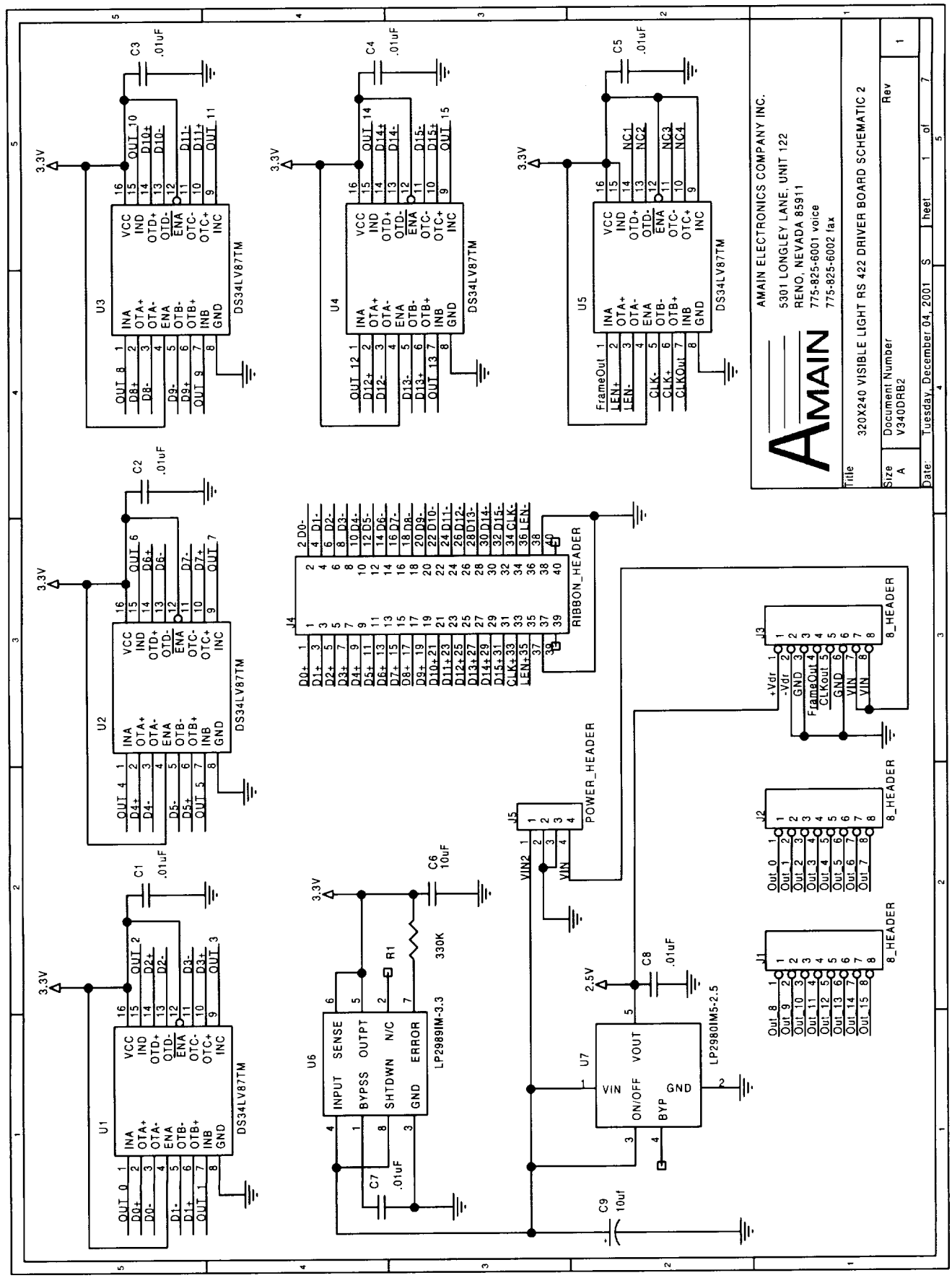
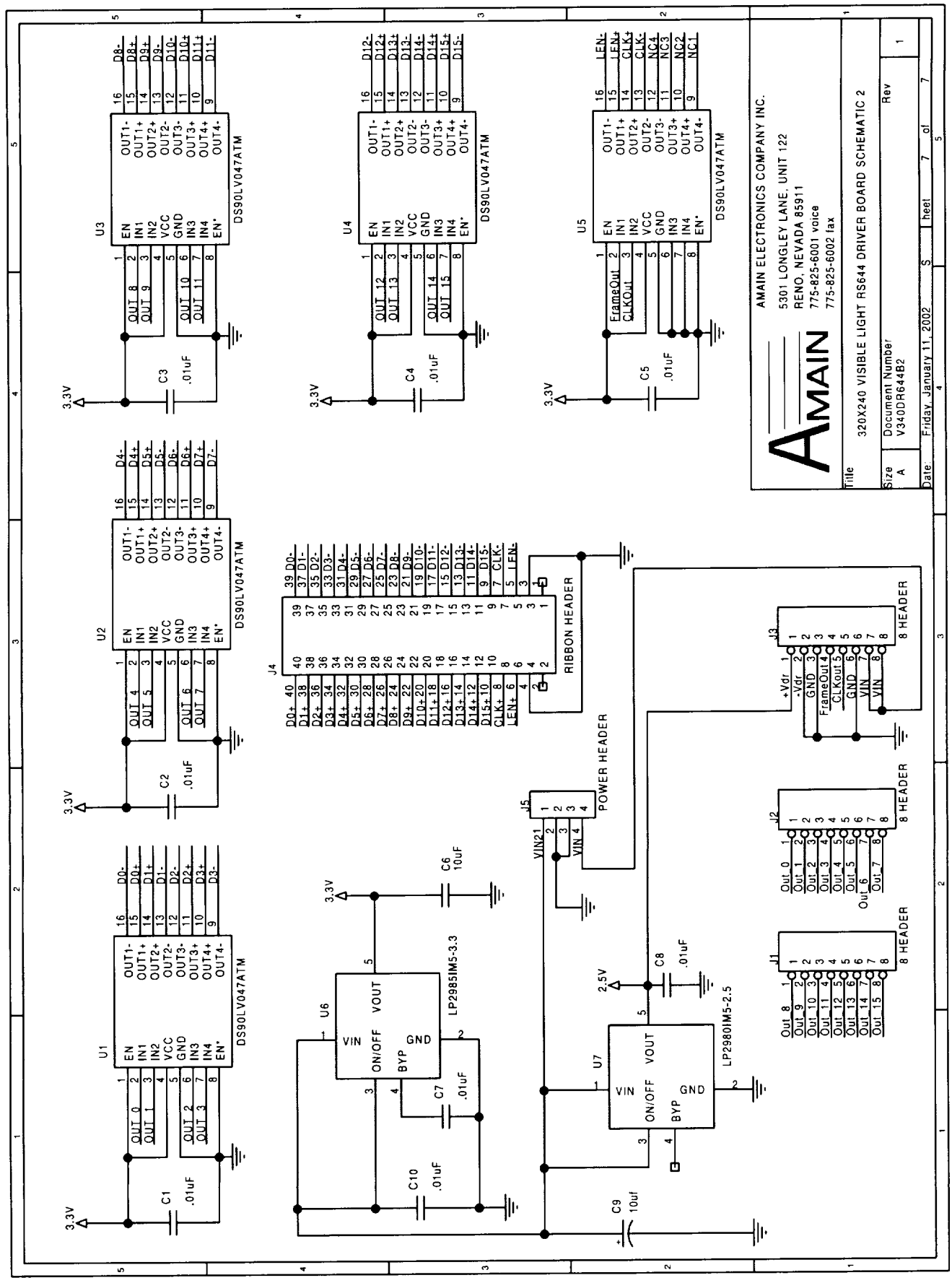


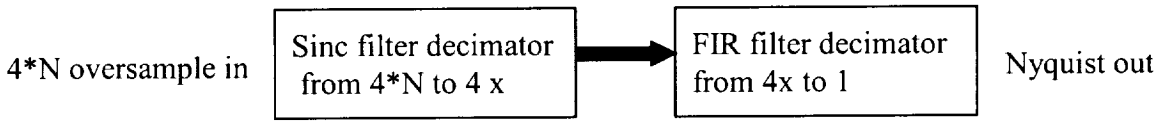
Figure 22 RS422 board layout


AMAIN ELECTRONICS COMPANY INC.
5301 LONGLEY LANE, UNIT 122
RENO, NEVADA 85911
775-825-6001 voice
775-825-6002 fax
AMAIN
Title
320X240 VISIBLE LIGHT RS 422 DRIVER BOARD SCHEMATIC 2
Size A
Document Number V340DRB2
Rev 1
Date: Tuesday, December 04, 2001
Sheet 1 of 7
U1 DS34LV87TM
U2 DS34LV87TM
U3 DS34LV87TM
U4 DS34LV87TM
U5 DS34LV87TM
U6 LP2989IM-3.3
U7 LP2980IM5-2.5
J1 8_HEADER
J2 8_HEADER
J3 8_HEADER
J4 RIBBON_HEADER
J5 POWER_HEADER
R1 330K
C1 .01uF
C2 .01uF
C3 .01uF
C4 .01uF
C5 .01uF
C6 10uF
C7 .01uF
C8 .01uF
C9 10uf
3.3V
2.5V


AMAIN ELECTRONICS COMPANY INC.
5301 LONGLEY LANE, UNIT 122
RENO, NEVADA 85911
775-825-6001 voice
775-825-6002 fax
AMAIN
Title
320X240 VISIBLE LIGHT RS644 DRIVER BOARD SCHEMATIC 2
Size A
Document Number V340DR644B2
Rev
Date Friday, January 11, 2002
Sheet 7 of 7
DS90LV047ATM
RIBBON HEADER
POWER HEADER
8 HEADER
LP2985IM5-3.3
LP2980IM5-2.5
.01uF
10uF
3.3V
2.5V

Digital Decimation Filter for Conventional Image Display

A two level filter approach was developed as the method for decimating the oversample one bit data generated by the camera and converting to Nyquist rate PCM data. This is shown in the following diagram. The first step in decimation reduces the sample rate from the staring value to four times Nyquist. A standard Sinc type filter is used in this step. The second step reduces the sample rate to Nyquist. A specially designed FIR filter is used in this step.



FIR coefficients for final 4 to 1 decimation filter were developed from previous designs. The original filter approach used 28 integer coefficient filter as the baseline approach. Filters studied as alternatives use 20, 18 and 16 integer coefficients. A 16 coefficient filter is selected as adequate.

Several first level decimation filter options were studied for a variable decimation factor. An oversample value of 4*N constraint is used where the variable decimation, N, takes place at the first level filter. The following derivations illustrate the coefficient generation process for $SINC^2$, $SINC^3$, and a modified $SINC^3$ filter.

$SINC^2$ filter option for 1 loop sigma delta
coefficients, 2N-1, sum of coefficients, N^2
example derivation for N=4

```
1 1 1 1
  1 1 1 1
    1 1 1 1
      1 1 1 1
-----------------
1 2 3 4 3 2 1,    7 coefficients (2N-1), weight 16 (N^2)
```

$SINC^3$ filter option for 1 loop and 2 loop sigma delta
coefficients, 4N-3, sum of coefficients, $2N^3-N^2$
example derivation for N=4

```
1  2  3  4  3  2  1
   1  2  3  4  3  2  1
      1  2  3  4  3  2  1
         1  2  3  4  3  2  1
            1  2  3  4  3  2  1
               1  2  3  4  3  2  1
                  1  2  3  4  3  2  1
-------------------------------------
1  3  6 10 13 15 16 15 13 10  6  3  1,   13 coefficients (4N-3), weight 112, (2N^3-N^2)
```

Modified $SINC^3$ filter used with present FIR filter
coefficients, 3N-2, sum of coefficients, N^3
example derivation for N=4

```
1 2 3 4 3 2 1
```

```
  1  2  3  4  3  2  1
     1  2  3  4  3  2  1
        1  2  3  4  3  2  1
-------------------------------
1  3  6 10 12 12 10  6  3  1,    10 coefficients (3N-2), weight 64, (N^3)
```

The following iterative routine calculates the modified sinc^3 coefficients for de decimation

```
gg = 0
For n = 0 To (de - 1) 'calculate first half and last half modified sinc3 coefficients
gg = gg + 1 + n
sinc3cof(n) = gg
Next n
For n = de To (de2 - 3) 'calculate middle modified sinc3 coefficients
gg = gg + de3 - 2 * n - 2
sinc3cof(n) = gg
Next n
```

Oversample requirements for 1 loop Delta Sigma are,

$$R(dB) = 6.02(N + 1.5D) - 3.41,$$

with dynamic range specified in dB for a N bit quantization and oversample of 2^D above Nyquist. One loop (nominal prediction, can achieve at least 2 to 3 bits better performance)

Analysis of a 320x240 FPA with a 1 loop, 1 bit delta sigma at each pixel operating at 28 times over sample.

Predicted dynamic range, 7.67 bits, expected performance, 10.6 bits.

Decimation filter through put requirement:

Modified sinc^3 decimation requirement, 28 / 4 = 7

coefficient count (3N-2), for N=7, 19 coefficients

Additions per pixel per frame 4*(3N-2) = 4*19 = 76

Total modified sinc^3 additions per frame, 4*(3N-2)*320*240 = 5,836,800

16 coefficient FIR pipeline addition (latent multiply) requirements based on integer coefficients

decimal	binary
-13	- 000001101
-34	- 000100010
-48	- 000110000
-24	- 000011000
65	001000001
215	011010111
378	101111010
485	111100101

Total number of ones used for gated add or subtract for all 16 coefficients is 58

FIR gated add/subtracts per frame 58*320*240 = 4,454,400

Total of all filter adds per frame 4,454,400 + 5,836,800 = 10,291,200

The filter algorithm was implemented in hardware with the Alacron FastFrame frame grabber board. Figure 23 is the functional diagram of the board showing its relationship to the

host processor PCI buss. There is a provision for two Trimedia processing units on the board. For this application only one processor was needed as shown in the diagram. Digital data for up to 32 pins is allowed, 16 pins were used to connect the camera. The board is supported with Windows 2000 (Rev2) based software that allows captured images to be displayed in real time.

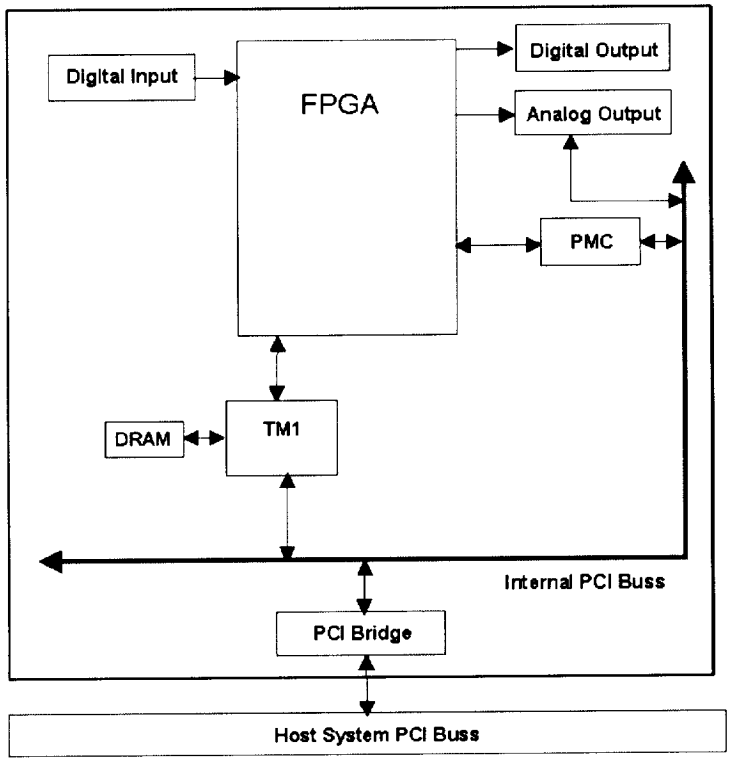


Figure 23 Alacron FastFrame Frame Grabber PCI board

DEVELOPMENT RESULTS

Second Iteration Device Fabrication

The development required three device process iteration to get to the present state. In the first iteration no demonstratable parts were achieved. A problem with internal voltage drops prevented outputs from being reliably read. In the second iteration two sets of masks were generated. The first set was discarded after a circuit error was uncovered during simulation checks. Wafers received from this second iteration were tested and it was found that only half of the array was working. Characterization at the wafer level tracked the problem to a metal mask error. The error is shown in figure 24 where there is a break in clock line CAB. The break is at the second half of the row scan logic. This prevents the second half of the array scan. The array is scanned in two parts. First the odd rows are scanned and read and then second the even rows are scanned and read. With the metal break only the odd rows could be scanned and readout in a normal operation. In characterizing the devices, it was found that the working pixels were limited to an operation range well below full dynamic range. Analysis indicated this was due to interference from the non-working pixels. Without a subtraction operation to remove charge, the non working pixels overflow into the adjacent working pixel through the read well.

The design of the read column uses a floating sense node to detect a response from the selected pixel. All of the pixels, even and odd, on the column are capacitively coupled to the node. In normal operation, only the selected pixel will dump charge onto the node and be detected. With the broken CAB line, the non-working pixels accumulated photo charge but have no way of being cleared of charge. This excess charge can leak into the read capacitor affecting node and being sensed as a false signal. If the image intensity is low, this leakage will be low and the sense amp can be biased to ignore it and see only a valid signal. For the photo gate it was found that the average image intensity could not exceed 15% of full scale. For the photo diode it was found to be about 10% of full scale. With these known limitations from the metal error, a test camera was built to check image quality from the working pixels.

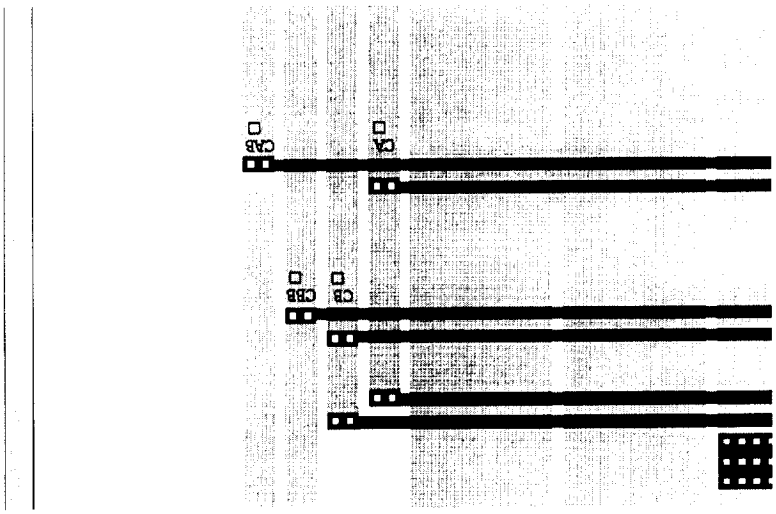


Figure 24 Composite layout showing CAB metal break

Selected die were packaged and mounted on a PC board with support electronics including power conditioning, timing and interface drivers. The assembly was housed in a plastic box with optics and external power supplies. Power included a small 9 volt battery for the camera electronics and a rectified transformer isolated 110 to 9 volt reduced source for the output drivers. The output drivers were connected to a frame grabber board with a ribbon cable. A C-mount type optics assembly was used to mount the optics. An old 35 millimeter camera made by AKA Rette was used as the source of the optics. These optics provides a selectable f number from 3.5 to 16 and a variable focal length that allowed focusing from 1 meter to infinity. Limitations of the frame grabber board allowed a maximum of only 2 megabytes of video data to be read continuously. This limited the oversample frame count to 432 frames of data for one sequence. The decimation factor was set at 28 to 1 which produced 10 usable PCM frames. To account for the missing pixels in creating an image, the analysis software was rewritten to insert the missing pixels. Each inserted pixel was calculated based on the average of the two pixels above and below the missing pixel. The range accuracy limit of the recordable data was set from 8 bits to12 bits. This data was mapped into an 8 bit BMP file format with a variable setting of a universal offset window and gain setting.

Figure 25 is a flat field image taken with the photo gate. This is an 11 bit dynamic range mapped onto the 8 bit BMP format. The image was taken through the circular lense mount with the lens removed. Xerox paper covered the hole to reduce the light intensity and provide some

nominal uniformity in the field of view. The recorded amplitude was approximately 10% of full dynamic range. Except for the smudge on the right edge, the uniformity was measured at an accuracy of better than 0.1%. The smudge is residual photo resist from the dicing operation. In normal cleaning of the wafer this was not apparent visually. There is also a measurable smooth variation, not visible, due to the COS^4 off axis photon flux variation.

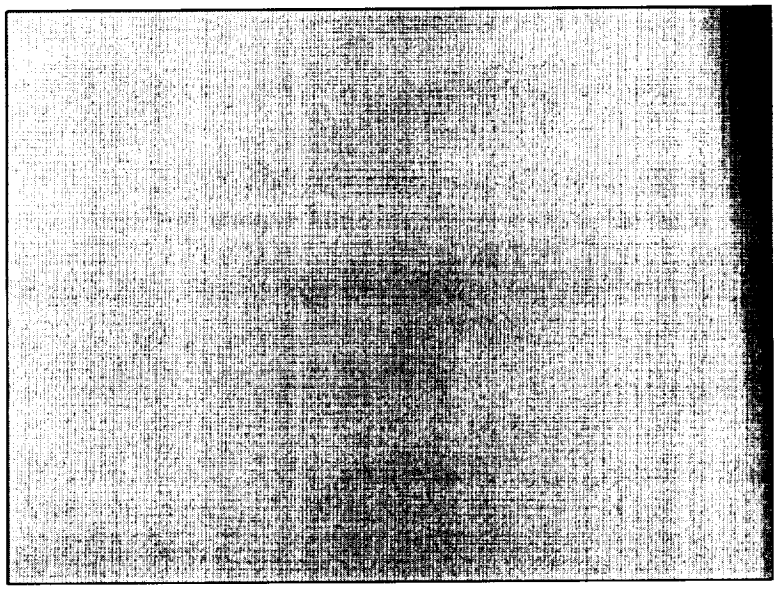


Figure 25 Flat field image with photo diode array

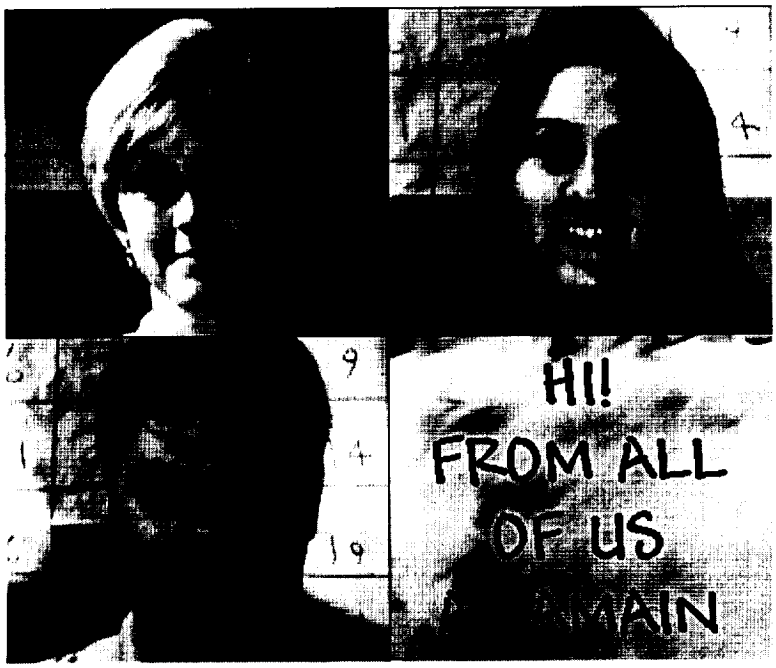


Figure 26 Images taken with photo gate camera

Images of people were taken under various lighting condition to validate the image quality. These are shown in figure 26. As with the flat field image, these images were in the range of approximately 10% of full scale. The issue of dynamic range limitation due to the non-

functional pixel induced noise was the limiting factor. These pictures were taken with the photo gate where the sense amplifier could be adjusted to sense small amplitude inputs. Similar measurements were made with the photo diode, however, it was much more sensitive and the sense amplifiers had less margin for adjustment. This prevented adequate analysis and noise measurements to be made.

Final Iteration Camera functional tests

A third and final iteration of the design was submitted to fabrication. The updates include fixing the CAB error and increasing the buss sizes on the chip. Also, additional power and ground pads were added to reduce voltage variations across the chip and improve noise performance. This design was fully functional and cameras were built with both the photo gate and the photo diode designs. With fully functional cameras, adequate noise analysis could be performed. It was found that the column compare sense amplifiers had high current switching spikes. There are 640 column sense amplifiers. Only the amplifiers detecting a pixel response will switch. Statistically, more amplifiers will switch as the signal intensity increased, thus causing higher reference noise from the combined current spikes. A new column compare sense amplifier was developed that will substantially reduce the switching current. This new design was not implemented in the final iteration.

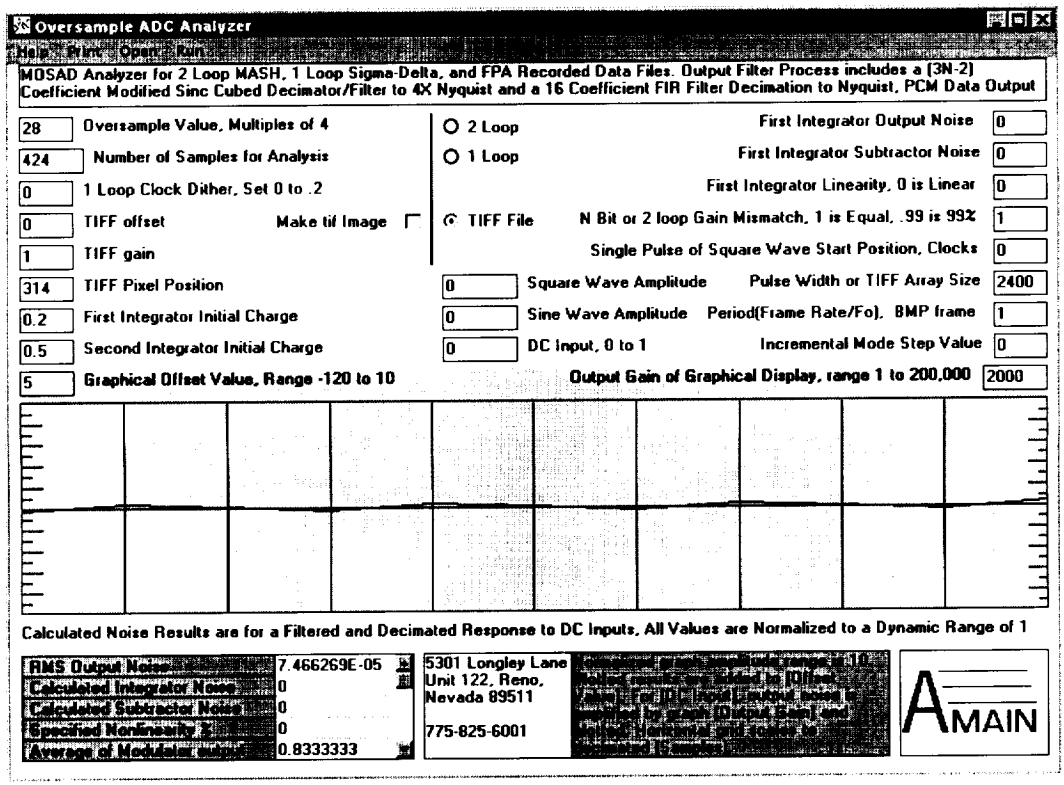


Figure 27 Background circuit noise performance exceeds 13 bits

In analyzing the noise performance of the cameras, it was found that the gate cameras had substantially less noise than the diode cameras. Figure 27 is the noise plot of one pixel from a gate camera. The measured noise over eleven frames is $7.5X10^{-5}$ normalized to a full scale of

one. This is an equivalent noise performance of 13.7 bits. Since this is a delta sigma operating at 28 oversample, quantization error will vary and in general be much higher as shown in figure 3. However, at this specific amplitude, (1- 0.83333), 16.66% of full scale, quantization error was small enough to observe accumulative background circuit noise and photon shot noise. There appears to be no impact from the column compare sense amplifier switching.

Figure 28 is a noise plot of the photo diode camera at approximately the same signal strength as that measured in the photo gate camera. Here the amplitude is, (1 - 0.8399), 16.11% of full scale. Noise is $8.1X10^{-3}$ over 100 time higher than the photo gate. There would be some variation from the delta sigma because of the slight difference in amplitude but not this magnitude. In looking at the plot there are two significant peaks that raise the average noise. This is typical for delta sigma if a bit is picked up or dropped in the digital data sequence.

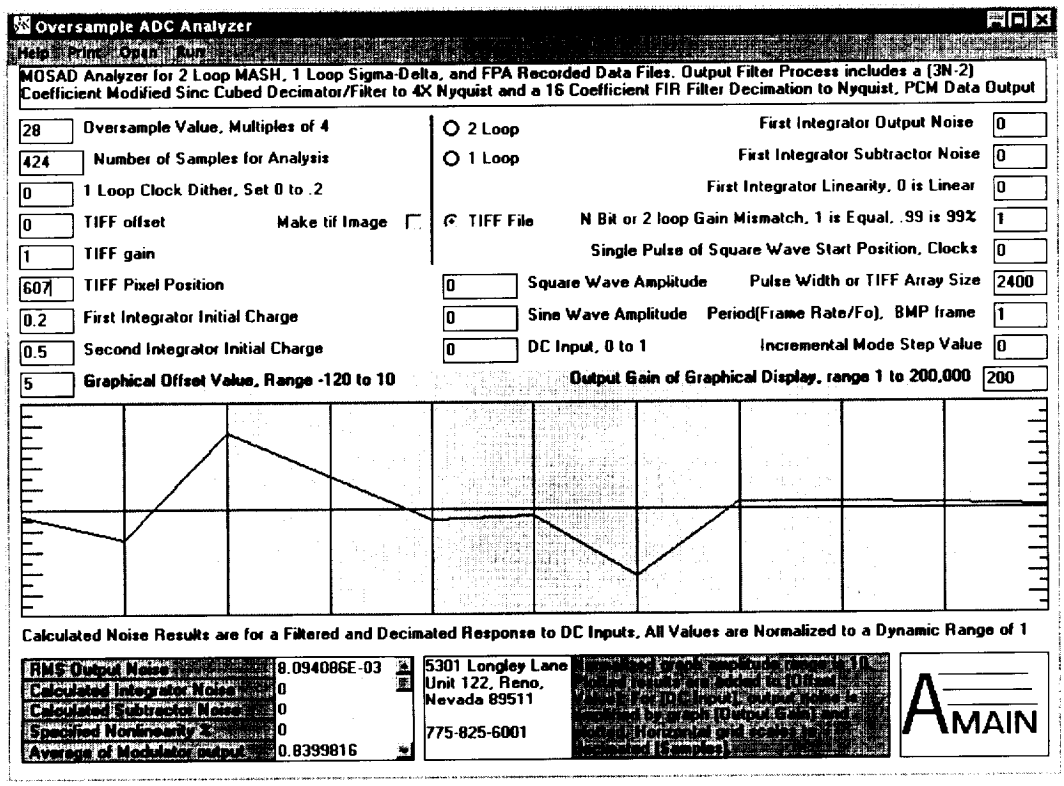


Figure 28 Noise impact of current spikes on the photo diode

To best illustrate the performance of the camera, a series of pictures were taken with both a photo gate camera and a photo diode camera. The cameras were operated at a clock rate of 2 MHz and decimated 28 to 1. This produces an effective frame rate of 14.4 fps and a signal bandwidth of 7.2 Hz. The data was decimated using the software filter developed for noise analysis. This set up uses the Itex frame grabber board to grab 2 megabytes of focal plane data and transfer the block to memory as a TIFF file. The TIFF raw data file is then converted to a sequence of BMP file frames. There are 11 frames generated, one of which is selected prior to run time for storage and display. This method was selected for picture generation over the Alacron realtime frame grabber and decimator because of the need to do noise analysis during the characterization. Though only the resultant pictures are illustrated in the report, noise analysis as typified by the above plots was run on all of the tests. This analysis was necessary to ultimately

pin point and resolve the issue of the column compare sense amplifier current spike problem. The following figures are picture with legends describing the camera type and scene.

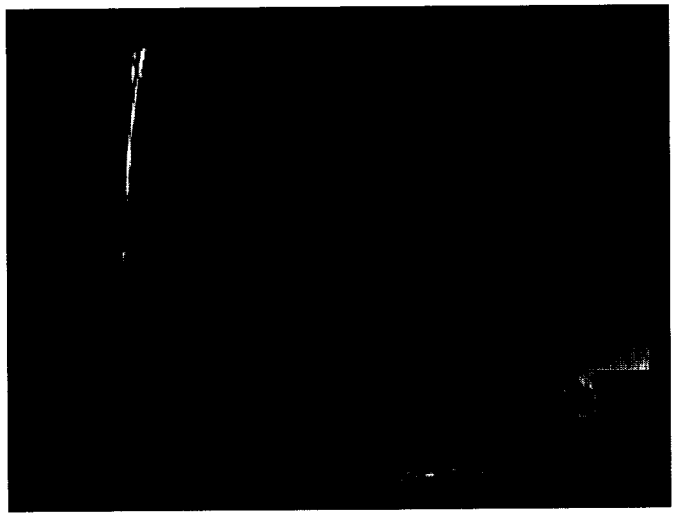


Figure 29 Photo gate looking outside

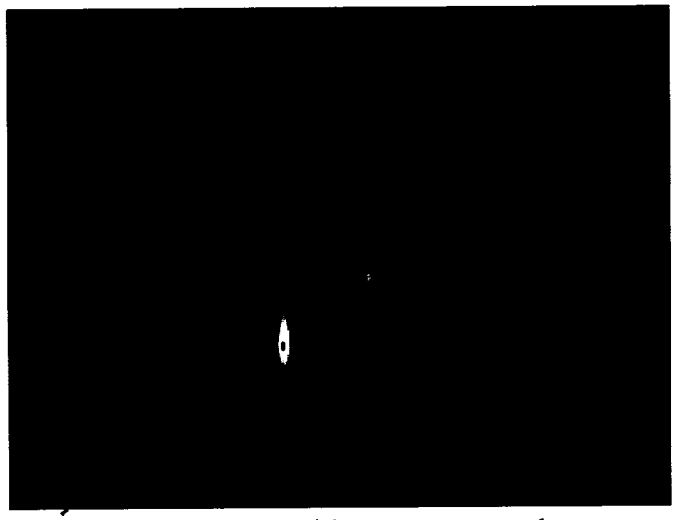


Figure 30 Photo gate with super saturated area

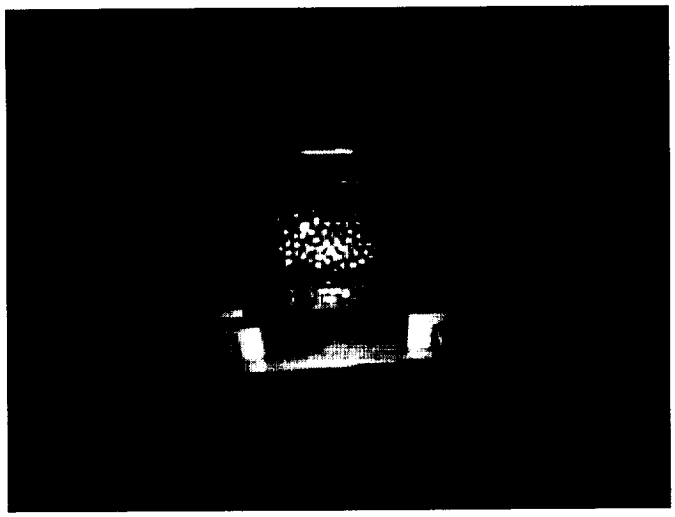


Figure 31 Photo gate 500 Watt Halogen lamp

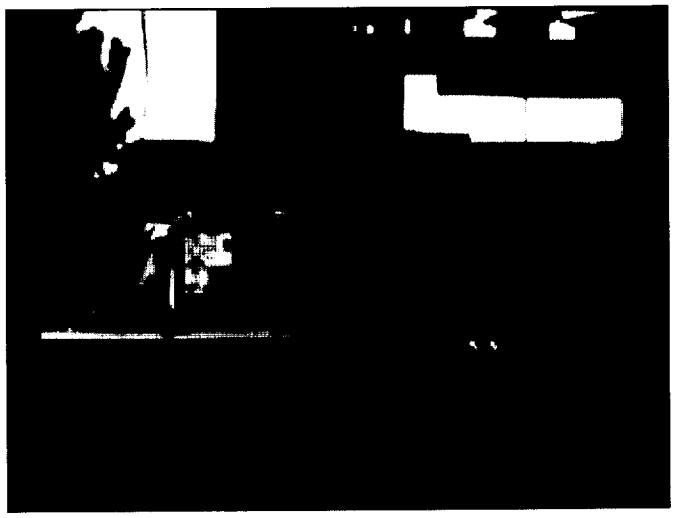


Figure 32 Photo diode with partial outside view

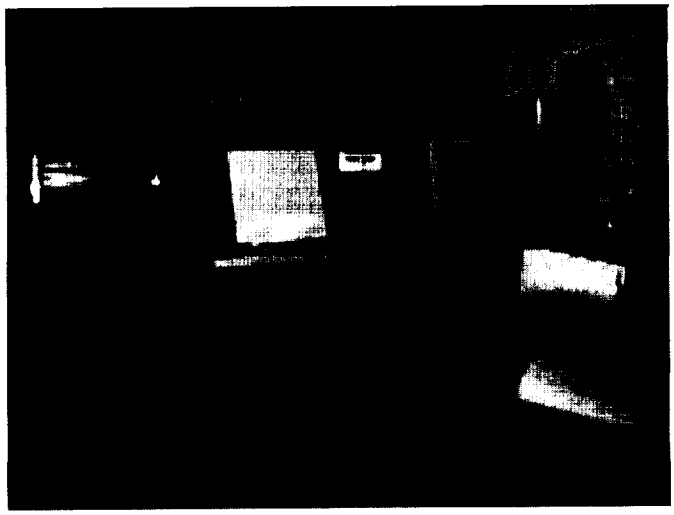


Figure 33 Photo diode lab view

Figure 34 Photo diode lunch room and person view

These pictures were taken with different cameras during the characterization study. The camera bias voltages, Vopamp and Vbarrier, were varied to provide differing noise rejection and gain. Surprising, though the photo diode was known to have more noise susceptibility, picture quality was similar to the photo gate. These pictures were all resolved to 8 bits dynamic range. There are visible effects of noise impact of the column compare sense amplifiers in both the gate camera and the diode camera. By adjusting Vopamp, noise susceptibility variations from sense amplifier to sense amplifier could be seen.

Sense Amplifier Design Resolution of the Current Spike

Designing the column compare sense amplifier has been the most significant issue in the development of the camera. The direct readout, DRO, approach used at the pixel is a non-amplifier buffered approach. It reduces signal amplitude with array size. The original sense amplifiers have been used successfully with buffered MOSAD with no effect. The buffered design have noise margins on the order of 1 volt. These new non-buffered MOSAD designs, DRO, used in this visible light camera were designed with a noise margin of 5 millivolts. If the floating column is erroneously driven negative by this 5 millivolt noise margin the pixel would have been considered to have responded. Evidence from measurements indicated that as more columns validly responded during a row read, non responding columns would be induced into responding. This causes a false subtraction response that destroys the fidelity of the Delta Sigma sequence and erroneously dumps charge.

There is a combination of design issues that had to be resolved to fix this problem that included layout, filtering and transient reduction. The DRO uses a floating column to capacitively couple the pixel into the sense amplifier. The column is referenced to +5 volt by the sense amplifier. Any sufficiently negative transition of the floating column is sense as a response. In the final iteration layout, the precharge P transistor for the column shares a common N well with the sense amplifier switching logic. If there is sufficient dip in the sense amplifier +5 volts during switching, it could couple through the well to the column, driving it more negative. This could be sensed as a signal. Internal power busses have about one ohm of resistance. A current transient of 800 microamps per amplifier could cause up to 0.5 volt power dip (640 sense amplifiers). To isolate this transient, a revision to the next generation design now separates the

column precharge well from the sense amplifier well.

The magnitude and timing of the transient current spike is the most critical aspect of the sense amplifier design. Figure 35 is a simulation of the switching response for one amplifier of the final iteration design that was built. The +5 volt current transient is shown in the bottom plot. At a point in time ahead of where the column is sensed, the current spike is shown to exceed 1.6 milliamps. Collectively this could reach 1 amp for the array. Timing is such that the amplifier can respond to the noise before the sense. The only other significant current spike occurs at precharge. This is only 150 microamps and does not occur while sensing. In combination with the connected well issue and the finite power buss resistance the 1.6 milliamp current spike will cause errors as seen with the photo diode camera.

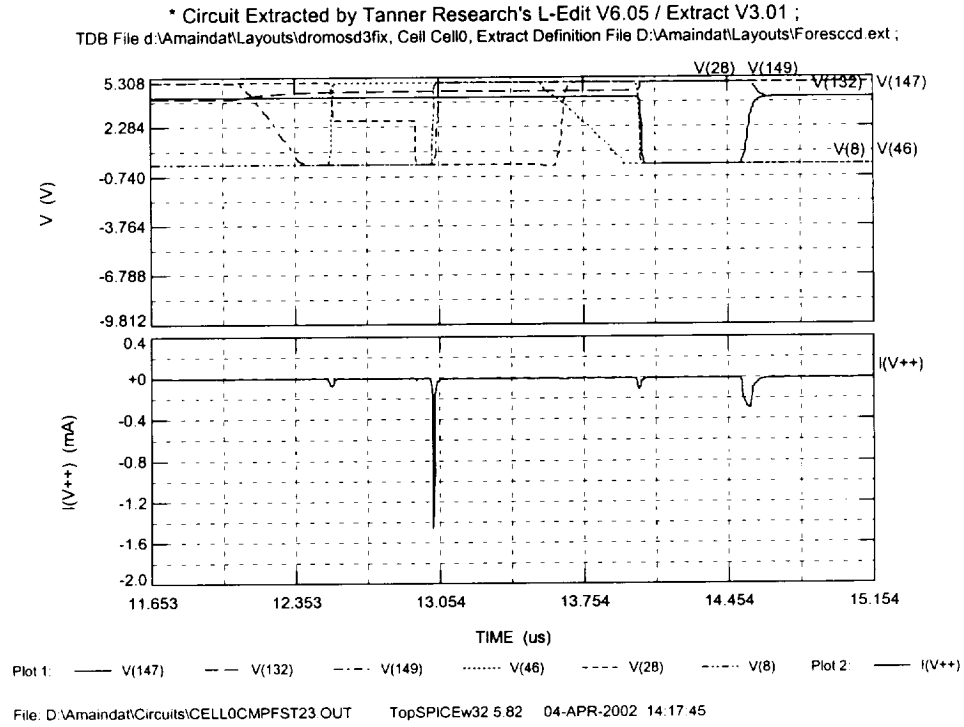


Figure 35 simulation of final iteration sense amplifier showing high current transient during the sense time

To correct this current transient problem, a new sample and hold sense amplifier was designed. The schematic of figure 7 shows this new design. The difference from the earlier design is both in timing and in current switching magnitude. In the new design, the sample and hold samples the output of the three stage amplifier into a capacitor. This holds the sense value at its current state. Any voltage errors on the floating column induced by the switching transient will not have time to ripple through the three stage amplifier before sampling is completed. The now sampled correct value is then used to determine the pixel state. Figure 36 is a simulation of the new design. In this simulation it can be seen that the current transient has been reduced substantially to less than 250 microamps. The peek current if all sense amplifiers were switching will be less than 160 milliamps. Worst case power rail fluctuation will now be under 160 millivolts and will occur in a period of time that will not harm the pixel readout.

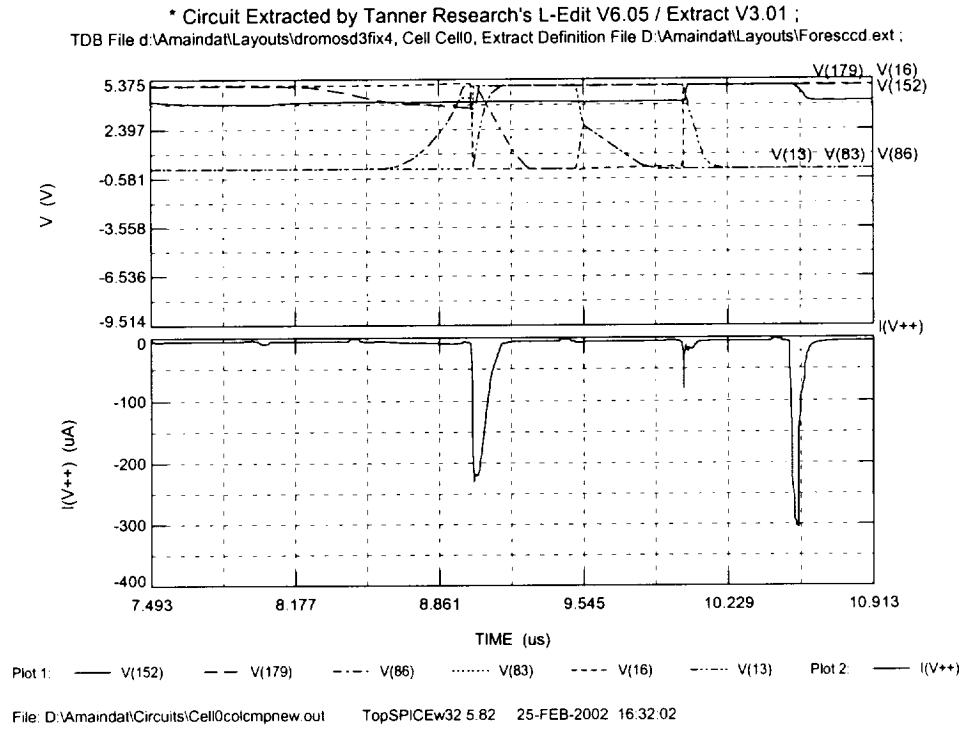


Figure 36 New sense amplifier design developed after final iteration fab

SUMMARY AND CONCLUSION

The MOSAD architecture developed in this program for monolithic visible light imaging represents a radical departure from present methods. The method of sensing and reading data from the pixel is totally different from present CCD, CID and CMOS imagers. This approach puts the equivalent of a delta sigma A/D converter at each pixel. The oversampling process used in Delta Sigma A/D conversion has the potential to provide better noise performance, improved linearity and high well capacity for high intensity imaging. It also offers the potential for radiation hard designs.

This development program culminated in the design, fabrication and demonstration of two camera approached based on the MOSAD technology. These included a photo diode sensor and a photo gate sensor. The detector area used charge well switching to implement the delta sigma A/D at the pixel. There were no pixel buffer amplifiers required, allowing a fill factor of 73% to be achieved, front side illuminated, in a pixel size where the maximum process limited fill factor was 87%. The two cameras were built with an array size of 320X240 with a pixel pitch of 16 micron. This fits the 1/3 inch array size used in CCTV cameras, allowing the use of low cost commercial optics. The process used to fabricate the parts is Supertex 1.2μ CCD/CMOS technology. The sensor array used surface N channel photo detectors in a P CCD well. Though the surface channel devices used are inherently noisier than buried channel devices, a noise floor for the MOSAD photo gate design was measured at 13.7 bits. Power consumption for the cameras with an oversample rate of 28 above Nyquist and a 15 frame per second sample rate was measured at 10 milliwatts. Uniformity was measured at below the noise floor of the one loop Delta Sigma quantization error. At approximately 10% of full scale this was within 11 bits. Though working cameras were built that exhibited outstanding performance and imagery, a

design flaw was uncovered in the internal sense amplifiers. A new design was developed but not implemented at program conclusion. This new design will improve noise performance, yield and power consumption over that already demonstrated.

Based on known accomplishments reported in the industry, the MOSAD approach is superior to CMOS visible cameras in overall image quality and power consumption. The CMOS benefits of random access and windowing can be available through MOSAD. MOSAD oversampling technique eliminated the temporal skew of progressive scanning without loss of sensitivity. CMOS, to eliminated temporal skew must snap shot, decreasing dwell time and sensitivity. Delta Sigma oversampling also allows large well capacity without noise penalty providing better noise performance for viewing bright objects. Oversampling with conventional readout for expanded well capacity increases noise with no net gain. MOSAD competes successfully with CCD in image quality but is much lower cost and lower power. There is no transfer efficiency loss in a radiation environment. Though a small 320X240, 16μ pixel array was demonstrated with 1.2μ processing, the approach introduces no fundamental limit to array size. A 16 million pixel array with 5μ pixel pitch is readily achievable with modern submicron processing. Delta Sigma has been shown by the industry to be capable of achieving noise floors below the limits of the circuits used. This is also inherently true for the MOSAD method of Delta Sigma A/D. This development program has shown that the MOSAD approach offers NASA the potential for a new direction in imagery providing better and more robust sensors.

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13. ABSTRACT *(Maximum 200 words)*

Two full custom camera systems using the MOSAD technology for visible light sensing were built and demontrated. They include a photo gate sensor and a photo diode sensor. The system includes the camera assembly, driver interface assembly, a frame grabber board with integrated decimator and Windows 2000 compatible software for real time image display. An array size of 320X240 with 16 micron pixel pitch was developed for compatibility with 0.3 inch CCTV optics. With 1.2 micron technology, a 73% fill factor was achiecved. Noise measurements indicated 9 to 11 bits operating with 13.7 bits best case. Power measured under 10 milliwatts at 400 samples per second. Nonuniformity variation was below noise floor. Pictures were taken with different cameras during the characterization study to demonstrate the operable range. The successful conclusion of this program demonstrates the utility of the MOSAD for NASA missions, providing superior performance over CMOS and lower cost and power consumption over CCD. The MOSAD approach also provides a path to radiation hardening for space based applications.

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