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Annual Report for NASA Grant NAG5-9493

Development of Submillimeter SIS Mixers and Broadband HEMT Amplifiers

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1 Introduction

This is an annual progress report for NASA grant NAG5–9493, entitled "Development of Submillimeter SIS Mixers and Broadband HEMT Amplifiers". The goal of this project is to develop and demonstrate a new generation of superconducting tunnel junction (SIS) receivers with extremely wide instantaneous (intermediate–frequency, or IF) bandwidths, of order 12 GHz. Such mixers would allow rapid submillimeter wavelength spectral line surveys to be carried out with SOFIA, and could potentially be used for future submillimeter space missions such as SAFIR.

There are two major components which are being developed: (1) SIS mixers with broad (12 GHz) IF bandwidths; and (2) low–noise, broadband microwave (6–18 GHz) amplifiers, which amplify the IF output from the SIS mixer. The work on these components is discussed in the two sections below. In addition, we have included as appendices a manuscript and a poster, which were produced for the NASA workshop on long–wavelength detectors, held in March 2002 in Monterey, CA.

Our work takes advantage of the vastly improved computer–aided design tools that are now available. Three–dimensional electromagnetic simulations are carried out using the Ansoft HFSS package, which allows the waveguide block and probe structure to be accurately simulated and optimized. Although these simulations are very intensive computationally, fast processors with GHz clock speeds, along with > 1 GB memory, allow such simulations to now be carried out in a few hours. This capability has radically improved the quality of mixer designs. We also use two–dimensional electromagnetic simulators to characterize planar circuit elements, such as the superconducting transmission lines used on the SIS chip. This allows us to include the effects of various geometrical discontinuities into the design.

In addition, we are using our recently developed "Supermix" software package[1] to simulate in full detail the behavior of the SIS mixer. The quantum–mechanical theory of SIS mixers was developed in the late 1970's by J. R. Tucker, and is now well verified.

[1]Supermix: `http://www.submm.caltech.edu/supermix/default.html`

Supermix implements the full Tucker theory, including multiple junctions, higher harmonics, a full nonlinear solution to the local oscillator waveform, and quantum noise. In addition, Supermix includes a complete linear circuit simulator, as well as an optimization capability. The end result is that it is now possible to perform a complete simulation and optimization of an SIS receiver. In the past, SIS receiver design was done on the basis of simplified design rules, which yielded mixers which were good but not completely optimized.

Another important aspect is that we now have much better information on the properties of the superconducting and dielectric films which are used on the SIS chip. We have performed careful measurements at 100 GHz (which were reported at the Monterey workshop) of the properties of superconducting microstrip lines. For the first time, we have obtained accurate values for all of the important parameters: phase velocity, attenuation, and characteristic impedance. From these, we can infer quantities such as the dielectric constant of the SiO insulating film and the magnetic penetration depth of the superconducting films. We have found important differences between these measurements and the values we have previously assumed for our designs. This improved knowledge of the relevant materials parameters should again lead to more highly optimized SIS mixer designs.

The end result is that we have invested much more care, time, and effort into this design, using much better design tools and materials parameters, than for any other previous SIS mixer design. We certainly hope that this will be evident from the experimental results!

2 Personnel

This project involves personnel at Caltech and at JPL. The personnel at Caltech include: the PI; a research staff member, Frank Rice (33% time); a physics Ph.D. student, Chip Sumner; a visiting graduate student (from U. Michigan, EE dept.), Robert Hu; and a staff engineer, D. Miller. Rice and Sumner are working on the SIS mixer, while Hu works on the IF amplifier. Miller is an electrical engineer who has developed the room–temperature IF amplifiers for the test receiver. At JPL, the project includes: Dr. S. Weinreb, who oversees the development of the IF amplifier; and Dr. H. G. LeDuc, whose group carries out the SIS device fabrication.

3 SIS Mixer Development

We have chosen to develop a new SIS waveguide mixer architecture, and are aiming for an initial demonstration in the 200–300 GHz band. While this is a lower frequency band than will be eventually needed for SOFIA, it allows relatively straightforward and accurate manufacturing of the waveguide components, simplified mixer assembly, and easier fabrication of the SIS devices themselves. Furthermore, receiver testing in this band is straightforward and can be done rapidly, since broadband electronically tunable local oscillators are readily available.

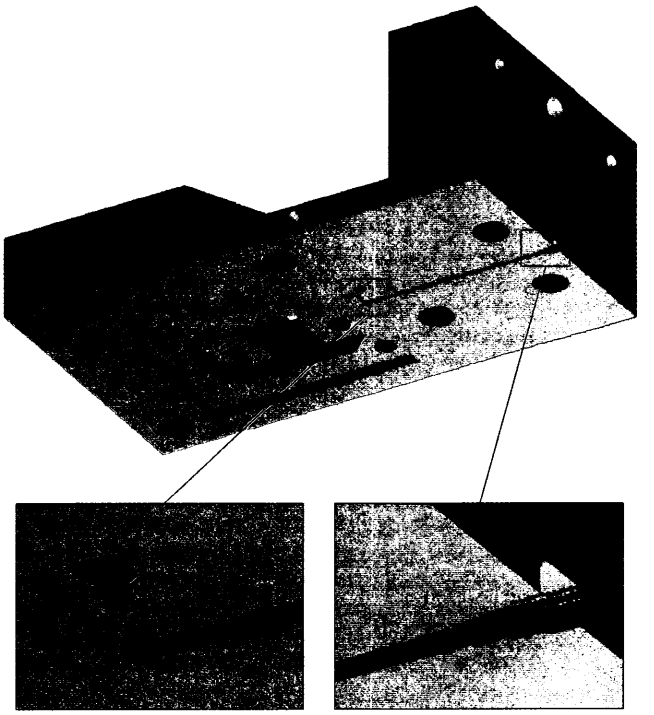

Figure 1: A 3D rendering of the top half of the waveguide block for the SIS mixer. This is a split–block design. The piece shown is viewed from the bottom, which is the plane of the split. Half of the waveguide is machined into this piece, and appears as the feature between the two rectangles. The other half of the waveguide is machined into the mating bottom piece (not shown). An expanded view of the waveguide input is shown on the right. This input will be fed by a corrugated horn. The steps are part of a transformer from the circular waveguide of the horn to the single–mode rectangular waveguide in the mixer block. On the left is an expanded view of the channel in which the SIS chip will be placed. The IF output from the chip will pass through a coaxial transmission line located very near the SIS chip, in the circular hole in the upper left of the expanded view.

3.1 SIS Mixer Chip Design

A major accomplishment this year is the completion of the detailed design of the SIS mixer chip. Figures showing the chip design are shown in Appendices A and B. The chip design involved several steps. First, detailed 3–D electromagnetic simulations of the waveguide structure and the probe were carried out. The probe couples the radiation from the waveguide onto the SIS chip, and is designed to have excellent performance over a 1.5:1 fractional bandwidth. In particular, the impedance of the probe is very constant over this band. Second, the SIS chip was designed using Supermix, paying close attention to the input reflection, conversion gain, noise temperature, and especially IF bandwidth. The chip includes a novel RF choke/IF matching circuit combination, which is essential to achieve the desired bandwidth. The SIS chip design is now complete, and has been submitted for fabrication at JPL. Details of the expected performance are given in the appendices.

3.2 SIS Mixer Chip Fabrication

The fabrication is now underway at JPL, and is being carried out by the low–temperature superconducting device group led by Dr. H. G. LeDuc. The fabrication will incorporate several innovative aspects. First, the chip uses a 25 μm silicon substrate, which is too thin to survive the fabrication process. Special silicon wafers have been procured, which consist of a thin 25 μm silicon layer bonded to a much thicker wafer, with an oxide layer in between. This oxide layer acts as an etch stop, so that the thick silicon can be etched away when the device fabrication is complete, yielding SIS chips on 25 μm silicon. This technique can readily be adapted to produce even thinner substrates, as would be needed at higher frequencies. In addition, it should be possible to use the etching step to define the lateral dimensions of the devices. This would eliminate the final mechanical "dicing" step, in which the wafer is partitioned into separate devices using a diamond saw. This etching method should give more precise control over the chip dimensions, and eliminate the breakage that occurs during dicing, which becomes severe as the substrate thickness decreases.

A second innovative aspect is the incorporation of gold "beam leads". These are very thin tabs which extend beyond the edge of the silicon substrate. Their purpose is to make good electrical contact to the mixer block; they are sandwiched in between the two halves of the waveguide block when it is assembled.

Although the SIS chips could also be produced with standard techniques, such as lapping to achieve the desired thickness, the advantage of the new fabrication techniques is that they can readily be scaled to much higher frequencies. Our end goal is to be able to produce and assemble high–frequency waveguide SIS mixers much more easily and reliably than is now possible.

3.3 Waveguide Block Design

Another key step forward this year was the detailed mechanical design of the waveguide mixer block. Figure 1 shows a three–dimensional rendering of the block. This is a split–block design, which can be fabricated using machining rather than electroforming. The design is very nearly complete, and will be submitted shortly to Custom Microwave Inc. for fabrication. Particular attention was paid to the design of the IF output. The coaxial line leading to the output connector ends very near the SIS chip, so that it will be possible to make the IF connection to the chip using a very short wire bond. This is necessary to obtain a broad IF bandwidth.

3.4 100 GHz Microstrip Transmission Line Measurements

These measurements are being carried out in connection with a different project, involving the development of antenna–coupled direct detectors for CMB measurements. This is a collaboration with A. Lange at Caltech, and J. Bock at JPL. A new method has been developed to carry out measurements at millimeter wavelengths of the properties of thin–film superconducting microstrip lines. Although such lines are widely used in SIS mixers and other devices, their properties have not been studied in detail

at mm wavelengths. Our measurements yield precise values for the phase velocity, attenuation, and the characteristic impedance. As mentioned in the Introduction, these measurements feed directly into the SIS chip design, and should result in better SIS mixer performance. A preliminary account of these measurements, presented last summer at the LTD–9 conference, is given in Appendix C. A detailed journal paper describing the latest results is in preparation.

4 6–18 GHz IF Amplifier Development

The main achievement this year is the design, fabrication, and testing of a second prototype of the 6–18 GHz IF amplifier. This is a "monolithic microwave integrated circuit", or MMIC. The active devices are InP–based High Electron Mobility Transistors, or HEMTs, which offer the lowest noise and low power dissipation at microwave frequencies. The chip design and layout are done at Caltech and JPL, and the devices are produced at TRW. Dr. S. Weinreb, who is an expert on MMIC devices at JPL, oversees this effort.

The first prototype, developed and tested during the first year of this grant, used resistive feedback to obtain flat gain and good input match. However, it was found that the noise of the amplifier was higher than expected, around 20 K, and it was thought that the problem was related to the feedback resistor. The second prototype eliminated the feedback resistor, and uses source inductance feedback instead. The initial measurements on the new prototype, described in more detail in the appendices, are very promising. In particular, the noise appears to be below 10 K, and is flat over the frequency range that has been measured. In order to obtain measurements over the entire frequency range, a new amplifier package is being developed. (The existing package exhibits undesirable resonances within the operating band of the amplifier.)

5 Goals for 2002–2003

Our goals for the third year of this effort are as follows:

- Complete the fabrication of the SIS mixer chips
- Fabricate the waveguide mixer blocks
- Assemble and test the mixer, initially using a 4–8 GHz IF amplifier
- Complete the characterization of the second–generation 6–18 GHz IF amplifier MMIC
- Produce several 6–18 GHz IF amplifiers
- Integrate and test the 6–18 GHz IF amplifier with the waveguide mixer
- Carefully compare the test results with simulations, and identify any areas for improvement