Nano-transistor modeling: Two dimensional Green's function method

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Two quantum mechanical effects that impact the operation of nanoscale transistors are inversion layer energy quantization and ballistic transport. While the qualitative effects of these features are reasonably understood, a comprehensive study of device physics in two dimensions is lacking (SIA Roadmap [1]). Our work addresses this shortcoming and provides: (a) a framework to quantitatively explore device physics issues such as the source-drain and gate leakage currents, DIBL, and threshold voltage shift due to quantization, and b) a means of benchmarking quantum corrections to semiclassical models (such as density-gradient and quantum-corrected MEDICI).

We have developed physical approximations and computer code capable of realistically simulating 2-D nanoscale transistors, using the non-equilibrium Green's function (NEGF) method. This is the most accurate full quantum model yet applied to 2-D device simulation. Open boundary conditions and oxide tunneling are treated on an equal footing. Acoustic phonon scattering is included, causing transport to deviate from ballistic in a realistic manner. Electrons in the ellipsoids of the conduction band are treated within the anisotropic effective mass approximation. Self consistent solution of Poisson-NEGF equations is numerically intensive because of the number of spatial and energy coordinates involved. This makes the use of parallel/distributed computing imperative. For the self consistent calculations presented here, parallelization is performed by distributing the solution of NEGF equations to various processors, energy wise. The calculations were performed on a SGI Origin 2000 at the NAS computing facility located at the NASA Ames Research Center.

We present simulation results for the "benchmark" MIT 25nm and 90nm MOSFETs [2]. We compare our results (labeled "quantum") to those from the PROPHET (classical) drift-diffusion simulator (labeled "DD") and the quantum-corrected MEDICI results (labeled "Medici") available in [1]. In the 25nm MOSFET, the channel length is less than ten times the electron wavelength, and the electron scattering time is comparable to its transit time. Our main results are: (i) Simulated subthreshold and drain current characteristics are shown in Fig. 1 (a,b) where the potential profiles are calculated self-consistently by the corresponding simulation methods. The current predicted by our quantum simulation has smaller subthreshold slope of the Vg dependence which results in higher threshold voltage. (ii) Quantum mechanically calculated electron density is much smaller than the background doping density in the poly silicon gate region near oxide interface. This creates an additional effective gate voltage (Fig. 2). Different ways to include this effect approximately will be discussed. (iii) We have developed a method to calculate the gate-oxide leakage current (tunnel current) within the context of the NEGF method. Fig. 3 compares the drain and gate-oxide leakage current for the MIT 25 nm MOSFET, which has 25 nm channel length and 50 nm gate length , and for the same device with a 25 nm gate length, for gate-oxide thickness of 1.5nm. There is an important difference in that the shorter gate length device has twenty times smaller off-current at zero gate bias than the longer gate length device, while the on-current at large gate voltages are comparable. This trend is true for a wide range of oxide thicknesses (Fig. 3 b) and should be a device consideration.

[1] International Technology Roadmap for Semiconductors http://public.itrs.net/
[2] The well tempered MOSFET information at http://www-mtl.mit.edu:80/Well

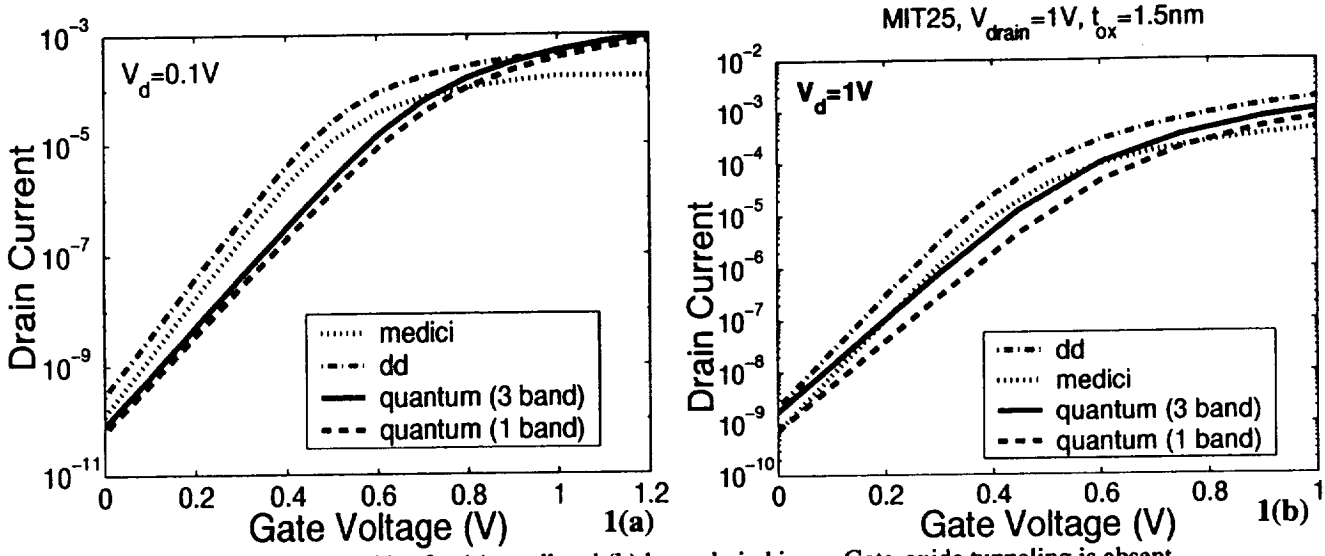

Fig.1. Drain current versus gate bias for (a) small and (b) large drain biases. Gate-oxide tunneling is absent.

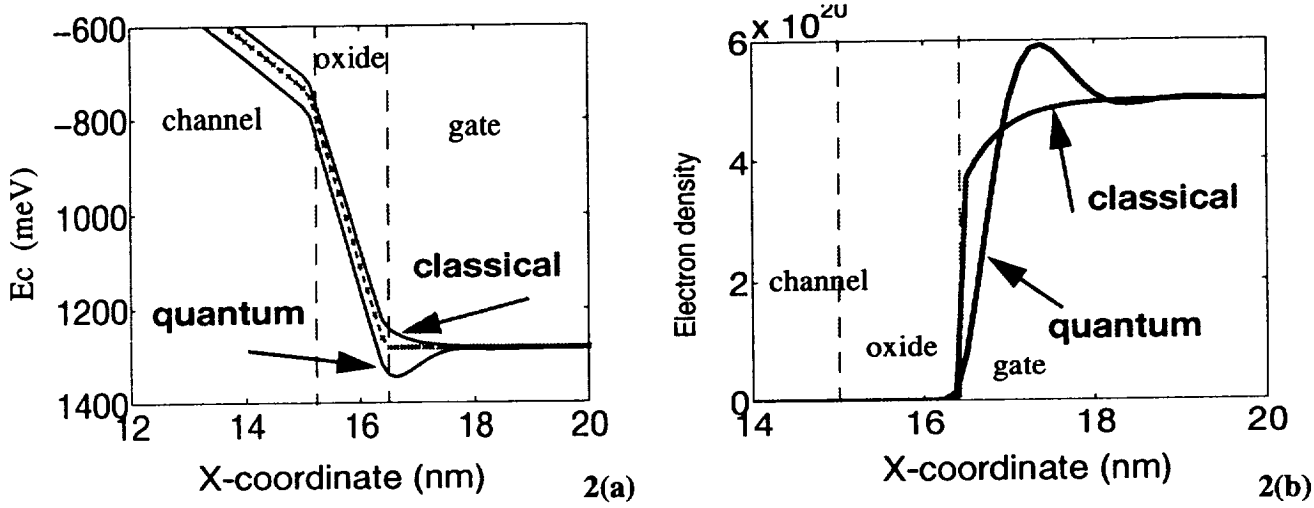

Fig. 2. Classical (DD) and quantum mechanically calculated potential profiles (a). The latter is lower than the former due to decay of electron density into the oxide (b).

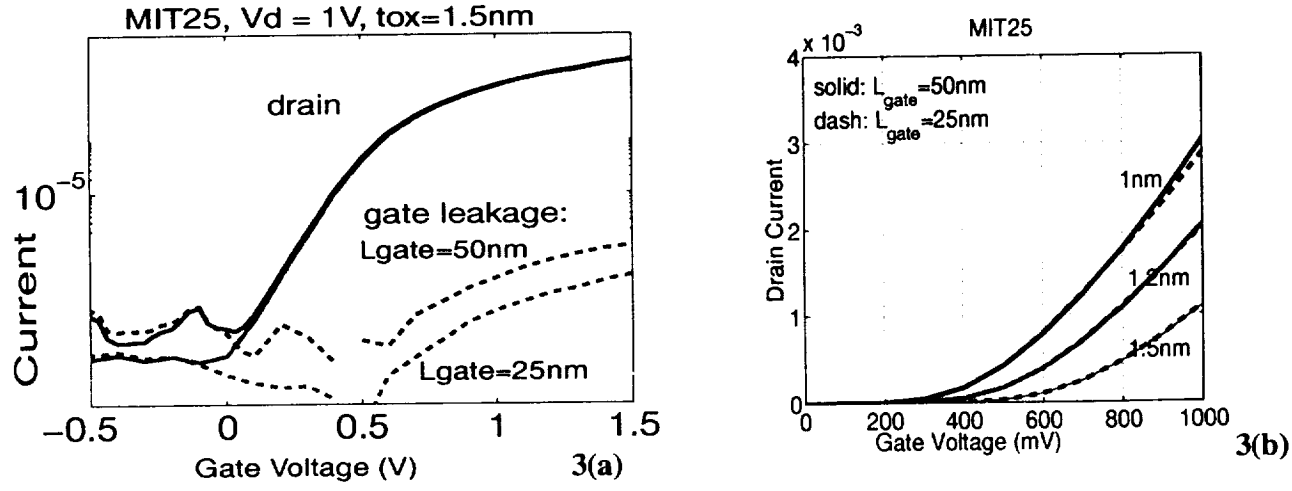

Fig. 3. Drain and gate leakage currents (a) for the MIT-25nm device with 25 and 50 nm gate lengths. Gate leakage is decreased by an order magnitude, while on-currents at Vg=1V are comparable (b).