Folded Coplanar Waveguide Slot Antenna on Silicon Substrates With a Polyimide Interface Layer

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Abstract– **A novel mm-wave Coplanar Waveguide (CPW) folded slot antenna is characterized on low-resistivity Si substrate (1 Ω-cm) and a high resistivity Si substrate with a polyimide interface layer for the first time. The antenna resonates around 30 GHz with a return loss greater than 14.6 dB. Measured radiation patterns indicate the existence of a main lobe, but the radiation pattern is affected by a strong surface wave mode, which is greater in the high resistivity Si wafer.**

I. Introduction

The possibility of low cost RF and microwave circuits integrated with digital and analog circuits on the same chip is creating a strong interest in silicon as a microwave substrate. Their operation on CMOS grade Si, however, is degraded by high loss of transmission lines and antennas. To overcome this problem researchers have used two different approaches. In the first approach, high resistivity Si (HRS) wafers are used (ρ>2500 Ω-cm) [1]-[2] and traditional microwave components have a performance similar to those on dielectric substrates, such as GaAs. In the second approach, polyimide layers are used on top of the CMOS substrate to create an interface layer that can host low loss microwave components. Both microstrip and coplanar waveguide transmission lines fabricated in this way have exhibited low attenuation for an optimum polyimide thickness [3]-[4].

This paper presents the characterization of Coplanar Waveguide (CPW) folded slot antennas with a resonant frequency around 30 GHz on a CMOS silicon substrate and an HRS wafer with a polyimide interface for the first time. Results from experimental measurements and 3-D Finite Element Method (FEM) analysis are presented.

II. Antenna Design and Fabrication

The folded-slot antenna is a broad bandwidth planar antenna with maximum radiation at the broadside that is used in a variety of applications [5]. It consists of a folded-slot with a circumference approximately equal to one guided wavelength (λ_g) and can be fed with a CPW or Finite Ground Coplanar (FGC) waveguide from one end. A schematic of a folded-slot antenna with various parameters is shown in Fig. 1. The actual CPW fed antenna had a finite width ground plane, but it was electrically large and thus not a true FGC folded slot antenna.

In order to operate such an antenna on a low resistivity (1-20 Ω-cm) Si wafer, the electric fields in the CPW must have minimum interaction with the lossy substrate. For this reason a thick layer (20 μm) of polyimide (DuPont WE 1111) is deposited and cured on top of the wafer. The transmission line feeding the antenna was also designed for minimum coupling with the substrate according to [6]. A schematic of the proposed CPW structure can be seen in Fig. 2. Original simulations with Ansoft's HFSS, which is based on the Finite Element Method (FEM), were performed to determine the antenna impedance at resonance. These simulations revealed a relatively high value of resistance at resonance (R~250 Ω) and, therefore, a quarter-wave transformer was designed for optimum matching between the feeding line (Zo=60 Ω) and the antenna. The transformer length was 1.075 mm while its impedance was approximately 124 Ω (s=10 μm, w=20 μm). The antenna resonance was fine-tuned further by inserting a 2.07 mm section of 60Ω line between the

transformer and the folded slot. Table I summarizes the various antenna parameters. For the fabrication of the folded slot antenna, standard lithographic techniques were used, and the conductors were Au electroplated to a thickness of 3 μm. The same antenna design was fabricated on an HRS wafer using the same processing steps.

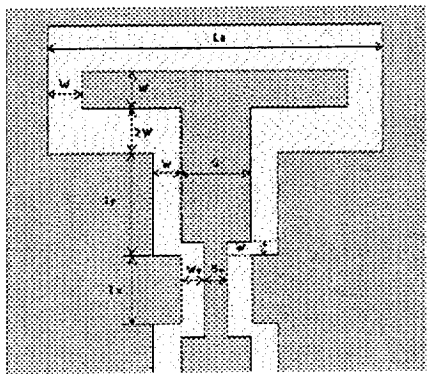


Figure 1: Geometry of folded slot antenna.

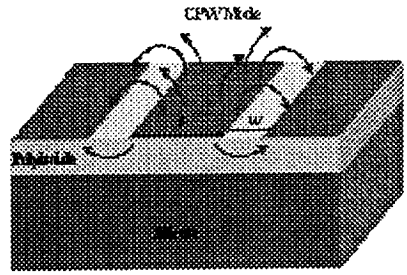


Figure 2: CPW line on Si substrate with a polyimide interface layer.

Table I. Design parameters for the folded-slot antenna

Parameter	La	L_F	L_T	W_T	S_T	S	W
Size (μm)	1024	2070	1075	20	10	50	10

III. RESULTS

Simulated results with Ansoft's HFSS for the return loss of the matched antenna on CMOS Si can be seen in Fig. 3, where a value of 16.5 dB is predicted at 30 GHz. The substrate was assumed to be 500 μm thick low resistivity silicon (σ=100 S/m, tanδ=0.0018) with a 20 μm polyimide overlay of ε_r= 2.8. The top and side-walls of the box surrounding the antenna were radiation boundaries. A perfect electric conductor was placed at the bottom of the Si substrate. Simulated E-plane radiation patterns at resonance are shown in Fig. 4, where a main lobe at broadside can be observed. For comparison purposes, the folded slot antenna was also simulated for high resistivity silicon using a parallel FDTD code developed by the ATHENA Research Group at Georgia Tech. The results indicated that under lossless conditions the antenna resonates near 27GHz, with return losses of 25.6dB at 27GHz and 2.65dB at 30GHz. EMAG Technologies, Inc. *em*PiCASSO™ indicated a resonant frequency at 27GHz for the same geometry. A comparison of the data generated by the ATHENA FDTD code and *em*PiCASSO™ is shown in Fig. 5. However, with the incorporation of loss, the resonant frequency is increased to 30GHz. The radiation patterns for the folded slot antenna were simulated with the ATHENA FDTD code, incorporating the matching network and *em*PiCASSO™, which did not include the matching network. From Fig. 6, it can be seen that a smaller lobe of radiation is emanating from the lower portion of the antenna. This is where the matching network is located for the folded slot antenna. The *em*PiCASSO™ simulations do not have this secondary radiation lobe.

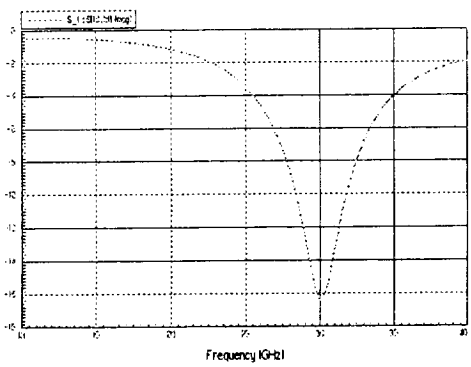


Figure 3: Simulated return loss of folded slot antenna on CMOS Si wafer with polyimide interface laver.

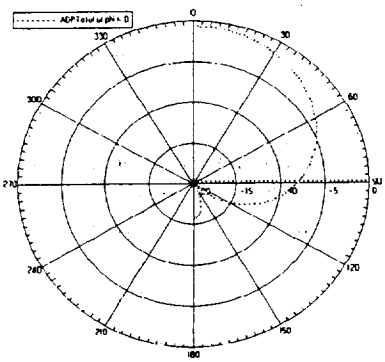


Figure 4: Simulated E-plane pattern with HFSS of a folded slot antenna on CMOS Si wafer.

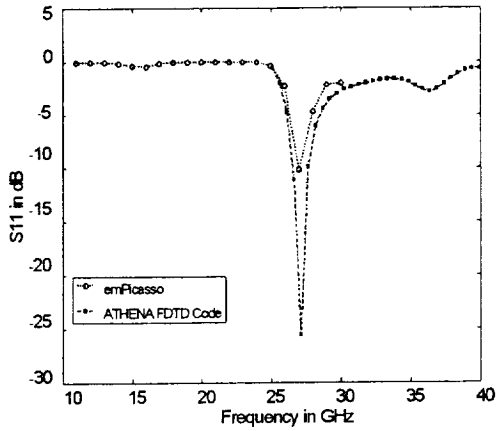


Figure 5: Simulated Return Loss of the Folded Slot Antenna Using *em*Picasso™ and GA Tech's ATHENA FDTD Code.

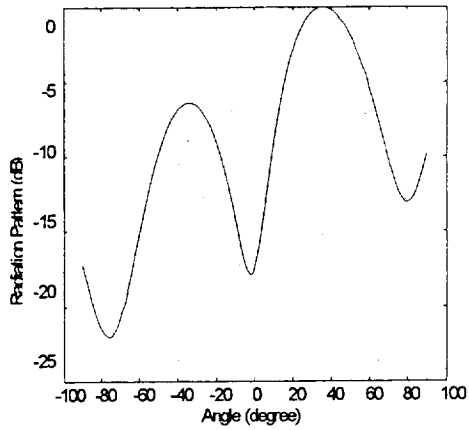
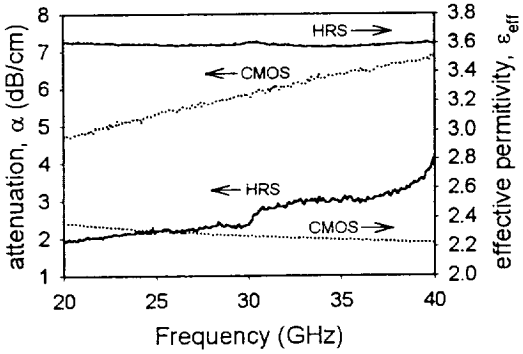


Figure 6: Simulated E-Plane Using GA Tech's ATHENA FDTD Code with Phi = 0.

The antenna was characterized experimentally using an HP8510 Vector Network Analyzer and GGB Industries coplanar probes. The probe-to-FGC transition was de-embedded with a TRL calibration using *Multical* [7], that set the reference plane 500 μm away from the transition. The effective dielectric constant and attenuation of the 60Ω lines on both substrates were measured and the results can be seen in Fig. 7. The measured attenuation is 5.7 dB/cm for the FGC line on CMOS Si and 2.3 dB/cm on HRS Si at 30 GHz. The return loss can be seen in Fig. 8, where a value of 14.6 dB was measured at 30 GHz for the antenna on CMOS Si, which agrees very well with the HFSS simulations. The same antenna on HRS has a stronger resonance at approximately 30.8 GHz, but it also has resonances at multiple frequencies due to surface wave modes and parallel plate waveguide modes between the CPW ground plane and the ground plane on the bottom of the wafer. It is seen in Fig. 8 that if the lower ground plane is removed and the wafer placed on quartz, most of the parasitic resonances are removed.



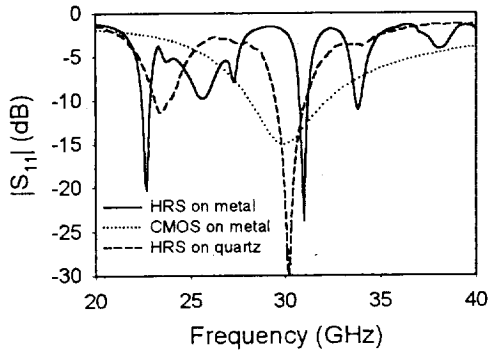


Figure 7: Measured attenuation and effective permittivity of CPW feed lines on CMOS and HRS wafers.

To characterize the radiation properties of the folded-slot antenna, the E- and H-plane patterns were measured at 30 GHz using a novel antenna pattern measurement system. The patterns are measured while the DUT antenna is excited by RF probes and the wafer is sitting on the metal wafer chuck of the RF probe station. The second antenna with the detector is swept in an arc around the DUT antenna. While this system permits quick radiation pattern measurements without dicing the Si wafer, the RF probe does shield the E-plane pattern results, which accounts for the asymmetry and the low power levels for angles less than –20 degrees in Fig. 9. Measurements are shown in Figs. 9 and 10 for the E- and H-planes, respectively. As can be observed in Fig. 9, the folded slot antenna has a main lobe around 0 degrees (broadside), but also radiates power in the

form of surface waves as witnessed by the strong lobe around 80 degrees. This surface wave mode radiation is higher for the HRS wafer, which agrees with the results discussed with regard to Fig. 8. HFSS simulations did not reveal this behavior since radiation boundaries are placed on the side-walls and the ground width was much larger. Figure 10 shows the un-normalized H-plane pattern, which is smooth with a maximum at 0 degrees as is expected. Figure 10 also shows that while folded slot antennas on an HRS wafer have higher surface wave mode problems, the lower line attenuation yields significantly higher gain.

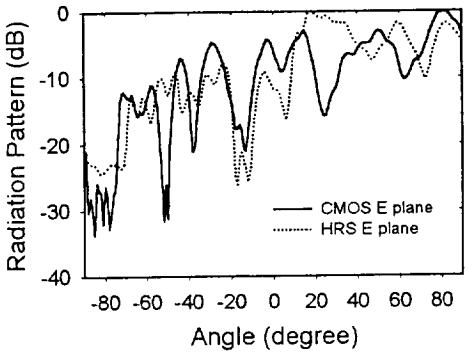


Figure 9: Measured E-plane pattern for folded slot antennas.

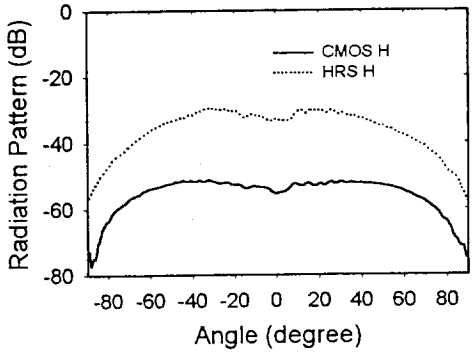


Figure 10: Measured H-plane pattern for folded slot antennas.

IV. Conclusions

A CPW folded slot antenna operating at 30 GHz has been characterized for the first time on a low resistivity Si substrate with a polyimide interface layer and compared to the same antenna on an HRS wafer. Experimental results of the antenna on CMOS showed a 30.5 GHz resonance with a 14.6 dB return loss, an E-plane pattern with a main lobe at broadside and strong surface waves around 80 degrees, as well as a smooth H-plane with a maximum at broadside. These results are in good agreement with HFSS simulations. The same antenna on HRS showed a stronger return loss resonance and higher antenna gain, but stronger surface wave mode issues that may limit its usefulness.

V. Acknowledgements

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VI. References

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