

# ISS Material Science Research Rack HWIL Interface Simulation

Philip J. Williams, Gary H. Ballard  
Dynamic Concepts, Inc.  
P.O. Box 97  
Madison, Alabama 35758  
[pwilliams, gballard]@dynamic-concepts.com

## KEYWORDS

HWIL, ISS, MSRR, Hardware in the Loop Simulator

## ABSTRACT

In this paper, the first Material Science Research Rack (MSRR-1) hardware-in-the-loop (HWIL) interface simulation is described. Dynamic Concepts developed this HWIL simulation system with funding and management provided by the Flight Software group (ED14) of NASA-MSFC's Avionics Department. The HWIL system has been used both as a flight software development environment and as a software qualification tool. To fulfill these roles, the HWIL simulator accurately models the system dynamics of many MSRR-1 subsystems and emulates most of the internal interface signals. The modeled subsystems include the Experiment Modules, the Thermal Environment Control System, the Vacuum Access System, the Solid State Power Controller Module, and the Active Rack Isolation Systems. The emulated signals reside on three separate MIL-STD-1553B digital communication buses, the ISS Medium Rate Data Link, and several analog controller and sensor signals. To enhance the range of testing, it was necessary to simulate several off-nominal conditions that may occur in the interfacing subsystems.

## MSRR-1 OVERVIEW

The MSRR-1 project is a joint venture involving the National Aeronautics and Space Administration (NASA), the European Space Agency (ESA), and NASA's Space Products Division (SPD). MSRR-1 was developed for the purpose of conducting high-temperature material science experiments in a microgravity environment onboard the International Space Station (ISS).

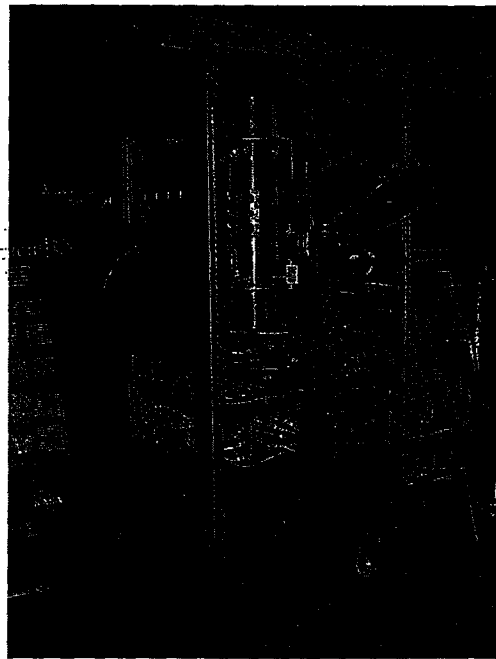
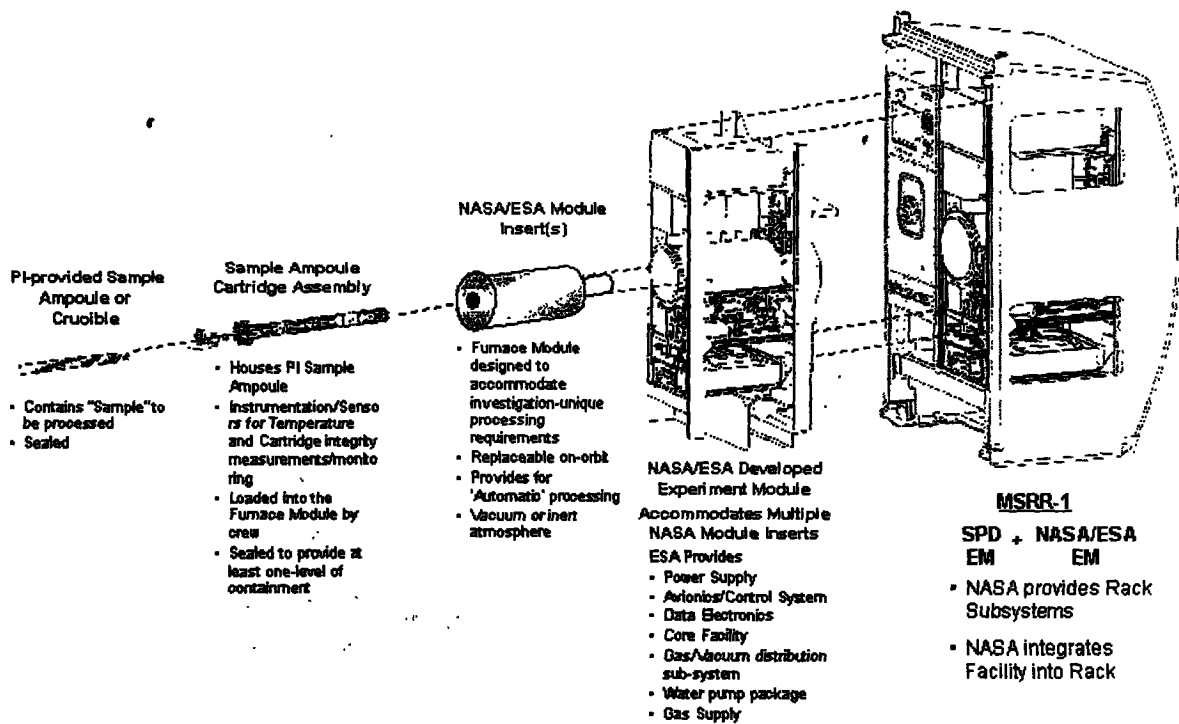


Figure 1 - MSRR-1 Mockup

The Microgravity Science & Applications Department at NASA's Marshall Space Flight Center manages the integration of the overall MSRR-1 system as well as the development of several of the rack support systems. MSRR-1 is a payload rack that will be located in the United States Laboratory Module of the International Space Station. The primary components of the MSRR-1 system consist of the Experiment Carrier (EC) and two furnace-type Experiment Modules (EMs). One of the two initial EMs is the European Space Agency Experiment Module - Material Science Laboratory (MSL). NASA SPD will provide the other furnace-type EM. The University of Alabama in Huntsville is developing the first SPD furnace.

Standard Payload Rack (ISPR), the Rack Support Subsystem (RSS), and the Active Rack Support System (ARIS) constitutes the MSRR-1 Experiment Carrier (EC). The RSS will provide the specific services required by the experiments. The RSS includes the Master Controller computer (MC), the Solid State Power Control Module (SSPCM), the Thermal Environment Control System (TECS), and the Vacuum Access System (VAS). The MC is the central computer that controls allocation of rack resources and communicates with the external ISS MDM computer. The SSPCM is a 40-channel power distribution module that supplies up to 6 kw of power (120 vdc and 28 vdc channels) to all the internal systems of the MSRR-1 rack.

NASA is responsible for the development of the EC components. The International



**Figure 2 - First Materials Science Research Rack Payload**

The TECS is a closed-loop controlled water-cooling system that removes the waste heat from all the internal systems via cold-plate heat exchangers. The VAS is the vacuum access system that allows the EM furnaces to conduct experiments in a vacuum environment. The ARIS is the rack vibration isolation system. Both EMs, the ARIS, and the SSPCM systems have onboard computers that communicate with the MSRR-1 MC computer via MIL-STD-1553B interfaces, while the TECS and VAS are controlled by analog commands generated by the MC computer.

## HWIL SYSTEM DESCRIPTION

The MSRR-1 hardware-in-the-loop simulator is called the Enhanced Master Controller Unit Tester (EMUT). The primary purpose for the EMUT is to aid the development and test of the flight software resident on the NASA built Master Controller computer. Dynamic Concepts developed the EMUT hardware and software systems with funding and management provided by the Flight Software group (ED14) of MSFC's Avionics Department. The EMUT system provides a simulation of every MC interface. EMUT has been used both as a flight software development environment and as a software qualification tool. To fulfill this role, the HWIL simulator accurately models the system dynamics of many internal subsystems and emulates most of the internal interface signals. Since many of the interfacing systems are developed by other non-NASA organizations, the EMUT has provided simulated communication interfaces when the actual system was not available. Furthermore, the EMUT can simulate off-nominal and error conditions that may not be easily produced by the real interfacing system. The modeled

subsystems include the ISS MDM, both EMs, TECS, VAS, SSPCM, and ARIS systems. The emulated signals reside on three separate MIL-STD-1553B digital communication buses, the ISS Medium Rate Data Link, and several analog controller and sensor signals.

Figure 4 shows the avionics diagram for the MSRR-1 EMUT. In this diagram, the yellow blocks represent subsystems simulated by EMUT, while the non-yellow blocks represent actual flight, or flight equivalent, components. As shown in Figure 3, EMUT is housed in a standard 19-inch rack and employs an array of commercial computer components purchased primarily from National Instruments<sup>TM</sup> and the Condor Engineering<sup>TM</sup> Company. The software is all custom developed object-oriented C++ running on the Microsoft<sup>TM</sup> Windows NT operating system. Most of the EMUT software employs an event-based state-machine architecture that runs on a 1 Hz major cycle, with some operations performed at a 10 Hz rate. The requirements for each of the modeled subsystems and interfaces were extracted from NASA's MSRR-1 interface control documents, and in some cases derived by analysis. The EMUT was verified for compliance to these requirements internally by NASA's ED14 software test team.

The EMUT's ISS MDM, ARIS, MSL EM, and SPD EM models are primarily MIL-STD-1553B message emulation simulations. In the deployed configuration, each of these systems have an onboard computer that have the dual responsibility for controlling their own internal components and maintaining 1553 communication with the central MC computer. There are three separate 1553 buses in the MSRR-1 system. The "ISS

bus” hosts the communication between the ISS MDM computer and all US Lab module payloads (including the MSRR-1 MC). The “Core bus” services communications for the MSL EM, SPD EM, and the SSPCM, while the “ARIS bus” is dedicated to solely MC-ARIS 1553 communication. Three separate NASA interface control documents govern the format of the specific message protocols for each bus.

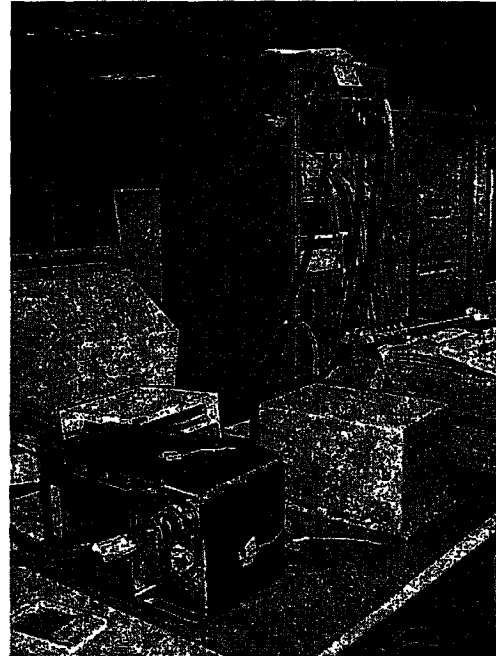


Figure 3 – EMUT Hardware

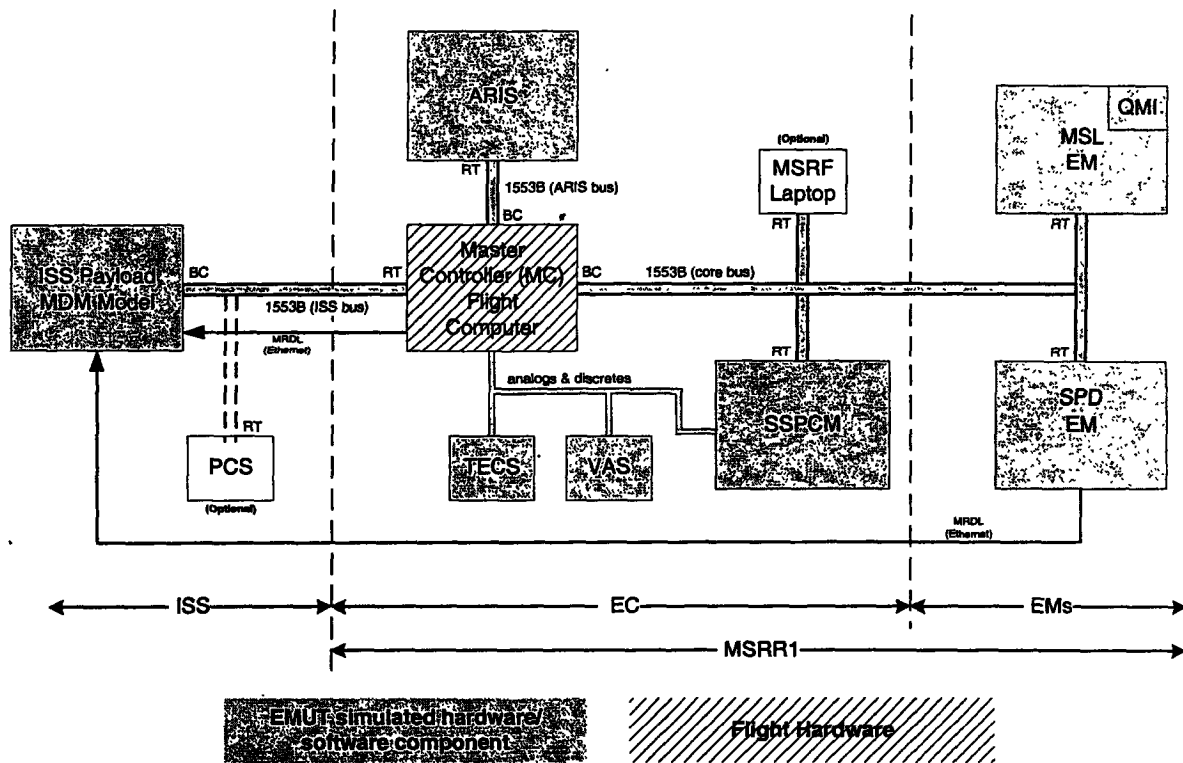


Figure 4 - EMUT Avionics Diagram

The EMUT Solid-State Power Control Module (SSPCM) model, shown in Figure 5, provides an output channel state model, the 1553B message handling model, and the thermal state model. The output channel state model of the SSPCM manages the state of all 40 output power channels (i.e., switches that are either open or closed). Each channel has programmable limits for over-current, under-voltage, and over-temperature trip protection. The 1553 message model provides emulated communication over 13 subaddresses with the MC computer. Provisions have been made to give the user the ability to generate off-nominal and error conditions via script file instruction. The third component of the SSPCM Model is the thermal state equation model. The thermal state equations are utilized to generate simulated heat rejection by the SSPCM during all modes of operations.

The EMUT system simulates the thermal/fluid dynamics of the MSRR-1 Thermal Environment Control System (TECS) system. The TECS is designed to collect waste heat from the MSRR-1 components and reject the heat to the ISS Moderate Temperature cooling loop. Figure 6 shows the TECS cooling loop schematic that was used as the basis for the derived system equations. The TECS model consists of two major components: the thermal/fluid interaction components and the conduit flow model component. The TECS system is dynamically modeled using an idealized lumped-parameter approach (e.g., assumes perfect mixing, etc.). In essence, the TECS model is responsible for reading and interpreting the MC generated analog commands, numerically integrating the model's governing differential equations, and generating the output voltages for the

simulated TECS sensors (flow meters and thermocouples). The simulated dynamics EMUT TECS model was designed to possess sufficient fidelity to thoroughly test the MC flight software, but was not intended to be a full fledged thermodynamics model.

To simulate the vacuum resources available in MSRR-1, EMUT includes dynamic models the Vacuum Access System (VAS) components. The EMUT VAS model consists of four modeled vacuum valves, two simulated pressure sensors, and five pressurized volumes or chambers. The VAS model is responsible for sensing the MC generated analog valve command signals, solving the VAS governing equations, and generating output commands to the simulated VAS sensor hardware. The VAS governing equations model the pressure decay and repressurization in the EM test chambers and VAS vacuum pipes. When a MC signal is received to change the state of a VAS vacuum valve, the VAS state equations are solved to determine the appropriate change in pressure over the cycle time increment. The output pressure sensor readings are updated at a 1 Hz rate.

## SUMMARY

The EMUT HWIL simulator has proven to be a valuable asset for the development and test of the Master Controller flight software. It has fulfilled its role as a testbed capable of producing simulated conditions that would otherwise be unattainable.

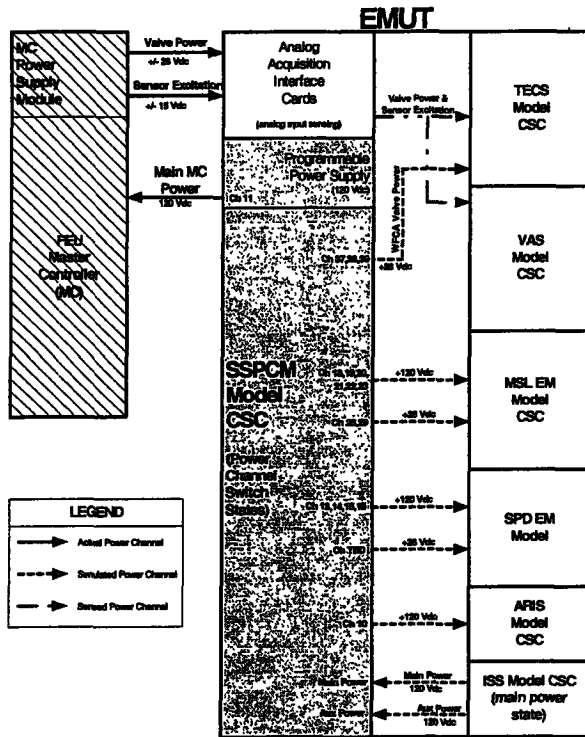


Figure 5 - SSPCM Model

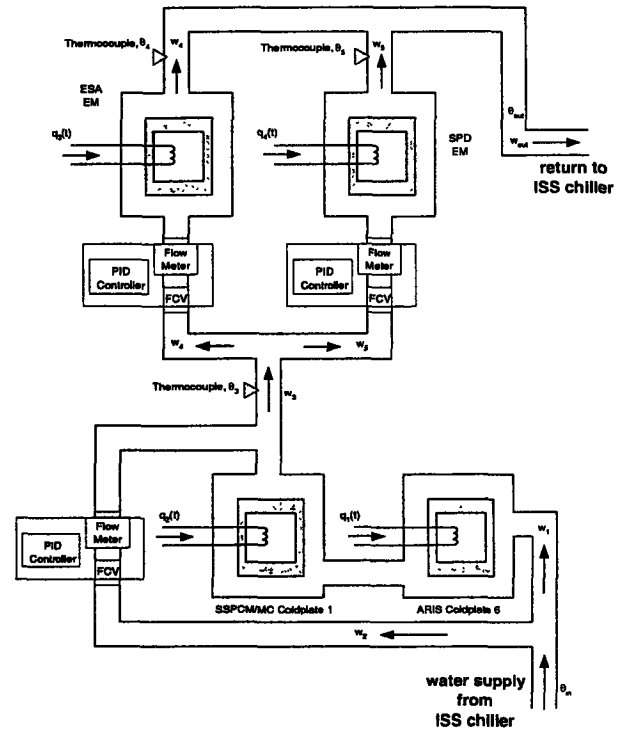


Figure 6 - TECS Schematic

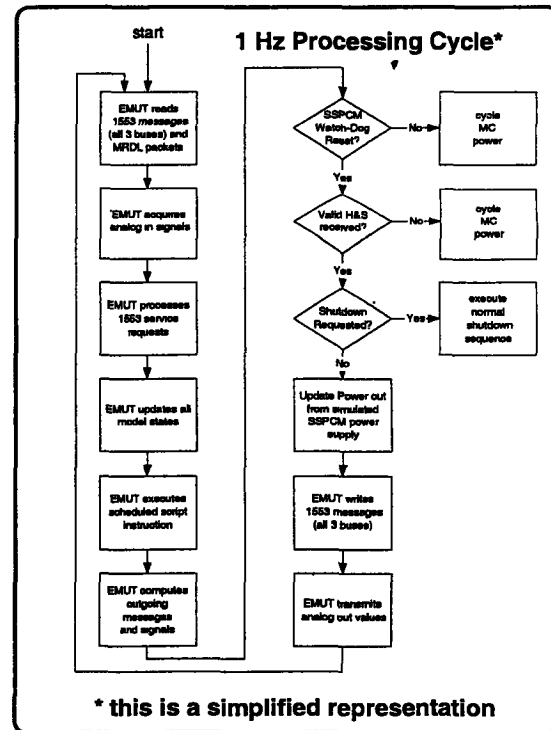
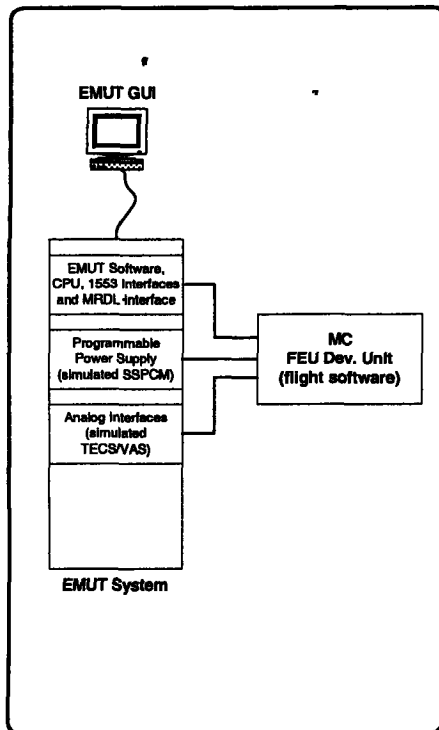


Figure 7 - EMUT Processing Cycle