High Mobility SiGe/Si Transistor Structures on Sapphire Substrates Using Ion Implantation

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ABSTRACT

High mobility n-type SiGe/Si transistor structures have been fabricated on sapphire substrates by ion implanting phosphorus ions into strained 100 Å thick silicon channels for the first time. The strained Si channels were sandwiched between $Si_{0.7}Ge_{0.3}$ layers, which, in turn, were deposited on $Si_{0.7}Ge_{0.3}$ virtual substrates and graded SiGe buffer layers. After the molecular beam epitaxy (MBE) film growth process was completed, ion implantation and post-annealing were used to introduce donors. The phosphorous ions were preferentially located in the Si channel at a peak concentration of approximately $1x10^{18}$ cm^{-3}. Room temperature electron mobilities exceeding 750 cm^2/V-sec at carrier densities of $1x10^{12}$ cm^{-2} were measured. Electron concentration appears to be the key factor that determines mobility, with the highest mobility observed for electron densities in the $1 - 2x10^{12}$ cm^{-2} range.

Keywords: HEMT, SiGe, sapphire, mobility

INTRODUCTION

Transceiver modules with high levels of analog and digital integration, which operate at K-band and higher frequencies (i.e above 18 GHz), are attractive for future commercial, military, and space broadband wireless communication systems.[1,2] In principle, silicon (Si)-based system-on-a-chip transceivers would significantly reduce the cost of beam-steering and data processing circuitry, thus enabling the development of low-cost phased array antennas. However, this development is impeded by the inability of Si-based circuitry to operate at such high frequencies.[3,4] Recent advances in SiGe technology have dramatically increased the speed of Si-based transistors, to levels that far surpass those necessary for K-band operation,[5] thus removing one of the factors that limit the high frequency performance of Si-based transceivers. A second parameter that limits high frequency operation is parasitic coupling between metallization layers and the Si substrate, which decreases inductor Q and increases RF transmission line loss.[6,7] These losses are substantially reduced by replacing the Si substrates with Si-on-sapphire technology.[8]

Development of SiGe/Si transistors with high carrier mobilities on sapphire substrates is a promising approach for satisfying the active and passive device requirements of high frequency transceivers. SiGe/Si n-type modulation doped field effect transistor (n-MODFETs) on silicon substrates have demonstrated room temperature electron mobility values ranging from 1300 - 2800 cm^2/V-sec.[9,10] The hole mobility of p-MODFET devices is sensitive to the Ge content of the channel; for channel compositions of $Si_{0.7}Ge_{0.3}$ and Ge, average hole mobilities of 250 and 1100 cm^2/V-sec, respectively, have been reported.[11] n-MODFET devices with Si channels grown on SiGe "virtual" substrates have higher electron mobilities than bulk Si because of the tensile strain

imparted by the larger lattice parameter of the relaxed SiGe lattice and minimal ionized impurity scattering. Likewise, hole mobility in p-MODFETs is enhanced by compressively strained SiGe channels. The ability to grow SiGe/Si p-type MODFETs on sapphire substrates has been shown.[12] Koester et al. reported p-MODFET structures on sapphire with hole mobilities of 800 cm^2/V-sec, and 0.1 μm gate length transistors fabricated from these transistors displayed cutoff (f_{max}) and transit (f_t) frequency values of 116 and 50 GHz, respectively. However, reports of n-type transistor structures with high electron mobilities on sapphire are lacking. In addition to the difficulties associated with high defect densities at the Si/sapphire interface, high mobility in n-type devices is further depressed by compressive strain in the Si films, which decreases electron mobility.[13]

In this paper, we report on the development of strained Si-channel transistor structures with n-type mobilities exceeding 750 cm^2/V-sec. Phosphorous doping was incorporated via ion implantation and post-annealing. The high electron mobility and short surface-to-channel distances of these structures are expected to provide a foundation for high electron mobility transistors (HEMTs) with high transconductance values and low parasitic capacitances. These transistors, together with the passive device performance enabled by the sapphire substrates, will be attractive for circuits working at K-band and higher frequencies. This advancement will also be useful in the development of high speed, high frequency complementary logic devices on sapphire.

EXPERIMENTAL

The structures presented in this article have properties similar to MODFETs, with the key difference being that the channel is doped. These structures are thus classified as HEMTs. Fabrication of SiGe/Si n-HEMTs on sapphire substrates was accomplished using a multi-step process. First, commercial sapphire substrates with 2700 Å thick Si films were obtained from St. Gobain Crystals, Inc. The crystalline quality of the Si films was improved using a solid phase epitaxy and regrowth process, similar to that reported earlier.[14] In our study, Si ions were implanted into the Si films at a dose $2x10^{15}$ cm^{-2}, at a beam energy of 180 keV. The samples were annealed for three hours at 1100 °C in flowing N_2, followed by an eight hour O_2 anneal, also at 1100 °C. The oxide was chemically etched to achieve an ~ 1000 Å Si layer. The SiGe virtual substrates and SiGe/Si HEMT structures were grown using molecular beam epitaxy. Two types of virtual substrates were targeted—one using a "thick" SiGe buffer layer and virtual substrate (5.5 μm) and one using "thin" (1.0 μm) buffer layer and virtual substrate. The "thick" buffer layers were grown by first depositing a 500 Å thick Si layer, followed by a 4.5 μm graded SiGe layer and a 1.0 μm $Si_{0.7}Ge_{0.3}$ virtual substrate. The "thin" virtual substrates were grown beginning with a 500 Å thick Si layer, followed by a series of SiGe/SiGeC layers (totaling 0.6 μm) with increasing Ge content, and a 0.4 μm $Si_{0.7}Ge_{0.3}$ virtual substrate.

Two types of HEMT structures were grown. In the first version, a 100 Å Si channel, followed by 300 Å $Si_{0.7}Ge_{0.3}$ and 200 Å Si layers were grown. In the second version, the 100 Å Si channel was followed by 150 Å $Si_{0.7}Ge_{0.3}$ and 50 Å Si layers. Donors were

introduced using phosphorous ion implantation, at accelerating voltages of 5 or 20 keV (for the 200 and 500 Å surface-to-channel distances, respectively), and dosages of $4x10^{12}$, $8x10^{12}$, or $1.6x10^{13}$ cm^{-2}.

The microstructural properties of the films were characterized using optical ellipsometry, high resolution x-ray diffractometry (HRXRD), Transmission Electron Microscopy (TEM), secondary ion mass spectroscopy (SIMS) and Atomic Force Microscopy. Room temperature carrier mobility was measured using the conventional van der Pauw technique, wherein the probes were placed at the four corners of $1cm^2$ samples. The applied magnetic field was 0.5 Tesla.

RESULTS AND DISCUSSION

Figure 1 is a low magnification cross-sectional transmission electron microscope (TEM) image of the graded SiGe buffer layer system. This figure shows that the dislocation density, which is substantial at the Si/sapphire interface, is reduced by the graded SiGe layer. Although dislocations are still apparent in the SiGe virtual substrate, the density is reduced by approximately one order of magnitude, and the dislocation density that propagates to the Si channel is approximately $5x10^8$ cm^{-2}. High resolution TEM imaging of the HEMT portion of the device is shown in the insert, and illustrates sharp, well-defined Si/SiGe interfaces and smooth layer formation.

After ion implantation, samples were post-annealed for 10 seconds at temperatures ranging from 700 – 990 °C. The highest electron mobilities were observed after the 700 °C anneals. Figure 2 plots room temperature mobility versus carrier concentration for all the samples that were phosphorous ion implanted and annealed at 700 °C for 10 seconds. Increasing the dosage resulted in significantly higher electron concentrations, but lower mobilities.

The key feature to emerge from figure 2 is that the electron mobility was highly dependent on electron concentration, and the highest mobilities were observed for the lowest experimental electron concentrations, i.e. in the $1 - 2x10^{12}$ cm^{-2} range. Decrease in electron mobility for SiGe/Si n-HEMTs as the electron concentration exceeds ~ $2x10^{12}$ cm^{-2} has been reported previously.[15] Despite the fact that the range of buffer layer/virtual substrate and surface-to-channel distances was considerably different for the four structures studied, all the samples displayed similar mobility versus electron concentration profiles. The key factors that control electron mobility appear to be the implant dosage and anneal temperature which in turn control the electron concentration.

Investigation of the dopant profiles in these films provides insights into the conduction mechanisms. Secondary Ion Mass Spectroscopy (SIMS) data after phosphorous ion implantation and rapid thermal annealing at 700 or 900 °C is shown in figure 3. The most notable feature is the high phosphorous content in the Si channel, and lower concentrations of phosphorous in the SiGe layers immediately adjacent to the Si channel. The phosphorous concentration in the Si channel reaches peaks at approximately $1x10^{18}$ cm^{-3}, dropping to less than $2x10^{17}$ cm^{-3} in the immediately adjacent SiGe layer.

Increasing the anneal temperature to 900 °C caused little change in the SIMS phosphorus profile. Although a detailed analysis of the diffusion behavior of phosphorous ions in SiGe/Si is outside the scope of this paper, it appears that the location of phosphorous in the silicon layer is due primarily to the implant energy, channeling and the higher diffusivity of phosphorous in SiGe relative to Si.[16] For samples with thinner (200 Å) surface-to-channel distances, similar behavior was observed.

Correlation of the mobility, TEM and SIMS data provides insights into the carrier mobility performance for the SiGe/Si n-HEMT structures on sapphire. The observed mobilities are significantly higher than bulk values (the bulk mobilities of Si and $Si_{0.7}Ge_{0.3}$, doped to $1x10^{18}$ cm^{-3}, are less than 300 cm^2/V-sec).[17,18] However, the mobility values are also substantially lower than have been reported for SiGe n-MODFET structures on Si substrates. The enhanced mobility vs. bulk materials is consistent with the existence of tensile strain in the Si channels, which causes splitting of the six-fold degenerate conduction band and the generation of two low energy bands that enable high electron mobility.[19] Although comprehensive mobility calculations that include strain, impurity effects and quantization have not been published, we believe the mobility is limited by scattering from the ionized donors in the channel, and non-optimal tensile strain in the Si channel.

The results of this study are encouraging for the development of Si-based circuitry for high frequency, broadband applications. The observed mobilities are sufficiently high for K-band and higher frequency operations. Furthermore, the simplicity of the ion-

implantation process and preferential location of phosphorous in the channel considerably simplify the film growth technique and relax the constraints necessary for device processing. Finally, the use of highly insulating sapphire substrates will substantially improve the Q values of inductors, minimize parasitic capacitances, and improve isolation between devices, thus enabling Si-based system-on-a-chip transceivers to be pushed to higher frequencies.

CONCLUSIONS

The advantages of insulating sapphire substrates for high performance passive devices and device isolation are well known, but the development of K-band n-type Si circuitry is limited by the electron mobility of these devices. This study demonstrates Si/SiGe transistor structures on sapphire substrates with n-type mobilities exceeding 750 cm^2/V-sec, where the donor ions are implanted into the Si channel using an ion implantation and post-anneal process. These results are encouraging for the development of system-on-a-chip transceivers on sapphire substrates

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LIST OF FIGURES

Figure 1. Cross-sectional TEM of graded SiGe buffer layer and SiGe virtual substrate, magnified at 12 kX. The high density of dislocations in the initial layer is largely relieved by the SiGe buffer layer. The insert shows a cross sectional TEM of the HEMT portion of device (magnification = 590 kX).

Figure 2. Room temperature mobility versus electron density, for SiGe/Si HEMTs with differing surface-to-channel distances, and SiGe graded layer thicknesses. (■) 5.5 μm buffer layer/virtual substrate 500 Å surface-to-channel distance; (□) 5.5 μm buffer layer/virtual substrate, 200 Å surface-to-channel distance; (▲) 1 μm buffer layer/virtual substrate, 500 Å surface-to-channel distance; (△) 1 μm buffer layer/virtual substrate, 200 Å surface-to-channel distance.

Figure 3. Secondary ion mass spectroscopy of HEMT portion of device, after 20 keV, $4x10^{12}$ cm^{-2} dose phosphorous implantation post-anneal. Samples post-annealed at: a) —700 °C for 10 seconds; and b) ····· 900 °C for 10 seconds). Surface-to-channel distance = 500 Å.

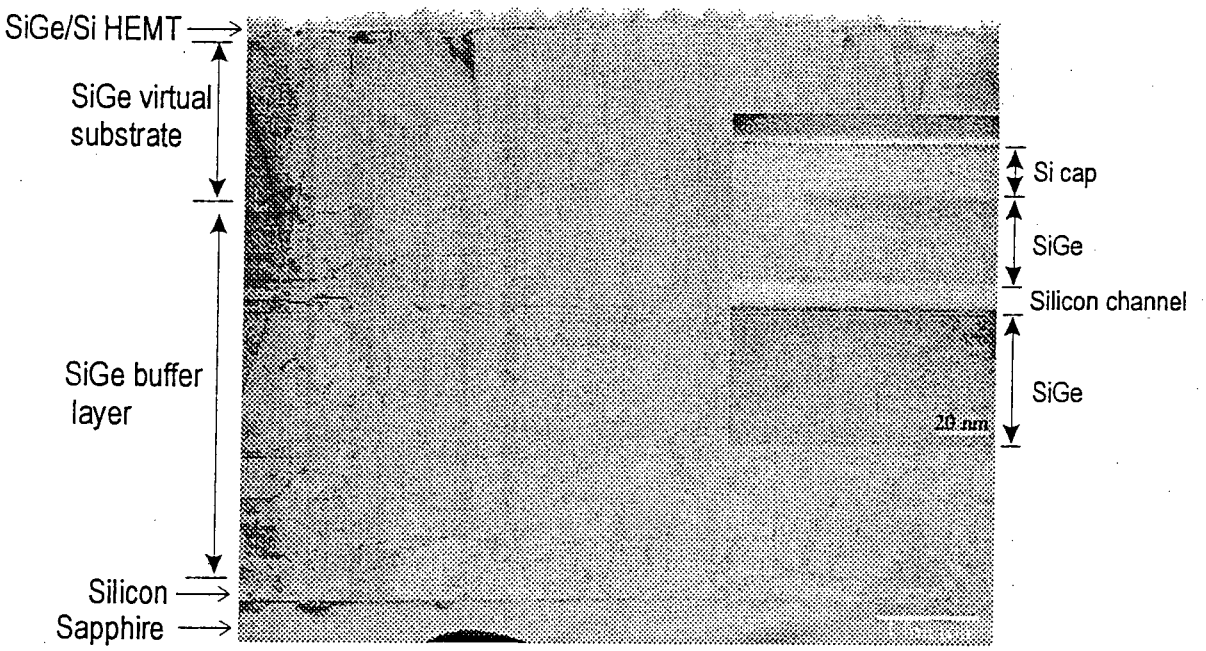
SiGe/Si HEMT
SiGe virtual substrate
SiGe buffer layer
Silicon
Sapphire
Si cap
SiGe
Silicon channel
SiGe
20 nm

Figure 1

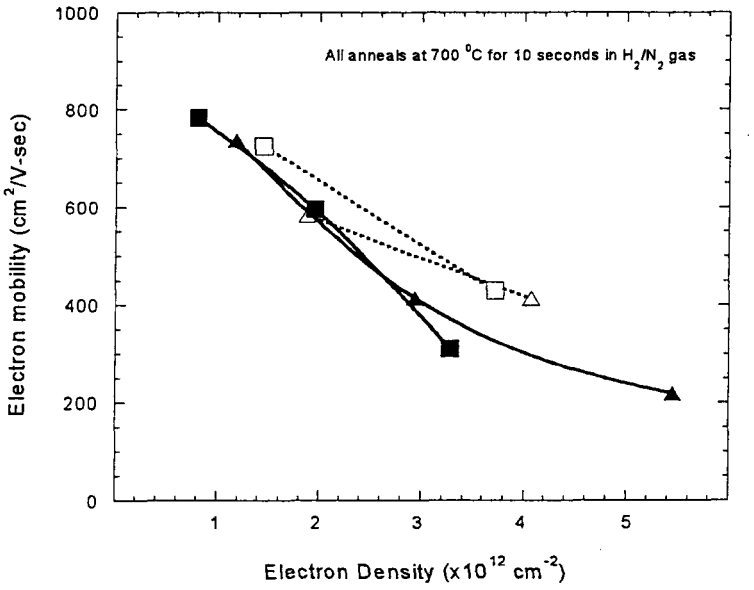

Figure 2

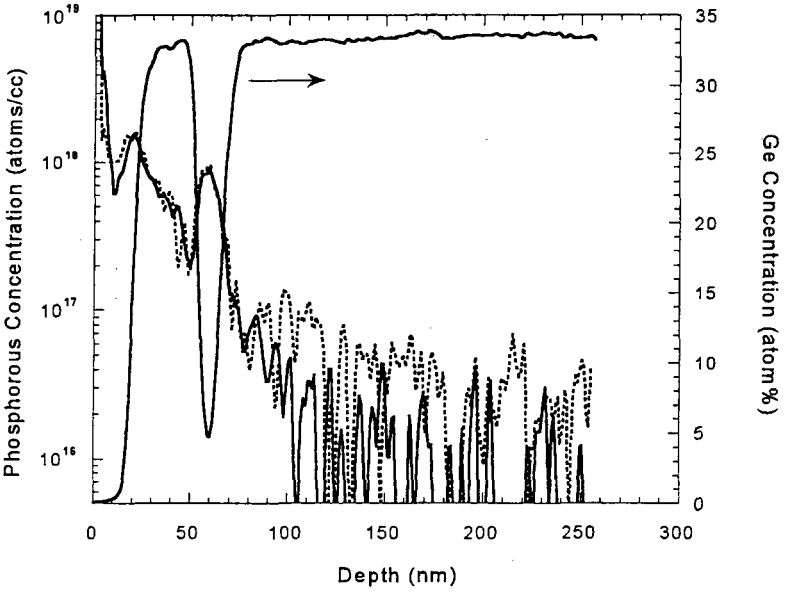

Figure 3