ADVANCED DATA ACQUISITION SYSTEMS

Introduction

Current and future requirements of the aerospace sensors and transducers field make it necessary for the design and development of new data acquisition devices and instrumentation systems. New designs are sought to incorporate self-health, self-calibrating, self-repair capabilities, allowing greater measurement reliability and extended calibration cycles. With the addition of power management schemes, state-of-the-art data acquisition systems allow data to be processed and presented to the users with increased efficiency and accuracy. The design architecture presented in this paper displays an innovative approach to data acquisition systems. The design incorporates: electronic health self-check, device/system self-calibration, electronics and function self-repair, failure detection and prediction, and power management (reduced power consumption). These requirements are driven by the aerospace industry need to reduce operations and maintenance costs, to accelerate processing time and to provide reliable hardware with minimum costs.

The project's design architecture incorporates some commercially available components identified during the market research investigation like:

- Field Programmable Gate Arrays (FPGA)
- Programmable Analog Integrated Circuits (PAC IC) and Field Programmable Analog Arrays (FPAA)
- Digital Signal Processing (DSP) electronic/system control

And investigation of specific characteristics found in technologies like:

- Electronic Component Mean Time Between Failure (MTBF), and
- Radiation Hardened Component Availability

There are three main sections discussed in the design architecture presented in this document. They are the following: (a) Analog Signal Module Section, (b) Digital Signal/Control Module Section and (c) Power Management Module Section. These sections are discussed in detail in the following pages.

This approach to data acquisition systems has resulted in the assignment of patent rights to Kennedy Space Center under U.S. patent # 6,462,684. Furthermore, NASA KSC commercialization office has issued licensing rights to Circuit Avenue Netrepreneurs, LLC, a minority-owned business founded in 1999 located in Camden, NJ.
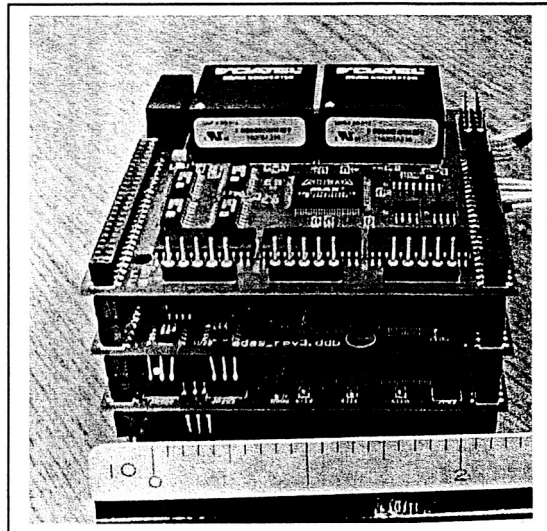
Example of ADAS prototype modules

Analog Signal Module Section

The Analog Signal Module design architecture presented in this document addresses the issue of signal redundancy and signal integrity without taking the traditional approach of providing total hardware redundancy for every channel and every function block of the Data Acquisition System.

In addition to signal redundancy issues, the need of self-calibration verification capability has also played a major role in defining the approach followed by this project when formulating architecture. Data acquisition systems like the ones used in spacecrafts need to have the capability of automated calibration without external intervention.

Furthermore, the quality of the measurement provided by the system is directly related to the capability of the system to assure a proper calibration through the life of the process being monitored.

Finally, the capability of the data acquisition system to perform system health checks, failure detection and failure prediction as well as to have automated self-repair capability plays a paramount importance in systems where operator intervention is not an option. Again, deep space spacecrafts and remote location instrumentation require the ability to automatically and autonomously reconfigure themselves when failures occur.

As mentioned above, traditional approaches to these problems have been basically to provide systems with total hardware and software redundancy to overcome failures. These approaches usually are very costly and add significant weight, size and power requirements to the systems they are supporting. All these qualities are undesirable when dealing with aerospace systems.

The approach taken in this project explores the concept we have called *"spare parts - toolbox"*. As with any process that has identifiable critical components, we have identified and assessed areas of the data acquisition system with specific reliability issues As mentioned above, an initial reliability assessment based on data acquisition system exposure to external conditions has been implemented. Data acquisition system's areas like signal inputs and outputs have been considered high-risk areas, while internal areas of the system not exposed to external variables have been considered lower risk areas. A more detailed assessment that includes component reliability assessment will be implemented when components are selected for the specific application to be monitored.

Based on the reliability rating given to these areas, we provide the system *"toolbox"* with *n* number of *"spare parts"* (components) necessary to assure continued operation of the system. The number of *"spare parts"* of each type and the different types of *"spare*

parts" contained in the *"tool box"* does not have to be the same for each identified area of the system. Areas with higher probability of failure (due to user interaction and/or environment) are stocked with a greater number of *"spare parts"* than areas well protected by the system, and therefore, with lower probability of failure. The overall diagram of the design architecture for the analog signal path is presented in Appendix A. The architecture presented here has been defined to demonstrate the conceptual ideas of this project (self-calibration, self-configurable, self-reparable).

In general, it is expected that the number of *"spare parts"* contained in the *"tool box"* will diminish as we go deeper into the system, where external factors will have a lesser effect. Of course, radiation effects (as Single Event Upsets and dose radiation) have to be considered in the reliability factors for each section.

The project relies on specific components to provide the desired flexibility and signal integrity. They are the following:

1. **Analog Switch Matrix.** The analog switch matrix configuration is used extensively in the analog path configuration of this project. This approach gives us the flexibility to reconfigure any section of the analog circuitry based on its health. The analog switch matrix approach allows external and internal bus lines to be real-time configured by the controller to provide alternate path to any analog signal.

2. **Analog Signal Conditioner.** To fully utilize the flexibility provided by the analog switch matrix approach, we have the capability to configure in real-time the analog signal conditioners to the specific requirements of each analog line. The *"toolbox"* in our system contains generic analog signal conditioner *"spare parts"* that can be incorporated in the circuit and reconfigured immediately to provide the desired signal integrity in this project.

3. **Calibration Circuit.** The calibration circuit provides real-time continuous calibration verification of the analog

channels. This feature is used in conjunction with the analog switch matrix and the analog signal conditioners to decide whether signal health and accuracy is within the specified by the system and if not, set an alternate path for the system that meets the requirements.

Digital Signal/Controller Module Section

The Digital Module (DM) will provide control, monitoring, and processing of several analog signals. The basic architecture of the Digital Module consists of one or more processors, and Field Programmable Gate Arrays (FPGAs). Mean Time Before Failure (MTBF), and redundancy requirements of the module determines the final number of processors and FPGAs used in the design.

1. The Digital Module (DM) provides redundant control and monitor for critical system functions as defined by the application.

2. The DM is designed for low power consumption including the implementation of sleep mode in the firmware. The firmware is designed to conserve power whenever possible.

3. The DM provides for external communication to the user via PC serial port. The external communication line is protected from spurious voltage spikes due to connection/disconnection. Other communication protocols can be incorporated as needed by the application.

4. The DM monitors the health of the system by processing defined measurements and/or trends. It automatically makes adjustments to the system for channel failures, temperature compensation, and calibration.

Processor: The processor monitors, controls and processes the analog input signals. It has the following capabilities:

- Serial Communication Interface (SCI) and Serial Peripheral Interface (SPI).
- JTAG Interface for online debugging and Flash programming.

- Flash memory for storing the main programs and program data.
- General Purpose Input/Outputs (GPIOs).

Design's Software/Firmware

The firmware of the DM monitors input signals, controls the output lines and performs signal processing. The firmware contains the following main functions:

- Detect signal path failures and perform self-repairs.
- Performs periodic calibrations on the Analog Module.
- Automatically detect system degradation and potential failures.
- Controls the analog switch matrices.
- Provides a communication interface with the FPGA for downloading FPGA programs.
- Provides external interface to users.
- Provides digital signal processing.

In a multiple processors configuration for the Digital Module, a master and a slave(s) are designated. If one of the processor fails, another processor assumes the tasks of the failed processor. These processors periodically communicate among themselves to perform health checks.

Graphic Users Interface (GUI): The GUI is the main interface between the user and the system (used during programming and debugging stage). It is capable of issuing commands and receiving status from the system. It displays the analog output for each channel in the system as well as configuration information.

Field Programmable Gate Arrays: The FPGA provides digital switching for multiple signal and control lines. The digital switches are re-configurable to route signal and control lines to the appropriate destination. The processor or internal logic within the FPGA automatically controls configuration of the digital switches. The FPGA functions are not limited to switching digital signals. It can be programmed to perform functions like signal processing and control functions.

Power Management Module Section

The Power Management Module (PMM) is designed to provide ADAS with a way to monitor, control, and manage the supply power to the different sections of the system.

The PMM uses several processors to perform monitoring and control functions. Each processor has an asociated watchdog circuitry that resets the processor if a problem is detected. Power consumption of each processor is also monitored by its counterparts. If a sudden increase in current consumption is detected in one of the processors (typical of a latch up condition), the alternate processor will cycle its power to allow it to recover before permanent damage occurs. Since processors operate in parallel under the same set of rules, the hand-off of the control following the failure of one of the processors can be performed without disruptions. The primary and backup processors can be interfaced to a host computer or master processor if the decision making process is driven by rules beyond the control of the PMM circuitry.

The PMM processors have control over a variety of solid-state switches which are used to distribute power to circuits under their control. The current flowing through each switch is monitored to allow for early detection of degradation in the circuitry being driven by such switches. The processors, based on a predetermined set of rules, can autonomously decide whether circuitry must be powered down following the detection of an anomaly. This allows for either processor to take control of the switches if the other processor is powered down.

Redundant power sources are used to power the system. The hand-off between power sources following the failure of one of them is done without the intervention of the processors. Power conditioning, over voltage protection, reverse polarity protection, and filtering is also provided by the circuitry.

Summary

The technology described here presents innovative solutions to problems associated with traditional data acquisition methods. As described before, the following areas have been addressed in the design:

· Electronic health self-check: Continuous health checks allow for failures to be detected and corrected within seconds.

· Device/system self-calibration: The calibration circuitry allows for continuous self-calibration of the system thus providing accurate measurements even under diverse environmental conditions.

· Electronics and function self-repair: Intelligence build into the processors allows for the system to automatically and autonomously re-route signals to maintain an accurate and stable measurement.

· Failure detection and prediction: The current state of the system is continuously compared against its historical information (stored locally within the system). Real-time analysis results in the prediction of components faced with imminent failure, as well as longer degradation trends.

· Power management, for reduced power consumption; Smart power management is used to reduce unnecessary power consumption.

ANALOG SIGNAL PATH

Analog Inputs

(N+2) x M Analog

N x M Analog

Analog Outputs

Channel 1
Channel 2
Channel 3
Channel N

Channel 1
Channel 2
Channel 3

Channel N

LEGEND

● Analog Switch (ON)

○ Analog Switch (OFF)

External Data Bus

Internal Data Bus (Raw Data)

Internal Data Bus (Conditioned Data)

Internal Data Bus (Synchronous Sampled Data to be digitized)

▪ ▪ ▪ ▪ Spare Data Bus line

Spare Component

○ μP Controlled

P x R Analog

M x P Analog