Close Out and Final Report for

NASA Glenn Cooperative Agreement NCC3-867

Packaging Technology for SiC High Temperature Circuits Operable up to 500 °C

OAI-02-043

Lian-Yu Chen

Introduction

NASA space and aeronautical missions need harsh-environment, especially, high-temperature operable MEMS sensors and electronics, such as sensors and electronics for in situ combustion/emission monitoring of aeronautical engines and space probes to the inner solar system. Various silicon carbide (SiC) high temperature operable MEMS sensors and electronics have been demonstrated at temperatures as high as 600 °C, but most of these devices were demonstrated only in the laboratory environment partially because long-term reliable packaging technology for supporting these sensors/devices at temperatures of 500 °C and beyond was not available. Thus, the development and validation of a systematic high temperature packaging technology for SiC-based devices is essential for both in situ testing and commercialization of high temperature SiC MEMS sensors and electronics.

Completed Research (FY01 and before)

Ceramic substrates (aluminum nitride and alumina) and gold (Au) thick-film metallization based high temperature electronic packaging technology had been demonstrated operable at 500 °C in oxidizing environment. The components of this prototype electronic packaging survived high temperature tests at 500 °C in oxidizing environment. Packaging components tested include electrical interconnection system (internal printed thick-film wire and wire bonds) and a SiC (diode) die-attach scheme using both substrates and gold thick-film materials. The electrical interconnection components were tested at 500 °C statically with a DC bias for over 5,000 hours, and evaluated in extremely dynamic thermal environment. As desired, the electrical resistances of the test loops (of thick-film printed wires, wire bonds, and lead bonds) soaked at 500 °C with or without current load were low and stable. The electrical failure percentage of 1 mil gold wire based interconnection system cycled at 32 °C/min and 53 °C/min for total of 235 cycles is 5%. And no electrical failure was observed for the electrical interconnection system based on 1 mil × 2 mil gold ribbon cycled at 53 °C/min between room temperature and 500 °C for over 500 cycles. Also as expected, the electrical isolation impedance between two neighboring printed wires (of prototype packages) that were not electrically jointed by a wire bond remained high during and after the 500 °C soak test.

Tensile strength of gold thick-film metallization on aluminum nitride has been preliminarily tested at room temperature and shear strength of metallization was tested at 500 °C using newly acquired high temperature shear module. The results of these tests were satisfactory.

Parametric study of thermo-mechanical characteristics of SiC die-attach assembly using gold thick-film material as die attaching layer was conducted using finite element analysis (FEA). The numerical calculation was performed at United Technologies Research Center (UTRC) with our significant involvement in selection of optimization parameters, abstraction of high temperature material properties, data analysis and interpretation. These results are important to assess the thermal reliability of the die-attach assembly and optimize thermal performance of the die-attach, especially, for high temperature MEMS packaging.

Considering the limit of capability of current material system an innovative low stress die-attach structure was proposed for packaging high temperature MEMS. The results of FEA simulation of 1 mm $\times$ 1 mm SiC die attached to aluminum nitride substrate showed low thermal stress in central device area in a temperature range of 600 °C.

Completed Research (FY02)

New high temperature low power 8-pin packages have been fabricated using commercial fabrication service. These packages are made of aluminum nitride and 96% alumina with Au metallization. The new design of these packages provides the chips inside with EM shielding.

Wirebond geometry control has been achieved for precise mechanical tests. Au wirebond samples with 45o heel-angle have been tested using wireloop test module. The geometry control improves the consistency of measurement of the wireloop breaking point.

A problem of stud pull test of thick-film metallization on ceramic substrates has been revealed and solved. Usually, people mount pull studs onto coating layer surface directly by epoxy for stud pull (adhesion) test. However we found that epoxy very often penetrated into thick-film/ceramic interface, therefore, generates extra/unexpected bonding between the thick-film and the substrates. In order to solve this problem we coated a compatible glass layer on the thick-film surface before mounting the studs. This technique enables precise measurement of the tensile strength of thick-film metallization on ceramic substrates.

Collaborating with OAI/GRC UTRC successfully simulated the thermal stress/strain of Au thick-film based SiC die-attach assembly using low yield strength and temperature dependent Au elasticity/plasticity. The stress/strain simulation helped us to assess the thermomechanical reliability of Au thick-film based die-attach and their failure mechanism. The stress/strain distribution of die-attach is important to high temperature MEMS packaging. Stress/strain distribution of Au wire wedgebond has also been calculated using FEA. After UTRC phasing out a research grant for FEA work at UM has been established.

The high temperature die-shear test module for Romulus IV Material Tester has been test-used for preliminary die shear testing at 500 °C. We have been working with Quad Group to improve the stability of the sample surface temperature. The module has been modified and will be delivered soon after tests at Quad Group.

In response to the need of wirebond on Pt chip metallization for SiC high temperature sensors/devices we have been working on Au/Pt and Pt/Pt wirebond. So far we have been able to

bond both Au and Pt wires onto Pt thick-film surface. We have also achieved preliminary success in bonding Au wire on Pt capped thin-film metallization on SiC chips.

A low thermal stress die-attach scheme has been further developed to reduce thermal stress due to material CTE mismatches of die-attach assembly. Die-attach thermal stress level is critical to the reliability of high temperature packaged MEMS.

The FE-SEM micrographs of Au wirebond samples tested in dynamic thermal environment have been analyzed with the direct optical observation of Au wires tested at high temperature with DC bias. It is concluded that the slow degradation of pure Au wires in dynamic thermal environment is due to crystallization of wire material accelerated by electro-migration at high temperatures.

In order to form a packaging system ceramic substrates based printed circuit boards (PCBs) have been developed. AlN and Al2O3 PCBs for single packaged device or single chip level package tests have been designed and fabricated. This PCB level joining technology is intended for multi chip level packages and passives interconnections. This packaging system will be tested with SiC high temperature sensors/devices when they are available.

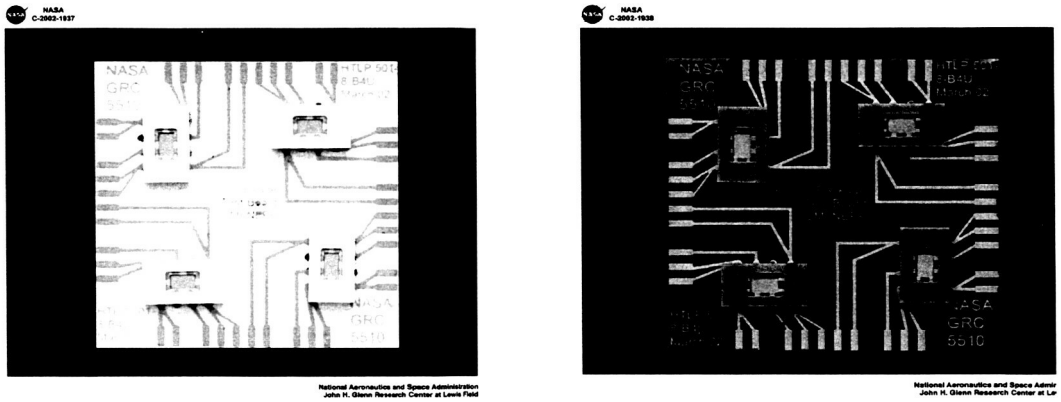

Figure 1: AlN and Al_2O_3 high temperature packaging systems including chip level packages and PCBs for SiC microsystems. The PCBs are designed for high temperature tests of single chip level package or single packaged microsystem/device.

Publications

Shun-Tien Lin, and Liangyu Chen, *Thermo-Mechanical Optimization of a Gold Thick-film based SiC Die-attach Assembly using Finite Element Analysis*, the 6th International High Temperature Electronics Conference (HiTEC), Albuquerque, New Mexico, June 2–5, 2002, (see Appendix).

Liangyu Chen, *High Temperature MEMS packaging*, Short Course, the 6th International High Temperature Electronics Conference (HiTEC), Albuquerque, New Mexico, June 2–5, 2002.

Patrick McCluskey, and Liangyu Chen, *Microsystem Packaging for High Temperature and Harsh Environments*, MSTNEWS—International Newsletter on MicroSystems and MEMS, Teltow, Germany, September 2001.

Philip G. Neudeck, Robert S. Okojie, and Liangyu Chen, *High Temperature Electronics: A Role for Wide Bandgap Semiconductors?*, Proceedings of the Institute of Electrical and Electronics Engineers, September 2001.

Liangyu Chen, and Jih-Fen Lei, *Packaging of Harsh Environment MEMS Devices*, the MEMS Handbook, edited by Mohamed Gad-el-Hak, CRC Press, Boca Raton, Florida, September 2001.

Liangyu Chen, Robert S. Okojie, Philip G. Neudeck, and Gary W. Hunter, *Material System For Packaging 500°C SiC Microsystems*, Proceedings of Symposium N of 2001 Material Research Society (MRS) Spring Meeting, San Francisco, California, April 16-20, 2001.

Appendix

The 6th International High Temperature Electronics Conference
Albuquerque, NM, June 2-5, 2002 at the Old Town Sheraton

Thermo-Mechanical Optimization of a Gold Thick-film based SiC Die-attach Assembly using Finite Element Analysis

Shun-Tien Lin
United Technologies Research Center
411 Silver Lane, MS 129-73
East Hartford, CT 06108
Email: Lins@utrc.utc.com

Liang-Yu Chen
OAI/NASA Glenn Research Center
21000 Brookpark Road, MS 77-1
Cleveland, OH 44135
Email: Liangyu.Chen@grc.nasa.gov

Abstract

A parametric study of the thermomechanical reliability of a Au thick-film based SiC-die-attach assembly using nonlinear finite element analysis (FEA) was conducted to optimize the die-attach thermo-mechanical performance for operation at temperatures from room temperature to 500 °C. This parametric study centered on material selection, structure design and process control. The die-attach assembly is composed of a 1 mm × 1 mm SiC die attached to a ceramic substrate (either 96% aluminum oxide (Al_2O_3) or aluminum nitride (AlN)) with a gold (Au) thick-film attach layer. The effects of die-size, Au attach layer thickness, substrate material, and stress relaxing temperature on the stress/strain distribution and relative fatigue lifetime of the die-attach assembly were numerically analyzed. By comparing the calculated permanent strain in the thick-film attach layer, FEA results indicate that AlN is superior to Al_2O_3. Thicker Au attach layers and smaller die sizes are recommended to reduce the permanent strain in thick-film die attach layer. Thicker SiC die also reduces the stress near the (top) surface region of the die. A stress relaxing temperature close to the midpoint of the operating temperature range further reduces the maximum stress/strain, thereby improving die-attach thermo-mechanical reliability. These recommendations present guidelines to optimize the thermo-mechanical performance of the die-attach assembly and are valid for a wide range of thermal environments.

1. Introduction

NASA is interested in using high temperature operable microsystems, including electronics and micro-electro-mechanical-systems (MEMS) based sensors, to characterize *in-situ* combustion environments in aerospace engines and the atmosphere of inner solar planets such as Venus. As an example, a high temperature pressure sensor is one of NASA's and the aerospace industry's most wanted high temperature sensor for application in the development of a new generation of aerospace engines. The sensor and on-chip electronics must operate at temperatures up to 500°C, and the devices are very often directly exposed to combustion chemical species including oxygen in air, hydrocarbon/hydrogen in fuel, and catalytically poisoning species such as NO_x and SO_x in combustion exhaust. The temperature in the atmospheric environment of Venus is also as high as 500°C, and Venus gas ambience is highly corrosive. Both of these potential operation environments can be summarized as high temperature, high dynamic pressure, and chemically corrosive. Various SiC semiconductor devices have been demonstrated to be operable at temperatures as high as 600°C [1,2]. But most of tests have so far been conducted only in a probe-station test environment partly because chip level packaging technology for high temperature (500°C and beyond) devices is still being developed and systematically validated. One of the core technologies needed for successful high temperature device packaging is a high temperature operable die-attach scheme.

The thermo-mechanical characteristics of a die-attach assembly are critical to the reliability of a packaged device expected to operate over a wide temperature range. Thermal stress generated in the die-attach assembly due to material property mismatches, especially the coefficient of thermal expansion (CTE) mismatch, can cause degradation and failure of packaged devices. Typical failure modes include die and substrate cracking and fatigue of the attach material. Thermally induced stresses can also cause undesired device thermal response, irreproducibility of device operation, and drift of the output signal. For devices/systems including MEMS components, these issues are even more significant because MEMS operations rely directly on micro-mechanical displacement or deformation of the device. Therefore, thermo-mechanical failures caused by CTE mismatch between the die-attach materials are expected to be key packaging reliability and durability issues for high temperature applications.

For high temperature device/system packaging, the thermal mechanical reliability of the die-attach assembly needs to be addressed at two levels: 1) Mechanical damage of the die-attach structure resulting from thermal mechanical stress. 2) Thermal stress/strain effects on the mechanical operation of the devices. Failures at both levels are rooted in the thermal mechanical stress of the die-attach. In order to minimize the overall thermal stress of the die-attach structure, thereby optimizing the thermomechanical reliability of a die-attach assembly, it is essential to establish guidelines for material selection, structure design, and optimization of the attaching process. However, the equations governing thermal mechanical configuration (displacements, stresses, and strains) are so complicated [3] that the 3D boundary value problem of a die-attach with simple geometry is still very difficult to solve. Therefore, closed analytical solutions for these equations are only possible in limited cases [4,5]. References 4-5 have investigated the design of conventional electronic packaging die-attach assemblies using closed analytical solutions by assuming linear elastic material properties. Nonlinear material properties were also considered in a simplified model in reference 5. Temperature independent material properties were used to obtain all these analytical solutions. In this paper, considering the wide operation

temperature range and the low yield strength of gold thick-film that is used for die-attach, a temperature dependent non-linear elastic-plastic finite element analysis (FEA) was performed to simulate Au thick-film based SiC die-attach.

2. Au Thick-film Based Die-attach

The SiC test die having a thin-film metallization electrical contact on the backside was attached to a ceramic substrate using an optimized two-step Au thick-film process [6]. After dicing, the 1 mm x 1 mm SiC die was attached (bonded) to either an AlN or 96% Al_2O_3 substrate using Au thick-film material as shown in Figure 1. This Au thick-film die-attaching scheme resulted in a low resistance electrical interconnection to the backside of the die, which is necessary for packaging many devices with vertical topologies. An attached shottky diode using this die-attach scheme was previously electrically tested at 500°C for over 1000 hrs.

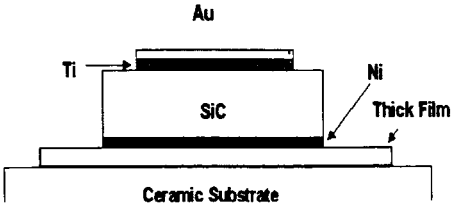

Figure 1: Au thick-film based die-attach. The ceramic substrate can be either alumina or aluminum nitride.

A thick film Au layer was screen-printed first on the substrate and cured at 850°C using a standard process. The SiC die was then attached to the cured thick film pattern using a subsequent Au thick film layer. Following the initial drying, the assembly was processed at a low final curing temperature of 600°C [6]. This optimized Au thick film die-attach process allows sufficient diffusion of inorganic binders towards the thick film/substrate interface resulting in strong binding to the ceramic substrate.

3. Thermal Mechanical Simulation of Die-attach

Material Properties

The basic mechanical properties of materials included in the die-attach, Au, SiC, AlN, and 96% Al_2O_3 and the temperature dependence of these material properties used in FEA simulation are listed in Table 1. The temperature dependence of AlN Young's modulus in a wide temperature range has not been reported, so it is extrapolated as a constant from the room temperature data. The Poisson's ratios of single crystal 4H-SiC and AlN have not been published, so they are estimated from those of other carbides and nitrides. The thermal and mechanical properties of 4H SiC are assumed to be isotropic.

Temperature dependent CTE data of substrate materials, AlN and Al_2O_3, are obtained from literature [7,8]. The CTE of SiC above 250°C was extrapolated from the data found between room temperature and 250°C. They are listed and plotted in Table 1 and Figure 2, respectively. We observed

Au material properties

Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	v
-15	14.04	11.09	0.44
20	14.24	10.99	0.44
105	14.71	10.83	0.44
205	15.23	10.59	0.44
305	15.75	10.28	0.44
405	16.29	9.92	0.44
505	16.89	9.51	0.44
605	17.58	9.03	0.44
705	18.38	8.50	0.44

AlN material properties

Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	v
-15	2.89	50.00	0.25
20	3.15	50.00	0.25
105	3.79	50.00	0.25
205		50.00	0.25
305	5.29	50.00	0.25
405		50.00	0.25
505	6.79	50.00	0.25
605		50.00	0.25
705	8.29	50.00	0.25

96% Alumina properties

Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	v
-15	4.27	44.00	0.21
20	4.57	44.00	0.21
105	5.29	43.58	0.21
205		43.06	0.21
305	6.99	42.51	0.21
405		41.93	0.21
505	8.69	41.34	0.21
605		40.74	0.21
705	10.4	40.13	0.21

SiC material properties

Temp (deg C)	CTE (xE-6/C)	E (xE6 psi)	v
-15	1.78	66.72	0.3
20	2.07	66.72	0.3
105	2.78	66.42	0.3
205		66.08	0.3
305	4.44	65.74	0.3
405		65.39	0.3
505	6.11	65.05	0.3
605		64.71	0.3
705	7.78	64.36	0.3

Table 1: Materials properties of Au, AlN, Al_2O_3, and SiC used for FEA [7, 8].

that material CTEs (mismatches) have the most significant effects on the die attach assembly thermal stress/strain.

The yield strength data of Au reported in the literature covers a wide range due to different pre-heat-treatments applied to the materials used for these experimental tests. We previously reported FEA results of Au thick-film based die-attach using the high yield strength (3000 psi) of quenched gold [9]. In this paper, we use low Au yield strength (250 psi) and temperature dependent plasticity of Au. These new results should be closer to stress/strain configurations of a Au thick-film based die-attach assembly sufficiently annealed (stored and operated) at elevated temperatures. Plasticity of gold thick-film is a primary factor responsible for thermally-induced stresses in a die-attach assembly. Only limited data of Au plasticity are available in published literature. Temperature dependent ultimate tensile strength of Au is listed in Table 2. 65% elongation was reported for annealed gold in Reference 5. Yield strength of gold is 250 psi [10] at room temperature and it is assumed to be temperature independent in our calculation. Based on these material properties and approximations and assumptions, temperature dependent plasticity behavior of gold was constructed as shown in Figure 3. Tangential modulus (or plasticity modulus) was assumed to be 28846, 28846, 26667, 21808, 14769 and 10385 psi at -15°C, 20°C, 105°C, 305°C, 505°C, and 705°C, respectively.

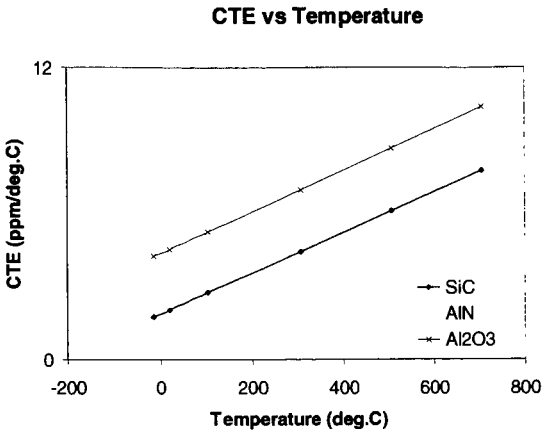

Figure 2: Temperature dependent CTE data of SiC and substrate materials [7, 8].

Temperature (°C)	Ultimate Tensile Strength (ksi)
20	19
200	16
400	13
600	7

Table 2: Ultimate Tensile Strength of annealed gold at various temperatures [10].

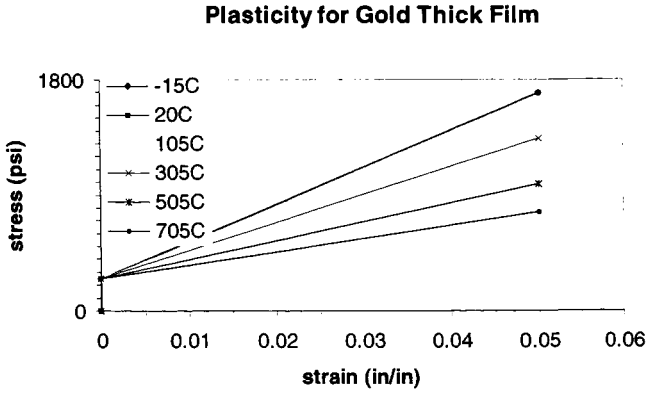

Figure 3: Temperature dependent plasticity of gold thick film. −15°C and 20°C data overlap with each other in the figure.

Finite Element Models

The baseline configuration of SiC die-attach is as follows: SiC die dimensions are 1 mm x 1 mm x 0.29 mm, the thickness of Au thick film is 20 μm, and the substrate is four times as large as the die and 0.635 mm thick. Both AlN and Al_2O_3 substrates were investigated in the stress/strain simulation. The die-attach was cured at 600°C then cooled down to room temperature. It was assumed that the die-attach assembly had relaxed at 600°C

before it was cooled down to the room temperature, and that the cooling process was so rapid that the stress/strain caused by temperature deviation from the relaxing temperature are accumulated without relaxation. Figure 4 shows a typical three-dimensional ANSYS finite element mesh for ¼ of the sample. Within the ANSYS FEA software tool, the Geometric Non-linearity Option was turned on and Automatic Time-step Process was employed with 10% of full temperature loading as initial time-step. A line search was used with Newton-Raphson iterative algorithm to improve and accelerate convergence. Initial time-step may be changed due to difficulties in convergence. For the purpose of good comparison in the parametric study, FEA non-linear parameters were set to be consistent.

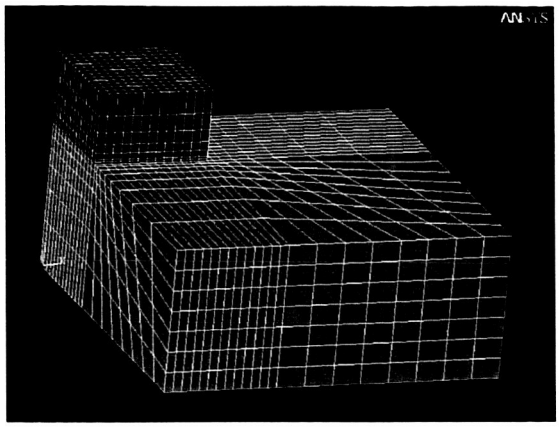

Figure 4: Three-dimensional finite element mesh of die-attach assembly (a quarter of the die-attach).

Results

Figures 5(a) and (b) show the contours of the first (tensile) component and the third (compressive) component of Principal Stress of a quarter of the SiC die in a SiC/Au/Al_2O_3 die-attach structure at room temperature with the relaxing temperature of 600°C. Figure 5(c) shows von-Mises Stress (the second deviatoric stress invariant) contour of the SiC die. Maximum tensile stress is the stress component that contributes most to die cracking. Von-Mises Stress is very often used to determine if yielding occurs. As indicated by Figure 5(a) (also Table 3), the maximum tensile stress in the SiC die is much lower then the tensile strength of SiC material, so die cracking is not expected. Maximum stresses are typically located at the bottom or the lower corner areas of the die. All these stress contours basically show that, vertically, stresses attenuate rapidly with the distance from the SiC/Au interface. This is understandable. The source of thermal stress of the die-attach structure is CTE mismatch at the bonding interfaces. With this picture of thermal stress distribution one can learn that flip-chip bonding would not be recommended for high temperature devices, especially MEMS devices, if the CTE mismatch is not well controlled, and that a thicker die (or a stress buffer layer of the same material) can significantly reduce the thermal stress at die top surface region. Figures 5 (d, e, and f) (also Table 3) show the contours of the first and the third components of Principal Stress and von-Mises Stress of the die-attach with an AlN substrate. Compared with those with an Al_2O_3 substrate, the maximums of all three stresses are reduced by a factor of two to three, so in terms of die stress AlN is a more suitable substrate material to package high temperature SiC devices.

Figures 6(a) and (b) show the contours of Equivalent Plastic Strain (EPS) in the Au thick-film layer of the die-attach with an Al_2O_3 substrate. The highest EPS in the Au layer are located at the area close to the corner. The interface between the SiC die and the gold thick-film at the corner is the most susceptible locations for crack initiation or delamination to occur due to thermal cycling fatigue. This may also imply that a smaller die-size/attaching-area may provide relatively better thermal mechanical reliability compared with larger dies. Figures 6 (e) and (f) show the EPS contours of the Au attaching layer of the die-attach with an AlN substrate. The

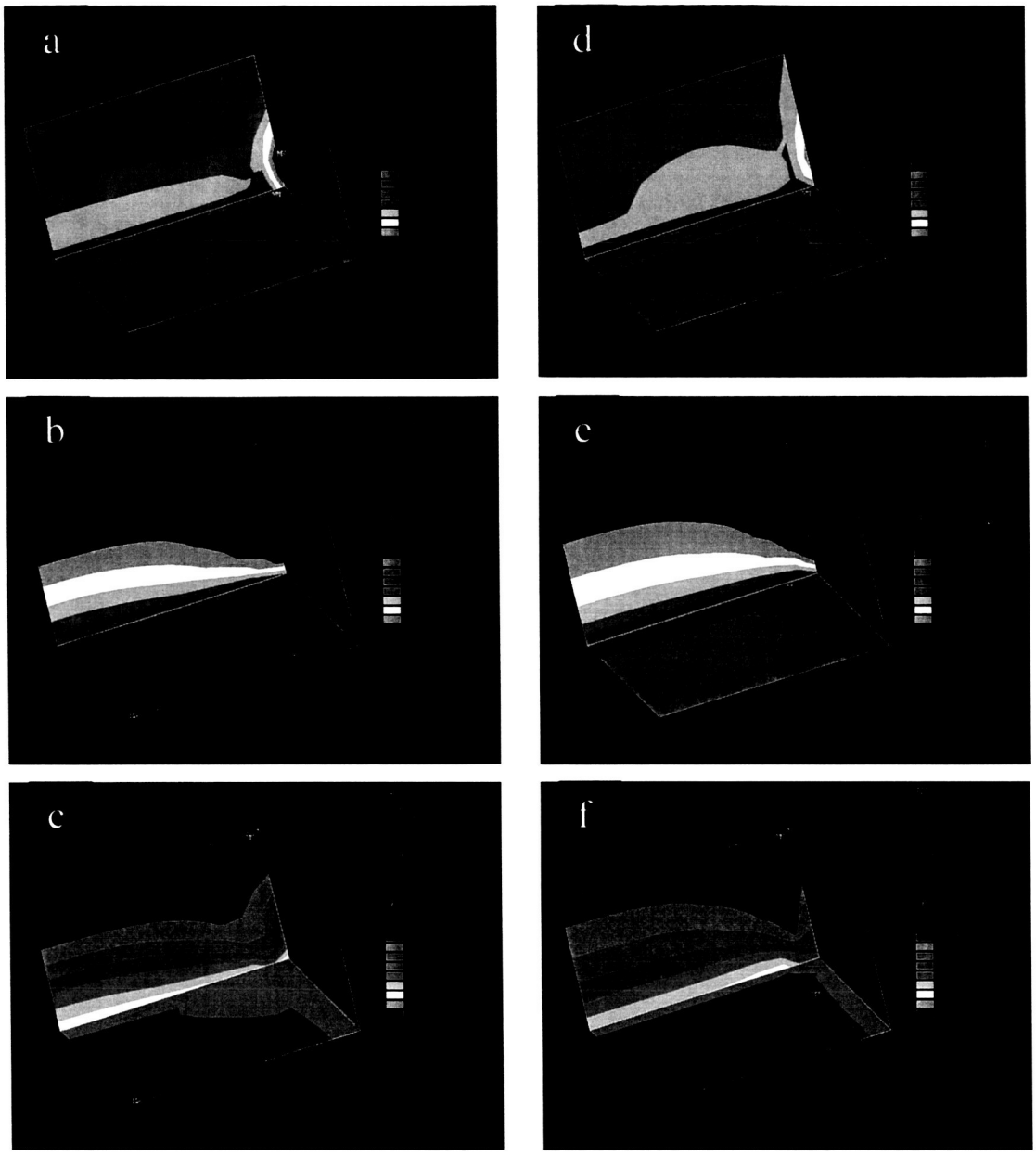

Figure 5: Thermal stress distribution contour in ¼ SiC die of baseline die-attach configuration at room temperature, the relaxing temperature is 600°C. (a) The first (tensile) component of Principal Stress of the SiC die an Al_2O_3 substrate. (b) The third (compressive) component of Principal Stress of the SiC die with an Al_2O_3 substrate. (c) Von-Mises stress distribution in SiC die with an Al_2O_3 substrate. (d – f) The distribution contours of the first and third components of Principal Stress and von-Mises stress in the SiC die with an AlN substrate.

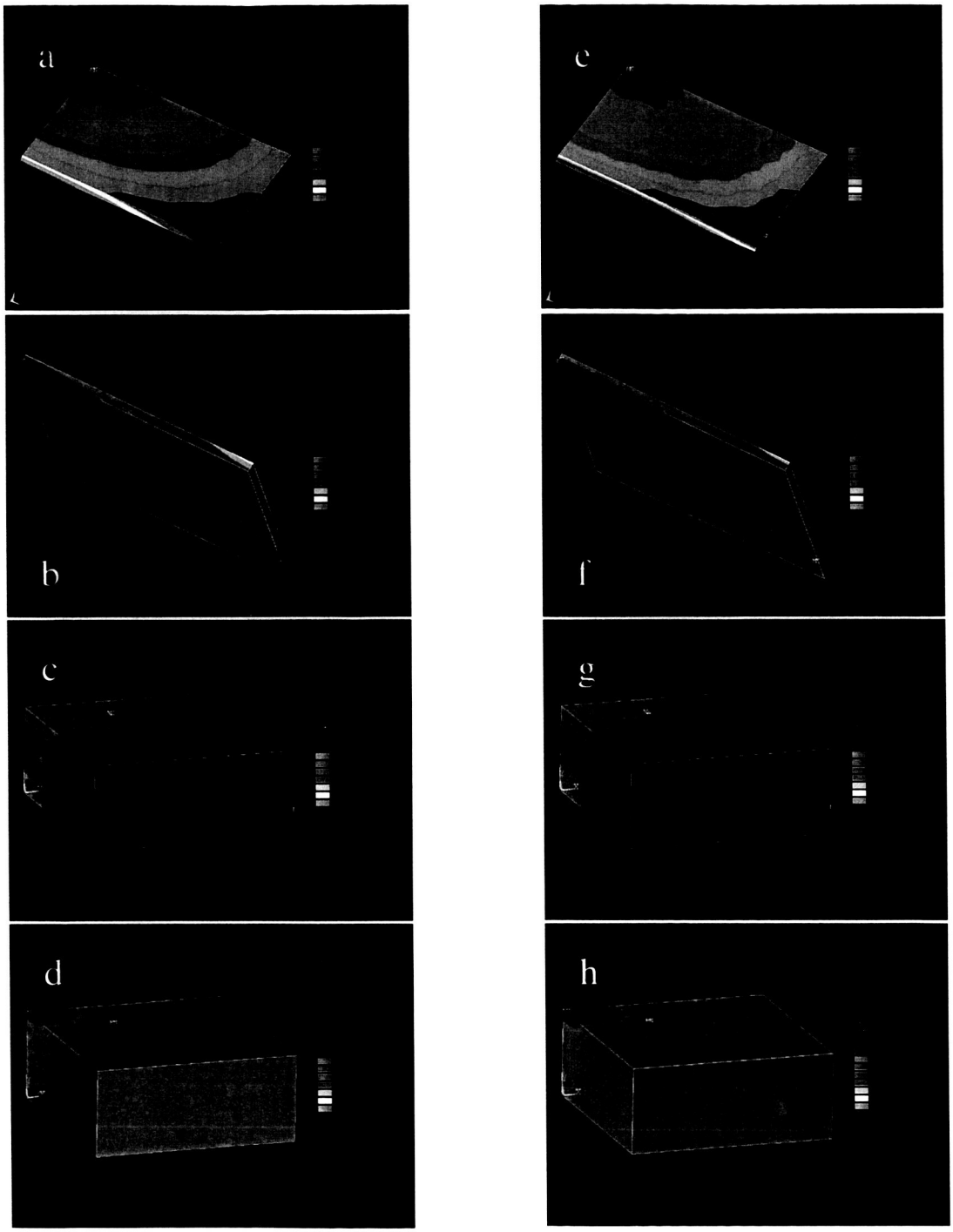

Figure 6: The contours of EPS in the Au die-attaching layer, and contours of Maximum Principal Stress and von-Mises Stress contours in substrates of ¼ model of the baseline die-attach configuration. (a) and (b) show the EPS distributions in the Au layer at interfaces of SiC/Au and Au/Al_2O_3. (c) and (d) show von-Mises and Maximum Principal Stresses in the Al_2O_3 substrate. (e) and (f) show the EPS distributions in the Au layer at interfaces of SiC/Au and Au/AlN. (g) and (h) show von-Mises and Maximum Principal Stresses in the AlN substrate.

96% Al2O3 Substrate		3D							
		Maximum Principal Stress (psi)				Maximum von Mises Stress (psi)		Maximum Equiv. Plastic Strain in Au Thick Film (in/in)	Coffin-Manson Fatigue Life of Au Thick-Film (comparison)
		SiC Chip (Tensile)	SiC Chip (Compress.)	Top of SiC Chip	Substrate	SiC Chip	Substrate		
Square SiC Die Sizes (mm)	0.5	323	-704	27	508	665	386	2.00E-02	2.12
	1	406	-1276	98	952	1402	861	3.13E-02	1.00
	2	428	-3386	287	2760	3496	2550	5.83E-02	0.36
	3	574	-6537	574	5414	6614	5232	2.35E-01	0.03

AlN Substrate		3D							
		Maximum Principal Stress (psi)				Maximum von Mises Stress (psi)		Maximum Equiv. Plastic Strain in Au Thick Film (in/in)	Coffin-Manson Fatigue Life of Au Thick-Film (comparison)
		SiC Chip (Tensile)	SiC Chip (Compress.)	Top of SiC Chip	Substrate	SiC Chip	Substrate		
Square SiC Die Sizes (mm)	0.5	387	-505	35	429	387	276	1.52E-02	3.34
	1	230	-681	21	477	563	417	1.89E-02	2.33
	2	210	-1545	65	1398	1611	1290	2.75E-02	1.25
	3	284	-2996	180	2756	3053	2656	3.76E-02	0.74

(a)

96% Al2O3 Substrate		3D							
		Maximum Principal Stress (psi)				Maximum von Mises Stress (psi)		Maximum Equiv. Plastic Strain in Au Thick Film (in/in)	Coffin-Manson Fatigue Life of Au Thick-Film (comparison)
		SiC Chip (Tensile)	SiC Chip (Compress.)	Top of SiC Chip	Substrate	SiC Chip	Substrate		
Au thick-film thickness (microns)	20	406	-1276	98	952	1402	861	3.13E-02	1.00
	30	260	-915	61	714	923	561	2.37E-02	1.59
	40	313	-818	41	596	706	434	2.01E-02	2.09
	50	399	-778	51	525	605	374	1.81E-02	2.49

AlN Substrate		3D							
		Maximum Principal Stress (psi)				Maximum von Mises Stress (psi)		Maximum Equiv. Plastic Strain in Au Thick Film (in/in)	Coffin-Manson Fatigue Life of Au Thick-Film (comparison)
		SiC Chip (Tensile)	SiC Chip (Compress.)	Top of SiC Chip	Substrate	SiC Chip	Substrate		
Au thick-film thickness (microns)	20	230	-681	21	477	563	417	1.89E-02	2.33
	30	259	-625	36	396	473	319	1.63E-02	2.96
	40	336	-611	53	375	482	286	1.52E-02	3.33
	50	457	-607	63	449	600	283	1.48E-02	3.51

(b)

96% Al2O3 Substrate	3D							
	Maximum Principal Stress (psi)				Maximum von Mises Stress (psi)		Maximum Equiv. Plastic Strain in Au Thick Film (in/in)	Coffin-Manson Fatigue Life of Au Thick-Film (comparison)
	SiC Chip (Tensile)	SiC Chip (Compress.)	Top of SiC Chip	Substrate	SiC Chip	Substrate		
600°C-RT	406	-1276	98	952	1402	861	3.13E-02	1.00
500°C-RT	352	-1129	85	836	1237	748	2.59E-02	1.38
400°C-RT	298	-982	73	721	1072	635	2.04E-02	2.05
300°C-RT	244	-833	60	605	906	523	1.49E-02	3.44

AlN Substrate	3D							
	Maximum Principal Stress (psi)				Maximum von Mises Stress (psi)		Maximum Equiv. Plastic Strain in Au Thick Film (in/in)	Coffin-Manson Fatigue Life of Au Thick-Film (comparison)
	SiC Chip (Tensile)	SiC Chip (Compress.)	Top of SiC Chip	Substrate	SiC Chip	Substrate		
600°C-RT	230	-681	21	477	563	417	1.89E-02	2.33
500°C-RT	203	-601	19	422	500	368	1.56E-02	3.21
400°C-RT	175	-523	17	366	438	320	1.23E-02	4.75
300°C-RT	147	-442	15	311	379	271	9.03E-03	7.96

(c)

Table 3: Three-dimensional non-linear FEA parametric study results: (a) Dependences of various stresses and strain on SiC die size. (b) Dependences of various stresses and strain on thickness of the Au attaching layer. (c) Dependences of various stresses and strain on environment/processing temperature. Both AlN substrate and Al_2O_3 substrate are included.

maximum EPS of the die-attach with an AlN substrate is lower than that with an Al_2O_3 substrate by a factor of 1.5, indicating that thermomechanical reliability of the die-attach with an AlN substrate is better

Figures 6 (c) and (d) show von-Mises Stress and the first component of Principal Stress in the Al_2O_3 substrate, respectively. Figure 6 (g) and (h) show von-Mises Stress and the first component of Principal Stress in the AlN substrate. Basically, the stresses attenuate vertically rapidly towards the bottom of the substrate. Both maximum von-Mises Stress and Maximum Principal Stress in the AlN substrate are lower than those in the Al_2O_3 substrate.

In order to explore the potential to optimize the thermomechanical reliability of the die-attach, single parametric dependences of stress/strain on die size, Au attaching layer thickness, and environment/processing temperature have been investigated in addition to the FEA simulation of baseline die-attach configuration. Die sizes of 0.5 mm x 0.5 mm, 1 mm x 1 mm, 2 mm x 2 mm, and 3 mm x 3 mm were used for die-size parametric investigation. The Au attaching layer thicknesses of 20, 30, 40, and 50 μm were also used for the parametric study. The temperature deviations from the relaxing temperature of 600°C, 500°C, 400°C, and 300°C, one of the process related parameters, were used for stress/strain analysis for the baseline die-attach configuration. Both Al_2O_3 and AlN substrates were considered in these single parameter (one at a time) studies. All the results are summarized in Table 3.

Table 3 (a) shows the dependences of various stresses/strain on SiC die size. The compressive Principal Stress in the die, the Maximum Principal Stress on die top surface, the Maximum Principal Stress in the substrate, von-Mises Stresses in both die and substrate, and EPS in the Au thick-film attaching layer all increase rapidly when the die size increasees from 0.5 mm x 0.5 mm to 3 mm x 3 mm, for both Al_2O_3 and AlN substrates. For the die-attach with an Al_2O_3 substrate, the relative Coffin-Mason fatigue life [3] determined by maximum thick-film EPS is reduced by a factor of 76 with respect to this die size increase. For the die-attach with an AlN substrate, the relative Coffin-Mason fatigue life determined by maximum thick-film EPS is reduced by a factor of 4.5 with respect to this die size increase.

Table 3 (b) shows the dependences of various die-attach stresses/strain on the thickness of Au thick-film attaching layer. Even though not all of the maximum stress/strain changes monotonically with respect to the increase of Au attaching layer thickness from 20 μm to 50 μm, the maximum EPS of the thick-film attaching layer reduces with the Au thickness increase. Therefore, Coffin-Mason Fatigue Life of Au thick-film is improved by the Au layer thickness increase for both Al_2O_3 and AlN substrates.

Besides the dependence of die-attach thermomechanical stress/strain on die size, substrate material, and the thickness of the attaching layer, the stress/strain also depends on the temperature deviation from the relaxing temperature, T_R, at which the structure is thermal-mechanically relaxed [3,11]. In order to assess the relaxing temperature effects on the thermal stress of the die-attach structure, the stress distribution of the die-attach at room temperature is simulated assuming that the structure is relaxed at various temperatures from 300 to 600°C. Table 3 (c) shows dependences of various stresses/strain on the temperature deviation from the relaxing temperature, from 600 to 300°C. As expected, all these stresses/strain reduce significantly in response to the decrease of temperature deviation from the relaxing temperature. The relative Coffin-Mason fatigue lifetime of the die-attach is improved at least by a factor of 3 with respect to this temperature drop. These results indicate that it would be optimal for the

stress/strain relaxing temperature to be set in the middle of the environment/operation temperature range.

4. Discussions and Summary

In all these FEA simulations, the boundary conditions at both SiC/Au-thick-film and Au-thick-film/substrate interfaces are assumed to be ideal bonds. This means that there is not any slip at either interface under shear stress. Mathematically, this assumption implies that all three displacements components are continuous at the two interfaces. We made this assumption since very limited interfacial thermomechanical properties of this material system are available. Further, it is difficult to either numerically model or experimentally measure these thermal and mechanical properties of interfaces, especially the temperature dependences of these interfacial thermomechanical properties. This assumption may have limited applicability for those relatively 'loosely' bonded interfaces, especially, at high temperatures.

The experimental measurement of 3D die-attach stress/strain distributions and detection of the thermal mechanical failure of the Au attaching layer sandwiched between a SiC die and a ceramic substrate can also be challenging, especially at elevated temperatures. Therefore, it is necessary to numerically validate the FEA results. First, the effect of mesh design/density on the numerical results was examined by changing the 3D FEA mesh. It was found that maximum von-Mises Stress of the SiC die changed only 0.5% after the mesh density was doubled. The stability of the stress/strain dependence upon the material properties, such as CTE of the ceramic substrate, was also examined by calculation of the stress/strain distribution with a small (virtual) upward and downward shifts of CTE – temperature curve of the substrate material. The simulation results were also stable with respect to the changes of substrate CTE.

In comparison with AlN substrate, 96% Al_2O_3 substrate has relatively higher CTEs (~ 4.6×10^{-6} / °C compare with ~3.2×10^{-6} / °C of AlN at room temperature). The FEA results basically indicate that using AlN substrate would result in an improvement of maximum von-Mises stress in SiC die by a factor of 0.40, an improvement of von-Mises stress in the substrate by a factor of 0.48, and an improvement of maximum EPS in Au thick-film layer by at least a factor of 0.6 for 1 mm x 1mm SiC. This dramatic improvement of thermal stress/strain corresponds to an improvement of fatigue lifetime of Au thick-film layer by a factor of 2.33 (assuming the power law exponent in Coffin-Mason model, C, is -0.4). So in terms of thermal mechanical reliability of a SiC die-attach, AlN is suggested for packaging SiC high temperature MEMS devices compared to 96% Al_2O_3 owing to the fact that the CTE of AlN is closer to that of SiC. Increasing the thickness of Au attaching layer would reduce the EPS in the Au layer, therefore, improve the reliability/life time of the die-attach assembly. Setting the stress relaxing temperature in the middle of the operation temperature range can significantly reduce the maximum stress of the die-attach caused by CTE mismatch even though it is not always physically possible for some die attaching materials.

References

1. P. G. Neudeck, G. M. Beheim, and C. Salupo, *600 °C Logic Gates Using Silicon Carbide JFET's*, 2000 Government Microcircuit Applications Conference, March 20-23, Anaheim, CA. An earlier review article: R. F. Davis, G. Kelner, M. Shur, J. W. Palmour, and J. A. Edmond, *Thin Film Deposition and Microelectronic and Optoelectronic Device Fabrication and Characyterization in Monocrystalline Alpha and Beta Silicon Carbide*, Special Issue on Large Bandgap Electronic Materials and Components, Proceedings of the IEEE, Vol.79, 5, 1991.

2. G. W. Hunter, P. G. Neudeck, G. C. Fralick et al, *SiC-Based Gas Sensors Development*, Proceedings of International Conference on SiC and Related Materials. Raleigh, North Carolina, Oct. 10-15, 1999.

3. J. Lau, C. P. Wong, J. L. Price, W. Nakayama, *Electronic Packaging – Design, Materials, Process, and Reliability*, McGraw-Hill, 1998.

4. J. M. Hu, M. Pecht, and A. Dasgupta, *Design of Reliable Die Attach,* The International Journal of Microcircuits and Electronic Packaging, Volume 16, Number 1, First Quarter 1993.

5. E. Suhir, *Die Attachment Design and Its Influence on Thermal Stresses in the Die and the Attachment.* Proceedings of 37th Electronic Components Conference, 508-517, 1987.

6. L.-Yu Chen, G. W. Hunter, and P. G. Neudeck, *Silicon Carbide Die Attach Scheme for 500 °C Operation,* MRS 2000 Spring Meeting Proceedings-Wide-Bandgap Electronic Devices (Symposium T), San Francisco, CA, Apr. 10 - 14, 2000.

7. H. K. Charles, and G.V. Clatterbaugh, *Packaging Considerations for High Temperature Operation*, Proc. of 2nd International High Temperature Electronics Conference, Charlotte, NC, pp.ix-3, 1994.

8. F. P. McCluskey, R. R. Grzybowski, and T. Podlesak, *High Temperature Electronics*, CRC press, 1996.

9. L.-Yu Chen, R. S. Okojie, P. G. Neudeck, G. W. Hunter, and S.-T. Lin, *Material System for Packaging 500°C SiC Microsystems*, Materials Research Society Symposium Proceedings Vol. 682E, 2001.

10. J. A. King, *Materials Handbook for Hybrid Microelectronics*, 1988.

11. G. D. Giacomo, *Reliability of Electronic Packaginges and Semiconductor Devices*, McGraw-Hill, 1997.

Acknowledgement

Authors want to thank Dr. Lawrence G. Matus, Dr. Gary W. Hunter, Dr. Philip G. Neudeck, and Dr. Jih-fen Lei for their contributions. This work is currently supported by NASA Electronic Parts and Packaging (NEPP) program and NASA Glennan Microsystem Initiative (GMI).