A Step Response Based Mixed-Signal BIST Approach

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Abstract

A new Mixed-Signal Built-in Self-test approach that is based upon the step response of a reconfigurable (or multifunction) analog block is presented in this paper. The technique requires the overlapping step response of the Circuit Under Test (CUT) for two circuit configurations. Each configuration can be realized by changing the topology of the CUT or by sampling two CUT nodes with differing step responses. The technique can effectively detect both soft and hard faults and does not require an analog-to-digital converter (ADC) and/or digital-to-analog converter(DAC). It also does not require any precision voltage sources or comparators. The approach does not require any additional analog circuits to realize the test signal generator and a two input analog multiplexer for CUT test node sampling. The paper is concluded with the application of the proposed approach to a circuit found in the work of Epstein et al [1] and two ITC'97 analog benchmark circuits.

1. Introduction

The push for the development of Built-In Self-Tests (BIST) for mixed-signal integrated circuits has been driven by the high cost associated with the production and field testing of complex mixed-signal VLSI circuits. A number of effective digital BIST techniques are currently available for implementing on-chip tests for the digital blocks of a mixed-signal circuit [2]. Unfortunately, this is not true for the analog blocks and the analog-digital interfaces between those blocks and digital circuits. Most of the current research in this area is primarily focused upon techniques to test these blocks and interfaces. Current analog/mixed-signal BIST techniques can be divided into two broad classes: (i) functional and (ii) fault-based [3] . In the functional approaches the analog block under test is driven with sinusoidal or multitone stimuli and measurements are obtained at the output or selected nodes [3,4,5]. This measurement data is subsequently processed with the DSP-core, in the ADC-DSP-DAC structure to detect system faults. Generally these techniques are based upon analog specifications like signal-to-noise ratio (SNR), frequency response or intermodulation distortion. The primary advantage of functional schemes is that they can detect both soft (or parameteric) and hard faults [3]. These techniques are often considered to be the most effective BIST approach because of this feature. Analog BIST techniques that employ fault coverage and fault detection base upon fault models of devices within the analog block or sub-blocks are called fault-based techniques. The major advantage of these techniques is that they are typically implemented with nonconventional stimuli or signatures that can easily be generated and processed on-chip with digital techniques. However, these techniques can only effectively detect hard or catastrophic faults. The overhead associated with the majority of proposed functional techniques is prohibitive if the mixed-signal system does not have the ADC-DSP-DAC structure. This is because the tests used in these BIST techniques are essentially based upon network

frequency spectrum analysis. They are generally implemented with the Fast-Fourier Transform (FFT), an $O(n \log_2 n)$ algorithm [6]. A relatively complex DSP-core is required for an algorithm with this time (and associated memory) complexity to implement effective functional tests (i.e. tests with high enough spectral resolution to detect faults in the analog subsystem). In addition, generally functional tests that are realized with the DAC-ADC loop-back structure also require analog-to-digital converters (ADC) and digital-to-analog converters (DAC) with more bits of resolution than is required for the original application [5].

A new functional analog BIST approach that does not require a ADC, DAC or complex DSP-core is presented in this paper. The technique is based upon a nonconventional stimuli, i.e. a step function, but can detect both soft (or parameteric) and hard faults. The technique only requires n modified buffers, n registers (where n corresponds to the number of unknown parameters in the CUT) a digital counter and a simple single-bit processor core (or DSP); this processor can be realized by reconfiguring on-chip digital circuits. A single-bit core can be used to compute the parameters in the proposed technique because digital circuits are typically must faster than analog circuits and only $n^2 + n$ evaluations are required per iteration of the Newton algorithm. The proposed technique is based upon the step response of the analog block under test (CUT).

The organization of the paper is as follows: the mathematical basis of the step response based BIST approach is presented in section 2. The digital circuit that acquires the timing information from the two CUT sampled nodes is described in section 3. Examples of the application of the proposed techniques is presented in section 4.Our conclusions are presented in section 5.

2. Problem Formulation

The proposed Mixed-Signal BIST techniques is essentially a parameter extraction or system identification approach that is based upon the step response of a reconfigurable or multi-output analog circuit. The Newton-Ralphson method is used to find the parameters of the CUT. The component functions used to construct the Jacobian matrix are functions of the CUT output voltage crossover point for two circuit configurations (i.e. the point in time where the CUT output exceeds a threshold or switching voltage), where the crossover point is determined by the threshold voltage of the logic gate that is driven by the CUT during BIST diagnosis.

Our primary objective in this section is to present the mathematical basis of this approach. The most effective way to do this is to apply the proposed approach to a simple circuit. The circuit selected for this demonstration, a passive first order highpass filter, is shown in Fig. 1. The transfer function of this filter is,

$$H(s) = \frac{s + \alpha p}{s + p} \tag{1}$$

its pole and DC gain are,

$$p = -\frac{(R_1 + R_2)}{R_1 R_2 C} \text{ and } \alpha = \frac{R_2}{R_1 + R_2} \tag{2}$$

respectively. These relationships, i.e. equation (1) and (2), are determined by the circuit topology and the

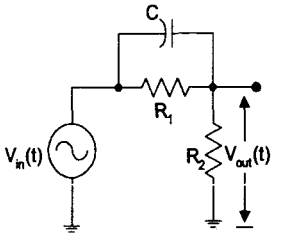

Figure 17 1st Order High-Pass Filter

value of the circuit elements. We assume that circuit faults do not change the circuit structure therefore, the only parameters required to identify the system defined by equation (1) is p and α. The time-domain output $V_{out}(t)$ of this filter for a step function with a peak value of V_{DD}, i.e.

$V_{in}(t) = V_{DD}u(t)$ is,

$$V_{out}(t) = V_{DD}[\alpha + (1-\alpha)e^{-\beta t}]u(t) \tag{3}$$

if we let $\beta = -p$. Now lets change the circuit topology as shown in Fig. 2.

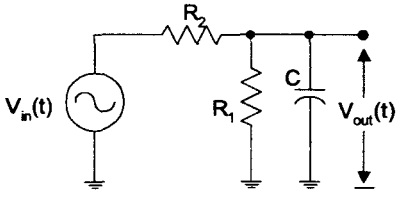

Figure 18 1st Order Low-Pass Filter

The step response of this circuit is,

$$V_{out}(t) = V_{DD}(1-\alpha)[1 - e^{-\beta t}]u(t). \tag{4}$$

If we equate the output voltage of the two circuit configurations, i.e. eq (3) and (4), and rewrite that expression such that it equals zero we derive the following function in terms of α and β,

$$f(\alpha,\beta,t_1,t_2) = V_{DD}\{2\alpha - 1 + (1 - \alpha)(e^{-\beta t_1} + e^{-\beta t_2})\} . \tag{5}$$

The time t_1 and t_2 in eq (5), corresponds to the point in time where the output voltage of the circuit in Fig. 1 equals the output voltage of the circuit in Fig. 2. These time points, hereupon referred to as crossover points, correspond to the time when the output voltage of both circuit configurations equals a reference voltage V_{ref}. The Newton method is used to find the above two parameters, i.e α and β. This method requires the following two partial derivatives,

$$\frac{\partial f(\alpha,\beta,t1,t2)}{\partial \alpha} = V_{DD}[2 - (e^{-\beta t_1} + e^{-\beta t_2})]$$

$$\frac{\partial f(\alpha,\beta,t1,t2)}{\partial \beta} = - V_{DD}(1 - \alpha)[t_1 e^{-\beta t_1} + t_2 e^{-\beta t_2}] \tag{6}$$

and two set of crossover points are to realize the Jacobian matrix. These two sets of points require two corresponding reference voltages V_{Ref1} and V_{Ref2} that correspond to the output voltage of the above circuits (i.e. configuration 1 and configuration 2 respectively) at (t_1, t_2) and (t_3, t_4) respectively. These expressions, i.e. eq. (6), are plotted as a function of the reference voltage in Fig. 3 (for V_{DD} = 5.0V, α = 0.3333 and β = 15.0). The partial derivative of $f(\alpha,\beta,t_1,t_2)$ with respect to β is symmetrical about the reference voltage V_{ref} at 2.5 volts. Therefore the Jacobian matrix will be non-singular as long as the two reference voltages V_{Ref1} and V_{Ref2} are not set to equal values above and below this symmetrical points, e.g. at 2.0 and 3.0 which both are 0.5 volt from 2.5 voltages. The Jacobian matrix is,

$$J(\bar{x}) = \begin{bmatrix} \dfrac{\partial f(\alpha,\beta,t1,t2)}{\partial \alpha} & \dfrac{\partial f(\alpha,\beta,t1,t2)}{\partial \beta} \\ \dfrac{\partial f(\alpha,\beta,t3,t4)}{\partial \alpha} & \dfrac{\partial f(\alpha,\beta,t3,t4)}{\partial \beta} \end{bmatrix}. \tag{7}$$

We obtain the following recursive formula,

$$\overline{x_{n+1}} = \overline{x_n} - \left[J(\overline{x_n})^{-1}\right] f(\overline{x_n}) \tag{8}$$

where,

$$f\left(\overline{x_n}\right) = \begin{bmatrix} f(\alpha,\beta,t1,t2) \\ f(\alpha,\beta,t3,t4) \end{bmatrix} \quad \overline{x_n} = \begin{bmatrix} \alpha \\ \beta \end{bmatrix}.$$

Now consider the above circuits, i.e. Fig. 1 and Fig. 2, for the following component values, R_1 = 2KΩ, R_2 = 1KΩ, V_{DD} = 5.0 volts, and C = 100μf. Then using eq. (3) we find that α = 1/3 and that β = 15.0. The step response of Fig. 1 and Fig. 2 for these values is shown in Fig. 4. If we let the reference voltages V_{Ref1} and V_{Ref2} equal 2.5 volts and 2.0 volts respectively, the crossover points are, $t_1 = t_2$ = 92.41962 mSec , t_3 = 61.08605 mSec, and t_4 = 153.5057 mSec. Now using the above crossover points and an initial value of α = 0.1 and β = 25.0 the Newton method converges rapidly (quadratically usually [7]) to the correct circuit parameter

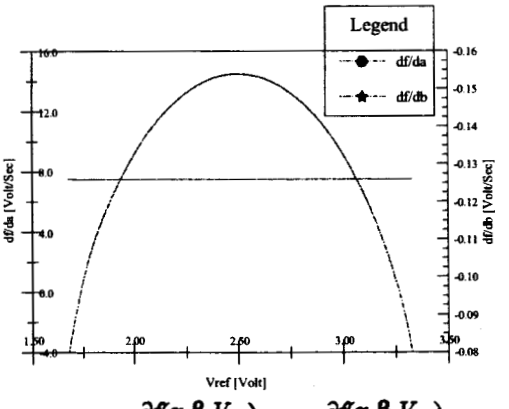

Figure 19 Plot of $\dfrac{\partial f(\alpha,\beta,V_{ref})}{\partial \alpha}$ *and* $\dfrac{\partial f(\alpha,\beta,V_{ref})}{\partial \beta}$ with respect to the reference voltage V_{Ref}

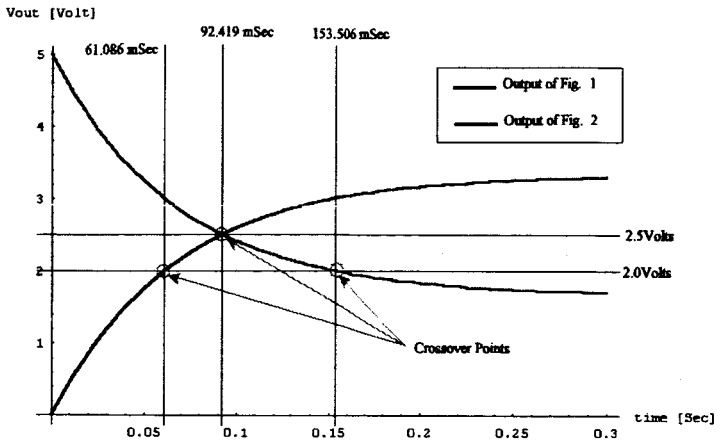

Figure 20 Output Voltage of above circuits

values as shown in Table 1. The parameter values at the 7th

Table 1: Convergence Behavior of BIST Approach

Iteration	α	β	Error
0	.1000000	25.00000	.10000E+04
1	.2771510	6.68585	.18315E+02
2	.5621070	14.96517	.82842E+01
3	.3333337	15.01813	.23482E+00
4	.3333334	14.99999	.18145E-01
5	.3333333	15.00000	.10830E-04
6	.3333333	15.00000	.23894E-11
7	.3333333	15.00000	.00000E+00

iteration corresponds to the value of α and β in eq (4) for the above component values. The transfer function of the highpass filter shown in Fig. 1 can then be computed as follows,

$$H(s) = \frac{s + \alpha\beta}{s + \beta} = \frac{s + 5}{s + 15} . \qquad (9)$$

Although the reference voltages V_{Ref1} and V_{Ref2} in this example were set, their values in general are not required for the proposed approach. The only requirement is that they be set to two distinct values that insure that the Jacobian matrix is non-singular. Therefore, precision voltage references and comparators are not required to implement the proposed technique.

3. Test Circuit

Digital techniques are used to excite and acquire the response of the analog CUT. The input waveform, i.e. CUT excitation, is generated with a digital circuit with sufficient drive to ensure that the input step function rising edge is shape enough to approximate an idea function. An additional requirement for this source is that it does not overdrive the CUT over the output signal range of the digital source, i.e. approximately from 0 to V_{DD}. The crossover points required by the proposed BIST technique are determined by comparing both CUT configuration outputs to some predefined reference voltages. The accuracy of the

$$V_{threshold} = \frac{V_{DD} - |V_{TP}| + \sqrt{K_R}\cdot V_{TN}}{1 + \sqrt{K_R}} \tag{10}$$

reference voltages, i.e. V_{Ref1} and V_{Ref2}, in the proposed approach is not important. Therefore the threshold voltage of a digital CMOS buffer or inverter can be used to implement the comparators in the analog-digital BIST interface. The threshold voltage of a CMOS buffer/inverter is determined by the ratio K_R of the transconductance parameter of the n-channel and p-channel devices. The threshold voltage of the buffer decreases with increase K_R as shown in eq. (10). Hence a buffer with differing where,

$$K_R = \frac{W_N \cdot k_n'}{W_P \cdot k_p'}.$$

K_R ratios can be used to realize the comparators. Although the threshold voltage of these comparators is not well controlled, due process and temperature variations, it can be used in the above analog BIST technique because it only requires that the reference voltages be distinct and relatively stable. The following circuit can be used to realized a test circuit for a CUT that require three threshold voltages. The content of the counter is loaded in the corresponding register *REG* when $V_{out}(t)$, i.e the output of the CUT, exceed or falls below the threshold voltage of the buffers in Fig. 5. The asynchronous edge detectors in this circuit products a pulse that is at least one clock cycle in duration whenever a transitions appears on the output of the associated buffer. This loads the corresponding register.

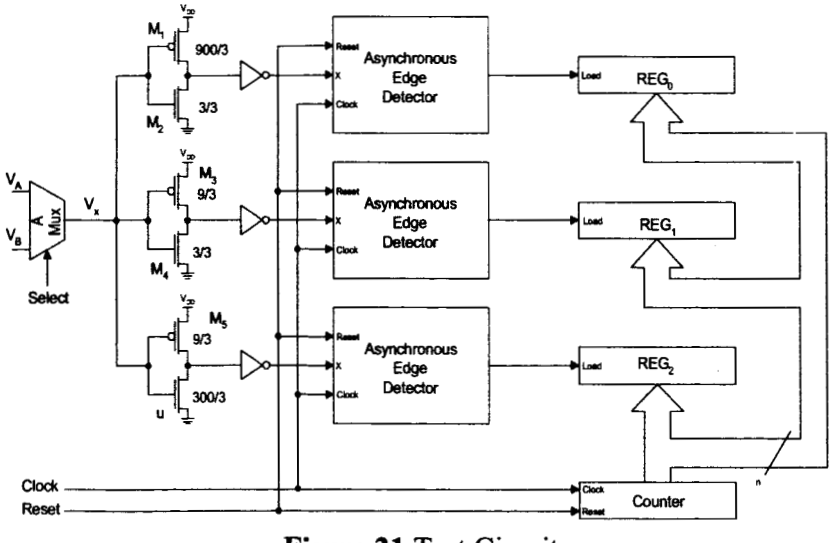

Figure 21 Test Circuit

4. Example

In this section we examine the application of the proposed approach to an Elliptical filter found in [1] and two ITC'97 analog benchmark circuits, i.e. the Continuous-time State-variable filter, and the Leap-frog filter described in [7]. Although, the proposed approach can extract parameters associated with the operational amplifiers in the benchmark circuits we omit these features here, i.e. operational amplifier poles, zeros, offset voltage, nonlinearity , etc., for simplicity .We first consider the Continuous-time State-variable filter in [7] with an analog multiplexer that selects the filter output that is processed by the digital test circuit (i.e. filter outputs BPO and LPO). The transfer functions of the selected nodes are,

$$H_1(s) = \frac{V_{out_1}(s)}{V_{in}(s)} = k_1 \cdot \frac{s^2}{\left(s + \alpha + \sqrt{\alpha^2 - \beta}\right)\left(s + \alpha - \sqrt{\alpha^2 - \beta}\right)}$$

$$H_3(s) = \frac{V_{out_3}(s)}{V_{in}(s)} = k_1 \cdot k_2 \cdot \frac{1}{\left(s + \alpha + \sqrt{\alpha^2 - \beta}\right)\left(s + \alpha - \sqrt{\alpha^2 - \beta}\right)} \qquad (11).$$

Therefore the transfer functions of the filter in Fig. 7 can be determine if the following four parameters α, β, K_1 and K_2 are known. The step response at the sampled nodes can take three forms because the poles pair in eq. (11) can appear as: two complex poles, two real but distinct poles, or two real identical poles. The step response of this filter at outputs $V_{out1}(t)$ and $V_{out2}(t)$ in terms of the above circuit parameters is

$$V_{out_1}(t) = \begin{cases} V_{DD}K_1 e^{-\alpha t}\left[Cos\left[\left(\sqrt{\beta-\alpha^2}\right)t\right] - \frac{\alpha}{\sqrt{\beta-\alpha^2}} Sin\left[\left(\sqrt{\beta-\alpha^2}\right)t\right]\right] u(t), & \beta > \alpha^2 \\ V_{DD}K_1 e^{-\alpha t}(1 - \alpha t)\, u(t), & \beta = \alpha^2 \\ V_{DD}K_1 e^{-\alpha t}\left[Cosh\left[\left(\sqrt{\alpha^2-\beta}\right)t\right] - \frac{\alpha}{\sqrt{\alpha^2-\beta}} Sinh\left[\left(\sqrt{\alpha^2-\beta}\right)t\right]\right] u(t), & \beta < \alpha^2 \end{cases}$$

$$V_{out_3}(t) = \begin{cases} \frac{V_{DD}K_1K_2}{\beta}\left\{1 - e^{-\alpha t}\left[Cos\left[\left(\sqrt{\beta-\alpha^2}\right)t\right] + \frac{\alpha}{\sqrt{\beta-\alpha^2}} Sin\left[\left(\sqrt{\beta-\alpha^2}\right)t\right]\right]\right\} u(t), & \beta > \alpha^2 \\ \frac{V_{DD}K_1K_2}{\beta}\left[1 - e^{-\alpha t}(1 + \alpha t)\right] u(t), & \beta = \alpha^2 \\ \frac{V_{DD}K_1K_2}{\beta}\left\{1 - e^{-\alpha t}\left[Cosh\left[\left(\sqrt{\alpha^2-\beta}\right)t\right] + \frac{\alpha}{\sqrt{\alpha^2-\beta}} Sinh\left[\left(\sqrt{\alpha^2-\beta}\right)t\right]\right]\right\} u(t), & \beta < \alpha^2 \end{cases} \qquad (12)$$

The step response of this filter for both outputs is shown in Fig.6 for the following circuit nominal component values (i.e. for $\beta > \alpha^2$): R_1 - R_5 = 10KΩ, R_6 = 3K, R_7 = 7K and C_1 - C_2 = 20nF. The step response of both outputs, i.e. $V_{out1}(t)$ and $V_{out3}(t)$, overlap over the 0.0 to -5.0 volts range. Therefore these outputs can be equated at any voltage within this range. The reference voltages should be set

to values in this range. The component function for this circuit (for $\beta > \alpha^2$) is,

$$g(\alpha,\beta,k_2,t_1,t_2) = e^{-\alpha t_1}\left[Cos(\rho t_1) - \frac{\alpha}{\rho}Sin(\rho t_1)\right] - \frac{K_2}{\beta}\left\{1 - e^{-\alpha t_2}\left[Cos(\rho t_2) + \frac{\alpha}{\rho}Sin(\rho t_2)\right]\right\} \quad (13)$$

where,

$$\rho = \sqrt{\beta - \alpha^2}.$$

This expression contains three unknowns, i.e α, β and K_2 and is insensitive to the step input voltage peak voltage, i.e V_{DD}. Three reference voltages are required to construct the Jacobian matrix. The following values where selected for these reference voltages: $V_{ref1} = -1.0V$, $V_{ref2} = -2.0V$ and $V_{ref3} = -3.0V$. The six crossover points found for these reference voltages and the above component values are: $t_1 = 0.23898$ msec, $t_2 = 0.13311$ msec, $t_3 = 0.19139$ msec, $t_4 = 0.19509$ msec, $t_5 = 0.14157$ msec and $t_6 = 0.24780$ msec respectively. An example of the convergence behavior for proposed approach for the above circuit (for $\alpha = 750$, $\beta = 4943.43$ and $K_2 = 2.5\times10^7$ and reference voltages $V_{ref1} = -1.0V$, $V_{ref2} = -2.0V$ and $V_{ref3} = -3.0V$) is shown in Table 2 for the following initial values, $\alpha = 1012.5$, $\beta = 4449.087$, and $K_2 = 15.0\times10^6$. The fourth parameter ,i.e. K_1,can be found using a similar approach.The Newton algorithm

Table 2
Convergence behavior Newton Algorithm

Iter.	α	β	K_2	Error
0	1012.500	4449.087	.1500000E+08	1000.000
1	745.2750	4990.371	.2516620E+08	.1016620E+08
2	750.1977	4943.415	.2499934E+08	166859.4
3	750.0017	4943.429	.2500000E+08	657.0998
4	749.9977	4943.432	.2500000E+08	9.471197
5	749.9983	4943.432	.2500001E+08	.2879982

converged for the two soft fault cases sited in [8], i.e. nominal plus 6σ case and nominal minus 6σ case.

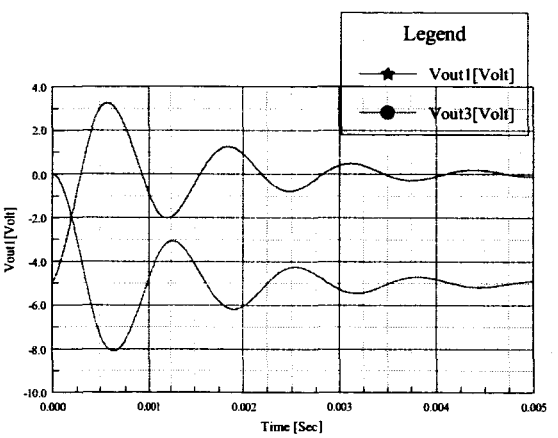

Figure 22 Step Response of a Continuous-Time State-Variable Filter

Similar results were found for the Leap-frog filter in [8] and the Elliptical filter in [1]. The number of

unknown parameters associated with each of these filters and the iteration count required to reduce the Newton loop error function to 10^{-6} or reach the loop limit, i.e. 25, is shown in Table 3.

Table 3:Proposed BIST Approach Convergence Behavior for Benchmark Circuits

Circuit	Soft Fault	No. Parameters	No. Iteration	Error
Continuous-time State-variable filter [8]	-6σ	4	25	0.017
	+6σ	4	25	0.28
Leap-frog filter [8]	-6σ	9	19	10^{-7}
	+6σ	9	25	0.1659
Elliptical filter [1]	-6σ	14	25	0.001
	+6σ	14	25	0.21

5. Conclusion

We presented a new mixed-signal BIST approach that is based upon the step response of the analog CUT. Although, this technique posses many of the characteristics of fault based BIST techniques such as using non-conventional stimuli and CUT output measurements it is also like functional BIST techniques in the sense that it can be used to detect both hard and soft faults. The CUT excitation circuit can be realized with digital techniques because of the above property and the time domain based realization of the proposed BIST technique. The test measurements are acquired with a digital circuit, and processed with a finite-state machine to construction and solve the matrix **J(x)** using to implement the Newton-Raphson equations. The proposed technique is effective under process drift because of these models. The technique is also insensitive to the initial state of the CUT and the switching voltage of the circuit driven by the CUT. The number of reference voltages required to implement this approach must equals the number of circuit unknowns. These references do not need to be known or precise. The CUT needs to be reconfigurable or needs to contain multiple outputs. The output of each configuration or output for the multiple output case must overlap to construct the component functions.

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