A NOVEL METAL-FERROELECTRIC-SEMICONDUCTOR FIELD-EFFECT TRANSISTOR MEMORY CELL DESIGN

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ABSTRACT

The use of a Metal-Ferroelectric-Semiconductor Field-Effect Transistor (MFSFET) in a resistive-load SRAM memory cell has been investigated. A typical two-transistor resistive-load SRAM memory cell architecture is modified by replacing one of the NMOS transistors with an n-channel MFSFET. The gate of the MFSFET is connected to a polling voltage pulse instead of the other NMOS transistor drain. The polling voltage pulses are of sufficient magnitude to saturate the ferroelectric gate material and force the MFSFET into a particular logic state. The memory cell circuit is further modified by the addition of a PMOS transistor and a load resistor in order to improve the retention characteristics of the memory cell. The retention characteristics of both the "1" and "0" logic states are simulated. The simulations show that the MFSFET memory cell design can maintain both the "1" and "0" logic states for a long period of time.

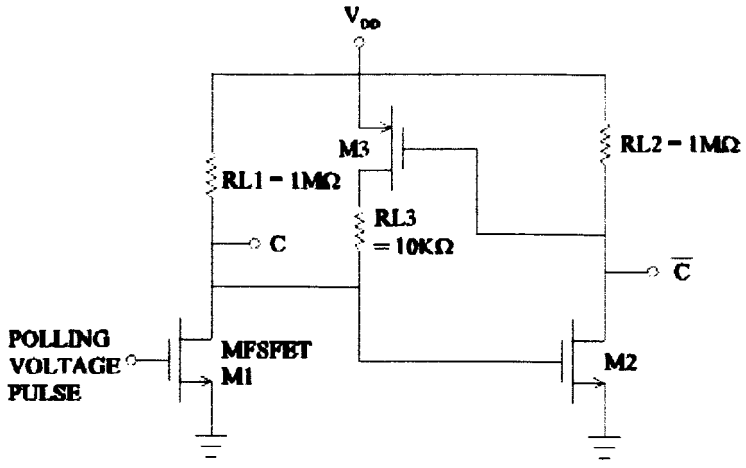

Figure 1: Modified MFSFET Resistive-Load SRAM Memory Cell

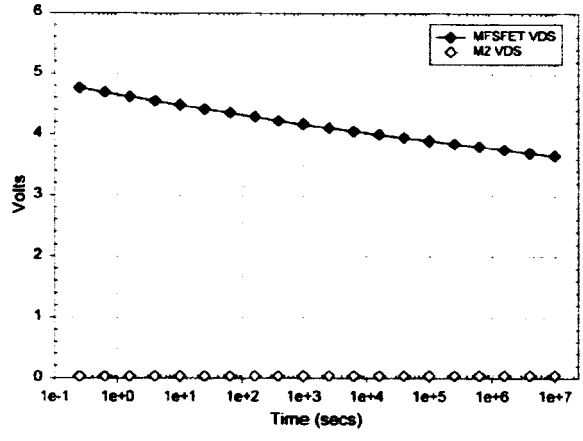

Figure 2: MFSFET Memory Cell "1" Retention

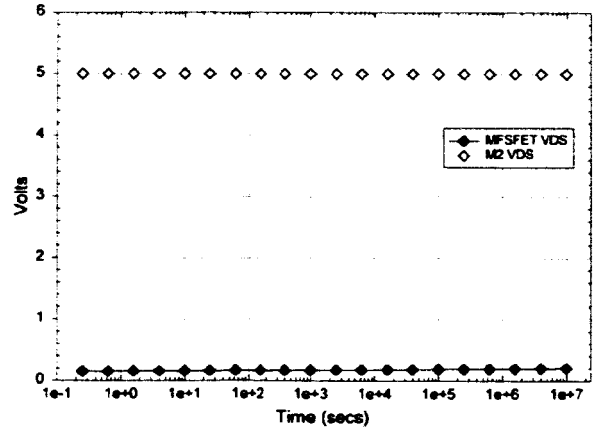

Figure 3: MFSFET Memory Cell "0" Retention