Progress in Low-power Digital Microwave Radiometer Technologies

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Abstract— **Three component technologies were combined into a digital correlation microwave radiometer. The radiometer comprises a dual-channel X-band superheterodyne receiver, low-power high-speed cross-correlator (HSCC), three-level ADCs, and a correlated noise source (CNS). The HSCC dissipates 10 mW and operates at 500 MHz clock speed. The ADCs are implemented using ECL components and dissipate more power than desired. Thus, a low-power ADC development is underway. The new ADCs are predicted to dissipated less than 200 mW and operate at 1 GSps with 1.5 GHz of input bandwidth. The CNS provides different input correlation values for calibration of the radiometer. The correlation channel had a null offset of 0.0008. Test results indicate that the correlation channel can be calibrated with 0.09% error in gain.**

I. Introduction

Digital microwave radiometry for Earth observation, like radiometry in general, finds its roots in radio astronomy. In 1968 in a letter to the *IEEE Proceedings*, Weinreb proposed a "digital radiometer" to measure a signal's spectrum [1]. The IF signal was quantized by a 1-bit analog-to-digital converter (ADC) or comparator. The resulting digital signal was processed with a tap-delay line, 1-bit multipliers (exclusive-or gates), and counters. This architecture was readily implemented with discrete logic operating at clock speeds of 1-10 MHz. Soon after, in the 1970's, the Very Large Array telescope was developed and a 3-level digital correlator system implemented [2]. Three-level multipliers are a mere handful of NAND gates and the small increase in complexity results in a significant increase in detector sensitivity. Nonetheless, the VLA is, as its name declares, a large array and its correlator fills part of a building. Like Weinreb's original idea, the 3-level correlator relies upon the signal's Gaussian characteristics, a technique which has proved to be effective. These simple and useful approaches have influenced digital radiometers for more than three decades.

With today's technology, more options are available for the real-time processing of digital signals. Field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and even general microprocessors can be programmed to filter, analyze, and transform complex signals. These devices, however, are through-put limited, especially when considering components suitable for the space environment. Today, clock rates are limited to ~100 MHz, which is usable for bandwidths of 25-50 MHz. An advantage of using more complex devices is the availability of higher-resolution samples, of 4, 8, or even 10 or 12 bits, which may be important for RFI mitigation. Clock rate limitations can be overcome by pipelining or parallelizing processors. A main disadvantage of such technology is power dissipation. A large FPGA handling 50 MHz of bandwidth could dissipate a few watts. If multiple processors are required for a multi-channel radiometer or interferometer, or if hundreds-of-megahertz to gigahertz of bandwidth needs to be processed, the total power required can quickly approach 100 watts. While this amount is not impractical, it is larger than that dissipated by the detectors (diodes and video amplifiers) of conventional radiometers. Given Moore's Law for semiconductors, however, the power-bandwidth product should continue to decrease.

Microwave radiometers for spaceborne Earth remote sensing have some distinct differences from radio telescopes. Besides their looking down and not up, they must operate in the space environment, consume a practical amount of spacecraft resources, and observe using bandwidths of 100's to 1000's of MHz. Because radiometers have typically been viewed as low-power instruments, the desire to transition to digital back-ends is met with a challenge. To meet this challenge, we have looked to technologies that utilize the low-bit resolution schemes in radio astronomy from the past and the high-bandwidth, low-power, integrated circuit technologies of today.

In this paper we discuss three component technologies. First, a 500-MHz 3-level digital cross-correlator was developed under the Advanced Technology Initiative (ATI) program [3]. Second, a 500-MSps, 1.5-GHz bandwidth, 2-bit/3-level ADC is being developed under the Advanced Component Technology (ACT) program. Finally, a correlated noise source was developed under the ATI program. While the last component is not specifically a digital technology, it is used to calibrate the detection system comprising the first two. Combining these three technologies, we have a bench-top microwave correlation radiometer, which could be used in a polarimeter.

II. Bench-top Radiometer

A bench-top radiometer was developed to demonstrate all three technology components in operation together. It is composed of a receiver, two ADCs and a correlator. A waveguide network and noise diode provide input stimuli. The radiometer block diagram is shown in Fig.1. The dual-channel X-band

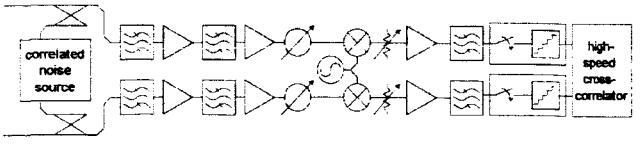

Fig. 1. Block diagram of benchtop digital radiometer containing the correlated noise source, dual channel receiver, and high-speed cross-correlator.

superheterodyne receiver has a nominal RF passband of 10.6-10.7 GHz. With a nominal LO frequency of 10.8 GHz, the IF passband is 100-200 MHz. The radiometer is designed to operate with input noise temperatures ranging from 10^2 K (ambient temperatures) to 10^4 K (attenuated noise diode temperatures). The input referred receiver temperatures were 137 K for channel A and 185 K for channel B. The receiver was characterized with a spectrum analyzer and vector network analyzer (VNA). During testing the LO was set to 10.795 GHz resulting in IF passbands of 98-206 MHz for channel A and 98-203 MHz for channel B as measured with the spectrum analyzer. The inter-channel balance was measured with the VNA. The measurement was made between the first stage RF filter and the IF output with an upconverter driven by the receiver's LO on the IF output. The amplitude and phase balance across the passbands is shown in Fig.2. There is an inband (10.6-10.7 GHz) average phase difference of 0.18° with a maximum range of 15°. The amplitude imbalance is an average 0.12 dB with a range of 1.77 dB. A variable attenuator was placed in the IF chain to balance the amplitude. Group delay was not measured through the channels, however, all hardware between A and B are identical (adjacent serial numbers) so the differential time delay is likely negligible. A passband equalization efficiency can be computed [4]

$$\eta = \frac{\int_{-\infty}^{+\infty} H_A(f)\, H_B^*(f)\, df}{\int_{-\infty}^{+\infty} |H_A(f)|^2\, df \cdot \int_{-\infty}^{+\infty} |H_B(f)|^2\, df} \qquad (1)$$

where $H_A(f)$ and $H_B(f)$ are the transfer functions of the two channels of the receiver. Using the VNA data, $\eta = 0.991\angle 1.1°$. A variable phase shifter was included in the design so the differential phase could be zeroed out. In our experience, the 1-degree phase imbalance is the approximate limit of adjustment given our X-band coaxial phase shifters.

In addition to the bench-top radiometer, we constructed a waveguide-based correlated noise source (WGNS) to provide additional stimulus to the radiometer. The WGNS was made by splitting the output of a noise diode output with a magic-tee. The outputs of two in-phase arms of the magic-tee were routed through waveguide phase shifters and variable attenuators. The WGNS can produce output noise temperatures ranging from ambient ~300 K to ~14,200 K. The WGNS passband equalization efficiency is 0.9999. The correlation coefficient into receiver, including receiver noise, can range between ±0.9887. Fig.3 displays the correlator output for varying WGNS correlation coefficients generated by changing the phase shift between the two arms.

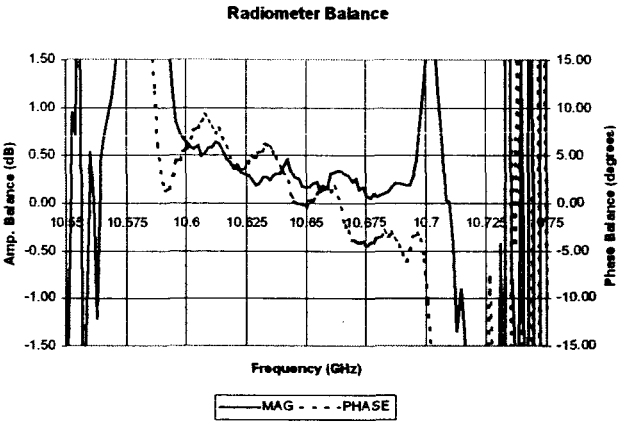

Fig. 2. Inter-channel amplitude and phase balance of the superheterodyne receiver.

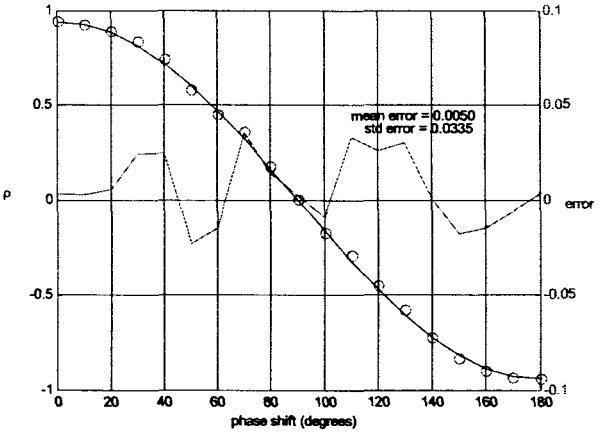

Fig. 3. Correlator output for varying WGNS input.

III. Digital Correlator

The low-power, high-speed, digital correlator IC for passive microwave polarimetry was developed under the Advanced Technology Initiatives (ATI) program. This section is based on the final report submitted for the project. This section summarizes the basic design and operation of the high-speed cross-correlator (HSCC). For further details on the design of the correlator IC, the reader is directed to [5]. Digital correlators can be used to cross-correlate signals received in orthogonal polarizations to estimate the polarization state of radiation incident on a microwave radiometer. In the past, correlators capable of the clock rates required to process hundreds-of-megahertz of bandwidth have been high power circuits using discrete logic. In the ATI project, a low power ASIC was developed to provide a realistic alternative for future instruments. A photograph of several correlator chips is shown in Fig.4.

The first digital correlators for Earth microwave polarimetry operated at 1 GSps and used high-power discrete ECL

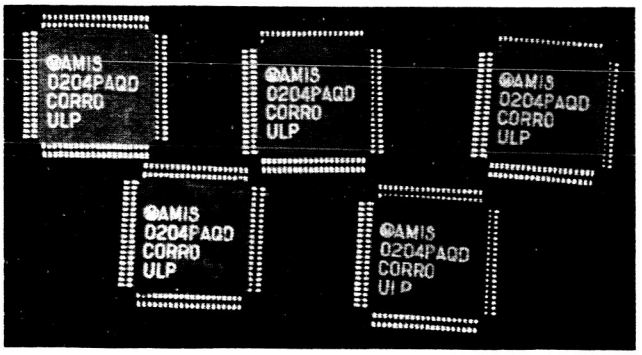

Fig. 4. Correlator chips.

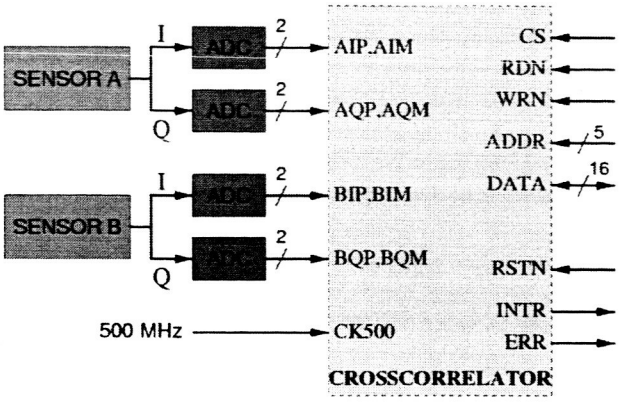

Fig. 5. Top-level correlator block diagram.

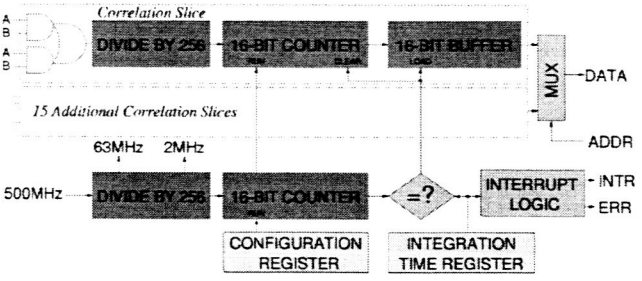

Fig. 6. Correlator block diagram.

logic ICs [6]. The ECL correlator dissipated about 25 W for two multiplications and measured approximately 10cm-by-20cm. The correlator board included four analog-to-digital converters (ADCs), high-speed multipliers, and divide-by-256 prescalars. A separate circuit board contained low-speed 16-bit accumulators and readout logic. The power dissipation is almost evenly distributed between ADCs, clock distribution, and the multipliers and accumulators. For comparison, a power of 8 W for the multipliers and accumulators will be used as the basis of comparison to the new technology. If we use the number of multiplications-per-second-per-watt as our figure of merit, then this older technology would have FOM equal to 250 megahertz-per-watt (MHz/W). This FOM excludes the power required for the ADCs.

The new correlator operates at 500 MSps and was fabricated in a CMOS ultra low-power radiation tolerant (CULPRT) process [7]. The new technology correlator still requires external ADCs, which has been implemented on an evaluation board using the same ECL technology as the previous work. The correlator contains four multipliers and includes the 16-bit accumulators on board the ASIC. The IC itself dissipates only 3 mW for the core logic and 7 mW for the readout logic. Thus, the FOM for the new technology is 200GHz/W, nearly three orders-of-magnitude (1000X) of improvement over the old technology. Note, the ADCs and clock distribution on the evaluation board dissipate 6 W of power (for two as opposed for four ADCs). If this power is included in the FOM, the improvement over the old technology is only a factor of two. This fact indicated a technology need for low-power ADCs, which are discussed later in this paper.

A. Theory of operation

The correlator chip was designed with 0.5-V inputs for the high-speed ADC information and 3.3-V I/O for the microprocessor interface. Fig.5 is a top-level block diagram showing two sensors, four ADCs, and the correlator with its I/O signals. In- and quadrature-phase signals from sensors A and B are quantized by four 3-level ADCs. The output bits of these ADCs are the sensor-A in-phase positive bit (AIP) and negative bit (AIM), the sensor-A quadrature-phase positive (AQP) and negative (AQM), and those from sensor B (BIP, BIM, BQP, BQM). These signals are processed according to Fig.6, the correlator block diagram. Sixteen products are computed and accumulated, each by a correlation slice. Eight slices count input states (the eight input bits), four count positive-positive and negative-negative correlations and the remaining for count the anti-correlations (positive-negative and negative-positive). There is an additional accumulator, which counts clock cycles. When a user specific number of clock cycles have elapsed, the accumulator values are latched into 16-bit buffers for readout. The accumulators are cleared and a new correlation measurement can begin while the old data is being read out. This double-buffering technique ensures that measurements can be made continuously with no wait states. A typical flow-chart for operating the correlator is given in the datasheet available soon at NASA Tech Briefs (www.nasatech.com). For theory on how to utilize the correlator data for remote sensing, see [6].

B. Evaluation Board Design

An evaluation board (EVB) was designed to allow the correlator chip to be used in the bench-top radiometer system. A picture of the EVB is shown in Fig.7. It contains two three-level ADCs, clock distribution, logic level translation, and an interface to a 32-bit digital I/O card for a PC. The correlator chip is mounted in an 80-pin PQFP clamshell adaptor. The analog-to-digital converters are designed using Motorola

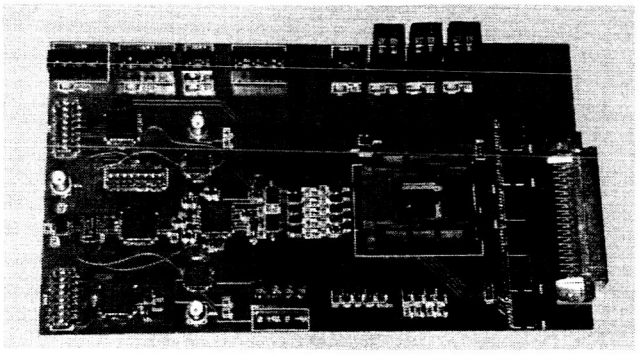

Fig. 7. Correlator evaluation board.

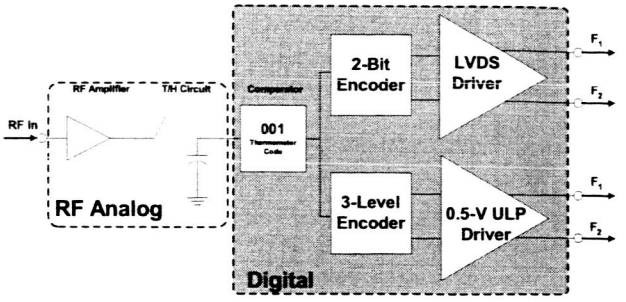

Fig. 8. Block diagram of RF-ADC.

ECLiPS 1-GHz comparators and D-Latch. Two comparators are used to make a 3-level flash-ADC and their outputs are latched for one complete clock-cycle. The outputs of the ADCs are in ECL logic voltages and must be translated to ULP logic voltages. This is accomplished by using an ECL-LVPECL translator, which moves the 800-mV amplitude ECL signal up in voltage to just below 3 V. Then a resistor network is used to (1) level-shift the signal down to 0 V, (2) reduce the signal amplitude to 500 mV, and (3) terminate the LVPECL output. The EVB clock was generated by an external RF signal source and coupled into a divide-by-two counter on the EVB. This 50% duty-cycle clock is then distributed by a fan-out buffer and can be controlled by programmable delay chips. The programmable delay chips provide up to 2 ns of delay controllable with 20-ps resolution. This flexibility was built in the EVB so that the setup and hold requirements of the correlator inputs could be verified. The datasheet values tested valid for normal operation.

IV. RF-ADC

As discussed in the previous section, the ADCs where identified as the next largest challenge in power dissipation. Unfortunately, there are not any COTS 2-bit ADCs available. This lack of availability, coupled with the previous design's high power dissipation, motivated the development of custom 2-bit ADCs. Silicon germanium (SiGe) heterojunction bipolar transistor (HBT) technology was quickly identified as promising for low-power high-speed design. Another ATI development was already using COTS SiGe parts [8] and the investigator was pleased with the results. Initial prototype work for the ADC in SiGe was completed as graduate research [9] and was seminal for this research. This section is based upon on-going work under the radio-frequency analog-to-digital converter (RF-ADC) ACT project.

The RF-ADC design is a 2-bit flash architecture with an integrated track-and-hold amplifier (THA). The block diagram for the circuit is shown in Fig.8. RF signals enter the IC and our buffered by the input amplifier. The THA samples the signal, which is then quantized by a ladder of comparators. The output of the quantizer is then encoded into 2-bits and 3-levels. The 2-bit code is output through a low-voltage differential-signal (LVDS) driver. The LVDS outputs can be terminated into 100 ohms and designed to meet LVDS standards for common-mode and differential-mode voltage amplitudes. The LVDS interface allows the RF-ADC to be flexibly combined with COTS FPGAs or ASICs with LVDS inputs. The 3-level code is output through a 0.5-volt driver with complimentary outputs. The 0.5-volt outputs can be terminated into 100 ohms and can be directly interfaced with the HSCC, thus removing the need for logic-translation circuits. For additional design details and initial prototype results, the reader is referred to [9].

The RF-ADC IC is currently in fabrication and parts are due in June 2004. The circuit is being fabricated in a 0.35um SiGe BiCMOS process with $f_T = 43$ GHz. Simulations suggest the input bandwidth exceeds 1.5 GHz and the maximum sampling rate will be at least 1 GSps. The DC power dissipation is expected to be less than 200 mW.

At the time of this writing, the authors are aware of at least three of SiGe ADCs, two COTS parts and one ASIC. The COTS parts are 10- and 14-bit ADCs using more complex quantization schemes rather than a simple flash architecture. The ASIC is a 2-bit flash ADC developed for the Atacama Large Millimeterwave Array (ALMA) radio telescope. The ALMA ADC dissipates 650 mW and operates at 4 GSps (ALMA Memo No. 426, May 16, 2002). If a figure-of-merit is defined as the ratio of DC power to the number of bits, the four ADCs can be plotted as in Fig.9.

V. Correlated Noise Source

Radiometer calibration is required to quantify the system coefficients in a radiometer equation. The radiometer equation for a correlation radiometer is

$$\begin{pmatrix} v_v \\ v_h \\ v_c \end{pmatrix} = \begin{pmatrix} G_{vv} & G_{vh} & G_{vc} \\ G_{hv} & G_{hh} & G_{hc} \\ G_{cv} & G_{ch} & G_{cc} \end{pmatrix} \begin{pmatrix} T_v \\ T_h \\ T_U \end{pmatrix} + \begin{pmatrix} o_v \\ o_h \\ o_U \end{pmatrix} \quad (2)$$

where the elements of v-vector on the left-hand side are the radiometer outputs for the vertical, horizontal, and correlation channels. The elements of T-vector on the right-hand side are input brightness temperatures. The gain matrix and offset vector are the system coefficients to be quantified during calibration. Each channel has four unknowns, so four independent

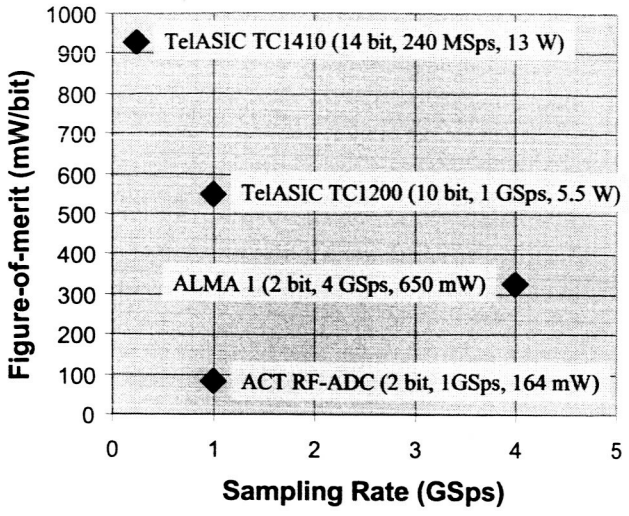

Fig. 9. DC power-per-bit versus sampling rate for four SiGe ADCs. The ALMA and ACT ADCs are flash architecture.

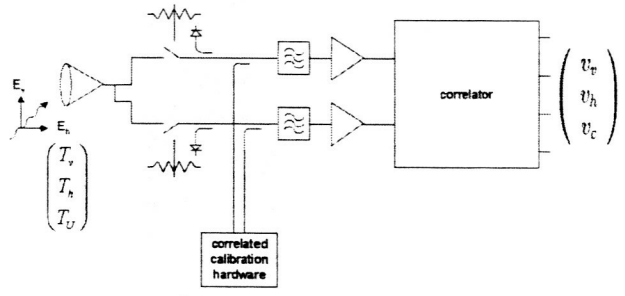

Fig. 10. Implementation of a correlated noise source in a correlation polarimeter.

calibration inputs need to be measured. The first two columns of the G-matrix and the offset vector can be determined using uncorrelated inputs of varying power levels. The last column of the G-matrix, however, requires some sort of correlated stimulus. In [6], an external polarized calibration target was observed through the feedhorn. This method was an appropriate end-to-end calibration because the feedhorn was the entire antenna. On proposed satellite systems, however, the antennas comprise both feedhorn and reflectors. For practical reasons a polarized calibration target, or any on-board calibration target for that matter, can be viewed through the reflector antenna systems. It is desirable, as is done in radio astronomy, to separate the calibration of the antenna and receiver; therefore, the feedhorn should be removed from the calibration loop. The feedhorn effects should then be included in the antenna pattern correction and the receiver can be calibrated independently. An internal correlated noise source (CNS) can make this possible. Like our digital radiometry techniques, the CNS finds its roots in radio astronomy [10]. A block diagram showing the usage of a CNS in a correlation polarimeter is shown in Fig.10.

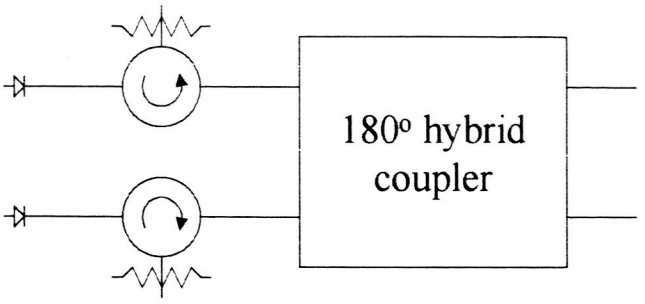

Fig. 11. Block diagram of correlated noise source.

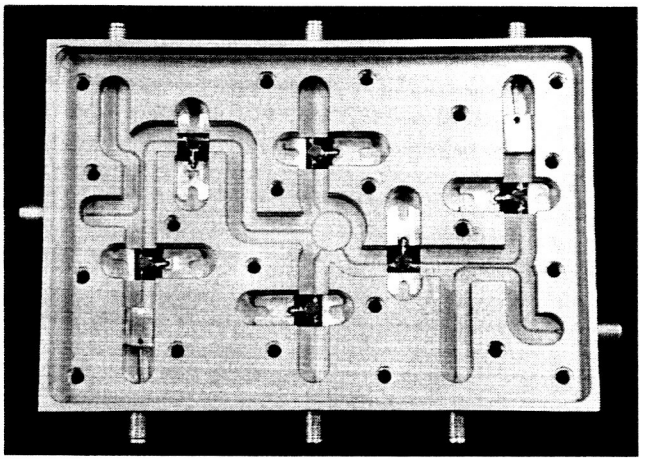

Fig. 12. Photograph of assembled CNS.

Perhaps the simplest method of generating correlated signals is demonstrated by the WGNS described previously. We adopted this technique and implemented it using microstrip circuits and isolators and miniature noise sources to create a compact CNS. A block diagram of the CNS is shown in Fig.11. The CNS comprises two noise diodes, multiple isolators (not all shown in the block diagram), and hybrid coupler. The hybrid coupler divides the outputs of the noise diodes to generate in- and out-of-phase correlated noise. A photograph of a assembled CNS is shown in Fig.12.

The CNS was installed in the bench-top radiometer and used to determine its passband equalization efficiency. The CNS has two noise diodes, denoted SUM and DIFF as determined by which port on the hybrid each excites. As shown in Fig.10, the CNS outputs were coupled into the receiver front-end using directional couplers. The total power channels on the radiometer were used to measure the effective noise temperature generated by the CNS. The results are:

Mode	SUM	DIFF
Channel A Temp	1400 K	2033 K
Channel B Temp	1248 K	1874 K
Expected Correlation	+0.6504	-0.7090
Measured Correlation	+0.6496	-0.6989

Averaging the results from the SUM and DIFF modes results in a radiometric calibrated $\hat{\eta} = 0.9922$ compared to the VNA-measured $\eta = 0.9913$ for a difference of 0.09%. The correlation offset was 0.0008.

VI. Discussion

In this paper, we have discussed the combination of three component technologies into a bench-top radiometer system. The three components are (1) a high-speed cross-correlator, (2) low-power analog-to-digital converters, and (3) a correlated noise source. Together these three components make a low-power digital correlation radiometer achievable. The correlator dissipates 10 mW and the ADCs are predicted to dissipate less than 200 mW each. Thus, it is possible to develop a 1 W digital correlation detector, which is competitive with conventional analog systems. In the near future we plan to integrate the HSCC and RF-ADCs into a PC-104 module for use in ground-based and aircraft radiometers.

VII. Acknowledgments

The authors extend thanks to Kevin Horgan for his assistance with the VNA measurements.

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